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|  | Students Interest Group „SNS Delta Power” |

**Design Challenge No. 4**

**Tester of Double Data IO IP core**

Version 0.1 18/12/2020

Hello SNS Delta Power,

The fourth design challenge is difficult and require wide knowledge. It means you will learn a lot.

The main task is to create an FPGA design to test DDIO interface. My idea is to create two RAM memory in FPGA device and state machine to control:

* transferring data from memory 1 to memory 2 by sending data outside the FPGA and receive them by using DDIO interface.
* checking if the data was correctly sent or not.

Please use your creativity to develop user interface (buttons, switches, LEDs) to show the current status of the state machine.

In this design challenge you will learn about:

* How you can manage data flow in FPGA
* Types of embedded memory in Cyclone V
* DDIO interface
* Timings for I/O interfaces
* Repeat knowledge about state machines
* Create Simulation with IP cores
* Debugging by using Signal Tap tool - (if you encounter big issues in the design)

This is my proposition how to solve the challenge.

1. **Pleas investigate what it is DDIO interface**   
   The first step should be to understand what you will test. I recommend reading briefly  
   <https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/ug/ug_altddio.pdf>  
   What is it?  
   How it works?  
   What kind of signals are required?  
   How does data and clocks look? (Timing relationship)
2. **Think and create the core design.**  
   If you know what you need to test, you can jump to the next step and start thinking how to test DDIO interface.  
   Please create a design with DDIO TX and DDIO RX and use hardware loopback on the development kit. The loopback should be jumper wires on GPIO Header.  
   What kind of data do you need to put to the DDIO TX?  
   What kind clock do you need to connect to the DDIO TX?  
   Do you need to a send clock outside or may you use an internal clock?  
   What kind of data will DDIO RX receive?  
   Do you need to use PLL or not?

How to create a simple design with DDIO TX and DDIO RX?  
What will look like an idea schematic of the design?  
How to create timing constrains for DDIO?

This is the documentation about basic things regarding timings:  
<https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/hb/qts/qts_qii53024.pdf>

1. **Simulation of DDIO core design.**  
   Now you have the core part of the design, so it would be nice to test it in a simulation.

The simulation will verify your understanding how the DDIO works and verify the core part of the design.

This is the documentation about ModelSim\* - Intel® FPGA Edition Simulation Quick-Start  
<https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/ug/ug_gs_msa_qii.pdf>

1. **Think how to test DDIO**  
   Now you should have knowledge and experience what DDIO is. Now you can think how to create a logic to test the design.  
   The main functions are:  
   1. Send data and receive them  
   2. Check the sent and received data (compare the data or CRC checksum)  
   **Questions to think:**

**AI 1:**  
How can you store data in Cyclone V?

What kind type of memories are in Cyclone V?  
Which one is better?

Documentation regarding Cyclone V:  
<https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/hb/cyclone-v/cv_51001.pdf#page=21>

Short info about M10k block   
<https://www.intel.com/content/www/us/en/programmable/quartushelp/13.0/mergedProjects/reference/glossary/def_m10k.htm>

How can you initialize memory?  
Is there only one way to instantiate a memory block? (Advanced Question)  
What kind of data are you going to use to test the interface? (Please check PRBS idea- pseudo-random bit sequence)   
Can you change the memory for TX to PRBS generator?  
How wide buses will you create between memory and DDIO?   
Are you able to create an idea schematic of this design phase?  
Do you need to make a simulation for this part of the design?  
**A2:**  
How can you compare sent and received data?  
Does there exist any IP core to compare memories?  
Are you able to create an idea schematic of this design phase?  
Do you need to make a simulation for this part of the design?

1. **Create a full design**In this step you should connect everything in one design as a state machine to allow run test and have ability to check if transmission had any errors  
   You need to have:

* an idea schematic of all sub-blocks and blocks (Have you created a hierarchical design?)
* a functional simulation of the top design
* created and double-checked pin assignment
* created timing assignment for DDIO
* Time Analyzer results (If you encounter any timing issues it will be a great opportunity to talk)

1. **Make hardware tests**

If you are sure that functional simulations pass, and you have correct pin assignments you can test the design in hardware.

Are you able to make a failure test in simulations or/and in hardware? (disconnect jumper during transmission?)

What kind of issues have you encountered during phase?

This task is complex, hard and require big effort to create it. I hope the challenge will increase your Team’s collaboration but also make contacts between SNS Delta Power and Intel Programmable Solutions Group more frequent. I expect that you will encounter some unknown issues. I would like to take them as opportunity for further learning. More issues, more knowledge you will get. Please raise questions during design phase by e-mail or ask for a meeting.

P.S.

I am a big fan of Elon Musk. He is one of today’s renaissance men. He is a CEO of SpaceX, Tesla and a founder of The Boring Company, Neuralink and others. He can manage multiple companies and topics. Moreover, he is a multidisciplinary engineer and he knows how to learn.

I would like to share one good video about how Elon learns. It could be useful tip for future.

<https://www.youtube.com/watch?v=xLkC-ODKQSc>

P.S.S.

What do you think about the task and this form of it?

Good luck! 😉

Regional FPGA Applications Team, Intel/Gdańsk

References:

1. “Altera Cyclone V SoC Development & Education Board (DE10-Standard)”, development kit board electrical diagrams: <https://rocketboards.org/foswiki/pub/Documentation/DE10Standard/DE10-Standard_Schematic.pdf>
2. “DE10-Standard User Manual”: <https://www.terasic.com.tw/cgi-bin/page/archive_download.pl?Language=English&No=1081&FID=551f9fbfa8ed07843cd51831db1b04dd>
3. Good Training Materials:

<https://software.intel.com/content/www/us/en/develop/topics/fpga-academic/learn/tutorials.html>

1. Time Analyzer tutorial/introduction

<https://ftp.intel.com/Public/Pub/fpgaup/pub/Teaching_Materials/current/Tutorials/Verilog/Timequest.pdf>

1. Timing Analyzer Design Examples

<https://www.intel.com/content/www/us/en/programmable/support/support-resources/design-examples/design-software/timinganalyzer.html>