Zynq PS/PL FFT Acceleration with DDR Input and BRAM Output via AXI DMA

OBJECTIVES:

1. To verify FFT Acceleration on Zynq using PL BRAM Input/Output and AXI DMA.

2. To Test the functionality of AXI DMA by sending bytes of data to PS DDR using the BRAM.

OVERVIEW:

Implemented the Fast Fourier Transform (FFT) using a hardware accelerator in the Zynq PL. Generated input data is first loaded into the PS DDR memory by the controlling Vitis software. The CPU then copies this data into an intermediate Block RAM (BRAM) in the PL. Subsequently, an AXI DMA controller reads the data from the intermediate BRAM, streams it to the FFT IP core, receives the results from the FFT, and writes them to a final Output BRAM in the PL. The PS can then read the results from the Output BRAM.

- **Architecture:**
    1. **Processing System (PS):** ARM Cortex-A9 runs control software, generates input data in DDR, performs the initial CPU copy to PL BRAM, configures/monitors AXI DMA.
    2. **Programmable Logic (PL):** Contains hardware accelerators and memory:
        - Intermediate BRAM (blk_mem_gen_0, Dual-Port) + AXI BRAM Controller (axi_bram_ctrl_0).
        - AXI DMA Controller (axi_dma_0) with MM2S and S2MM channels.
        - FFT IP Core (xfft_0).
        - Output BRAM (blk_mem_gen_1, Dual-Port) + AXI BRAM Controller (axi_bram_ctrl_1).
        - AXI SmartConnect (axi_smc) for routing AXI Memory-Mapped traffic.
        - Processor System Reset Module (proc_sys_reset_0).
- **Data Flow:**
    1. **CPU Copy:** PS DDR (Input Data) -> PS (M_AXI_GP0) -> AXI SmartConnect -> Intermediate BRAM Controller (axi_bram_ctrl_0) -> Intermediate BRAM (blk_mem_gen_0).
    2. **DMA Transfer:** Intermediate BRAM (blk_mem_gen_0) -> Intermediate BRAM Controller (axi_bram_ctrl_0) -> AXI SmartConnect <- AXI DMA (MM2S Read) -> AXI DMA (MM2S Stream Out) -> FFT IP Core -> FFT IP Core (Stream Out) -> AXI DMA (S2MM Stream In) -> AXI DMA

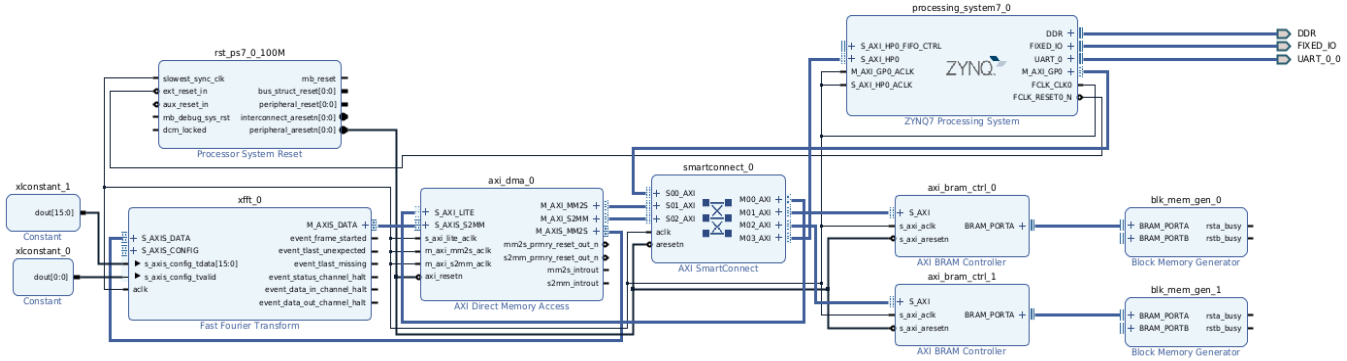
(S2MM Write) -> AXI SmartConnect -> Output BRAM Controller (axi_bram_ctrl_1) -> Output BRAM (blk_mem_gen_1).

- **Result Retrieval:** PS (M_AXI_GP0) -> AXI SmartConnect -> Output BRAM Controller (axi_bram_ctrl_1) -> Output BRAM (blk_mem_gen_1).
- **Control Flow:** The PS generates data, performs the CPU copy, configures and starts the AXI DMA for the main transfer, polls for DMA completion, and finally reads the results from the Output BRAM.

Reference Files:

- signal.coe: Generated by the Python script, used to initialize Input BRAM.
  f1=50 Hz, f2 = 120 Hz fs=1000 Hz
  f1=75 Hz, f2 = 200 Hz
  f1=90 Hz, f2 = 300 Hz
- fft_output.txt: Generated by the Python script, contains expected packed hex values (in bit-reversed order) for comparison.

VIVADO BLOCK DIAGRAM:



TESTING WITH NUMATO STYX:

Vitis Code: fft_numato_test

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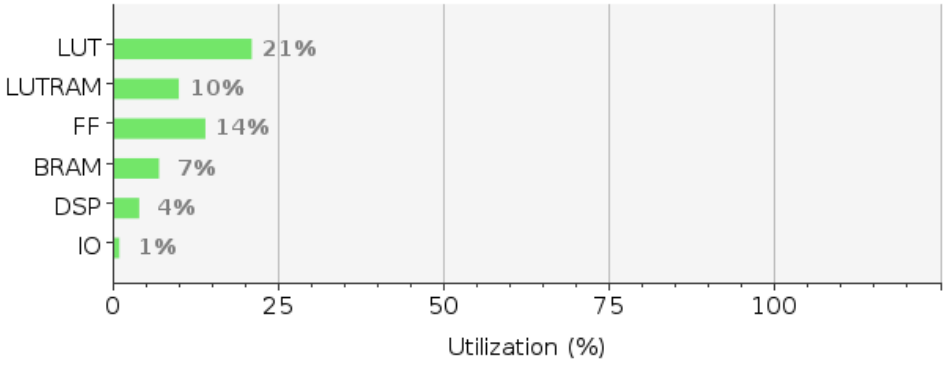
FFT Output Samples:
  [  0] Real:      0, Imag:  21202
  [  1] Real:      0, Imag:  -3154
  [  2] Real:      0, Imag:   -532
  [  3] Real:      0, Imag:  -3154
  [  4] Real: -17675, Imag: -30873
  [  5] Real:   -457, Imag:  -1880
  [  6] Real:    295, Imag:   -677
  [  7] Real:  -1702, Imag:  -5936
  [  8] Real:  -5478, Imag:   1222
  [  9] Real:   9109, Imag:   8484
  [ 10] Real:  -9110, Imag:   8484
  [ 11] Real:   5477, Imag:   1222
  [ 12] Real:   1702, Imag:  -5936
  [ 13] Real:   -296, Imag:   -677
  [ 14] Real:    456, Imag:  -1880
  [ 15] Real:  17674, Imag: -30873
```

UTILIZATION:

Resource	Utilization	Available	Utilization %
LUT	11054	53200	20.78
LUTRAM	1798	17400	10.33
FF	14425	106400	13.56
BRAM	9.50	140	6.79
DSP	9	220	4.09
IO	2	200	1.00



TIMING REPORTS:

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	2.277 ns	Worst Hold Slack (WHS):	0.019 ns	Worst Pulse Width Slack (WPWS):	3.750 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	50560	Total Number of Endpoints:	50560	Total Number of Endpoints:	17596

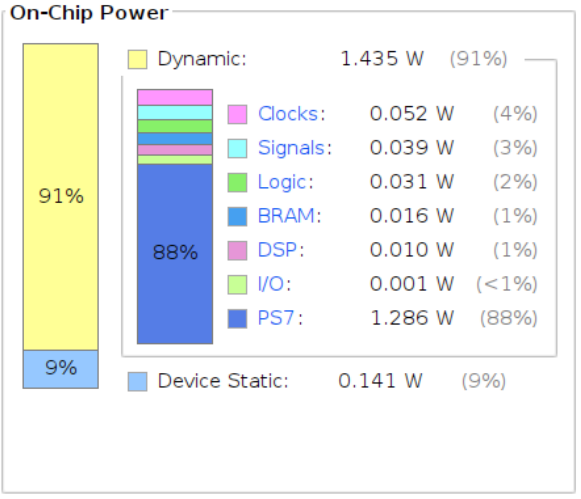
All user specified timing constraints are met.

POWER:

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**1.577 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**43.2°C**
Thermal Margin:	41.8°C (3.5 W)
Ambient Temperature:	25.0 °C
Effective θJA:	11.5°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



LEARNINGS:

1. The AXI transaction or memory access, especially when accessing address 0x01000000 (DDR_SOURCE_ADDR), was an issue. This address is outside the typical valid DDR memory range for the majority of Zynq boards, unless it has been properly mapped or configured.
Error: Memory write error at 0x100000. AP transaction timeout.
Cannot reset APU. APB AP transaction error, DAP status 0xF0000021.
Solution: DDR_SOURCE_ADDR is not needed because DDR_Source_Buffer is already your source buffer in on-chip memory. Remove all references to DDR_SOURCE_ADDR (and its printout) and pass the actual pointer DDR_Source_Buffer directly.

2. Numato styx board drive installation:
Location for FTDI cable_driver installation for Vitis/Vivado for Styx Numato Board.

- Location: /home/mr_madeshwar_flightelectronics/Downloads/Vivado/Downloads/Vitis/2024.2/data/xicom/cable_drivers/lin64/install_script/install_drivers.
- Run ./install_drivers binary there and then restart udev services.

3. Constraints to be added :
set_property -dict {PACKAGE_PIN T22 IOSTANDARD LVCMOS33} [get_ports UART_0_0_rxd]
set_property -dict {PACKAGE_PIN T21 IOSTANDARD LVCMOS33} [get_ports UART_0_0_txd]

4. Incrementing of the BRAM address:
The AXI DMA controller's MM2S channel hardware is responsible for generating the sequence of incrementing AXI addresses based on the initial configuration (start address, length).The AXI Interconnect routes these AXI transactions (with the incrementing addresses) to the correct destination slave. The AXI BRAM Controller receives these AXI transactions, translates the incrementing AXI addresses into native BRAM addresses, and drives the addra pins of the BRAM IP. The BRAM IP passively accepts the address provided by the controller on addra and returns the corresponding data on douta.

5. FFT ip config data:
Need to give appropriate input to this signal s_axis_config_tdata for N- point FFT.
Eg: 1024 point FFT : NFFT[4:0] = 01010