Zynq PS/PL FFT Acceleration with real-time input using SPI RX interface

OBJECTIVES:

1. To verify FFT Acceleration on Zynq with the real time inputs using the SPI receiver interface.

2. To test the functionality of FFT using AXI DMA by making sure to work synchronously with the real time inputs.

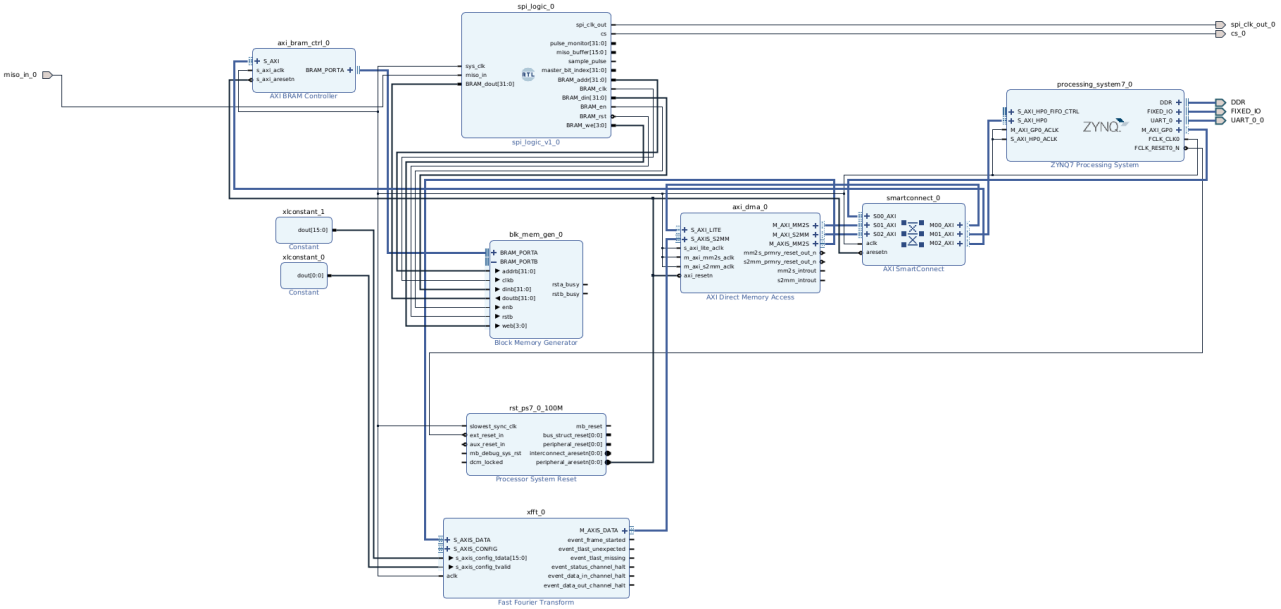
OVERVIEW:

Implemented the Fast Fourier Transform (FFT) using a hardware accelerator in the Zynq PL. Real-time input data is first loaded into the native true dual port BRAM by the SPI receiver interface. Subsequently, an AXI DMA controller reads the data from that BRAM, streams it to the FFT IP core, receives the results from the FFT, and writes them to the DDR memory of PS.

ACTUAL DATA FLOW :

- STM32 Nucleo sends data via SPI to the FPGA.
- The spi_logic module in the FPGA captures the SPI data and writes it to BRAM.
- The PS writes to a specific BRAM location to signal the PL to start the SPI transfer.
- The AXI DMA MM2S transfers the data from BRAM to the FFT IP core.
- The FFT IP core processes the data and sends the results to the AXI DMA S2MM.
- The AXI DMA S2MM transfers the FFT results to DDR memory.
- The PS reads the FFT results from the DDR memory.

BLOCK DIAGRAM:



ARCHITECTURE:

Programmable Logic (PL): Contains hardware accelerators and memory:

- Native True Dual port BRAM (blk_mem_gen_0, Dual-Port) + AXI BRAM Controller (axi_bram_ctrl_0).
- AXI DMA Controller (axi_dma_0) with MM2S and S2MM channels.
- FFT IP Core (xfft_0).
- AXI SmartConnect (axi_smc) for routing AXI Memory-Mapped traffic.
- Processor System Reset Module (proc_sys_reset_0).
- SPI_RX (spi_logic_0).

DATA & CONTROL FLOW:

1. SPI Data Acquisition Flow:

- STM32 Nucleo (SPI Master) -> FPGA (MISO pin) -> spi_logic -> BRAM (spi_input_bram)

2. SPI Trigger Flow:

- PS -> (M_AXI_GP0) -> AXI SmartConnect -> BRAM Controller (axi_bram_ctrl_0) -> BRAM (spi_input_bram) (Write of SPI_ENABLE_FLAG_VALUE)

3. FFT Data Transfer Flow:

- BRAM (spi_input_bram) -> BRAM Controller (axi_bram_ctrl_0) -> AXI SmartConnect -> AXI DMA (MM2S Read) -> AXI DMA (MM2S Stream Out) -> FFT IP Core -> FFT IP Core (Stream Out) -> AXI DMA (S2MM Stream In) -> AXI DMA (S2MM Write) -> AXI SmartConnect -> BRAM Controller (axi_bram_ctrl_1) -> BRAM (fft_output_bram)

4. FFT Result Retrieval Flow:

- PS -> (M_AXI_GP0) -> AXI SmartConnect -> BRAM Controller (axi_bram_ctrl_1) -> BRAM (fft_output_bram)

VITIS CODE FLOW:

- SPI Receiver (PL) writes data to BRAM.
- PS triggers SPI/enables data path (by writing to BRAM).
- AXI DMA (MM2S) reads from BRAM.
- AXI DMA streams data to FFT IP.
- FFT IP streams results back to AXI DMA (S2MM).
- AXI DMA writes results to the destination DDR buffer.
- PS reads results from the destination DDR buffer.

REFERENCE FILES:

- signal.coe: Generated by the Python script, used to initialize Input BRAM.
  f1=50 Hz, f2 = 120 Hz fs=1000 Hz
  f1=75 Hz, f2 = 200 Hz
  f1=90 Hz, f2 = 300 Hz
- fft_output.txt: Generated by the Python script, contains expected packed hex values (in bit-reversed order) for comparison.

FFT IP CONFIGURATION:

Transform length: 1024
No of Channels : 1
Target Clock frequency : 250 MHz
Target Data Throughput : 50 MSPS
Data format : Fixed point
Scaling options : Scaled
Rounding modes : Truncation
Input Data width : 16
Butterfly arithmetic : use CLB logic
Output ordering : Bit/Digit reversed order
S_axis_config_data : 1010 (1024 point fft)
S_axis_config_tvalid : 1 (always ready to accept the data).

RELEVANT DOCS:

- SPI_RX : spi_rx_vhdl_explanation
- FFT IP (Iterations with Numato) : FFT_IP_Numato- REPORT
- FFT VITIS CODE : FFT_VITISCODE_Realtime
- FFT ip : FFT_IP_REPORT

CONNECTION SETUP:

FPGA pin (P4 header)	STM
13	SCK (PA_5)
5	CS (PA_4)
9	MISO(PA_6)

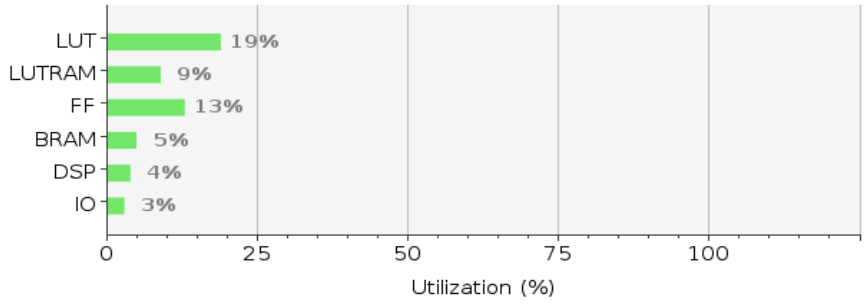
OUTPUT:

```
--- Entering FFT DMA Test (BRAM to DDR via FFT) ---
AXI BRAM Controller Base Addr: 0x2802E0000000
SPI Data Start in BRAM (DMA Source): 0x6802E0000000
Dest DDR Buffer Addr:   0x10C840E0000000
Transfer Size:          114357799224320 bytes (3 samples)
Writing SPI enable flag (0x00000001) to BRAM address 0x680240000004.
Enable flag written. PL spi_receiver should now be active if it polls this address
SPI trigger sent to BRAM. Assuming BRAM is being populated by PL...
DMA Reset Complete.
AXI DMA Initialized.
Starting DMA transfer (BRAM to DDR)...
S2MM (Device to DMA) transfer configured for DDR 0x00001000, length 4096.
MM2S (DMA to Device) transfer configured for BRAM 0x00001000, length 4096.
Waiting for MM2S (BRAM to FFT) transfer to complete...
MM2S Transfer Done.
Waiting for S2MM (FFT to DDR) transfer to complete...
S2MM Transfer Done.
DMA Transfer completed.
Reading FFT results from DDR 0x10C840E0000000...
Cache invalidated for destination DDR range: 0x10D8400010D840 to 0xFFFFFFFF
--- FFT Output Samples (from DDR) ---
Sample   0: Real =      0, Imag =  22541 (0x0000580D)
Sample   1: Real =   2191, Imag =   -467 (0x088FFE2D)
Sample   2: Real =      0, Imag =  -2589 (0x0000F5E3)
Sample   3: Real =  -2191, Imag =   -467 (0xF771FE2D)
Sample   4: Real =  13703, Imag =   4941 (0x3587134D)
Sample   5: Real =  -2117, Imag =  -1664 (0xF7BBF980)
Sample   6: Real =    911, Imag =    461 (0x038F01CD)
Sample   7: Real =   1963, Imag =  -8296 (0x07ABDF98)
Sample   8: Real =  12525, Imag =  -3053 (0x30EDF413)
Sample   9: Real =   1662, Imag =  -1901 (0x067EF893)
Sample  10: Real =  -1663, Imag =  -1901 (0xF981F893)
Sample  11: Real = -12526, Imag =  -3053 (0xCF12F413)
Sample  12: Real =  -1964, Imag =  -8296 (0xF854DF98)
Sample  13: Real =   -912, Imag =    461 (0xFC7001CD)
Sample  14: Real =   2116, Imag =  -1664 (0x0844F980)
Sample  15: Real = -13704, Imag =   4941 (0xCA78134D)
Sample  16: Real =   7666, Imag =  20495 (0x1DF2500F)
Sample  17: Real =   2450, Imag =  -2560 (0x0992F600)
```

REPORTS:

Utilisation:

Resource	Utilization	Available	Utilization %
LUT	10171	53200	19.12
LUTRAM	1571	17400	9.03
FF	13361	106400	12.56
BRAM	7.50	140	5.36
DSP	9	220	4.09
IO	5	200	2.50



Timing :

Setup

Worst Negative Slack (WNS):	0.837 ns
Total Negative Slack (TNS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	45783

Hold

Worst Hold Slack (WHS):	0.016 ns
Total Hold Slack (THS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	45783

Pulse Width

Worst Pulse Width Slack (WPWS):	3.750 ns
Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	16113

All user specified timing constraints are met.