Design and Analysis of a 1x2 Demultiplexer using Cadence Virtuoso

Aim: To design a 1x2 Demultiplexer (DEMUX) using Cadence Virtuoso, perform transient analysis, and create its symbol for circuit integration.

Theory:A 1x2 Demultiplexer is a combinational logic circuit that takes a single input and routes it to one of the two outputs based on the control signal. It acts as a single-input, two-output switch controlled by a select line. The circuit consists of logic gates (such as AND and NOT gates) implemented using CMOS technology.

The select line determines which output receives the input signal:

1. When the select line is **0**, the input is routed to **Output 0**.
2. When the select line is **1**, the input is routed to **Output 1**.

The CMOS implementation of a 1x2 Demux ensures low power consumption and high-speed operation. Transient analysis helps observe the switching behavior of the circuit, including propagation delays and power dissipation due to capacitive effects.

Procedure:

1. **Setup in Cadence Virtuoso:**
    1. Open Cadence Virtuoso and create a new library for the 1x2 Demultiplexer design.
    2. Attach the library to the appropriate technology file.
2. **Design the Schematic:**
    1. Create a new cell view for the schematic.
    2. Implement the 1x2 Demux using CMOS logic gates (AND, NOT) based on transistor-level design.
    3. Connect the circuit with appropriate wiring for inputs, outputs, power supply (VDD), and ground (GND).
3. **Verification:**
    1. Check the schematic for connectivity errors.
    2. Correct any design issues before proceeding with simulations.
4. **Perform Transient Analysis using ADE L:**
    1. Set up model libraries in the Analog Design Environment (ADE L).
    2. Define voltage sources, select signals, and simulation parameters.
    3. Run the simulation and observe the dynamic response of outputs based on input and select signal transitions.
5. **Create a Symbol for the Demultiplexer:**
    1. Generate a symbol view from the schematic.

2. Define input (Data, Select) and output terminals (Output 0, Output 1).

6. **Testing the Symbol:**

   1. Use the symbol in a larger hierarchical circuit.
   2. Simulate and validate its functional correctness.

7. **Analysis and Validation:**

   1. Observe the transient waveforms.
   2. Verify that the circuit correctly routes the input to the appropriate output based on the select signal.

By following these steps, a 1x2 Demultiplexer is designed and analyzed for its transient behavior, ensuring its efficiency and usability in larger digital circuits.

Circuit Diagram:

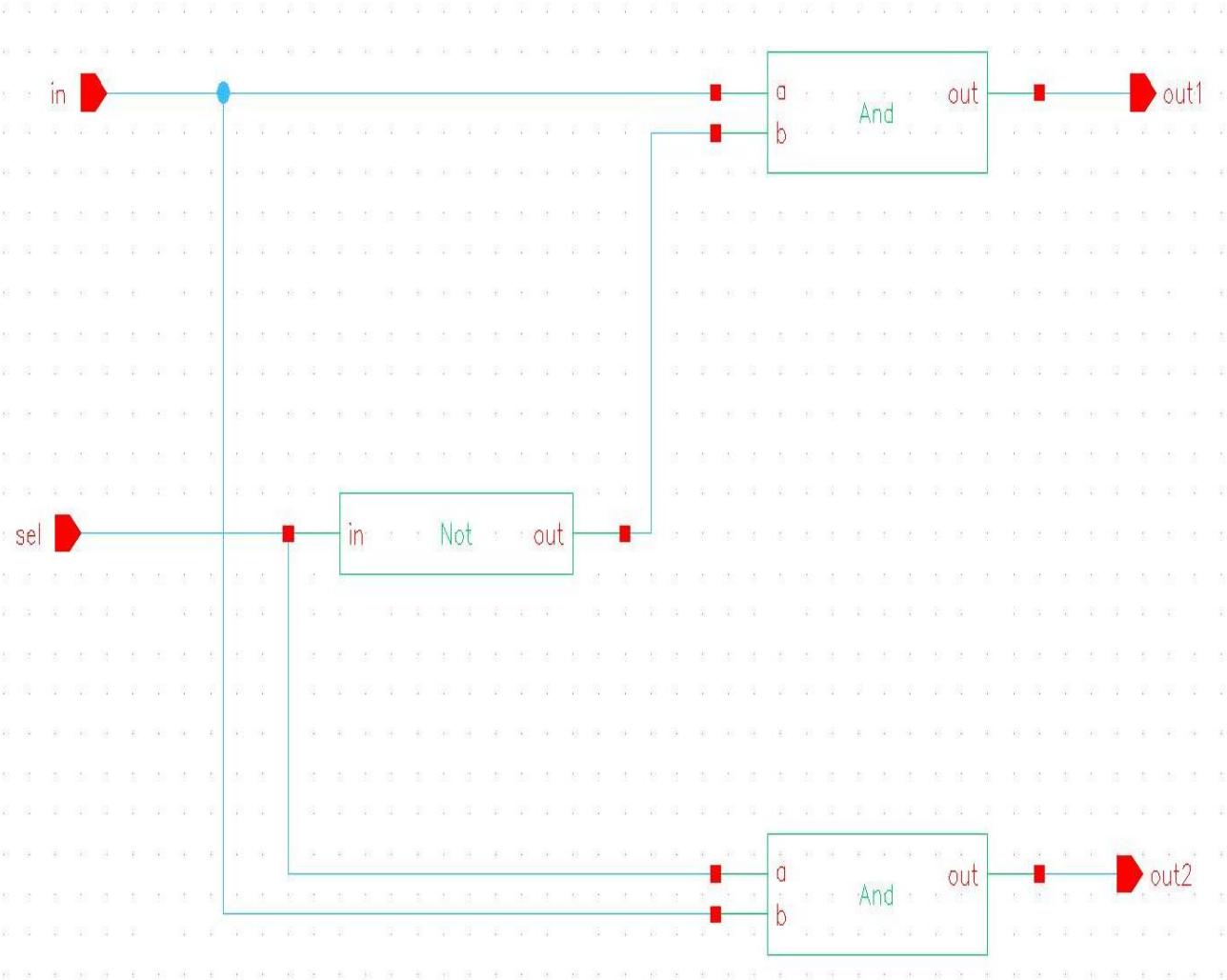

Figure 10.1:Schematic of 1x2 DeMultiplexer

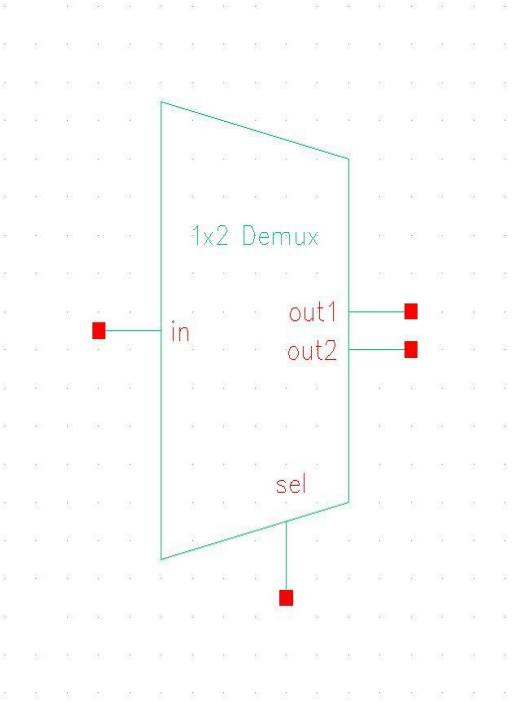

Figure 10.2: Symbol of 1x2 DeMultiplexer

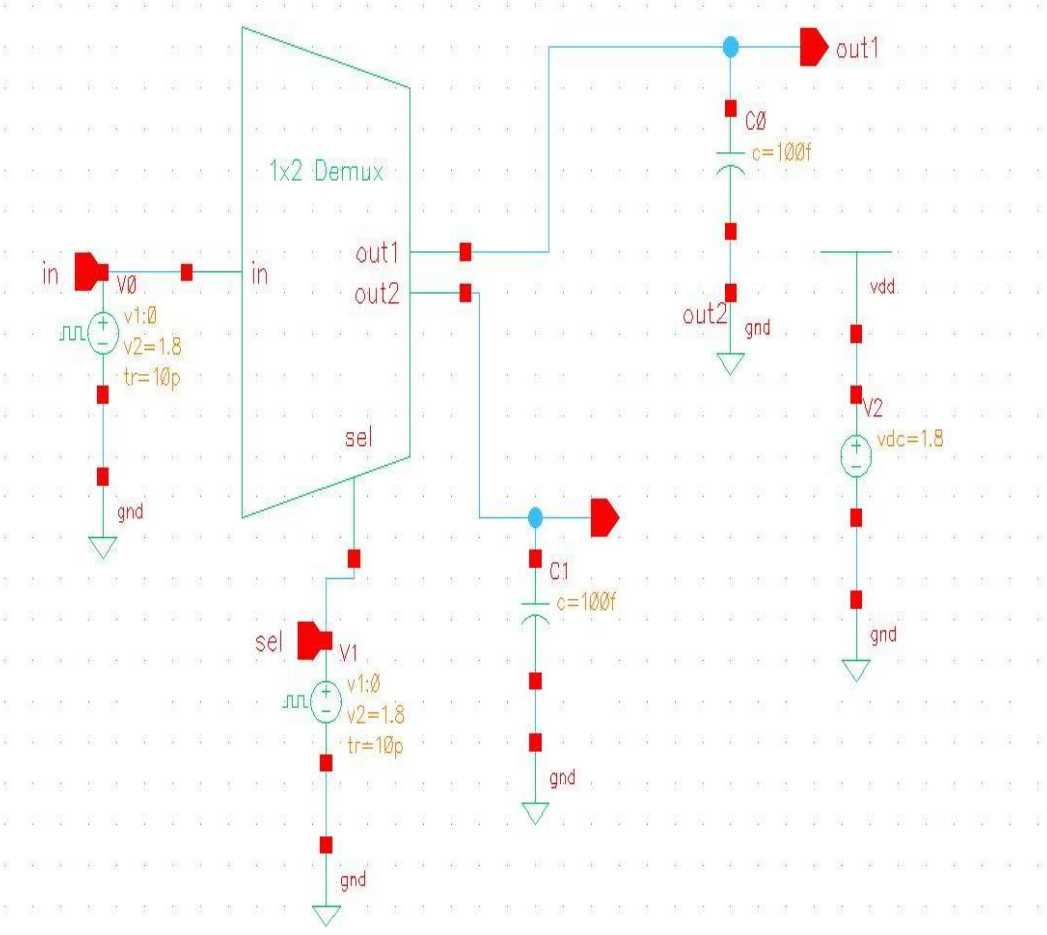

Figure 10.3: Test Schematic of 1x2 DeMultiplexer

Result:

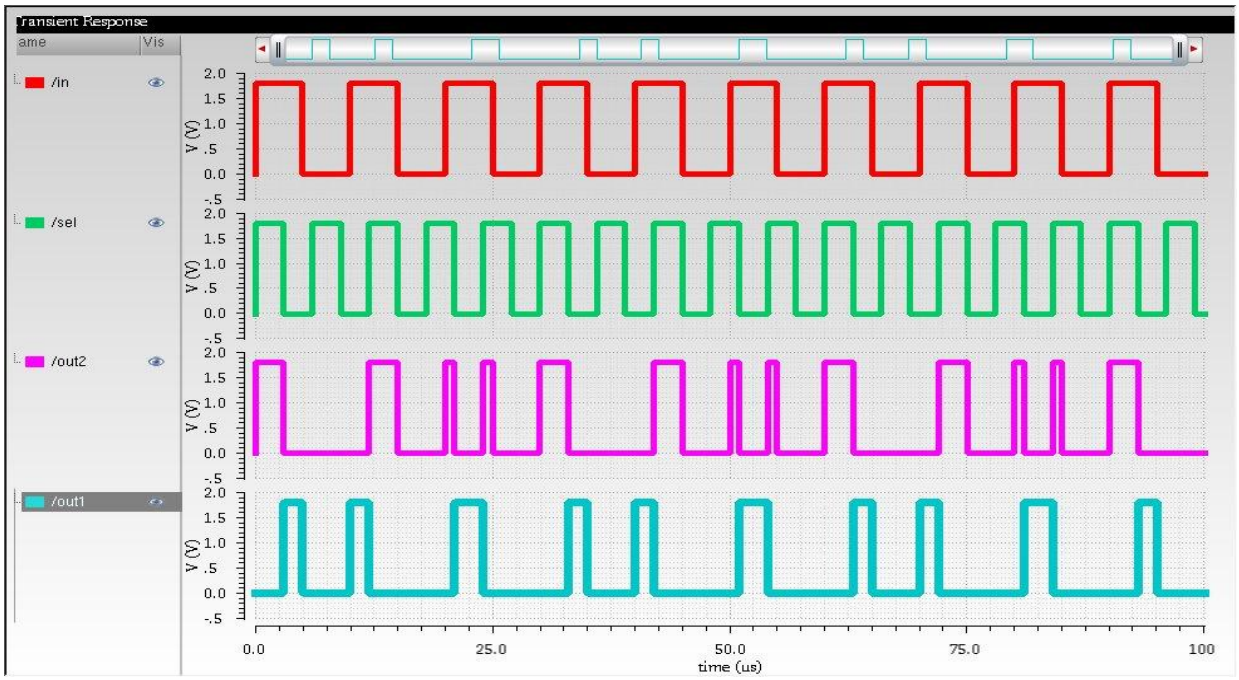

Figure 10.4: Transient Analysis

Observation: The CMOS 1×2 Demultiplexer was designed and tested in Cadence Virtuoso, demonstrating correct logic functionality. Transient analysis confirmed that the input signal was successfully routed to the selected output based on the control signal. A small propagation delay was observed, with power dissipation occurring mainly during switching due to capacitive effects. The created Demultiplexer symbol was successfully tested and integrated into circuit design, ensuring its reusability in complex logic circuits.

Conclusion: The CMOS 1×2 Demultiplexer was designed and simulated in Cadence Virtuoso, showing expected transient behavior and correct logic functionality. The symbol was successfully created, making it reusable for hierarchical circuit designs.