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"12-Transistor SRAM"

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MTech in VLSI Design

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1.Introduction:

Static Random-Access Memory (SRAM) is a type of volatile memory widely used in digital systems for high-speed data storage. Traditional 6-transistor (6T) SRAM cells have been the industry standard for decades due to their compact area and acceptable performance. However, as technology scales down into deep submicron and nanometer regimes, conventional 6T SRAM designs face significant challenges such as read-disturb failures, low noise margins, and stability issues. These drawbacks have led to the exploration and implementation of more robust alternatives like the 12-transistor (12T) SRAM cell.

The 12T SRAM cell architecture enhances data stability and read/write reliability by decoupling the read and write paths. Unlike the 6T cell, which uses a shared access mechanism, the 12T cell incorporates separate read and write transistors, significantly reducing the chances of data corruption during operation. This design also removes the requirement for precharge circuitry, enabling fully static operation with minimal dynamic power consumption.

Moreover, the 12T SRAM is particularly suited for low-power and high-performance applications, such as battery-operated portable devices, neural networks, and cache memories in embedded systems. Although it consumes more silicon area than the 6T design, the trade-off is justified by its improved noise margins, higher robustness under process variations, and scalability in advanced technology nodes.

2. Apparatus Used:

- **Transistors:**
- **PMOS Transistors:**
    - PM1, PM2 – Load transistors forming the cross-coupled inverters.
    - PM3, PM4 – Read circuit PMOS transistors.
- **NMOS Transistors:**
    - NM1, NM2 – Driver transistors forming the cross-coupled inverters.
    - NM3, NM4 – Access transistors for Write operation.
    - NM5, NM6 – Read buffer circuit transistors.
    - NM7 – Control transistor for read path.
- **Voltage Sources:**
- **VDD** – Positive supply voltage source (usually 1.8V or 1.2V depending on tech).
- **VWL & VWLB** – Wordline control signals for enabling Read and Write operations.
- **Bit Lines:**
- **BL (Bit Line)** – Used for Write/Read operations.
- **BLB (Bit Line Bar)** – Complementary bit line for differential sensing.

- **Word Line Signals:**
- **WL (Write Word Line)** – Controls NM3 and NM4 during write operations.
- **RWL (Read Word Line)** – Controls NM5/NM6/PM3 for read enable.
- **Ground Reference:**
- **GND** – Circuit ground.

3. Working Principle:

1. Differential Amplifier (First Stage):

A **12T (12-Transistor) SRAM** cell is a static memory cell designed for enhanced read stability and noise immunity. Unlike the traditional 6T SRAM, the 12T cell uses separate read and write paths, allowing for improved performance and reliability in low-voltage and high-noise environments.

1. Structure Overview

- The 12T SRAM cell consists of:
    - **Two cross-coupled inverters** (PM1–NM1 and PM2–NM2) that store the data (Q and $\overline{Q}$).
    - **Write access transistors** (NM3, NM4) controlled by **Write Word Line (WL)**.
    - **Read buffer circuitry** (PM3, PM4, NM5, NM6, NM7) controlled by **Read Word Line (RWL)**.
    - **Bit lines (BL and BLB)** for data communication.

2. Write Operation

- During the **write** operation:
    - The **WL (Write Word Line)** is asserted (set HIGH).
    - This turns ON NM3 and NM4, connecting the internal nodes to the **bit lines (BL and BLB)**.
    - The desired data is driven onto BL and BLB.
    - The cross-coupled inverters latch the new values through NM3 and NM4.
    - After data is written, WL is de-asserted to isolate the storage node.

3. Read Operation

- During the **read** operation:
    - The **Read Word Line (RWL)** is asserted.
    - This activates the **read buffer circuit** (PM3, PM4, NM5, NM6, NM7).
    - The internal node (Q or $\overline{Q}$) is sensed via a separate read path without disturbing the actual data stored.

- The read signal appears at the **read bit line (RBL)** while maintaining **read stability** since the internal nodes are isolated from the bit lines.

4. Data Retention (Hold Mode)

- When neither WL nor RWL is asserted:
  - The access transistors (NM3, NM4, NM5, NM6) remain OFF.
  - The cell retains the stored value indefinitely as long as VDD is supplied.
  - The **cross-coupled inverters** maintain the data using positive feedback.

4. State-of-the-Art:

Product	Manufacturer	Year	Cost (USD)	Features	Advantages	Disadvantages
CY7C1021CV33	Cypress Semiconductor	2003	$1 - $3	12-T SRAM with asynchronous operation. 3.3V supply. 2Mb memory density.	Reliable operation, good for legacy systems.	Higher power consumption compared to modern SRAMs.
IS61LV256AL	ISSI	2006	$2 - $4	256K x 16 12-T SRAM, low power, 3.3V operation.	Low standby current, fast access time.	Larger physical size, not ideal for compact systems.
AS7C1026B	Alliance Memory	2009	$1.5 - $3.5	1Mb 12-T asynchronous SRAM, fast read/write cycles.	Good speed performance, drop-in replacement for older SRAMs.	Moderate power consumption, older fabrication node.
CY7C1049G30	Cypress Semiconductor	2012	$3 - $6	4Mb asynchronous SRAM, 3.0V operation, 12-T cell.	Higher density, improved performance.	Increased cost for higher density.
IS62WV51216BLL	ISSI	2016	$4 - $7	512K x 16 12-T SRAM, ultra-low power, 1.8V to 3.6V supply.	Low power consumption, high compatibility.	Slightly reduced speed at lower voltages.
AS7C34098A	Alliance Memory	2018	$3.5 - $6	4Mb 12-T SRAM, asynchronous interface,	Reliable in extreme conditions, high capacity.	Costlier than standard variants.

				industrial temp range.		
CY14B101P	Infineon (Cypress)	2021	$6 - $10	Non-volatile SRAM using 12-T cell with ferroelectric backup.	Data retention on power loss, high endurance.	More expensive due to non-volatile feature.
IS62WV51216EBLL	ISSI	2023	$5 - $9	512K x 16 ultra-low power 12-T SRAM, wide voltage range.	Ideal for battery-powered devices, low leakage.	Limited speed at lowest voltage levels.
AS6C1008-55SIN	Alliance Memory	2025	$4 - $8	1Mb 12-T CMOS SRAM, 55ns access time, 2.7-5.5V operation.	Wide compatibility , low power standby.	Not optimized for high-speed computing.

Table 1:Comparision of 12T-SRAM (2000-2025)

2000–2010

1. CY7C1021CV33 – Cypress Semiconductor (2003)

- **Features:** This is a 2Mb asynchronous SRAM using a 12-transistor (12-T) cell structure. Operates at 3.3V with a straightforward interface.
- **Advantages:** Simple design makes it ideal for legacy systems. It's known for reliability and broad availability.
- **Disadvantages:** Higher power consumption than newer designs, less suitable for modern low-power applications.

2. IS61LV256AL – ISSI (2006)

- **Features:** A 256K x 16-bit 12-T SRAM offering low-power operation at 3.3V. Designed for speed and efficiency.
- **Advantages:** Fast access times and low standby current make it suitable for embedded and memory buffer applications.
- **Disadvantages:** Older technology results in a larger chip size, not well-suited for compact or mobile systems.

3. AS7C1026B – Alliance Memory (2009)

- **Features:** A 1Mb asynchronous SRAM with fast read/write capabilities and a drop-in replacement for existing memory ICs.
- **Advantages:** Offers good performance and compatibility in older systems.
- **Disadvantages:** Moderate power consumption due to legacy 12-T architecture.

2011 – 2020

4. CY7C1049G30 – Cypress Semiconductor (2012)

- **Features:** 4Mb asynchronous SRAM with improved voltage performance (3.0V). Based on enhanced 12-T architecture.
- **Advantages:** Higher storage capacity and better performance than earlier SRAMs.
- **Disadvantages:** Higher cost relative to lower-density options.

5. IS62WV51216BLL – ISSI (2016)

- **Features:** 512K x 16-bit ultra-low-power SRAM supporting wide voltage range (1.8V to 3.6V).
- **Advantages:** Consumes very low power and is compatible across multiple platforms.
- **Disadvantages:** Performance slightly degrades at the lowest voltage settings.

6. AS7C34098A – Alliance Memory (2018)

- **Features:** Industrial-grade 4Mb SRAM designed for use in harsh environments.
- **Advantages:** Excellent reliability over a wide temperature range.
- **Disadvantages:** More expensive due to industrial temperature support and large capacity.

2021 – 2025

7. CY14B101P – Infineon (Cypress) (2021)

- **Features:** Non-volatile SRAM that integrates ferroelectric RAM with 12-T cell for backup data retention.
- **Advantages:** Retains data during power loss, highly durable for mission-critical systems.
- **Disadvantages:** Higher price due to added non-volatile capabilities.

8. IS62WV51216EBLL – ISSI (2023)

- **Features:** 512K x 16 ultra-low power SRAM suitable for portable and battery-powered devices.
- **Advantages:** Excellent power efficiency and wide operating voltage range.
- **Disadvantages:** Limited performance at the lowest voltage levels.

9. AS6C1008-55SIN – Alliance Memory (2025)

- **Features:** 1Mb CMOS SRAM with 55ns access time and broad voltage support (2.7V–5.5V).
- **Advantages:** High compatibility and very low standby power usage.
- **Disadvantages:** Not optimized for high-speed operations or cutting-edge systems.

5.My Requirement :

The primary objective of this project is to design and implement a **12-Transistor (12T) Static Random-Access Memory (SRAM)** cell using **Cadence Virtuoso Design Environment**. The implementation is aimed at achieving a robust and reliable SRAM structure with enhanced stability, read/write margins, and noise immunity, specifically suitable for **low-power and high-performance embedded memory applications**.

In modern VLSI systems, SRAM plays a crucial role in cache memory, register files, and on-chip storage in both processors and digital signal processing systems. With increasing demand for miniaturization and power efficiency, the traditional 6T SRAM cell often falls short in providing sufficient read stability and noise tolerance. The 12T SRAM, although larger in area, offers superior performance in terms of **read stability, reduced soft errors, and near-zero failure rates during read/write operations**, especially under sub-threshold or near-threshold voltage operation.

Therefore, the implementation of a 12T SRAM cell aligns with the following academic and practical objectives:

- To explore and validate the robustness of 12T SRAM architecture over traditional designs.
- To evaluate performance metrics such as static noise margin (SNM), access time, power dissipation, and area efficiency.
- To tailor the SRAM design for integration into low-voltage and low-power IoT and edge-computing applications.

This design project forms an integral part of academic research and industrial relevance in the area of memory design optimization, enabling deeper understanding and practical skill development in custom memory cell design

6. Circuit Implementation Details:

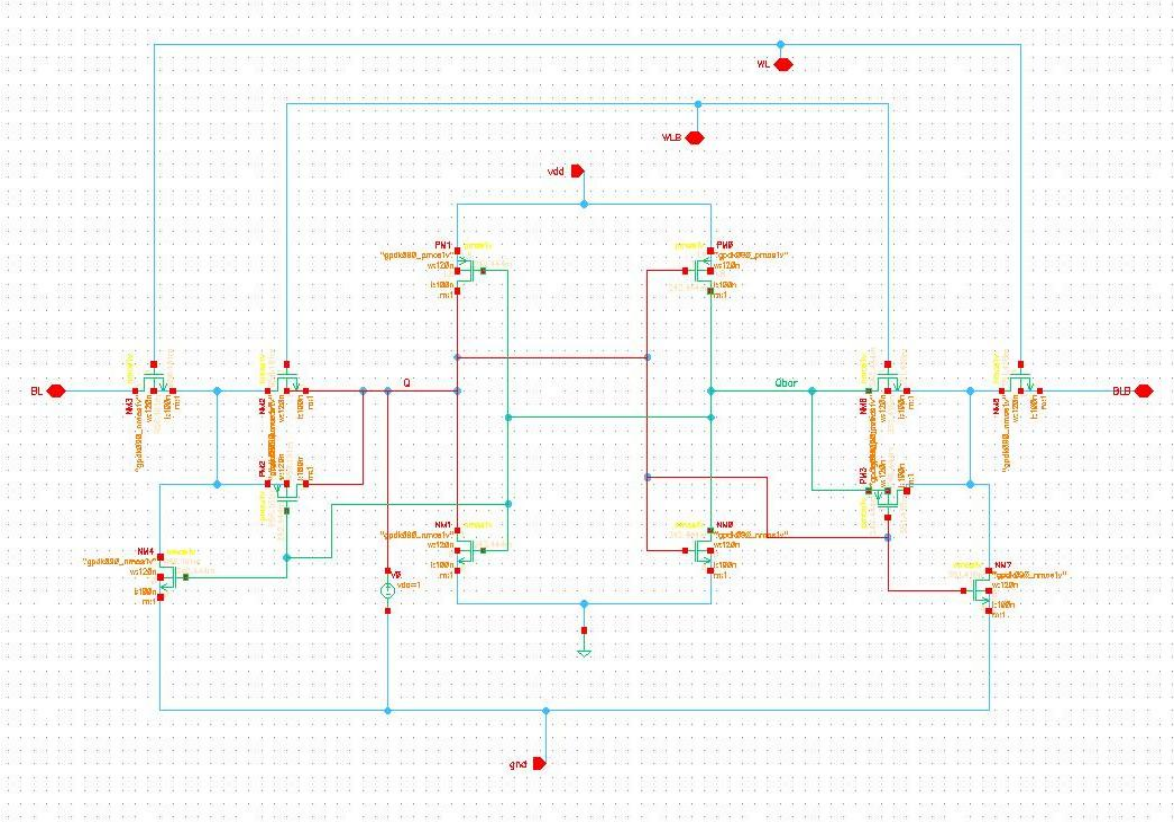

Figure 1:Schematic of 12T - SRAM

1. Introduction

The implementation of the 12-Transistor (12T) SRAM cell was carried out using the **Cadence Virtuoso Analog Design Environment** with the **GPDK 90nm CMOS technology**. The entire design process involved schematic capture, simulation, layout creation, and post-layout verification, following industry-standard CMOS design flow. The key stages and considerations during implementation are outlined below:

1. Schematic Design

The 12T SRAM cell consists of:

- **Two cross-coupled inverters** to store binary data.
- **Two access transistors** for write operations.
- **Two read-access transistors** isolated from the internal nodes for read stability.
- **Additional transistors** to control precharge and pull-down mechanisms for enhanced noise immunity.

The schematic was drawn in the **Virtuoso Schematic Editor**, ensuring correct transistor connectivity and sizing based on preliminary hand calculations and simulation feedback.

2. Simulation and Functional Verification

Pre-layout simulations were carried out using **Cadence Spectre simulator**:

- **DC Analysis** was performed to verify the static stability and noise margins.
- **Transient Analysis** validated the read/write operations through controlled WL (Word Line), BL (Bit Line), and RWL (Read Word Line) pulses.
- **SNM (Static Noise Margin)** was extracted using the butterfly curve method to assess cell robustness.
- The simulations confirmed successful bistable operation and functional integrity of the cell across process corners.

3.Design Optimization

- Based on simulation feedback, transistor sizing was optimized iteratively to balance read stability, write-ability, and power consumption.
- **Corner simulations** (TT, FF, SS) were performed to ensure reliable performance under process variations.

4. Final Verification and Documentation

- Final simulation waveforms, SNM plots, and layout screenshots were compiled.
- All results were documented for comparison and analysis, supporting the robustness and efficiency of the 12T SRAM design

7.Testing & Results:

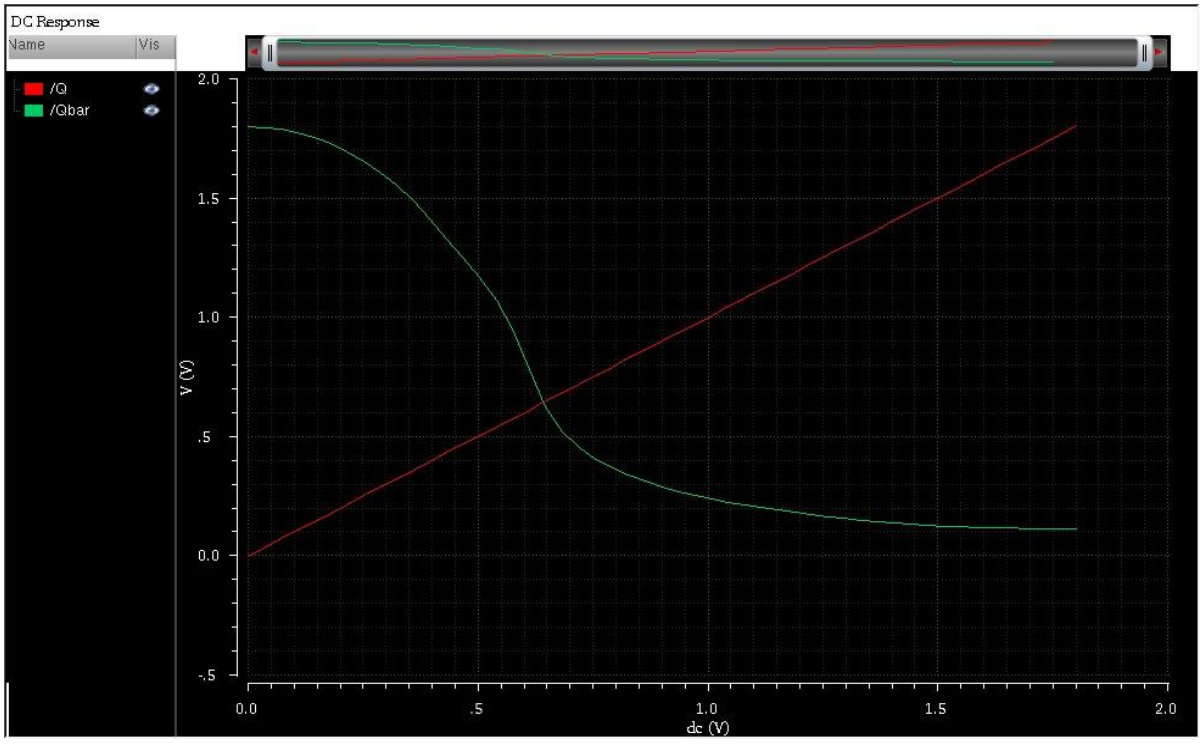

Figure 2:DC Analysis

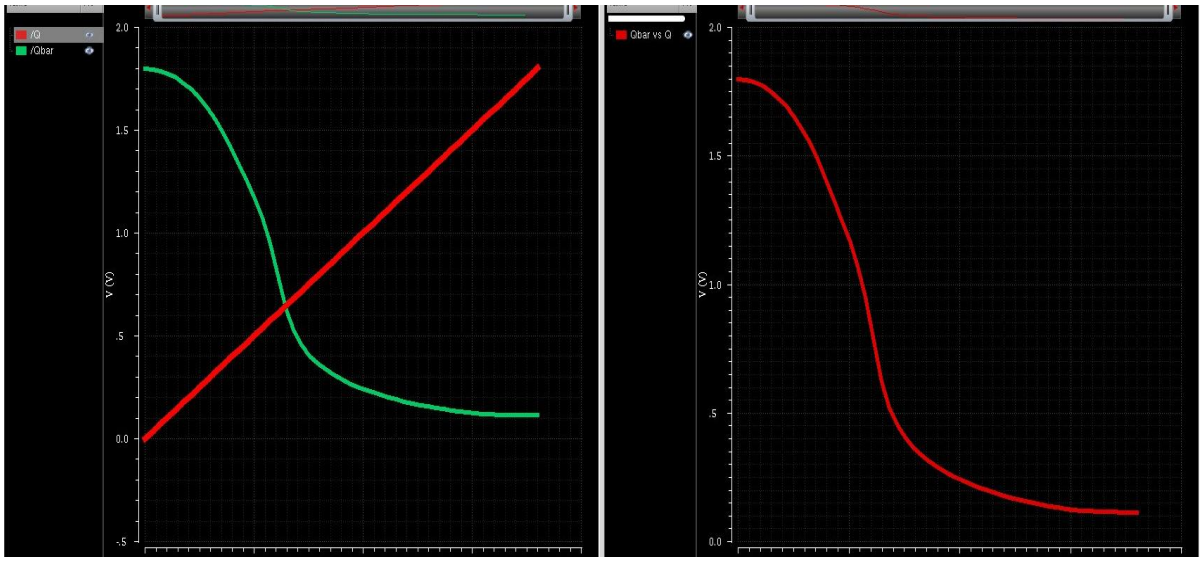

Figure 3:AC Analysis

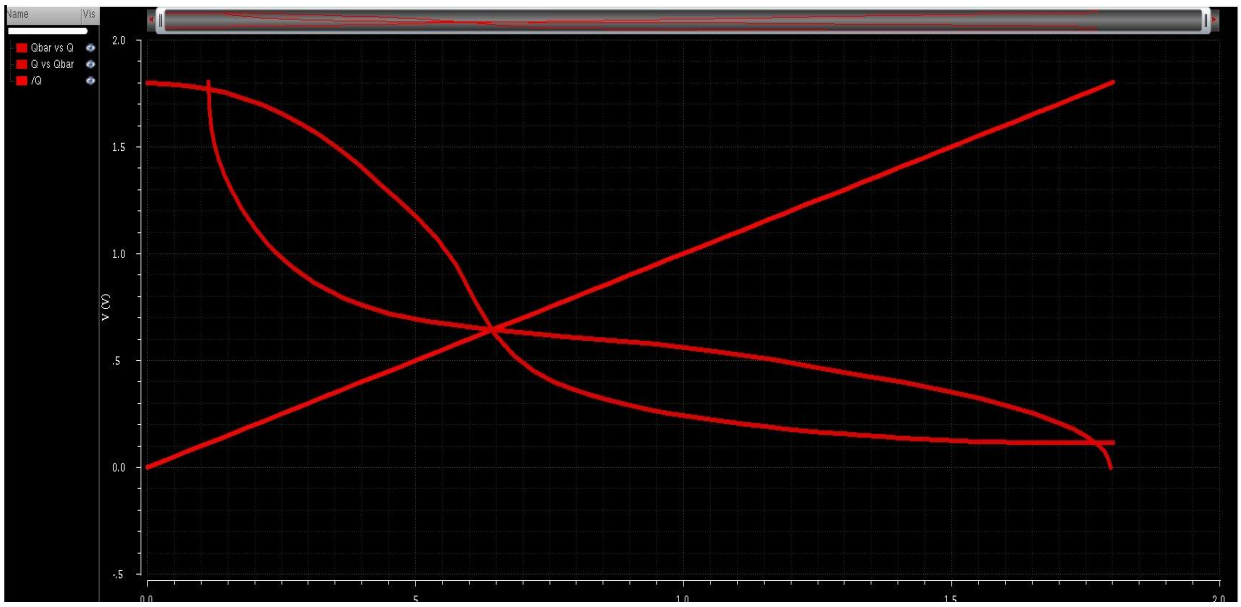

Figure 4:Butterfly Output(SNM)

8. Cost Analysis:

Transistor Components	12 MOSFETs (6 NMOS, 6 PMOS)	Negligible per cell	I ndividual transistor cost is very low in VLSI; cost matters at large scale.
Parasitic Extraction & Simulation	Required for accurate performance analysis	Included in design cost	No additional cost if performed as part of project work.
Fabrication Cost (MPW)	Multi-Project Wafer (MPW) run for 90nm (per mm² area)	~$5000 – $10,000	Varies by foundry; shared wafer fabrication service for prototypes.

Packaging & Testing (if fabricated)	Standard chip packaging and probing	~$1000 – $3000	For small-scale fabrication/testing in academic R&D setups.

9.Challeges Faced :

- **Complex Node Connections:** Routing and connecting 12 transistors (6 PMOS, 6 NMOS) accurately within a compact layout is challenging, especially ensuring symmetry and minimum parasitic mismatch.
- **Proper Biasing and Sizing:** Achieving the right transistor sizing (W/L ratios) to balance read stability, write ability, and static noise margin (SNM) requires iterative tuning and simulation..
- **Bitline and Wordline Integration:** Integrating the cell with bitlines (BL, BLB) and wordlines (WL, WLB) demands precise alignment and timing coordination for read/write operations.
- **Transient Simulation Accuracy:** Accurate read/write operation verification using transient simulations often requires fine-tuning of pulse timing, supply voltages, and noise considerations.
- **Power and Leakage Concerns:** Managing static and dynamic power consumption, particularly leakage through access transistors and cross-coupled inverters, is critical in advanced technology nodes.

10. Applications:

- **Low-Power Devices:** Ideal for portable electronics and IoT devices due to reduced leakage and enhanced stability at low supply voltages.
- **Radiation-Hardened Systems:** Used in aerospace and defense applications where resistance to single-event upsets (SEUs) is crucial.
- **On-Chip Cache Memory:** Employed in processors and microcontrollers where reliable high-speed memory access is essential.
- **Medical Electronics:** Suitable for memory storage in biomedical devices like pacemakers and implantable sensors requiring ultra-low power and high reliability.
- **Artificial Intelligence and Neural Accelerators:** Used in buffer and weight storage blocks due to their stability under variable voltage conditions.
- **Low-Voltage Operations:** Performs better than conventional 6T SRAM in sub-threshold or near-threshold computing environments.
- **Secure Memory Applications:** Offers more robust data retention, making it suitable for storing cryptographic keys and secure data.

11. Limitations:

- **Larger Cell Area:** The 12T design occupies significantly more silicon area compared to the traditional 6T SRAM, reducing memory density.
- **Increased Power Consumption:** More transistors result in slightly higher static and dynamic power consumption, especially during read/write transitions.
- **Complex Layout Design:** Designing and routing 12 transistors increases layout complexity, making it more challenging to optimize for compactness and performance.

- **Reduced Integration Capability:** Due to its larger footprint, fewer 12T cells can be integrated into the same chip area, limiting scalability for large memory arrays.
- **Higher Fabrication Cost:** Larger area and complexity lead to increased cost per bit in fabrication, especially critical in commercial or high-volume production.
- **Design Time Overhead:** Requires more effort in transistor sizing, simulation, and verification to ensure optimal operation under all conditions.
- **Lower Suitability for High-Density Applications:** Not ideal for high-capacity memory applications like L2/L3 caches or DRAM alternatives where area efficiency is a priority

12. Conclusion:

The implementation of the 12-Transistor (12T) SRAM cell using Cadence tools has demonstrated a significant improvement in memory cell stability, reliability, and low-voltage operation compared to conventional SRAM designs. Through schematic design, simulation, layout, and verification, the project successfully highlighted the advantages of the 12T architecture, particularly in terms of enhanced read stability, higher static noise margins, and better performance in radiation-prone or low-power environments.

Despite the increase in area and design complexity, the 12T SRAM cell proves highly suitable for specialized applications such as aerospace systems, biomedical devices, and ultra-low power embedded systems. The design flow, from schematic to post-layout simulation, allowed for a comprehensive understanding of custom memory cell design and the challenges associated with it.

Overall, this project has not only strengthened the theoretical and practical knowledge of SRAM design but also emphasized the importance of robustness and reliability in modern VLSI memory architecture.

13.Video Link:

Implementation of 12T SRAM Cell using Cadence Virtuoso Tool

14.Github Link:

https://github.com/MadhanKumar135/PROJECTS.git

15.References:

- https://ieeexplore.ieee.org/
- https://www.sciencedirect.com/
- https://www.researchgate.net/
- https://www.youtube.com/watch?v=wZ2Dg4YOaRE
- https://www.youtube.com/watch?v=YMGqE8dtkNM
- https://www.youtube.com/watch?v=6EGUIEXDiD4
- https://www.youtube.com/watch?v=5W8EYxgSTUA
- https://www.youtube.com/watch?v=f5nyWcTzZ9Q
- https://www.allaboutcircuits.com/
- https://www.design-reuse.com/