MAVEN SILICON
Centre of Excellence in VLSI

CELEBRATING 100 BATCHES

CELEBRATING 14 YEARS OF EXCELLENCE IN VLSI TRAINING

Advanced VLSI Design & Verification Course

Offline | Blended | Online

4500+
Global Alumni

250+
Hiring Partners

Hands-on Training

Placement Assistance

1:1 Mentoring

24/7 Lab Access & Support

MAVEN SILICON

Maven Silicon is a leading provider of VLSI training for students and professionals. We offer a range of high-quality VLSI training programs and internships, taught by experienced industry professionals, aimed at helping engineers to upskill and advance their careers in the fast-growing Semiconductor Industry. From digital design and verification to physical design and design for testing, Maven Silicon covers a wide variety of topics along with labs and projects through Industry standard EDA tools. Our state-of-the-art training facilities, coupled with innovative training methods, provide students with hands-on experience and a strong foundation in the latest VLSI technologies. Our curriculum is designed to meet the demands of the industry and is constantly updated to keep pace with the latest advancements. In addition, Maven Silicon offers flexible scheduling options and customized training programs to accommodate student's busy schedules.

With a commitment to excellence and a passion for empowering students and professionals, Maven Silicon is dedicated to providing the highest quality hands-on training to help engineers reach their full potential in the Semiconductor industry.

My vision is to create an excellent learning ecosystem of superior technical expertise, hands-on training experience, and industry-oriented courses with innovative learning processes.

For more than 14 years, Maven Silicon has been a benchmark for the VLSI training ecosystem in India, offering high-quality VLSI training courses for VLSI aspirants, professionals, and organizations across the globe.

Sivakumar P R
Founder and CEO

Our CEO, Sivakumar P R, has 25+ years of experience in the engineering and semiconductor industries. He has worked as a Verification Consultant in the top EDA companies like Synopsys, Cadence, and Mentor Graphics. During this tenure, he worked very closely with various ASIC and FPGA design houses and helped them to use the EDA solutions effectively for the successful tape-outs of multi-million gate designs.

To know more about our CEO, visit https://www.linkedin.com/in/sivapr/

Five reasons to muse with MAVEN SILICON

01 Dynamic VLSI courses designed and delivered by Industry experts

Maven Silicon is the Best VLSI training center which provides high-class industry standard VLSI training. The courses have been designed by industry experts, based on the job opportunities and career growth in the semiconductor industry and we keep updating our VLSI Curriculum as per the latest industry trends.

02 Superior Training Methodology and Infrastructure

Our training methodology is unique. It helps our students to learn even complex technologies in a short span of time and make them experts. 70% of the course time is dedicated to the labs, mini projects, and the final project. Our training courses help you to acquire the technical skills which are highly required to get a job in the semiconductor industry.

03 100% Placement Support

Maven Silicon provides 100% placement assistance to the trainees of job-oriented programs and keeps supporting them till they get placed. Our primary objective is to help electronics engineers successfully build a career in the semiconductor/VLSI Industries. We work closely with various VLSI products & services companies and identify the right opportunities. Most of our students have been successfully placed in reknowned semiconductor companies.

04 Excellent Support

Maven Silicon offers 1:1 mentoring and 24/7 online support through the MASS platform. The trainees have 24/7 lab access to enhance technical skills and participate in group discussions to gain new knowledge. Business communication sessions and mock interviews provide the necessary skills to succeed in a professional setting.

05 Free Internship

Maven Silicon's free internship program offers trainees the opportunity to gain hands-on experience working with complex IPs, VIPs, and SoCs, as well as a thorough understanding of the entire project life cycle from architecture to synthesis, making the trainees industry-ready.

EDA Partner

SIEMENS

Siemens is a leader in Electronic Design Automation. Its innovative products and solutions help engineers conquer design challenges in the seemingly daunting world of board and chip design.

https://eda.sw.siemens.com/en-US/

SYNOPSYS®

Synopsys is at the forefront of Smart Everything with the world's most advanced tools for silicon chip design, verification, IP integration, and application.

https://www.synopsys.com/

COURSE CURRICULUM

Advanced VLSI Design & Verification Course

21 Modules

OS - Linux Ubuntu | **EDA Tools -** Synopsys, Siemens, Xilinx, Aldec

Introduction to VLSI

Module I

- VLSI Design Flow
- ASIC vs FPGA
- RTL Design Methodologies
- Introduction to ASIC Verification Methodologies
- VLSI Design Flow Steps – Demo

Introduction to Linux

Module II

- Components of the UNIX system
- Directory Structure
- Utilities and Commands
- Vi Editor

Advanced Digital Design

Module III

- Introduction to Digital Electronics
- Arithmetic Circuits
- Data processing Circuits
- Universal Logic Elements
- Combinational Circuits – Design and Analysis
- Latches and Flip flops
- Shift Registers and Counters
- Sequential Circuits - Design and Analysis
- Memories and PLD
- Finite State Machine
- Microcontroller Design

Verilog HDL - RTL Coding and Synthesis

Module IV

- Introduction to Verilog HDL
  - Applications of Verilog HDL
  - Verilog HDL language concept
  - Verilog language basics and constructs
  - Abstraction levels
- Data Types
  - Type Concept
  - Nets and registers
  - Non-hardware equivalent variables
  - Arrays
- Verilog Operators
  - Logical operators
  - Bitwise and Reduction operators
  - Concatenation and conditional operators
  - Relational and arithmetic operators
  - Shift and Equality operators
  - Operators precedence
- Assignments
  - Type of assignments
  - Continuous assignments
  - Timing references
  - Procedures
  - Blocking and Non-Blocking assignments
  - Execution branching
  - Tasks and Functions
- Finite State Machine
  - Basic FSM structure
  - Moore Vs Mealy
  - Common FSM coding styles
  - Registered outputs
- Advanced Verilog for Verification
  - System Tasks
  - Compiler directives
  - Internal variable monitoring
  - File input and output

Verilog HDL - RTL Coding and Synthesis

Continued...

- Synthesis Coding
  - Unwanted latches
  - Synthesizable operators
  - RTL coding styles
  - Synthesis errors

Static Timing Analysis

Module V

- Introduction to STA
- Comparison with DTA
- Timing Path and Constraints
- Different types of clocks
- Clock domain and Variations
- Clock Distribution Networks
- How to fix timing failure
- Methods to improve timing

FPGA Architecture

Module VI

- PLD
  - General Structure and Classification
  - CPLD Vs FPGA
- Xilinx CPLD - Xc9500
  - Block Diagram of CPLD
  - Detailed study of each block
  - Timing Model
- Xilinx FPGA
  - FPGA Architecture
  - CLBs and Input/Output Blocks
  - Luts, SLICE DFFs
  - Dedicated MUXes
  - Programmable Interconnects
  - Architectural Resources
  - Power Distribution and Configuration
- FPGA Architecture of Xilinx Families

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Code Coverage

Module VII

- Statement coverage
- Branch Coverage
- Expression Coverage
- Path Coverage
- Toggle Coverage
- FSM - State, Transition coverage

Verilog Mini Project RTL Coding and Synthesis

Module VIII

- Project Specification Analysis
- Understanding the architecture
- Module level implementation and verification
- Building the top-level module

CMOS Fundamentals

Module IX

- Non-Ideal characteristics
- BJT vs FET
- CMOS Characteristics
- CMOS circuit design
- Fabrication Process Overview
- Transistor sizing
- Layout and Stick Diagrams
- CMOS Technology - Current Trends
- CMOS Processing Steps

Design Automation using Scripts - Perl

Module X

- Introduction to Perl
- Functions and Statements
- Numbers, Strings, and Quotes
- Comments and Loops
- Regular Expressions
- File Operations

ASIC Verification Methodologies

Module XI

- Directed Vs Random
- Functional verification process
- Monitors and reference models
- Stimulus Generation
- Verification Planning and management
- Bus functional model
- Coverage Driven Verification

SystemVerilog HVL

Module XII

- Introduction to SystemVerilog
  - New Data types
  - Tasks and Functions
  - Interfaces
  - Clocking blocks
- Object Oriented Programming and Randomization
  - OOP Basics
  - Classes - Objects and handles
  - Polymorphism and Inheritance
  - Randomization
  - Constraints
- Threads and Virtual Interfaces
  - Fork Join
  - Fork Join_any
  - Fork Join_none
  - Event controls
  - Mailboxes and semaphores
  - Virtual Interfaces
  - Transactors
  - Building verification environment
  - Testcases
- Callbacks
  - Facade Class
  - Building Reusable Transactors
  - Inserting Callbacks
  - Registering Callbacks

SystemVerilog HVL

Continued...

- Direct Programming Interface
- Functional Coverage
  - Coverage models
  - Coverpoints and bins
  - Cross coverage
  - Regression testing

Advanced SystemVerilog

Module XIII

- Environment Configuration
- Reference Models and Predictor Logics
- Using Legacy BFMs
- Scenario Generation
- Testcases - Random, Directed, and corner case
- Coding styles for VIP

UVM - Universal Verification Methodology

Module XIV

- Introduction to UVM Methodology
- Overview of Project
- UVM TB Architecture
- Stimulus Modeling
- Creating UVCs and Environment
- UVM Simulation Phases
- Testcase Classes
- TLM Overview
- Configuring TB Environment
- UVM Sequencers
- Connecting DUT-Virtual Interface
- Virtual Sequences and Sequencers
- Creating TB Infrastructure
- Connecting multiple UVCs
- Building a Scoreboard
- Introduction to Register Modeling
- Building reusable environments

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21 Modules

OS - Linux Ubuntu | **EDA Tools -** Synopsys, Siemens, Xilinx, Aldec

Verification Mini Project

Module XV

- Verification and RTL sign-off
- Project specification analysis
- Defining verification plan
- Creating Testbench architecture
- Implementing the transactors - Generator, Driver, Receiver, and Scoreboard
- Defining Transaction
- Implementing the coverage model
- Building the top-level verification environment
- Building regression test suite
- Coverage Analysis and Coverage Closure

Interfaces and Protocols

Module XVI

- Lectures by Industry Experts

Verification Planning and Management

Module XVII

- Verification Plan
- TB Architecture
- Coverage Model
- Tracking the simulation process
- Building regression test suite
- Test suite optimization

Assertion Based Verification - SVA

Module XVIII

- Introduction to ABV
- Immediate Assertions
- Simple Assertions
- Sequences
- Sequence Composition
- Advanced SVA Features
- Assertion Coverage

Business communication

Module XIX

- Transition from College to Corporate
- Interpersonal skills and Presentation Skills
- Email Etiquette
- Resume writing
- Mockup Interviews Technical/HR
- Interview Skills: Group Discussion and HR Round Preparation

Design for Testability - DFT

ELECTIVE MODULE

- Introduction to DFT
- Types of Testing
- Basic Testing Principles
- Fault Collapsing
- Introduction to Tessent Shell
- Structured Techniques
- BIST & Boundary Scan
- DFT Techniques - Ad-hoc Techniques
- Scan Chain
- Test Coverage
- Fault Change
- Tessent Shells
- System Modes & TSDB

RISC V Processor

Module XX

- RISC-V Instruction Set Architecture
  - RISC-V processor overview
  - RISC-V ISA Overview
  - RV32I - R and I Type Instruction
  - RV32I - S and B Type Instructions
  - RV32I - J and U Type Instructions
  - RV32I - Assembly Programs
- RISC-V RV32I RTL Architecture Design
  - RISC-V Execution Stages and Flow
  - RISC-V Register File and RV32I Instructions Format
  - RV32I - R and I Type ALU Datapath
  - RV32I - S Type ALU Datapath - Load and Store
  - RV32I - B and U Type ALU Datapath
  - RV32I - J Type ALU Datapath - JAL and JALR
- RISC-V RV32I 5 Stage Pipelined RTL Design
  - CPU Performance and RISC-V 5 Stage Pipeline Overview
  - RISC-V 5 Stage Pipeline - Data Hazards and Design Approach
  - RISC-V 5 Stage Pipeline - Control Hazards and Design Approach

Industry Standard Project

Module XXI

- Design specification analysis
- Creating the design architecture
- Partitioning the design
- RTL coding in Verilog
- RTL functional verification
- RTL Synthesis
- Building regression test suite
- Coverage Analysis and Coverage Closure

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