

Simulation and Analysis of Memristor-Based Circuits Using LTspice

Atigadda MadhanKumar Chetty
Department of Electrical and Electronic Engineering
Gitam University
Email: matigadd@gmail.com

Abstract—This paper presents a comprehensive simulation-based analysis of memristors, highlighting their nonlinear properties and memory-like behavior. Using LTspice and related circuit schematics, we explore the memristor's I-V characteristics, circuit response, and structural implementation including a crossbar array. This study aims to showcase the applicability of memristors in non-volatile memory and neuromorphic computing through practical circuit modeling and GUI-based visualization. The memristor, theorized by Leon Chua and later physically realized by HP Labs, is a fundamental passive circuit element that establishes a relationship between electric charge and magnetic flux. Unlike traditional resistors, capacitors, and inductors, the memristor exhibits memory-dependent resistance, making it highly promising for next-generation computing architectures, such as non-volatile memory and neuromorphic systems. This project presents a comprehensive simulation and modeling approach for memristor behavior using the Joglekar window function within LTspice. A custom symbol was created to emulate memristive behavior accurately, followed by the development of basic and advanced circuits, including a 2×2 memristor crossbar array with parasitic elements. Furthermore, a graphical user interface (GUI) was designed to allow interactive simulation, enabling users to visualize I-V characteristics and dynamic resistance changes in real time. The results confirm the characteristic pinched hysteresis loop and support the theoretical behavior of memristors. This work serves as a foundational step for further exploration of memristor-based analog computing and memory technologies.

Index Terms—Memristor, LTspice, Crossbar Array, Neuromorphic Computing, Circuit Simulation

I. INTRODUCTION

The memristor is a fundamental passive circuit element proposed by Leon Chua in 1971 and later physically realized by HP Labs. It offers a direct relationship between electric charge and magnetic flux linkage. Its resistance changes based on the history of charge flow, making it highly useful in circuits requiring memory without power. This work provides a visual and simulation-based understanding of memristor behavior using LTspice and GUI tools. The memristor, short for "memory resistor," is recognized as the fourth fundamental passive circuit element, alongside the resistor, capacitor, and inductor. First theoretically proposed by Leon Chua in 1971, the memristor establishes a direct relationship between charge and magnetic flux, effectively storing information as resistance. Its value is not fixed but varies based on the history of current that has passed through it, making it inherently non-volatile. This unique property allows memristors to retain

information even when power is turned off, offering immense potential in memory storage, neuromorphic computing, and adaptive learning systems.

II. WORKING PRINCIPLE

A memristor functions as a variable resistor whose resistance is dependent on the integral of current. This behavior is often modeled with window functions such as the Joglekar model, allowing for a gradual and history-dependent change in resistance. LTspice simulations replicate this behavior by using nonlinear dependent sources and switching resistances to reflect memristive effects. The memristor, or memory resistor, operates based on the principle that its resistance changes according to the amount and direction of charge that has flowed through it. This behavior creates a history-dependent resistance, meaning the device can "remember" its past electrical activity. This unique property is what distinguishes the memristor from traditional passive components.

Mathematically, the memristor is defined by the relationship between the charge $q(t)$ and the magnetic flux $\phi(t)$, such that:

$$M(q) = \frac{d\phi}{dq}$$

where M is the memristance, a charge-dependent resistance. In practice, this means that the voltage across the memristor is a function of the current and its internal state:

$$v(t) = M(x) \cdot i(t)$$

Here, x represents the internal state variable of the memristor, which evolves over time based on the current flowing through it. The dynamics of this internal state are typically modeled using differential equations. In this project, we have employed the Joglekar window function model, which modifies the state update equation to prevent boundary saturation and maintain numerical stability. The state update equation with the window function is expressed as:

$$\frac{dx}{dt} = k \cdot i(t) \cdot f(x)$$

$$f(x) = 1 - (2x - 1)^{2p}$$

III. WHY USE MEMRISTORS?

Memristors provide significant benefits in emerging electronic systems:

- **Non-volatility:** Retains resistance state even without power.
- **Scalability:** Nanoscale dimensions allow for high-density storage.
- **Energy Efficiency:** Low power requirements make them ideal for portable and embedded systems.
- **Neuromorphic Capability:** Can mimic the plasticity of synapses in neural networks.
- **Energy Efficiency and Non-Volatility:** Memristors retain their resistance state even when the power is turned off, enabling ultra-low power standby modes. This non-volatile nature makes them ideal for memory applications where energy efficiency is crucial, such as in portable electronics, embedded systems, and IoT devices.

IV. SIMULATION AND VISUAL RESULTS

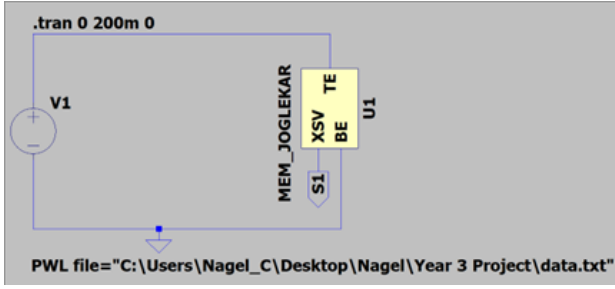


Fig. 1: Basic Memristor Circuit in LTspice

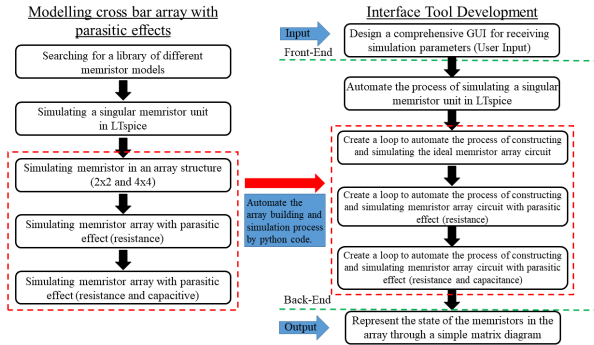


Fig. 2: Flowchart outlining the step-by-step methodology of the memristor modeling and simulation project. It begins with a literature review and model selection to identify a suitable memristor equation (Joglekar window function).

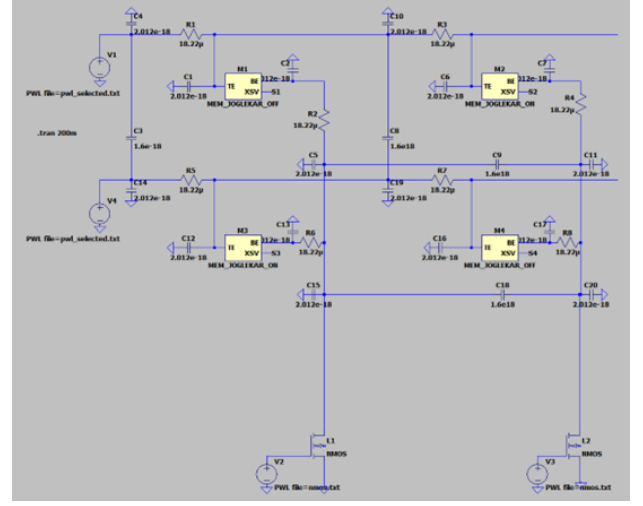


Fig. 3: A 2x2 grid schematic representing a memristor crossbar array with line resistance and parasitic capacitance. This figure illustrates how real-world effects such as wire resistance and interconnect capacitance are incorporated into the simulation model.

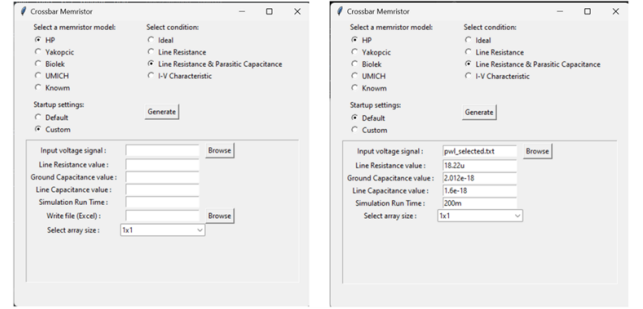


Fig. 4: A graphical user interface (GUI) built for parameter tuning and circuit analysis. Users can interactively vary the memristor's properties and observe its electrical response in real-time, enabling intuitive design and testing.

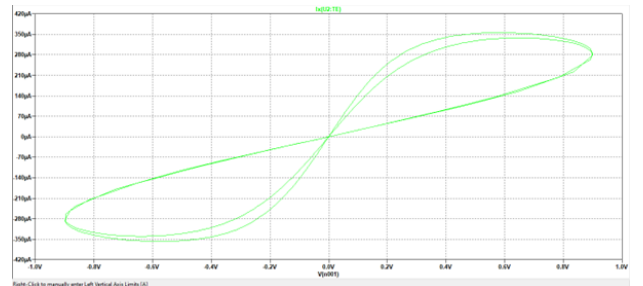


Fig. 5: Simulated current-voltage (I-V) curve for the Joglekar memristor, showing the characteristic pinched hysteresis loop. This verifies the proper implementation of the memristive behavior and the validity of the LTspice model.

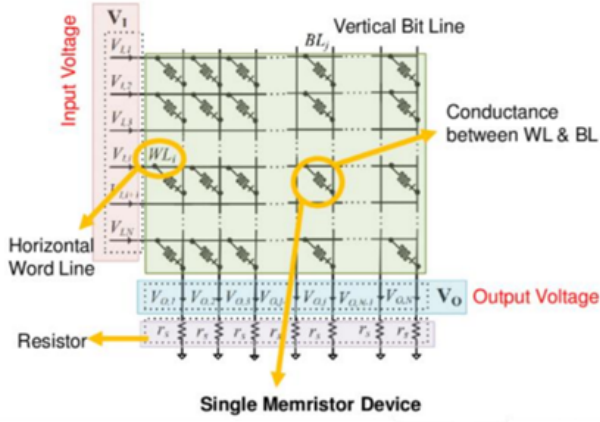


Fig. 6: A conceptual illustration of a memristor crossbar array used in neuromorphic and non-volatile memory applications. Each junction represents a memristive element capable of storing a weight or logic state.

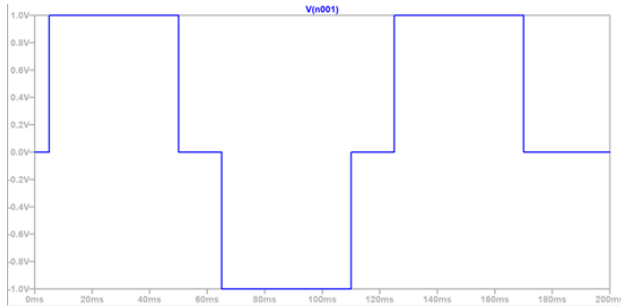


Fig. 7: Input sinusoidal voltage waveform applied to the memristor circuit. This signal helps evaluate the memristor's dynamic response to alternating current and determine how its resistance evolves over time.

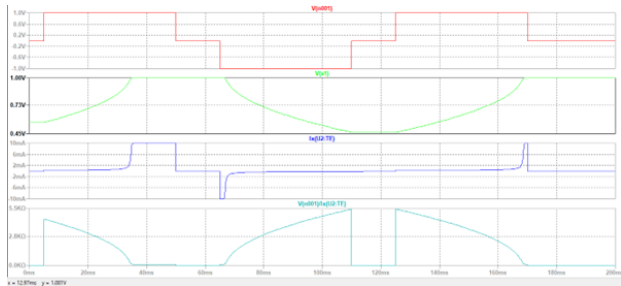


Fig. 8: Simulated memristor behavior showing variation in resistance over time. The plot confirms the memory effect of the memristor, where resistance is influenced by the integral of past current.

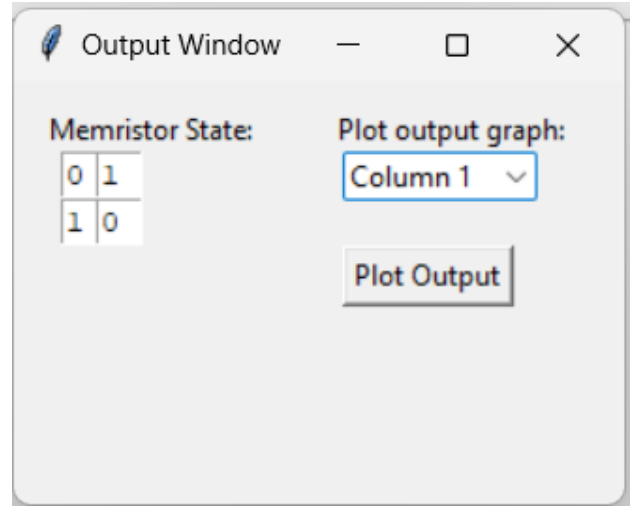


Fig. 9: Output voltage waveform from the 2x2 resistive grid simulation. This result shows how voltages are distributed across the memristor array, useful for memory read/write operations in crossbar-based architectures.

V. CONCLUSION

This project demonstrates the significance of memristors in next-generation electronic circuits. Through schematic simulations and GUI-based design tools, key features such as I-V response and structural modeling were explored. The results support the memristor's potential in both memory applications and neuromorphic architectures.

REFERENCES

- [1] L. O. Chua, "Memristor — The missing circuit element," *IEEE Transactions on Circuit Theory*, vol. 18, no. 5, pp. 507–519, Sep. 1971.
- [2] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," *Nature*, vol. 453, no. 7191, pp. 80–83, May 2008.
- [3] Y. N. Joglekar and S. J. Wolf, "The elusive memristor: properties of basic electrical circuits," *Eur. J. Phys.*, vol. 30, no. 4, pp. 661–675, 2009.
- [4] R. S. Williams, "How we found the missing memristor," *IEEE Spectrum*, vol. 45, no. 12, pp. 28–35, 2008.
- [5] S. Pi et al., "Memristor crossbar arrays with 4.5 nm half-pitch and 2 nm critical dimension," *Nature Nanotechnology*, vol. 14, pp. 35–39, 2019.
- [6] S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviya, P. Mazumder, and W. Lu, "Nanoscale memristor device as synapse in neuromorphic systems," *Nano Letters*, vol. 10, no. 4, pp. 1297–1301, Apr. 2010.
- [7] J. J. Yang, D. B. Strukov, and D. R. Stewart, "Memristive devices for computing," *Nature Nanotechnology*, vol. 8, no. 1, pp. 13–24, Jan. 2013.
- [8] S. Kvaterny, E. G. Friedman, A. Kolodny, and U. C. Weiser, "TEAM: Threshold adaptive memristor model," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 1, pp. 211–221, Jan. 2013.
- [9] Y. V. Pershin and M. Di Ventra, "Memory effects in complex materials and nanoscale systems," *Advances in Physics*, vol. 60, no. 2, pp. 145–227, Mar. 2011.
- [10] A. Mehonic and A. J. Kenyon, "Emulating the electrical activity of the neuron using a silicon oxide RRAM cell," *Frontiers in Neuroscience*, vol. 14, p. 117, Feb. 2020.