Analog IC Design : Assignment-2

Spring 2026, IIIT Hyderabad, Due date : 23 Feb, 2026 (18:00 hrs)

(Instructor: Prof. Abhishek Srivastava, CVEST, IIIT Hyderabad)

Instructions:

1. Submit your assignment as a single pdf (Name_RollNo.pdf) at moodle on or before the due date
2. Hand-written/typed (latex/word) submissions are allowed
3. Report should be self explanatory and must carry complete solution - Answers with schematics, netlist, annotated waveforms, inference/discussion on results
4. Use the 180 nm SCL technology file provided earlier for SPICE simulations

---

1. Considering $V_{DS} = 1$V, for an n-channel MOSFET ($\frac{W}{L} = \frac{500n}{180n}$) in the previously given SCL 180 nm technology,
   (a) Plot I_D vs V_{GS} and g_m vs V_{GS} for i) $V_{SB} = 0$V, ii) $V_{SB} = 0.9$V, iii) $V_{SB} = -0.9$V. Superimpose all I_D plots in same graph and all g_m plots in other graph. Clearly show schematic used for the simulation by mentioning sizes, bias voltages/currents and variable(s) swept for the simulation. Briefly discuss the variations in I_D and g_m values for three cases - cause and does it match with intuitive-thinking/analytical-models.
   (Hint: Use deriv command to plot g_m vs V_{GS})
   (b) Find $I_D = I_{D0}$ for $V_{SB} = 0$V and $V_{GS} = 0.9V$.
   (c) Report the variation in g_m for the cases for $V_{GS} = 0.9V$ considering $V_{SB} = 0$ as the reference case.
   (d) Report the variation in g_m for the cases for $I_D = I_{D0}$ considering $V_{SB} = 0$ as the reference case.
2. Consider an n-channel MOSFET as shown in Fig. 1. Consider $V_{dd} = 1.8$V.

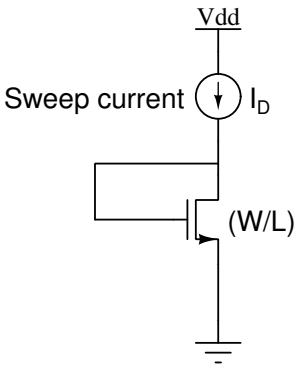

Figure 1

   (a) Sweep I_D from 10 μA to 1 mA and plot g_m vs I_D curve using $g_m = 2I_D/(V_{GS} - V_T)$ for (W/L) = $\frac{3\mu m}{1\mu m}$ and (W/L) = $\frac{0.45\mu m}{0.18\mu m}$. Which case gives g_m plot closer to expected form and why?
   (Hint : Run DC. Use V_T extracted from previous assignment.)

(b) What are the maximum value of transconductance ($g_{m_{max}}$) do you observe in two cases. At what values of I_D, g_m saturates. For what value of I_D, a transconductance ($g_{m_{use}}$) of $0.8 \times g_{m_{max}}$ can be obtained.

(c) How will you scale the design parameters to obtain a required transconductance ($g_{m_{req}}$) of $4 \times g_{m_{use}}$ to ensure same speed of the circuit. Show the results' (g_m vs I_D) plot for both the cases.

3. Use the transconductance efficiency $\frac{g_m}{I_D}$ based approach discussed in lecture and design a common source amplifier with an ideal current source load to achieve following specifications: DC voltage gain $A_v > 60$, unity gain bandwidth $f_u = 100$ MHz, load capacitance $C_L = 1$ pF, Supply $V_{DD} = 1.8$ V, a design parameter $V^* = \frac{2I_D}{g_m} = 200$ mV. Design should try to minimize the power consumption, maximize the -3 dB bandwidth, maximize the output swing for the given gain.

   (a) Plot intrinsic gain $g_m r_o$ with respect to V_{DS} for different channel length (L) and choose the channel length for the desired gain. From the plot identify the output voltage swing range.

   (b) Plot $g_m r_o$ vs V_{DS} for the chosen L across process (tt, ff, ss) and temperatures: {-40, 25, 80, 125} °C.

   (c) Show the necessary calculations and simulations for estimating the required values of g_m, I_D and W.

   (d) Perform transient analysis to demonstrate the functionality of the amplifier and attach clearly annotated plots. Measure and report THD for the maximum input swing. Attach necessary simulation results.

   (e) Perform AC analysis and verify f_u. Report f_{-3dB} and AC gain from the plots across process and temperature corners mentioned before.

4. Design a common source amplifier (shown in Fig. 2) with a resistive load of 10 kΩ for a voltage gain > 5 and an overdrive voltage (of input and cascode transistors) of 200 mV. The minimum input signal frequency is 100 Hz. Design for the minimum power consumption. Clearly write your assumptions (if any).

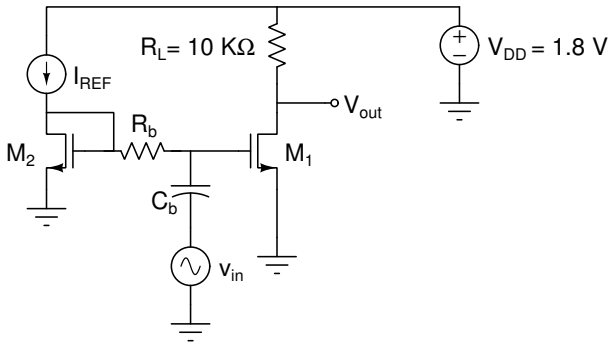

Figure 2

   (a) Show the design procedure with calculations for sizes of transistors, I_{REF}, C_b and R_b. What is the overall power consumed by your amplifier.

   (b) Give the transient (4-5 cycles) simulations plots showing the gain and considering $v_{in} = 10sin(2\pi(1000)t)$ mV.

   (c) Show the AC response plots ($20log|A_v|$ vs frequency) and find unity bandwidth frequency (f_u). Vary the frequency from 1 Hz to 1 GHz for AC simulations.

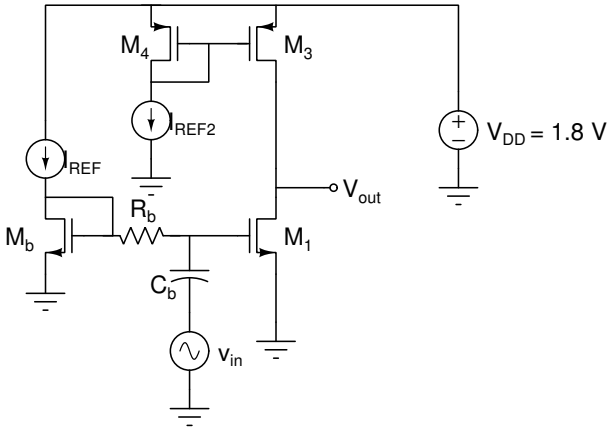

Figure 3

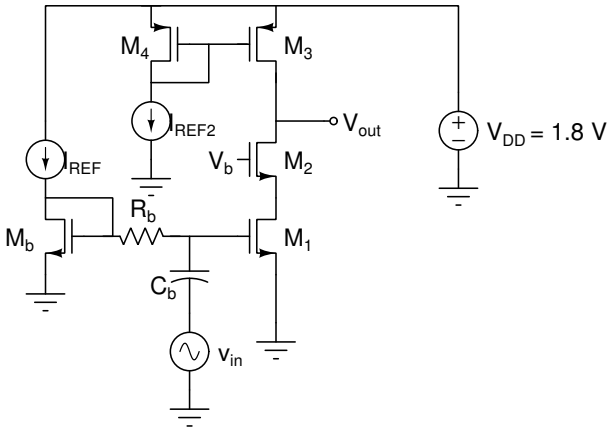

Figure 4

(d) Replace the load resistor with a PMOS current source load as shown in Fig. 3 and redesign the circuit for a voltage gain > 15. Show the design procedure, transient and AC response of this amplifier also.

(e) For the bias current obtained in part (d), design a cascode amplifier (as shown in Fig. 4) by stacking a cascode device of roughly the same size as input device. What is the gain of this cascode amplifier. Does the gain match with the hand calculations. Show the design procedure, transient and AC response of this amplifier also.

(f) Tabulate the comparison of the three amplifiers for power, gain and output voltage swing. Table should contain quantitative comparison and remark explaining the results. Support your comparison with appropriate simulation results.

5. **Suggested practice problems: Single stage amplifiers (Razavi), CMOS amplifiers (Allen and Holberg).** (No need to submit it.)
