Analog IC Design : Assignment-1, Spring 2026

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Due date : 19 Jan, 2026 (18:00 hrs)

Instructions:

1. Submit your assignment as a single pdf (Name_RollNo.pdf) on moodle on or before the due date
2. Hand-written/typed (latex/word) submissions are allowed
3. Report should be self explanatory and must carry complete solution - Answers with schematics, netlist, annotated waveforms, inference/discussion on results
4. Print your name and roll number in your graphs
5. Use the 180 nm TSMC/SCL/IBM technology file given in tutorial for SPICE simulations

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1. Install LTSPICE. Run the given simulations (in tutorial) and observe the results (no need to submit this part).
2. Use the given SCL model file and plot I_D vs V_{GS} for $\frac{10\mu}{1\mu}$ NMOS transistor and estimate its V_T from the graph for the following cases : (Suggested read: Operation and Modeling of the MOS Transistor, second ed, by Tsividis (sections 10.4 and 4.10))
   (a) V_{DS} = 50 mV and V_{GS} is swept from 0 to 1.8 V in a step of 0.1 V
   (b) V_{DS} = 1.8 V and V_{GS} is swept from 0 to 1.8 V in a step of 0.1 V
   (c) Do you observe any difference in V_T values in case (a) and (b) ? If yes, explain why and which one will you use for hand calculations with simple MOS models?
   (d) Estimate technology parameter μC_{ox} from simulations and simple MOS models.
   (e) Plot $\log(I_D)$ vs V_{GS} for V_{DS} = 50 mV and V_{DS} = 1.8 V. Clearly mark subthreshold region on graphs. From plots and using simple exponential relationship $I_D = I_0 exp(\frac{V_{GS}}{\eta V_{Thermal}})$, estimate the process parameter η.
3. Finding unity current gain frequency f_T of technology node.
   (a) Use minimum size NMOS and find the f_T (unity current gain frequency, where $\frac{|i_d|}{|i_g|} = 1$) for the 180 nm TSMC, 180 nm SCL and 130 nm IBM technology. You are expected to show the method, plots and your explanation.
   (b) Suggest a method to compare the intrinsic gains ($g_m r_o$) of minimum size transistors for the three model files given to you. Show the schematic, netlist, simulation results with necessary discussions.

   (Hint: Useful commands: .lib 'ts18sl_scl.lib' tt_18, .include TSMC_180nm.txt, .include IBM130nm.txt, use nmos4 and edit model name as n18.1, CMOSN130, CMOSN calculate AS/AD/PS/PD and substitute in MOS parameters)
4. Using TSMC model file, draw a circuit for an analog amplifier using complementary NMOS (5μm/1μm), PMOS (10μm/ 1μm) configuration discussed in class. Use only one DC source $V_{DD} = 1.8$V and generate other voltages using resistive dividers. From simulations find out the bias point and maximum input amplitude (A_{max}) for the maximum gain and THD<10%. Report the bias point and the maximum gain. How will you cascade two such amplifiers ? Show the scheme with the exact schematic and simulation results (gain and THD) for the cascaded amplifier for A_{max}.
