Analog IC Design: Assignment-2

Spring 2026, IIIT Hyderabad

Name: _____ Roll No: _____

Due Date: February 23, 2026 (18:00 hrs)

Instructions

- Technology: 180 nm SCL technology file.
- Content: Schematics, netlists, annotated waveforms, and inference/discussion are required for each solution.

Question 1: n-channel MOSFET Characteristics

Considering $V_{DS} = 1\text{V}$ and $\frac{W}{L} = \frac{500\text{n}}{180\text{n}}$:

(a) I_D vs V_{GS} and g_m vs V_{GS} Plots

Cases: (i) $V_{SB} = 0\text{V}$, (ii) $V_{SB} = 0.9\text{V}$, (iii) $V_{SB} = -0.9\text{V}$.

Schematic and Simulation Setup

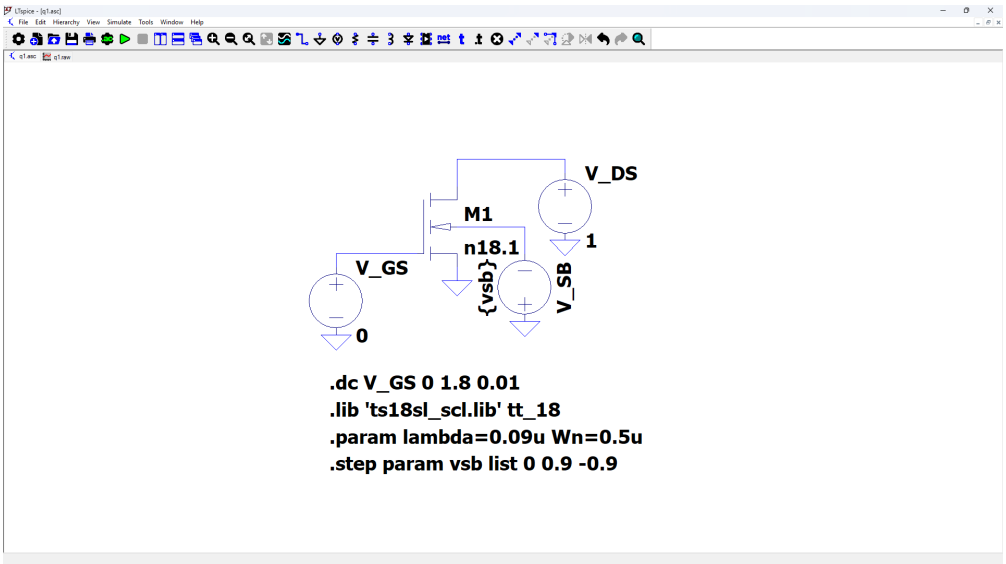

Figure 1: Schematic for I_D vs V_{GS} and g_m vs V_{GS} simulations.

Simulation Results (Plots)

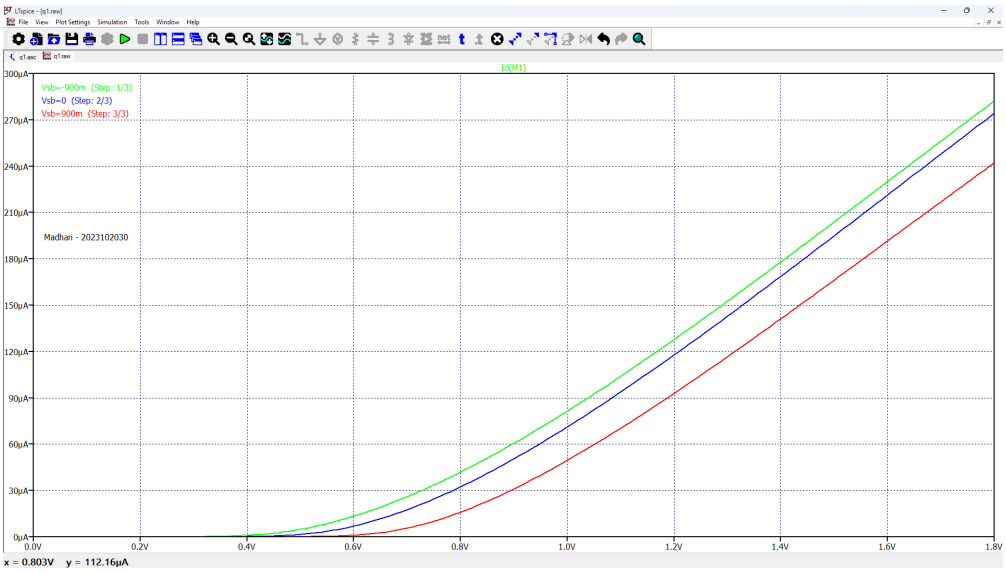

Figure 2: Simulated I_D vs V_{GS} for different V_{SB} values.

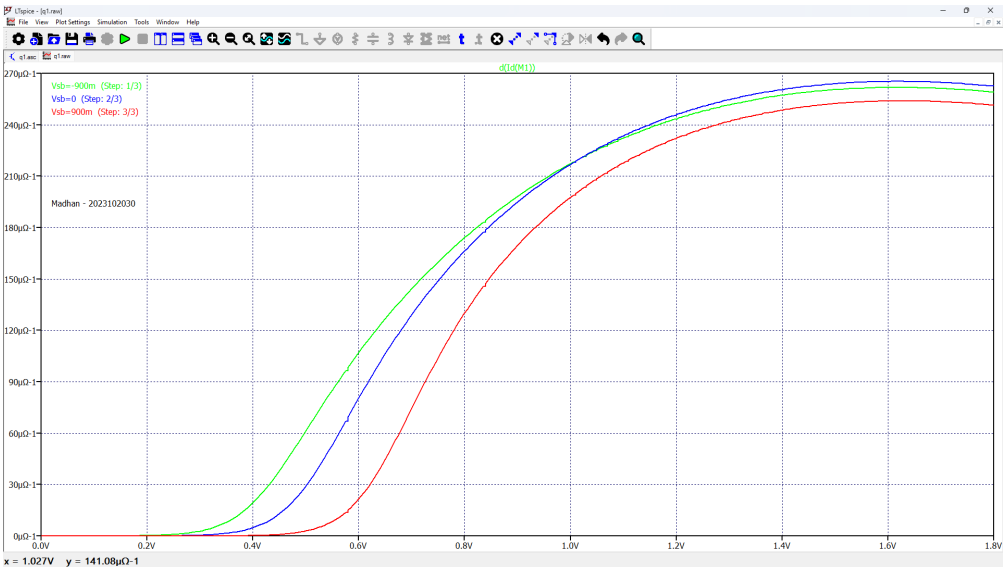

Figure 3: Simulated g_m vs V_{GS} for different V_{SB} values.

Discussion

Discussion:

(b) Reference Current I_{D0}

For $V_{SB} = 0$V and $V_{GS} = 0.9$V:

- $I_{D0} =$ _____

- $g_{m0} =$ _____

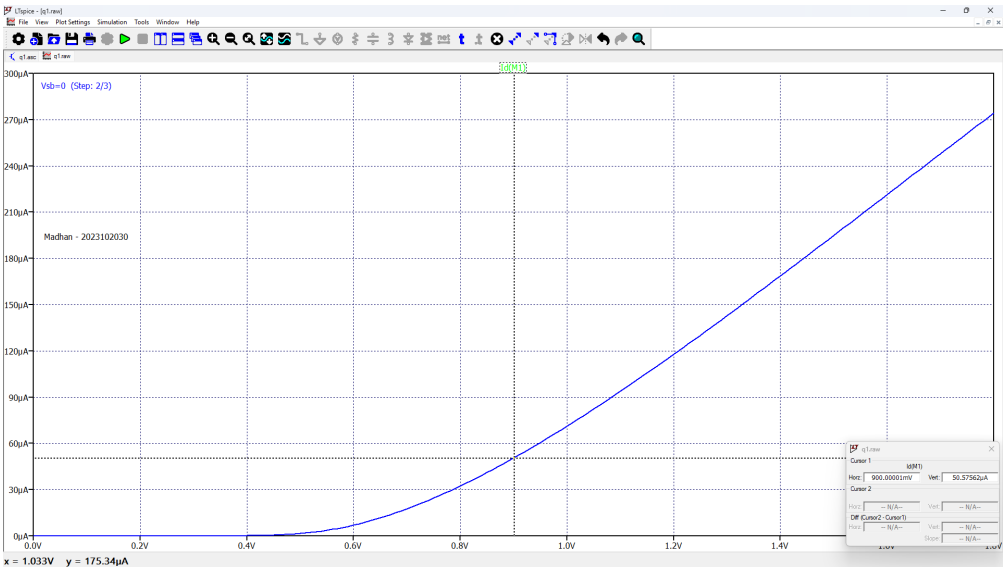

Figure 4: I_{D0} value at $V_{GS} = 0.9$V and $V_{SB} = 0$V.

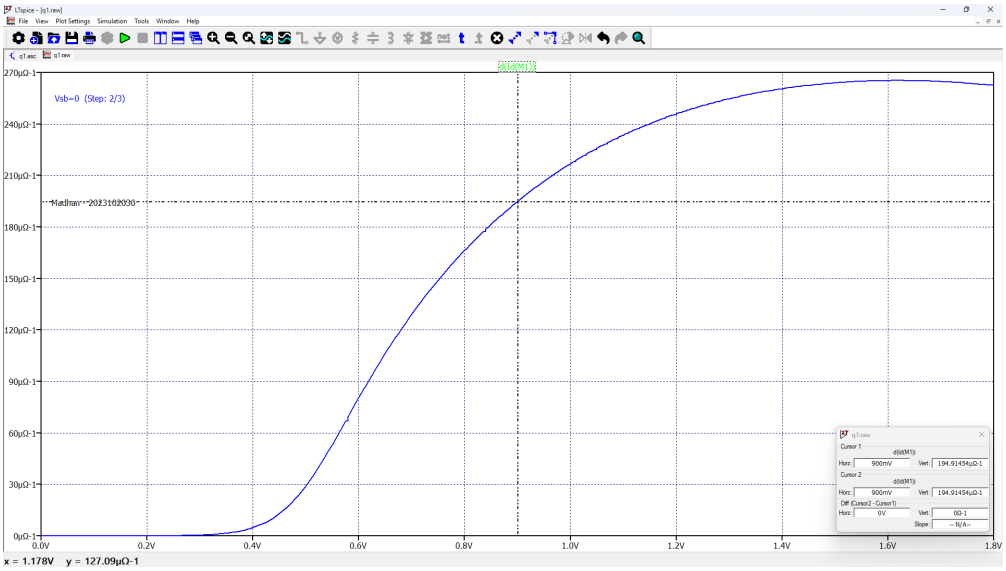

Figure 5: g_{m0} value at $V_{GS} = 0.9$V and $V_{SB} = 0$V.

(c) g_m Variation for $V_{GS} = 0.9$V

- Case $V_{SB} = 0.9$V: Variation =
- Case $V_{SB} = -0.9$V: Variation =

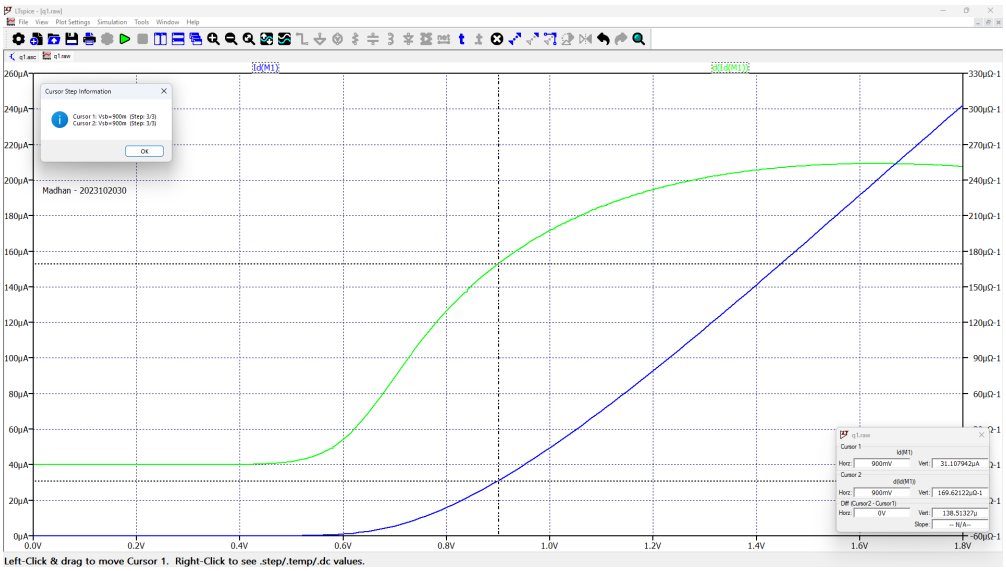

Figure 6: g_m variation at $V_{GS} = 0.9\text{V}$ for different $V_{SB} = 0.9$.

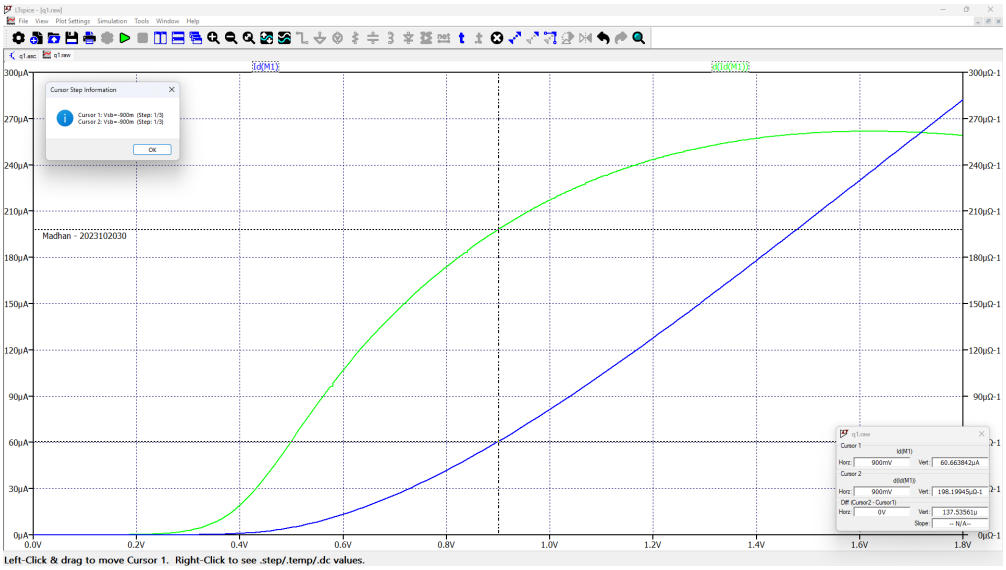

Figure 7: g_m variation at $V_{GS} = 0.9\text{V}$ for different $V_{SB} = -0.9$.

(d) g_m Variation for $I_D = I_{D0}$

- Case $V_{SB} = 0.9\text{V}$: Variation =
- Case $V_{SB} = -0.9\text{V}$: Variation =

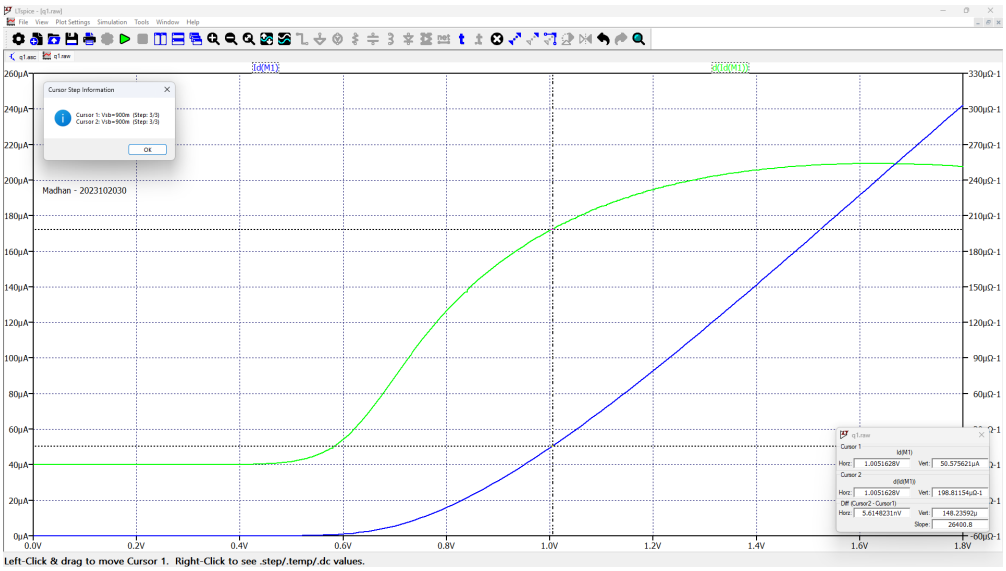

Figure 8: g_m variation at $I_D = I_{D0}$ for different $V_{SB} = 0.9$.

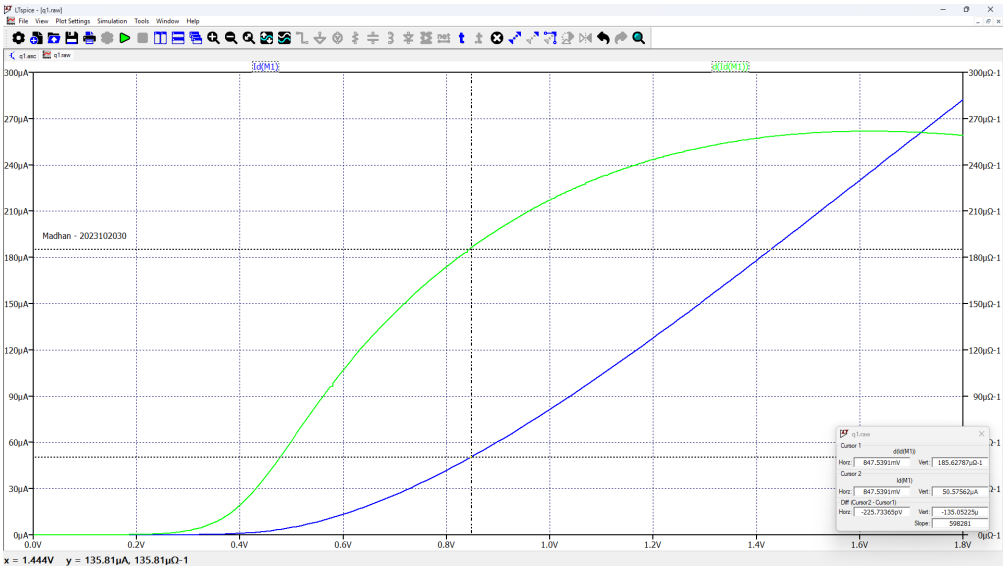

Figure 9: g_m variation at $I_D = I_{D0}$ for different $V_{SB} = -0.9$.

Question 2: Transconductance Analysis

Using the circuit in Figure 1 with $V_{DD} = 1.8\text{V}$.

(a) g_m vs I_D Curve

Sweep I_D from $10\,\mu\text{A}$ to 1mA for: 1. $(W/L) = \frac{3\,\mu\text{m}}{1\,\mu\text{m}}$ 2. $(W/L) = \frac{0.45\,\mu\text{m}}{0.18\,\mu\text{m}}$

[Insert super-imposed g_m vs I_D plot here]

Inference: Which case is closer to the expected form $g_m = \frac{2I_D}{V_{GS}-V_T}$ and why?

(b) Max Transconductance and Saturation

- $g_{m,max}$ observed: _____
- I_D at which g_m saturates: _____
- I_D for $g_{m,use} = 0.8 \times g_{m,max}$: _____

(c) Scaling Parameters

To obtain $g_{m,req} = 4 \times g_{m,use}$ while ensuring the same speed:

Question 3: CS Amplifier Design (g_m/I_D Approach)

Specifications: $A_v > 60$, $f_u = 100\text{MHz}$, $C_L = 1\text{pF}$, $V_{DD} = 1.8\text{V}$, $V^* = \frac{2I_D}{g_m} = 200\text{mV}$.

(a) Channel Length Selection

[Insert plot of $g_m r_o$ vs V_{DS} for different L] **Chosen L: _____ Output Swing Range: _____**

(b) Process and Temperature Variations

[Insert $g_m r_o$ vs V_{DS} plot for corners: tt, ff, ss and temps: -40, 25, 80, 125 °C]

(c) Design Calculations

- Calculated g_m:
- Calculated I_D:
- Calculated W:

(d) Transient Analysis and THD

[Insert annotated transient plots] **THD for maximum input swing: _____**

(e) AC Analysis

[Insert AC Response plots]

- Verified f_u:
- f_{-3dB}:
- AC Gain:

Question 4: Common Source Amplifier Variants

$R_L = 10\text{k}\Omega$, $V_{DD} = 1.8\text{V}$, $A_v > 5$, Overdrive $= 200\text{mV}$, $f_{min} = 100\text{Hz}$.

(a) Design Procedure (Resistive Load)

Total Power Consumption: _____

(b) Transient Simulation

[Insert transient plots for $v_{in} = 10\sin(2\pi \cdot 1000t)\text{mV}$]

(c) AC Response

[Insert AC plots 1Hz to 1GHz] **Unity Bandwidth f_u:** _____

(d) PMOS Current Source Load

[Insert design procedure, Transient, and AC plots for $A_v > 15$]

(e) Cascode Amplifier Design

[Insert design procedure, Transient, and AC plots] **Observed Gain:** _____ **Comparison with Hand Calculations:**

(f) Comparison Table

Table 1: Comparison of Amplifier Topologies

Topology	**Gain**	**Power**	**Output Swing**	**Remarks**
Resistive Load				
PMOS Load				
Cascode				