Assignment 1 Solutions

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Question 2

a

Linear Region Threshold voltage extraction: ($V_{DS} = 50\text{mV}$), since V_{DS} is very small ($V_{DS} << V_{GS} - V_{Th}$), the MOSFET is in the triode region. The current is approximately (neglecting the α parameter) modeled as:

$$I_D = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T)V_{DS}$$

The transconductance $g_m = \frac{\partial I_D}{\partial V_{GS}}$ is maximum at the point of strongest inversion. A tangent line is drawn to the I_D curve at this maximum slope point. The x-axis intercept of this tangent ($V_{GS,int}$) is identified. The threshold voltage is then calculated using the Tsividis correction:

$$V_T = V_{GS,int}$$

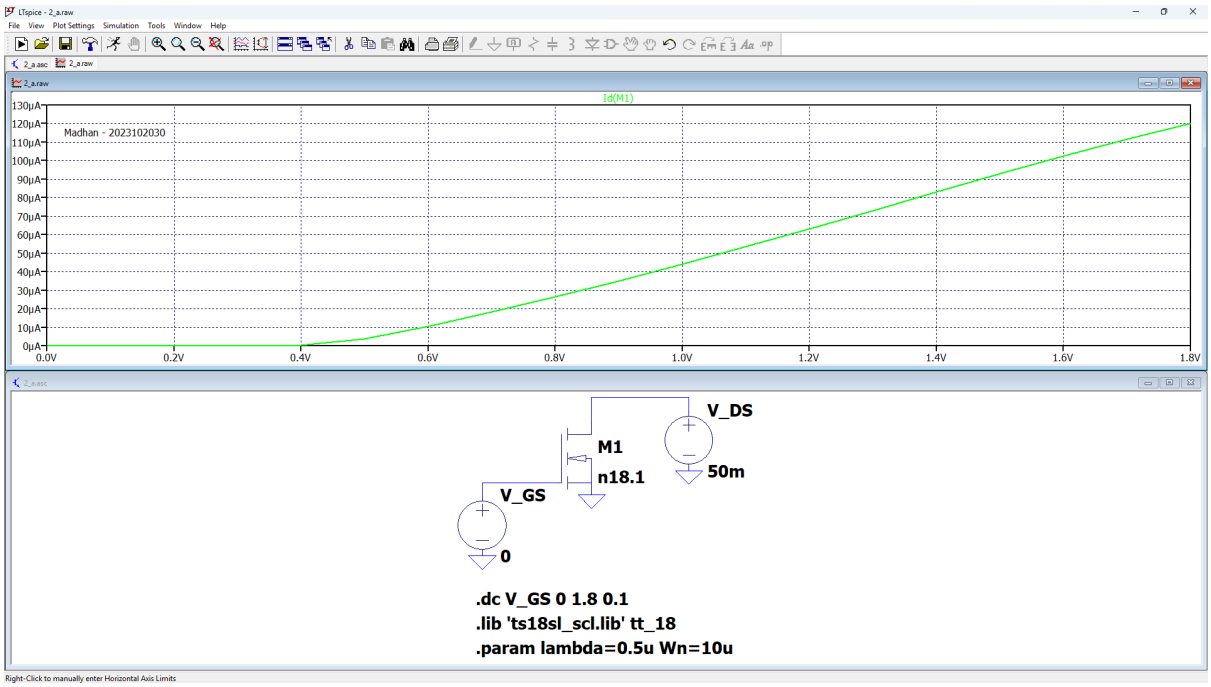

Figure 1: Plot of I_D vs. V_{GS} for $V_{DS} = 50mV$

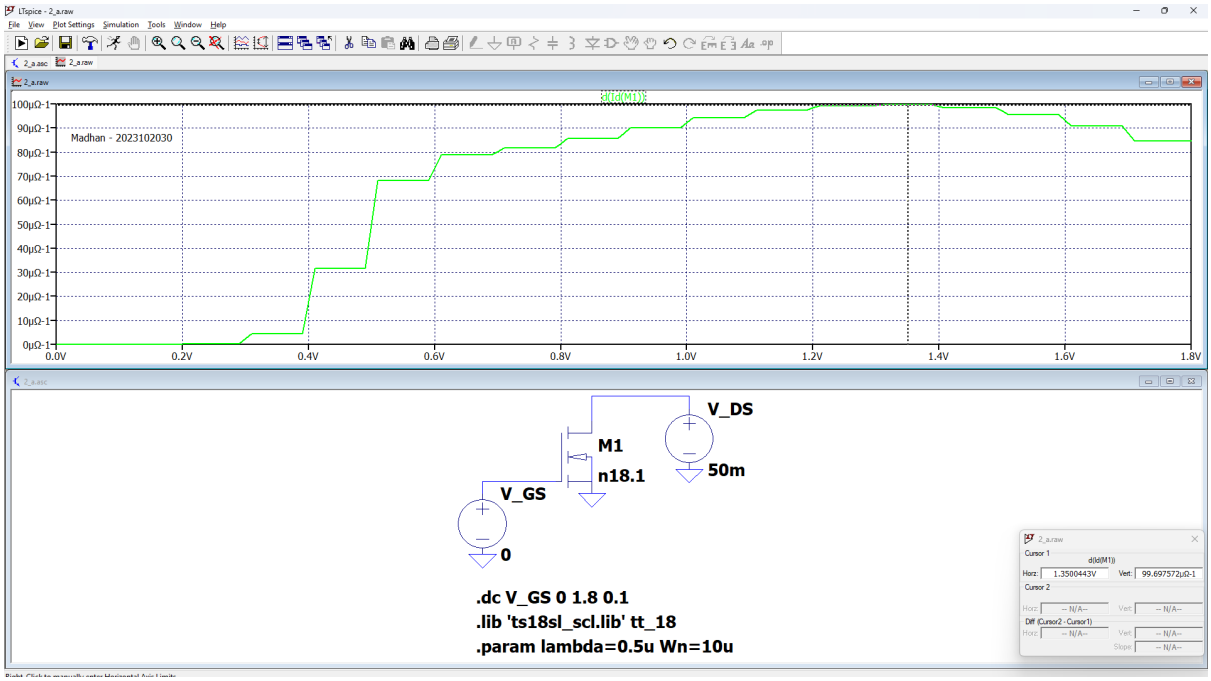

Figure 2: Plot of $\frac{dI_D}{dV_{GS}}$ vs. V_{GS} for $V_{DS} = 50mV$

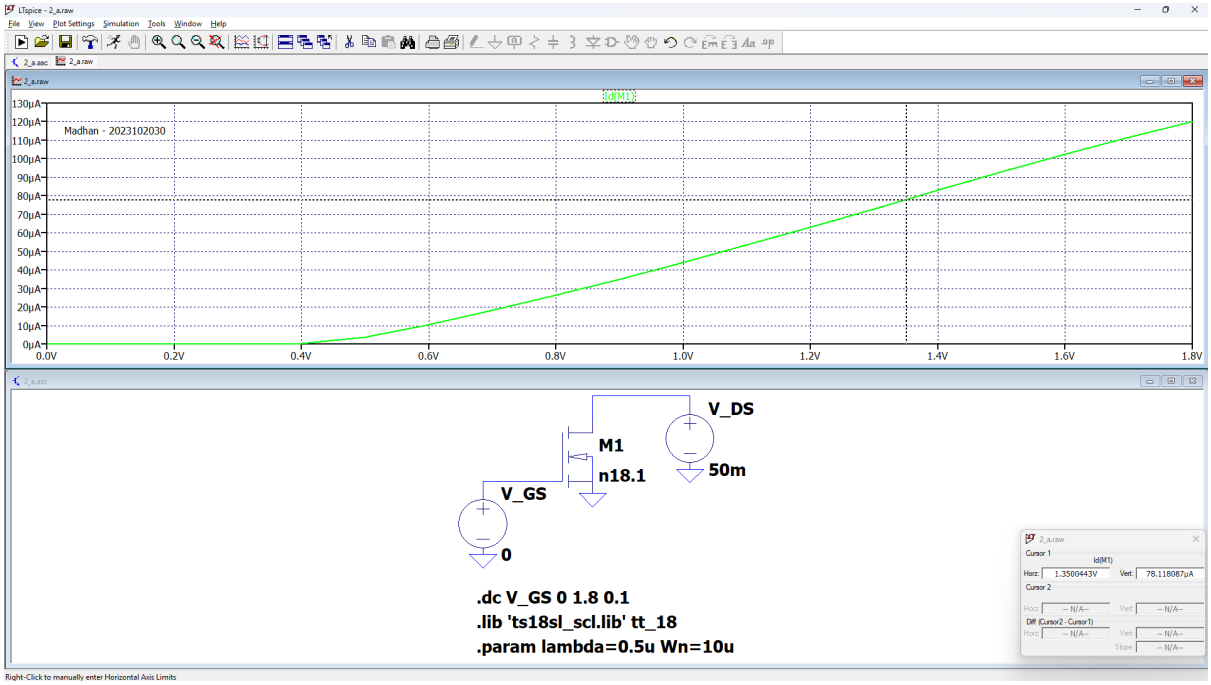

Figure 3: Tangent Line at Maximum Slope Point for $V_{DS} = 50mV$

Slope (m): 99.697572×10^{-6} S (or μA/V)
Point (V_{GS0}, I_{D0}): (1.35 V, 78.167927 μA)

The equation of the line is given by:

$$y - y_0 = m(x - x_0)$$

Substituting your values (using μA for current):

$$I_D - 78.167927 = 99.697572(V_{GS} - 1.35)$$

$$V_{GS,int} = V_{Threshold} = \frac{56.423795}{99.697572}$$
$$V_{Threshold,linear} \approx 0.56595 \text{ V}$$

b

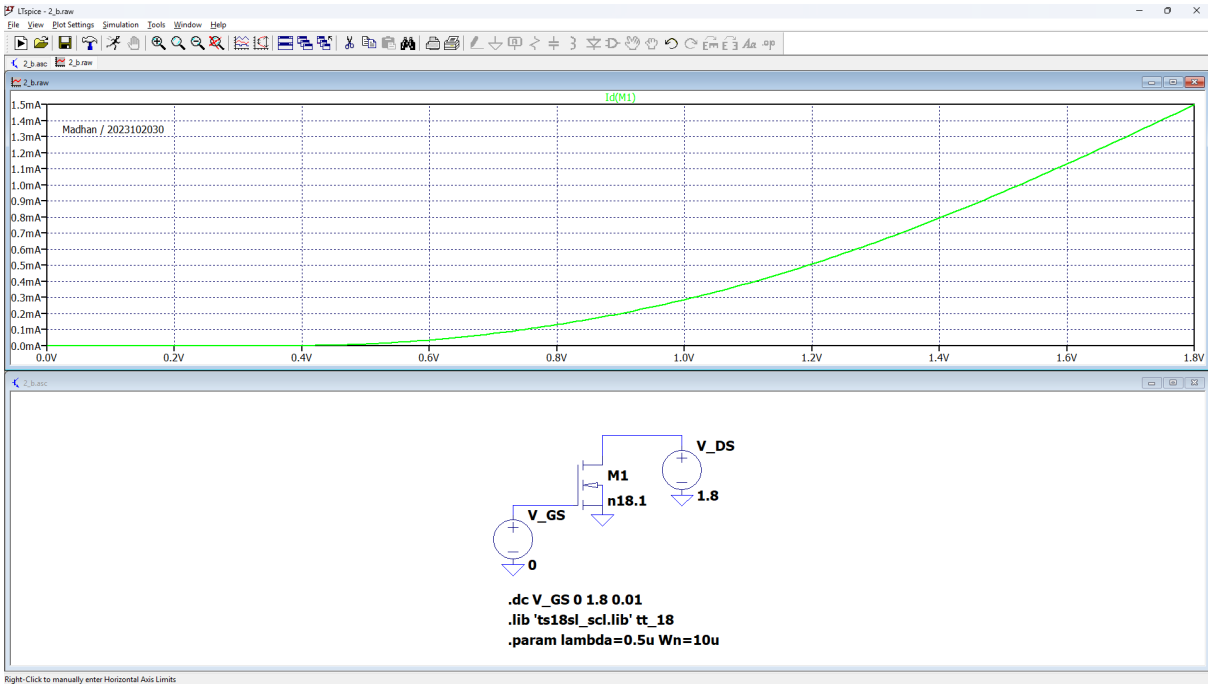

Figure 4: Plot of I_D vs. V_{GS} for $V_{DS} = 1.8V$

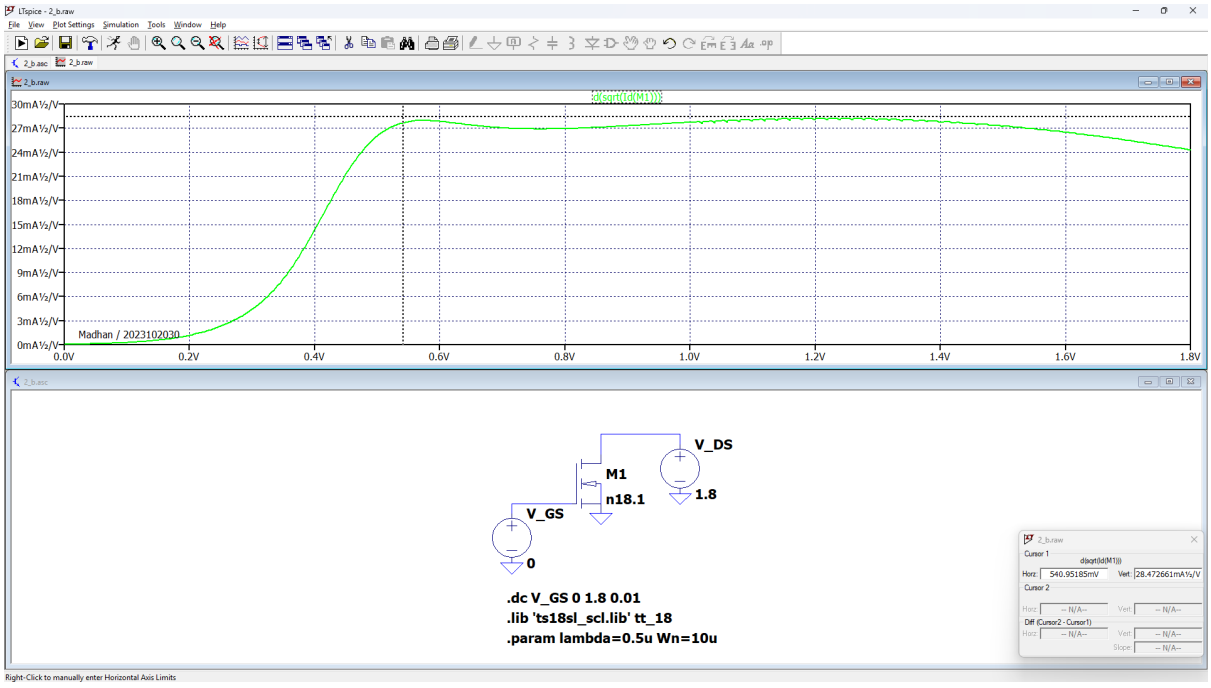

Figure 5: Plot of $\frac{d\sqrt{I_D}}{dV_{GS}}$ for $V_{DS} = 1.8V$

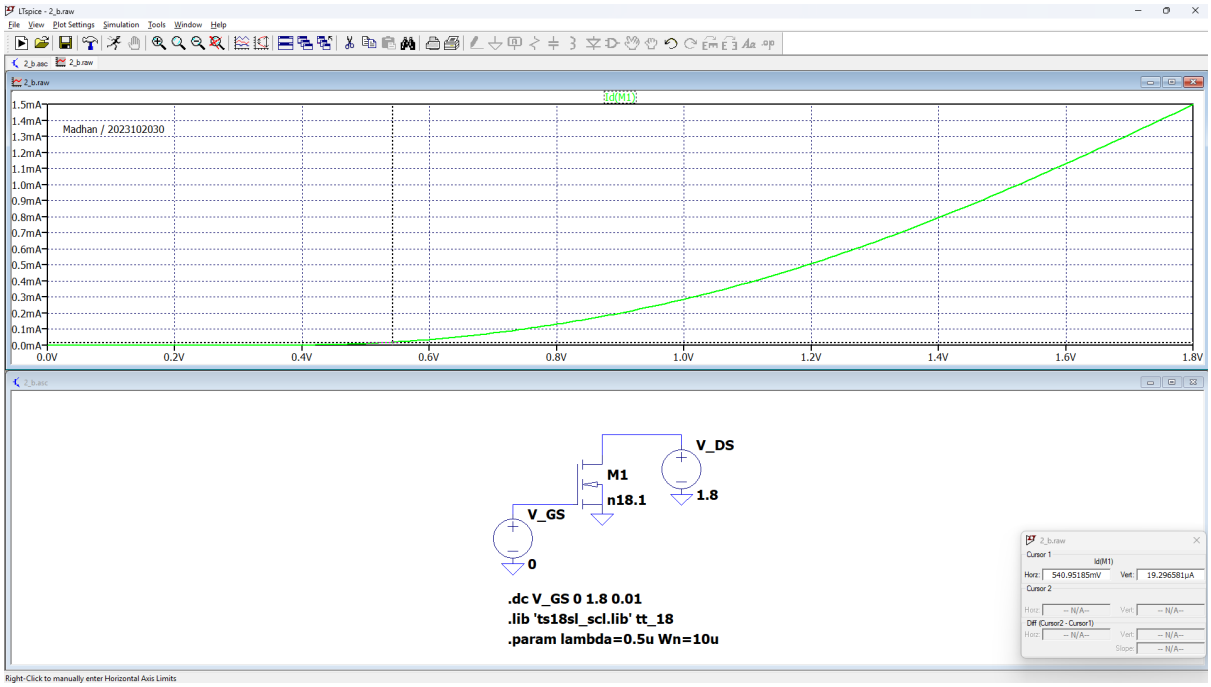

Figure 6: Tangent Line at Maximum Slope Point for $V_{DS} = 1.8V$

The standard square-law model for an NMOS in saturation ($V_{DS} \geq V_{GS} - V_T$) is:

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T)^2$$

To extract V_T through linear extrapolation, we take the square root of both sides of the saturation equation:

$$\sqrt{I_D} = \sqrt{\frac{1}{2}\mu_n C_{ox} \frac{W}{L}} \cdot (V_{GS} - V_T)$$

This matches the equation of a straight line, $y = mx + c$, where:
$y = \sqrt{I_D}$
$x = V_{GS}$
Slope $(m) = \sqrt{\frac{1}{2}\mu_n C_{ox} \frac{W}{L}}$
Constant $(c) = -m \cdot V_T$

When you plot $\sqrt{I_D}$ vs. V_{GS}, the plot will have a linear portion. By extending (extrapolating) this linear part down to the x-axis (where $\sqrt{I_D} = 0$), the intercept gives the saturation threshold voltage directly.

Analytical Step: If you have the slope (m) and a point $(V_{GS0}, \sqrt{I_{D0}})$ from the linear region: Find the intercept form: $\sqrt{I_D} = m \cdot V_{GS} + c$ The x-intercept occurs when $\sqrt{I_D} = 0$:

$$0 = m \cdot V_{GS,int} + c$$

$$V_{GS,int} = -\frac{c}{m}$$

$V_{T,sat} = V_{GS,int}$
Slope (m): $28.472661\sqrt{\mu\text{A}}/\text{V}$
Point $(V_{GS0}, \sqrt{I_{D0}})$: $(0.54095185\ \text{V}, \sqrt{19.296581}\sqrt{\mu\text{A}})$
$\sqrt{I_{D0}} \approx 4.392787\sqrt{\mu\text{A}}$

Using the point-slope form $y - y_0 = m(x - x_0)$ where $y = \sqrt{I_D}$ (in μA):

$$\sqrt{I_D} - 4.392787 = 28.472661(V_{GS} - 0.540952)$$

Expanding to find the intercept form ($\sqrt{I_D} = m \cdot V_{GS} + c$):

$$\sqrt{I_D} = 28.472661 \cdot V_{GS} - (28.472661 \times 0.540952) + 4.392787$$

$$\sqrt{I_D} = 28.472661 \cdot V_{GS} - 15.402338 + 4.392787$$

$$\sqrt{I_D} = 28.472661 \cdot V_{GS} - 11.009551$$

$$V_{GS,int} = V_{Threshold} \frac{11.009551}{28.472661}$$

$$V_{GS,int} \approx \mathbf{0.38667}\ \text{V}$$

In the saturation region ($V_{DS} = 1.8$V), the x-intercept of the $\sqrt{I_D}$ plot is directly taken as the threshold voltage:

$$V_{Threshold,saturation} = \mathbf{0.387}\ \text{V}$$

The transition frequency is fundamentally governed by the ratio of the transconductance to the total input capacitance:

$$f_T \approx \frac{g_m}{2\pi(C_{gs} + C_{gd})}$$

SCL 180nm vs. TSMC 180nm
Even though both technologies share the same 180nm feature size, the SCL 180nm (64.9 GHz) significantly outperforms the TSMC 180nm (43.26 GHz). This discrepancy is likely due to differences in the process parameters provided in their respective library files. SCL may have a thinner gate oxide (t_{ox}), leading to a higher C_{ox} and thus higher g_m for the same bias. Additionally, lower parasitic overlap capacitances in the SCL model would lead to a higher f_T.

c

Case (a) Linear Region ($V_{DS} = 50$mV): $V_{T,lin} \approx 0.541$V
Case (b) Saturation Region ($V_{DS} = 1.8$V): $V_{T,sat} \approx 0.387$V

The threshold voltage decreases by approximately 154mV as the drain-source voltage increases from 50mV to 1.8V.

The primary physical reason for this difference is Drain-Induced Barrier Lowering (DIBL).

In a MOSFET, the threshold voltage represents the gate potential required to lower the energy barrier between the source and the channel enough to allow significant carrier flow. In modern sub-micron nodes like the 180nm process, the depletion region around the drain extends significantly toward the source as V_{DS} increases.

This high drain potential effectively "pulls down" the potential barrier at the source end of the channel. Since the drain is assisting the gate in lowering this barrier, a lower gate voltage (V_{GS}) is required to reach the same level of inversion (turning the transistor "on"). This results in the observed drop in the effective threshold voltage at high V_{DS}.

Selection for Hand Calculations: For hand calculations using simple MOS models (such as the square-law equation), you should use the V_T extracted from Case (a) ($V_{DS} =$ 50mV).

Reasoning: Intrinsic Accuracy: Simple models assume V_T is a constant technology parameter. The extraction at very low V_{DS} provides the "intrinsic" threshold voltage, as it minimizes secondary high-field effects like DIBL and Channel Length Modulation. Model Consistency: Basic equations like $I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_T)^2$ do not have built-in terms to account for V_T shifting with V_{DS}. Using the linear-region V_T ensures that your hand calculations remain closer to the fundamental process specifications provided in the PDK.

d

To estimate the technology parameter $\mu_n C_{ox}$ (also known as the process transconductance parameter k'_n), we use the slopes extracted from your simulation data and relate them to the simple square-law MOS models for both the linear and saturation regions.

1. Estimation from the Linear Region ($V_{DS} = 50$mV)

In the linear region, the simple MOS model for drain current is:

$$I_D = \mu_n C_{ox}\frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

The transconductance (g_m), which is the slope of the I_D vs. V_{GS} curve, is:

$$g_{m,lin} = \frac{\partial I_D}{\partial V_{GS}} = \mu_n C_{ox}\frac{W}{L}V_{DS}$$

Using your simulated values: Slope ($g_{m,lin}$): 99.697572×10^{-6} A/V
Drain-Source Voltage (V_{DS}): 0.05 V
Aspect Ratio (W/L): $10\mu\text{m}/1\mu\text{m} = 10$

$$\mu_n C_{ox} = \frac{g_{m,lin}}{(W/L)\cdot V_{DS}} = \frac{99.697572 \times 10^{-6}}{10 \times 0.05}$$

$$\mu_n C_{ox} \approx \mathbf{199.40}\ \mu\text{A/V}^\mathbf{2}$$

2. Estimation from the Saturation Region ($V_{DS} = 1.8$V)

In the saturation region, the square-law relationship is:

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_T)^2$$

Linearizing this by taking the square root gives:

$$\sqrt{I_D} = \sqrt{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}} \cdot (V_{GS} - V_T)$$

The slope of the $\sqrt{I_D}$ vs. V_{GS} curve is:

$$m_{sat} = \sqrt{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}}$$

Using your simulated values: Slope (m_{sat}): 28.472661 $\text{mA}^{1/2}/\text{V} = 0.028472661\ \text{A}^{1/2}/\text{V}$
Aspect Ratio (W/L): 10

$$\mu_n C_{ox} = \frac{2 \cdot m_{sat}^2}{W/L} = \frac{2 \cdot (0.028472661)^2}{10}$$

$$\mu_n C_{ox} \approx \frac{2 \cdot 0.00081069}{10} \approx 0.00016213$$

$$\mu_n C_{ox} \approx \mathbf{162.13}\ \mu\text{A/V}^2$$

3. Discussion and Model Selection

You will observe that the $\mu_n C_{ox}$ calculated from the linear region (199.4 $\mu\text{A/V}^2$) is significantly higher than that from the saturation region (162.1 $\mu\text{A/V}^2$).

Why the values differ: Mobility Degradation: In saturation, the vertical electric field (from the gate) and the lateral electric field (from the drain) are much higher. This causes carriers to collide more frequently with the oxide interface, reducing the effective mobility (μ_{eff}) compared to the low-field linear case. Velocity Saturation: At $V_{DS} = 1.8\text{V}$, the carriers reach their scattering-limited velocity, which prevents the current from increasing quadratically as the simple model predicts, leading to a lower "apparent" $\mu_n C_{ox}$ in saturation.

e

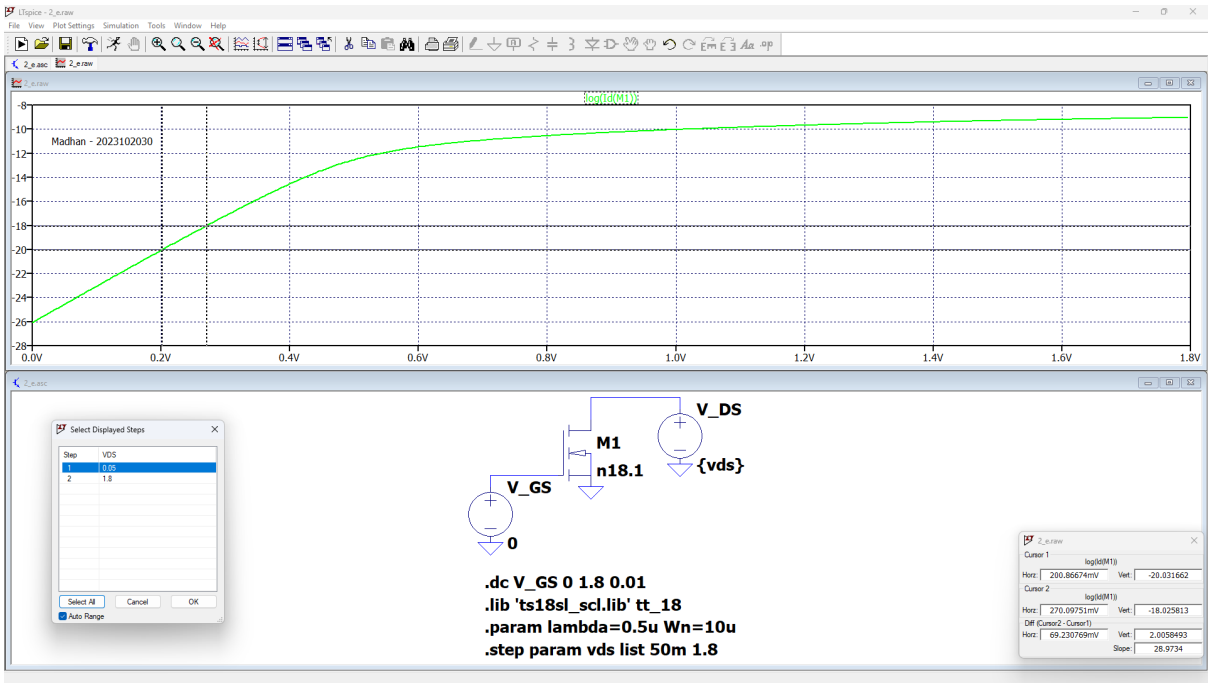

Figure 7: Plot of $\ln(I_D)$ vs. V_{GS} for $V_{DS} = 50mV$

The y-values provided (around -20) represent the natural logarithm of the drain current, $\ln(I_D)$, which is standard when identifying the subthreshold slope.

Point 1: $(V_{GS1}, \ln(I_{D1})) = (200.867\ \text{mV}, -20.032)$
Point 2: $(V_{GS2}, \ln(I_{D2})) = (270.098\ \text{mV}, -18.026)$

2. Mathematical Relationship

The subthreshold current is given by:

$$I_D = I_0 \exp\left(\frac{V_{GS}}{\eta V_{thermal}}\right)$$

Taking the natural log:

$$\ln(I_D) = \ln(I_0) + \frac{1}{\eta V_{thermal}} \cdot V_{GS}$$

This takes the form of a line $y = mx + c$, where the slope m is:

$$m = \frac{\Delta \ln(I_D)}{\Delta V_{GS}} = \frac{1}{\eta V_{thermal}}$$

Rearranging for η:

$$\eta = \frac{1}{m \cdot V_{thermal}}$$

3. Calculation

Change in Gate Voltage (ΔV_{GS}):

$$\Delta V_{GS} = 270.09751 \text{ mV} - 200.86674 \text{ mV} = 69.23077 \text{ mV} = 0.06923 \text{ V}$$

Change in Log Current ($\Delta \ln(I_D)$):

$$\Delta \ln(I_D) = -18.025813 - (-20.031662) = 2.005849$$

Slope (m):

$$m = \frac{2.005849}{0.06923} \approx 28.973 \text{ V}^{-1}$$

Using the standard thermal voltage at 27°C ($V_{thermal} \approx 25.86$ mV):

$$\eta = \frac{1}{28.973 \times 0.02586}$$

$$\eta \approx \mathbf{1.335}$$

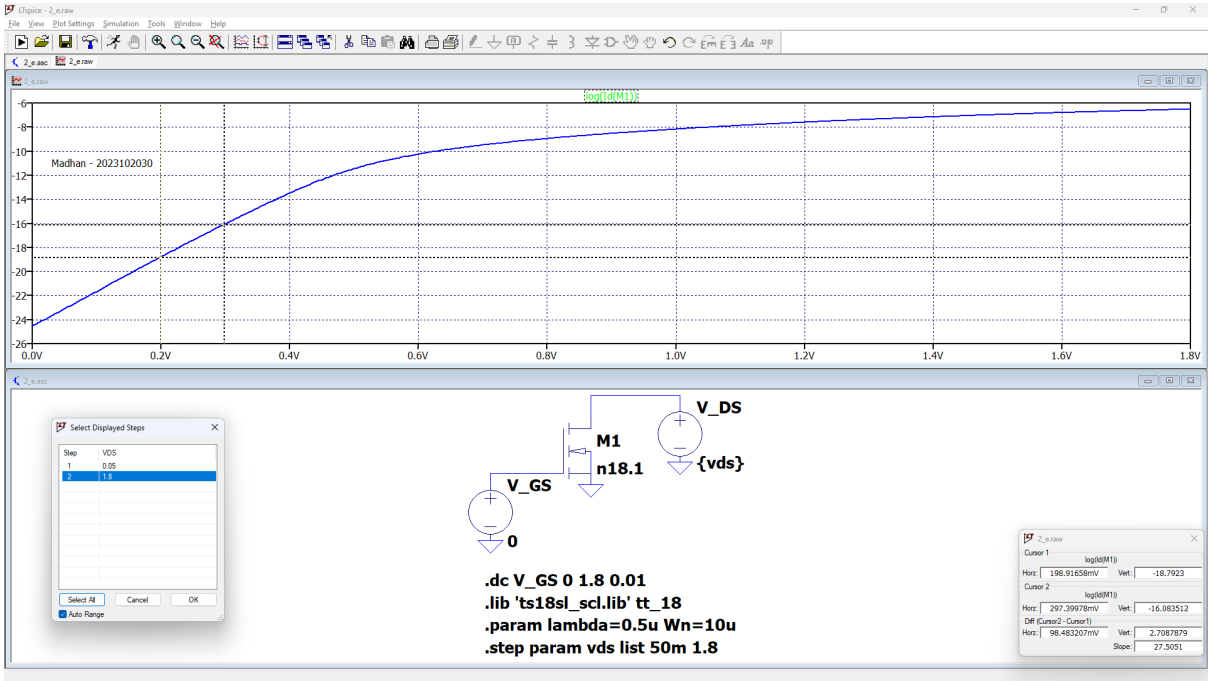

Figure 8: Plot of $\ln(I_D)$ vs. V_{GS} for $V_{DS} = 1.8V$

The y-axis values are provided as the natural logarithm of the drain current, $\ln(I_D)$.

Point 1: $(V_{GS1}, \ln(I_{D1})) = (198.91658 \text{ mV}, -18.7923)$

Point 2: $(V_{GS2}, \ln(I_{D2})) = (297.39978 \text{ mV}, -16.083512)$

2. Mathematical Relationship

The subthreshold current is modeled as:

$$I_D = I_0 \exp\left(\frac{V_{GS}}{\eta V_{thermal}}\right)$$

Taking the natural logarithm:

$$\ln(I_D) = \ln(I_0) + \frac{1}{\eta V_{thermal}} \cdot V_{GS}$$

The slope (m) of the $\ln(I_D)$ vs. V_{GS} plot is:

$$m = \frac{\Delta \ln(I_D)}{\Delta V_{GS}} = \frac{1}{\eta V_{thermal}}$$

Rearranging to solve for the subthreshold swing factor η:

$$\eta = \frac{1}{m \cdot V_{thermal}}$$

3. Numerical Calculation

Change in Gate Voltage (ΔV_{GS}):

$$\Delta V_{GS} = 297.39978 \text{ mV} - 198.91658 \text{ mV} = 98.4832 \text{ mV} = 0.0984832 \text{ V}$$

Change in Log Current ($\Delta \ln(I_D)$):

$$\Delta \ln(I_D) = -16.083512 - (-18.7923) = 2.708788$$

Slope (m):

$$m = \frac{2.708788}{0.0984832} \approx 27.505 \text{ V}^{-1}$$

Using a standard thermal voltage at 27°C ($V_{thermal} \approx 25.86$ mV):

$$\eta = \frac{1}{27.505 \times 0.02586}$$

$$\eta \approx \mathbf{1.406}$$

Question 3

a

Theoretically, $f_T \approx \frac{g_m}{2\pi(C_{gs}+C_{gd})}$. As technology scales from 180nm to 130nm, capacitances decrease significantly, and f_T increases. You should expect the 130nm node to have a much higher f_T than the 180nm nodes.

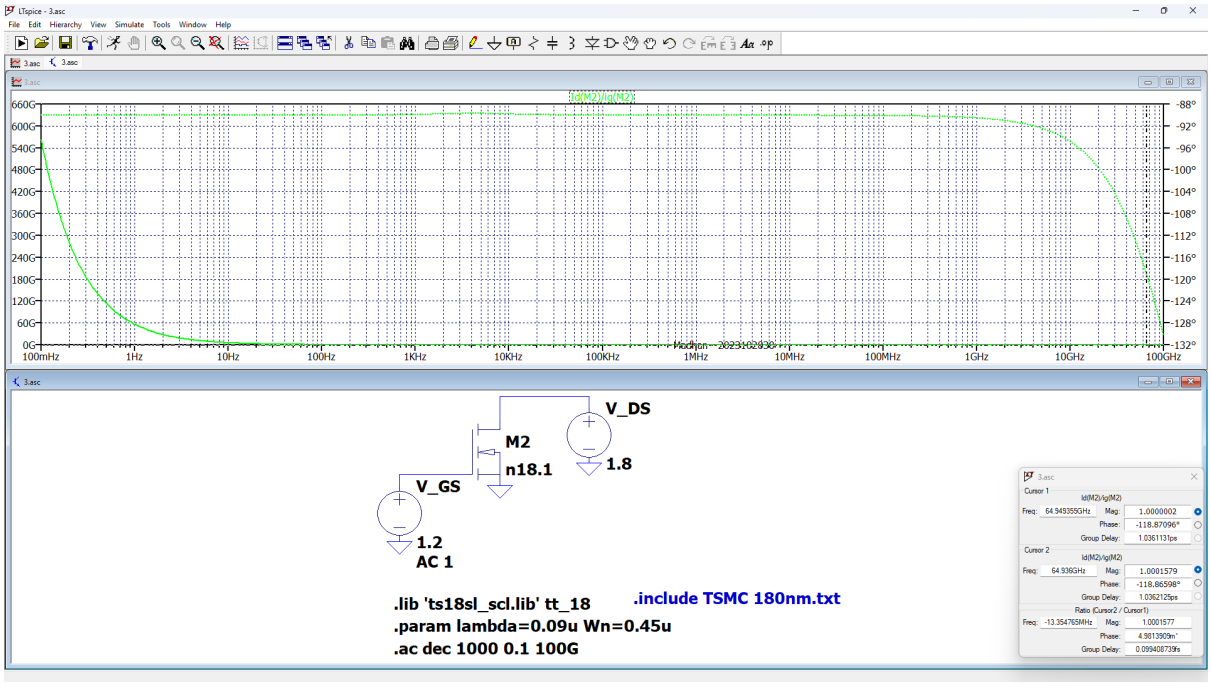

Figure 9: Plot of Gain vs. V_{GS} for SCL180nm technology node

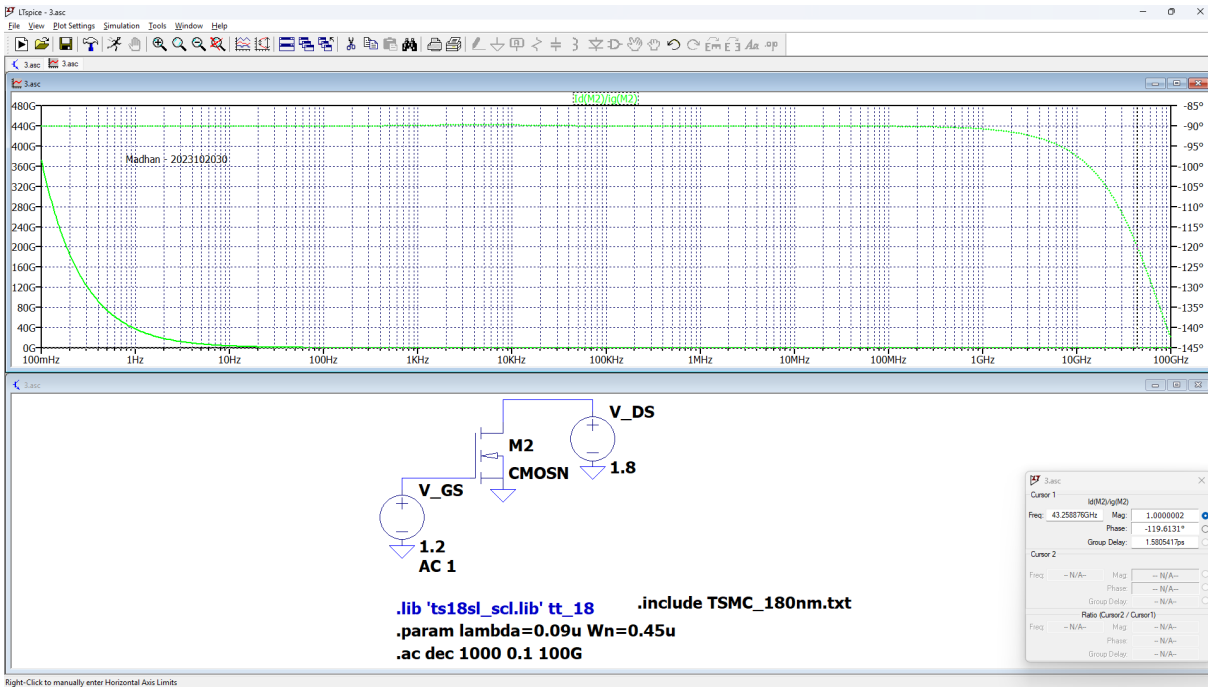

Figure 10: Plot of Gain vs. Frequency for TSMC180nm technology node

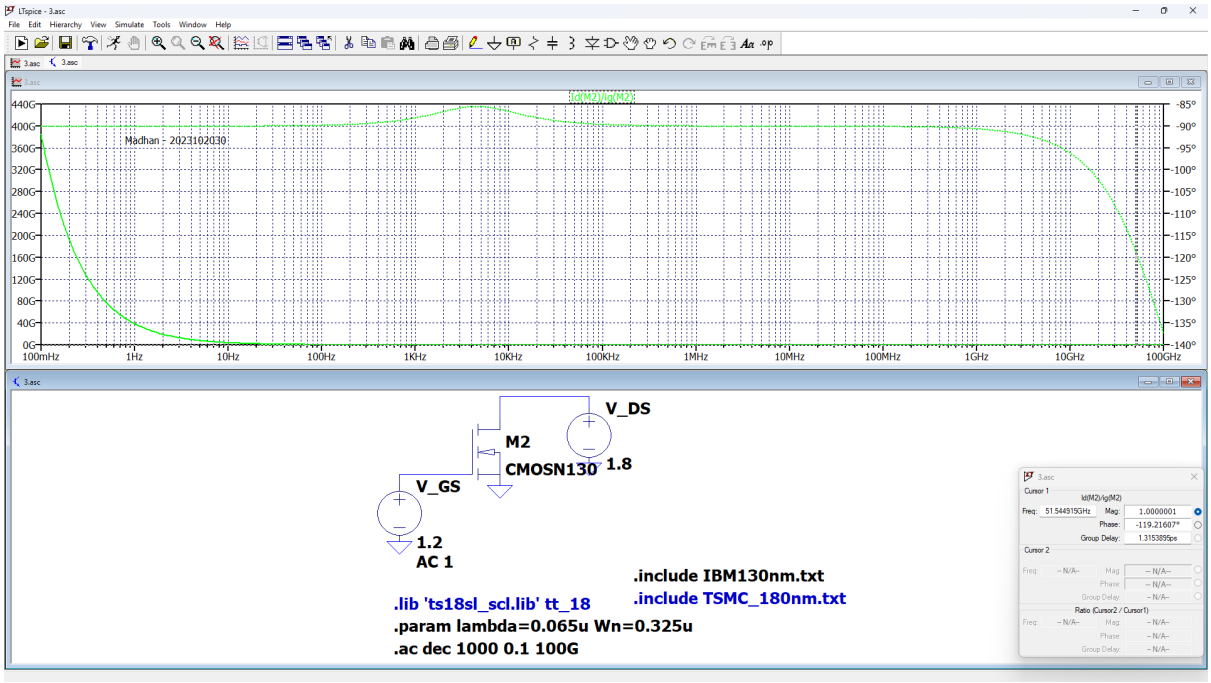

Figure 11: Plot of Gain vs. Frequency for IBM130nm technology node

Table 1: Comparison of Unity Current Gain Frequency (f_T) for Minimum Size NMOS across Technology Nodes ($V_{GS} = 1.2$V, $V_{DS} = 1.8$V)

Technology Node	**Feature Size (L_{min})**	**Extracted f_T (GHz)**
SCL 180nm	180 nm	64.90
TSMC 180nm	180 nm	43.26
IBM 130nm	130 nm	51.54

Note:

All reported frequencies were extracted at a gate-source voltage (V_{GS}) of 1.2 V to ensure the devices are biased in the strong inversion saturation region, thereby capturing high-frequency performance metrics.

The transition frequency is fundamentally governed by the ratio of the transconductance to the total input capacitance:

$$f_T \approx \frac{g_m}{2\pi(C_{gs} + C_{gd})}$$

SCL 180nm vs. TSMC 180nm

Even though both technologies share the same 180 nm feature size, the SCL 180 nm (64.9 GHz) significantly outperforms the TSMC 180 nm (43.26 GHz). This discrepancy is likely due to differences in the process parameters provided in their respective library files. SCL may have a thinner gate oxide (t_{ox}), leading to a higher C_{ox} and thus higher g_m for the same bias. Additionally, lower parasitic overlap capacitances in the SCL model would lead to a higher f_T.

IBM 130nm vs. 180nm Nodes

One might expect the 130 nm node to have the highest f_T due to the smaller channel length (L). In theory, f_T scales with $1/L^2$. However, your data shows SCL 180 nm > IBM 130 nm.

Velocity Saturation: In the 130 nm node, carriers reach velocity saturation much earlier. Once velocity is saturated, g_m no longer increases linearly with decreasing L, causing f_T to scale more like $1/L$ rather than $1/L^2$.

Parasitic Dominance: At 130 nm, parasitic capacitances (like fringe and overlap capacitances) become a much larger fraction of the total gate capacitance compared to the intrinsic channel capacitance, which can dampen the expected speed gains from scaling.

b

Scaling vs. Gain: You will likely observe that the 130nm node has the lowest intrinsic gain. This is because as L decreases, the Channel Length Modulation (λ) effect becomes more severe, increasing g_{ds} (lowering r_o) and killing the gain.

TSMC vs. SCL: Even though both are 180nm, they will have different doping profiles and oxide thicknesses. The one with the lower g_{ds} (higher r_o) is "better" for high-gain analog design.

Hand Calculation Model: In simple models, we use $A_v = \frac{2}{\lambda(V_{GS}-V_T)}$. This suggests that to maximize gain in any node, you should use lower overdrive voltages and longer channel lengths.

Question 4

Cascading Two Stages

When cascading, you cannot connect the output of Stage 1 directly to the gate of Stage 2 because their DC levels might conflict. You must use AC Coupling.

Cascaded Schematic: Stage 1: Identical to the first circuit. Interstage Coupling: Connect a capacitor ($C_{cascade}$) from the output of Stage 1 to the gate of Stage 2. Stage 2 Biasing: Stage 2 needs its own resistive divider to set its gate to $0.9V$.

Expected Cascaded Results: Total Gain: $A_{total} = A_{v1} \times A_{v2}$. If one stage gives -30, the cascade should give roughly +900 V/V (Note the phase becomes positive). THD for A_{max}: Because the gain is now much higher, the A_{max} you found for a single stage will cause massive clipping in the second stage.

Observation: You will find that for the two-stage amplifier, the new A_{max} is significantly smaller (often in the micro-volt range) to keep the second stage from saturating and keeping THD ¡ 10