Analog IC Design: Assignment-2

Spring 2026, IIIT Hyderabad

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Due Date: February 23, 2026 (18:00 hrs)

Question 1: n-channel MOSFET Characteristics

Considering $V_{DS} = 1\text{V}$ and $\frac{W}{L} = \frac{500\text{n}}{180\text{n}}$:

(a) I_D vs V_{GS} and g_m vs V_{GS} Plots

Cases: (i) $V_{SB} = 0\text{V}$, (ii) $V_{SB} = 0.9\text{V}$, (iii) $V_{SB} = -0.9\text{V}$.

Schematic and Simulation Setup

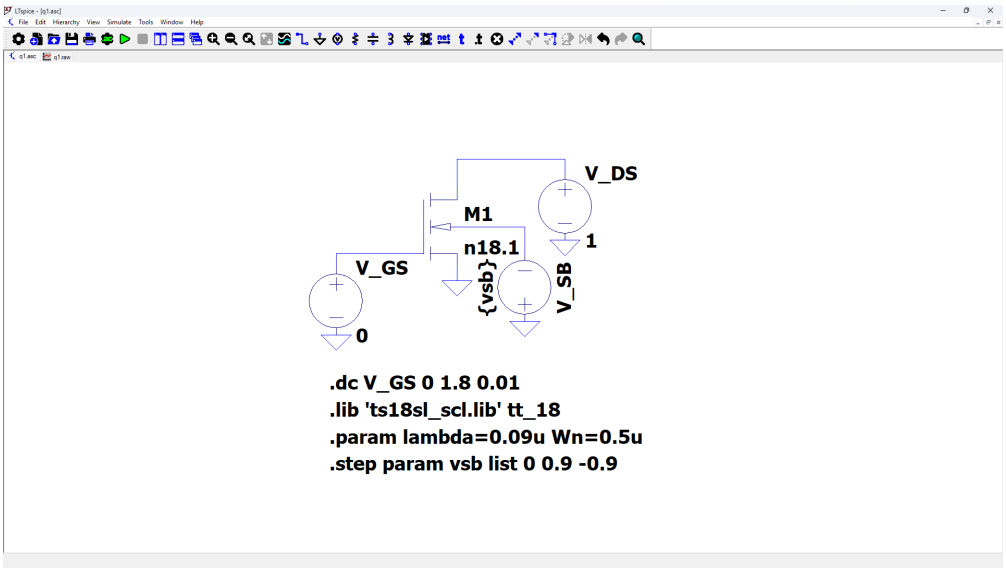

Figure 1: Schematic for I_D vs V_{GS} and g_m vs V_{GS} simulations.

(b) Reference Current I_{D0}

For $V_{SB} = 0\text{V}$ and $V_{GS} = 0.9\text{V}$:

- $I_{D0} = 50.576\mu A$
- $g_{m0} = 174.914\mu S$

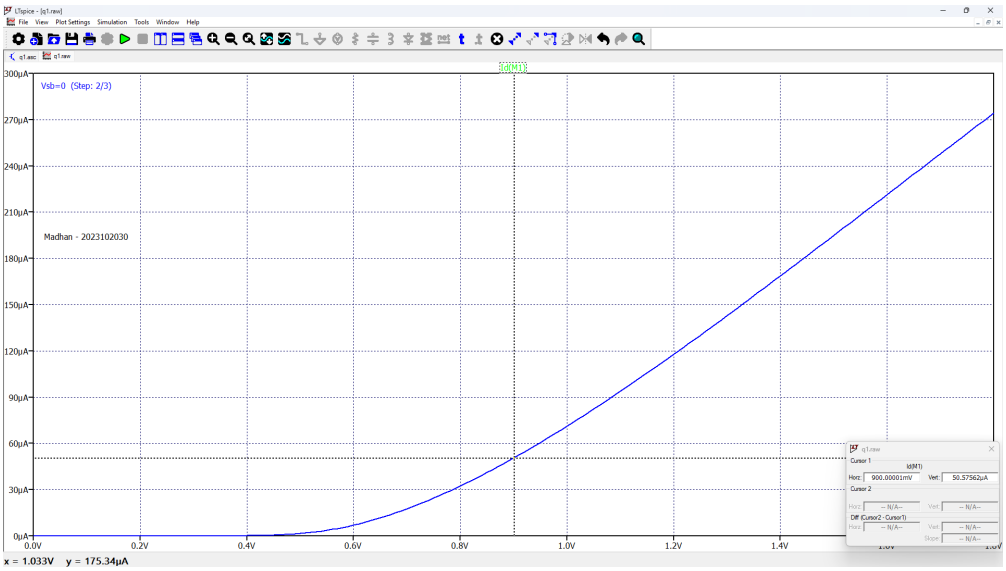

Figure 2: I_{D0} value at $V_{GS} = 0.9$V and $V_{SB} = 0$V.

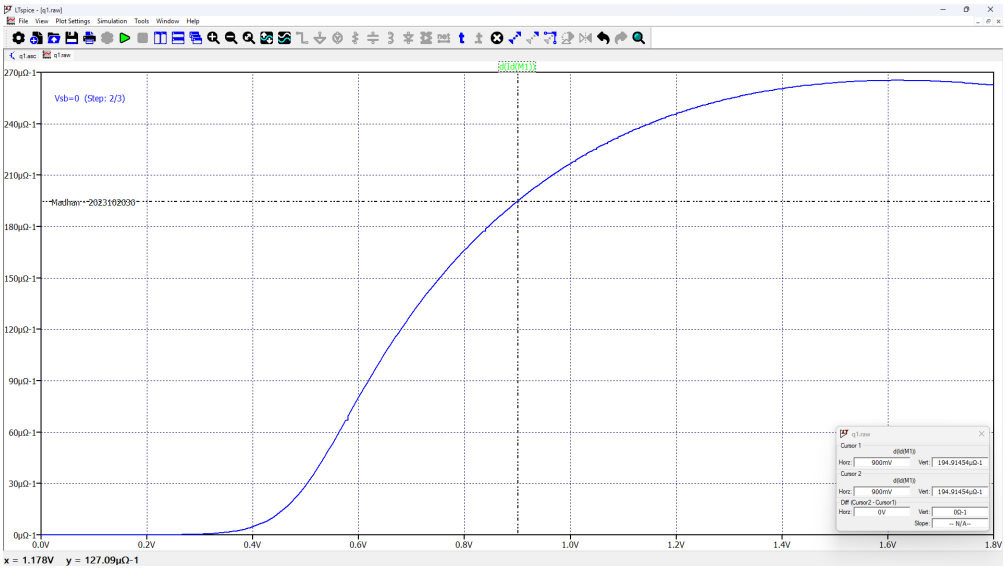

Figure 3: g_{m0} value at $V_{GS} = 0.9$V and $V_{SB} = 0$V.

(c) g_m variations for $V_{GS} = 0.9$V

- Case $V_{SB} = 0.9$V:
  $V_{SB} = 0.9$V: $I_D = 31.1079\mu A$, $g_m = 169.21\mu S$
  $V_{SB} = -0.9$V: $I_D = 60.6638\mu A$, $g_m = 198.199\mu S$
  $V_{SB} = 0$V: $I_D = 50.576\mu A$, $g_m = 194.914\mu S$
  Variation when $V_{SB} = 0.9$V $= \frac{169.21-194.914}{194.914} \times 100\% = -13.65\%$
  Variation when $V_{SB} = -0.9$V $= \frac{198.199-194.914}{194.914} \times 100\% = 1.68\%$

- Case $V_{SB} = -0.9$V:

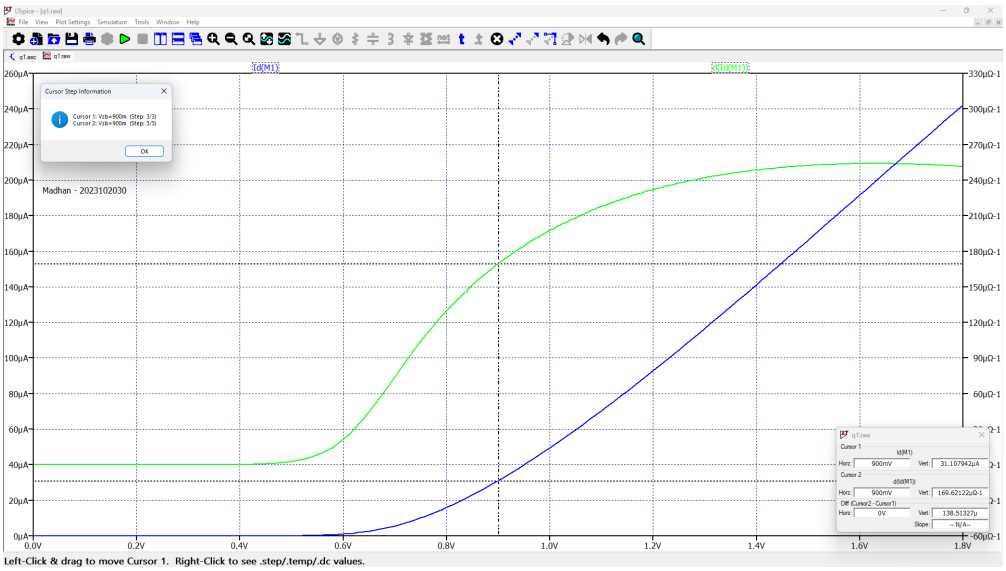

Figure 4: g_m variation at $V_{GS} = 0.9\text{V}$ for different $V_{SB} = 0.9$.

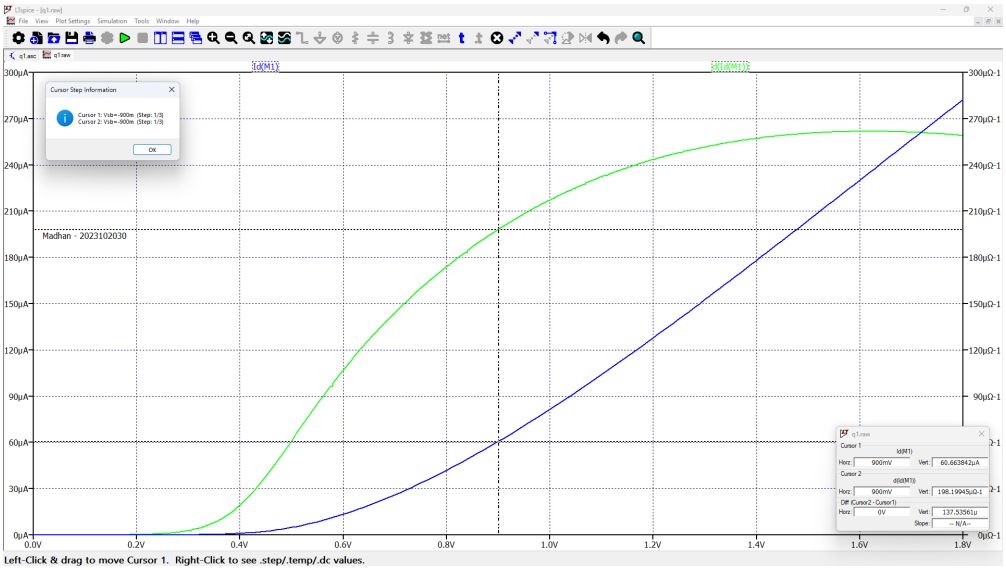

Figure 5: g_m variation at $V_{GS} = 0.9\text{V}$ for different $V_{SB} = -0.9$.

(d) g_m Variation for $I_D = I_{D0}$

- Case $V_{SB} = 0.9\text{V}$:
  $V_{SB} = 0.9\text{V}$: $I_D = 50.5756\mu A$, $g_m = 198.811\mu S$
  $V_{SB} = -0.9\text{V}$: $I_D = 50.57562\mu A$, $g_m = 185.627\mu S$
  $V_{SB} = 0\text{V}$: $I_D = 50.576\mu A$, $g_m = 194.914\mu S$
  Variation when $V_{SB} = 0.9\text{V} = \frac{198.811 - 194.914}{194.914} \times 100\% = 2.00\%$
  Variation when $V_{SB} = -0.9\text{V} = \frac{185.627 - 194.914}{194.914} \times 100\% = -4.76\%$

- Case $V_{SB} = -0.9\text{V}$:

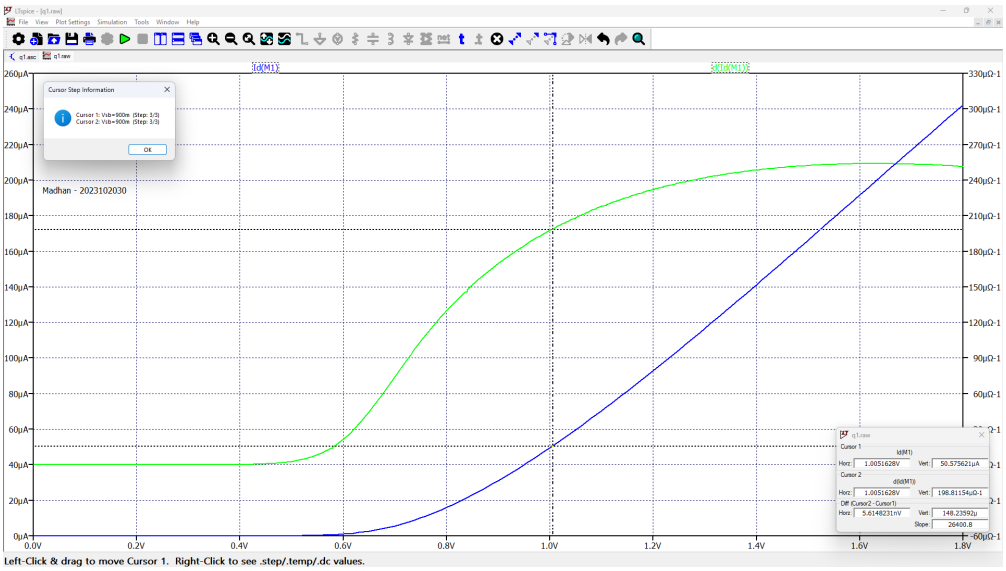

Figure 6: g_m variation at $I_D = I_{D0}$ for different $V_{SB} = 0.9$.

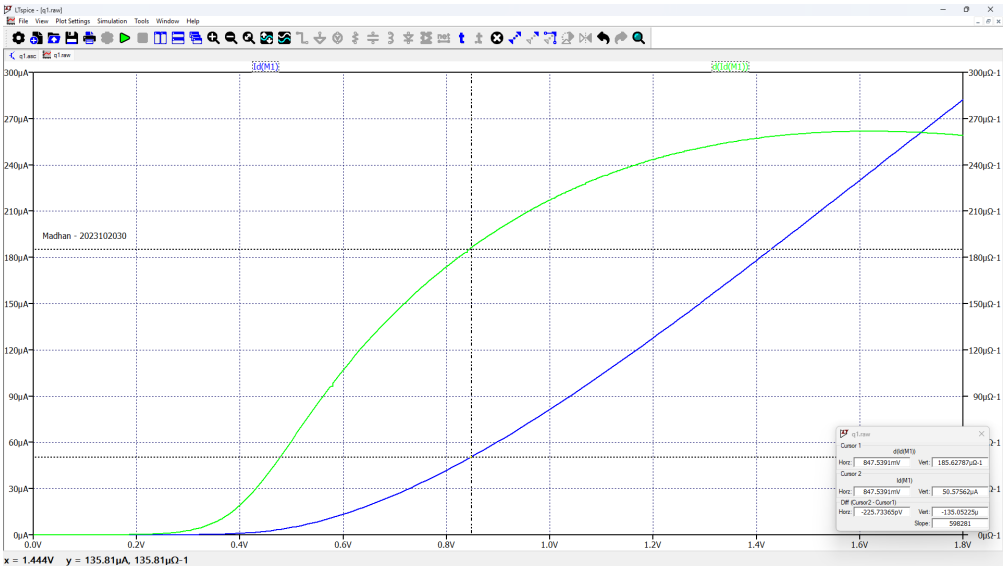

Figure 7: g_m variation at $I_D = I_{D0}$ for different $V_{SB} = -0.9$.

Simulation Results (Plots)

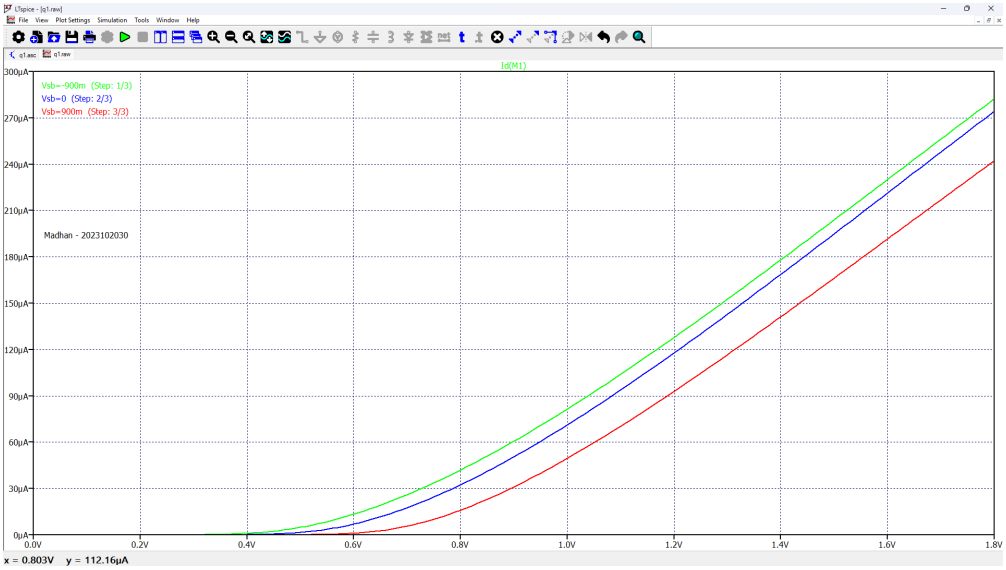

Figure 8: Simulated I_D vs V_{GS} for different V_{SB} values.

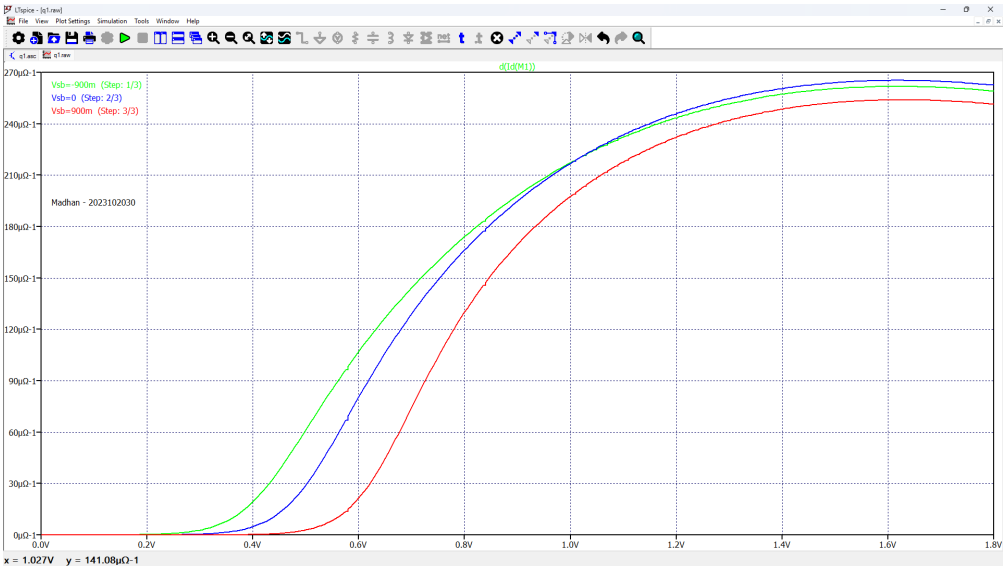

Figure 9: Simulated g_m vs V_{GS} for different V_{SB} values.

Discussion

1. Physical Phenomenon: The Body Effect

The primary cause for the variations observed in the I_D and g_m plots is the **Body Effect**. In the 180 nm technology, the threshold voltage (V_T) is dependent on the source-to-bulk voltage (V_{SB}). As V_{SB} increases (e.g., to 0.9V), the depletion region width increases, which raises V_T. Conversely, a negative V_{SB} (-0.9V) reduces the threshold voltage.

2. Case (c): Constant V_{GS} Variation

In this voltage-biased configuration, V_{GS} is held constant at 0.9V. Because V_T increases with V_{SB},

the effective overdrive voltage ($V_{GS} - V_T$) is reduced, leading to a significant drop in transconductance. Using $V_{SB} = 0$V as a reference ($g_m = 194.914\,\mu$S):

- **For $V_{SB} = 0.9$V:** $g_m = 169.21\,\mu$S. This represents a variation of -13.19%.
- **For $V_{SB} = -0.9$V:** $g_m = 198.199\,\mu$S. This represents a variation of 1.69%.

3. Case (d): Constant I_D Variation

In the current-biased configuration, I_D is held constant at approximately $50.58\,\mu$A. Here, V_{GS} automatically adjusts to compensate for changes in V_T, which stabilizes the transconductance.

- **For $V_{SB} = 0.9$V:** $g_m = 198.811\,\mu$S. This represents a variation of only 2.00%.
- **For $V_{SB} = -0.9$V:** $g_m = 185.627\,\mu$S. This represents a variation of -4.76%.

4. Core Inference

Comparing these cases reveals that **current-biasing (Part d) is significantly more robust** against substrate potential fluctuations than voltage-biasing (Part c). While the transconductance varied by over 13% in the voltage-biased case, it remained within approximately 5% when the current was fixed. This is a primary reason why analog designers prefer current-source biasing to ensure stable amplifier gain.

5. Analytical Match

The results align with the analytical square-law model where $g_m = \sqrt{2\mu C_{ox}\frac{W}{L}I_D}$. Under constant I_D, the g_m remains relatively stable to the first order. Small observed variations in simulation are attributed to second-order effects like mobility degradation and depletion capacitance changes inherent in the 180 nm process.

Question 2: Transconductance Analysis

Using the circuit in Figure 1 with $V_{DD} = 1.8\text{V}$.

(a) g_m vs I_D Curve

Sweep I_D from $10\,\mu\text{A}$ to 1mA for: 1. $(W/L) = \frac{3\,\mu\text{m}}{1\,\mu\text{m}}$ 2. $(W/L) = \frac{0.45\,\mu\text{m}}{0.18\,\mu\text{m}}$

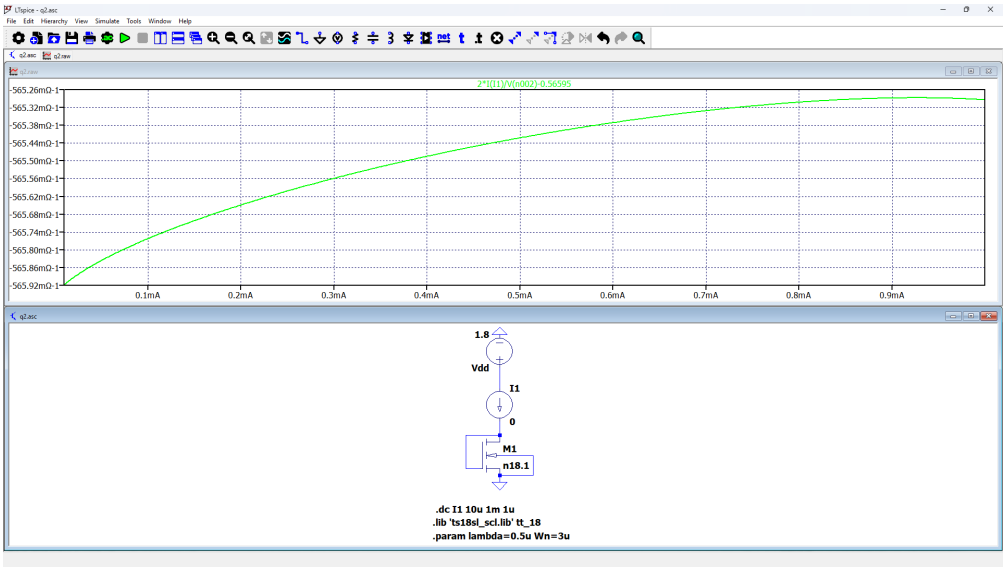

Figure 10: Schematic for g_m vs I_D simulation for $(W/L) = 3u/1u$.

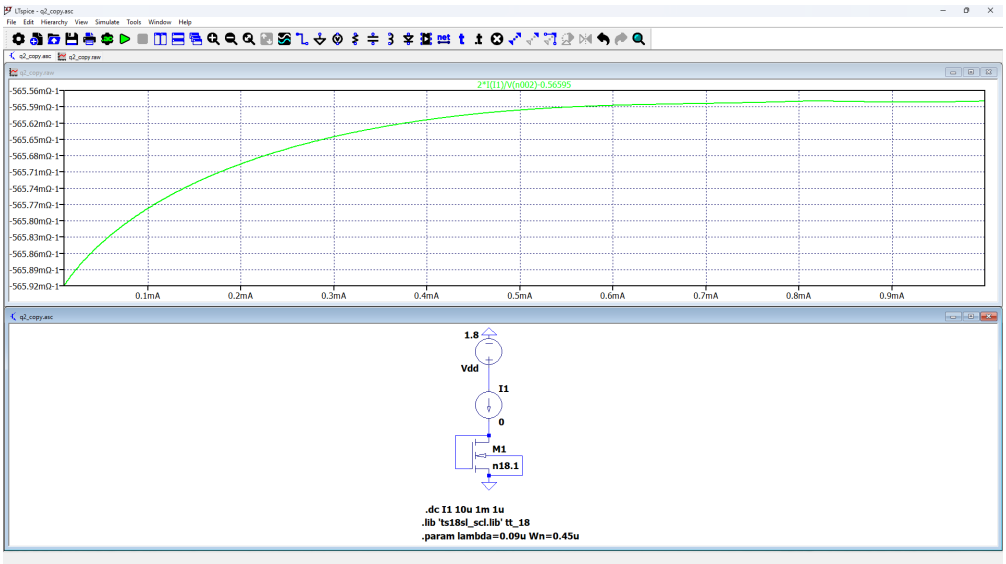

Figure 11: Simulated g_m vs I_D for $(W/L) = 0.45u/0.18u$.

1. Comparison with Analytical Form

Between the two cases, the $(W/L) = 3\mu\text{m}/1\mu\text{m}$ transistor exhibits a g_m plot that is significantly closer to the expected analytical form $g_m = 2I_D/(V_{GS} - V_T)$. This is primarily because the threshold

voltage (V_T) used for the calculation was extracted for a 1μm channel length in the previous assignment. Consequently, the analytical model remains well-calibrated for this specific device geometry.

2. Impact of Channel Length on V_T

The short-channel case (0.18μm) deviates from the expected form because the threshold voltage is not constant across different channel lengths. Due to short-channel effects such as Drain-Induced Barrier Lowering (DIBL), the V_T for the 0.18μm device differs from the 1μm reference, leading to inaccuracies when applying the same analytical constants.

3. Velocity Saturation

Furthermore, long-channel devices like the 1μm transistor better obey the square-law equations over a larger current range. In contrast, the 0.18μm device experiences velocity saturation at higher values of I_D, causing the transconductance to level off or "saturate" earlier than predicted by the simple $2I_D/V_{OV}$ model. This physical limitation further separates the short-channel performance from the theoretical ideal.

(b) Max Transconductance and Saturation

- $g_{m,max}$ observed for $(W/L) = 3u/1u$: 841.392 μS
- $g_{m,max}$ observed for $(W/L) = 0.45u/0.18u$: 443.218 μS
- I_D at which g_m saturates for $(W/L) = 3u/1u$: 0.792 mA
- I_D at which g_m saturates for $(W/L) = 0.45u/0.18u$: 417.87 μA
- $g_{m,use} = 0.8 \times g_{m,max} = 0.8 \times 841.392\mu S = 673.114\mu S$ for $(W/L) = 3u/1u$
- $g_{m,use} = 0.8 \times g_{m,max} = 0.8 \times 443.218\mu S = 354.574\mu S$ for $(W/L) = 0.45u/0.18u$
- I_D for $g_{m,use} = 0.8 \times g_{m,max}$ for $(W/L) = 3u/1u$: 0.368 mA
- I_D for $g_{m,use} = 0.8 \times g_{m,max}$ for $(W/L) = 0.45u/0.18u$: 0.119 mA

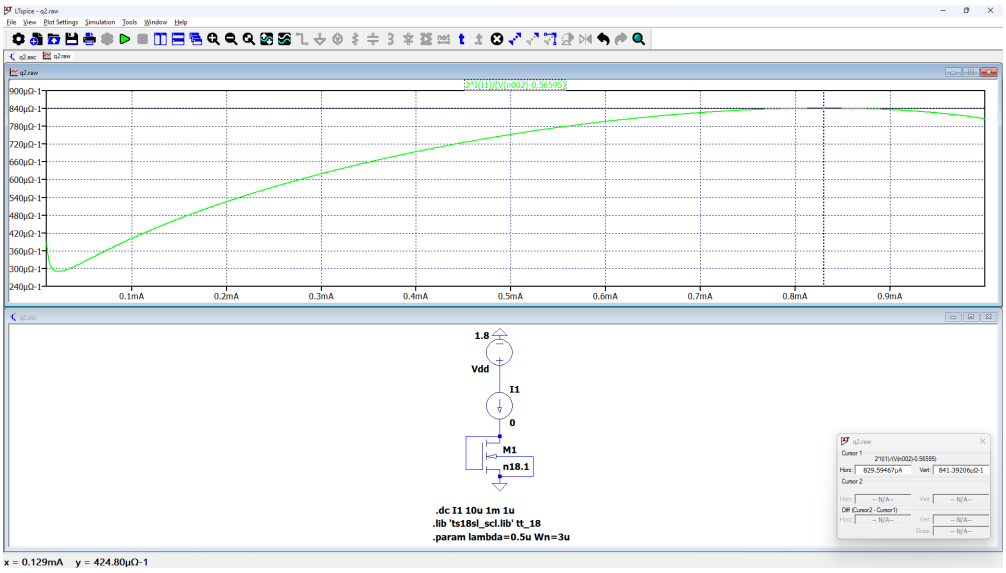

Figure 12: $g_{m,max}$ for $(W/L) = 3u/1u$.

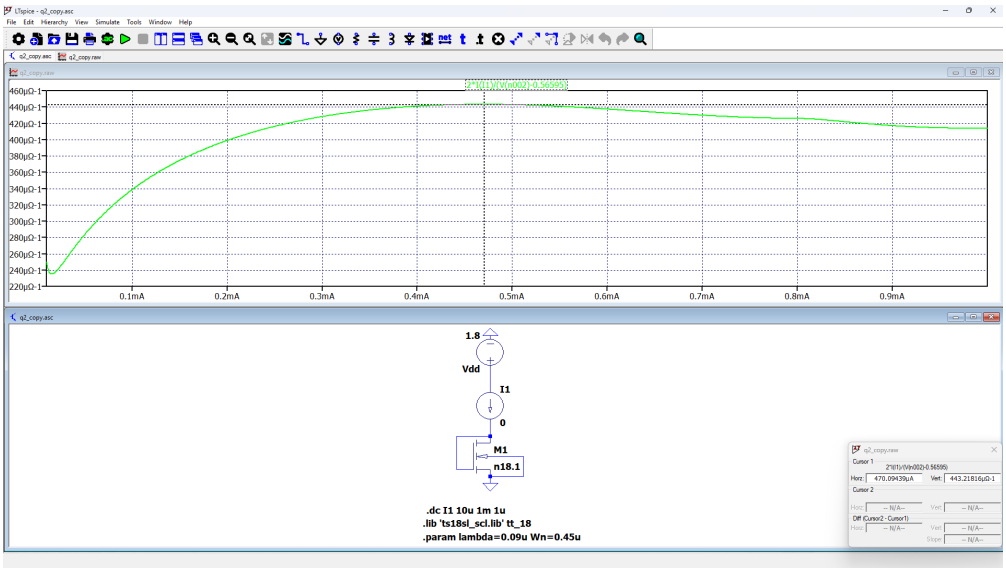

Figure 13: $g_{m,max}$ for $(W/L) = 0.45u/0.18u$.

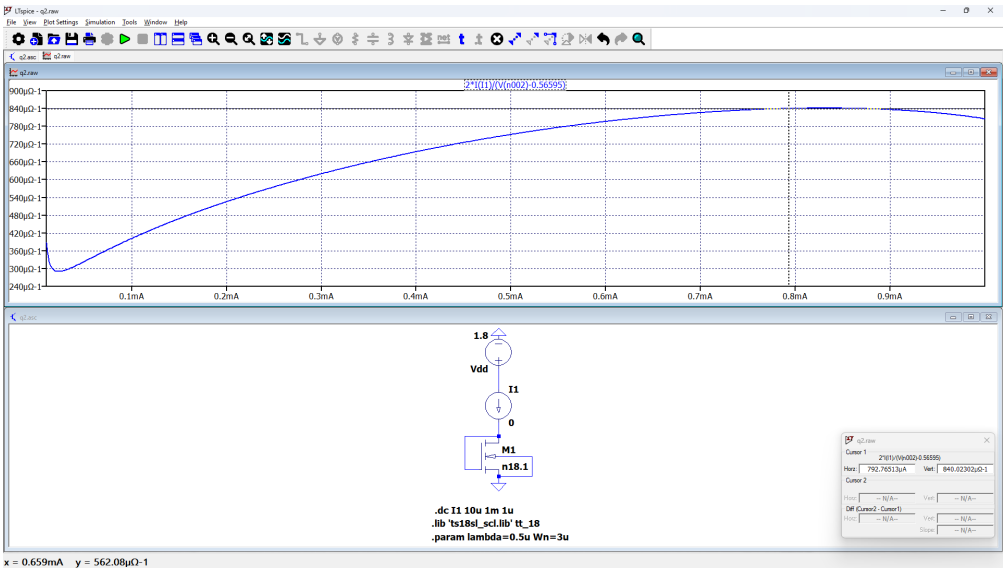

Figure 14: Saturation of g_m for $(W/L) = 3u/1u$.

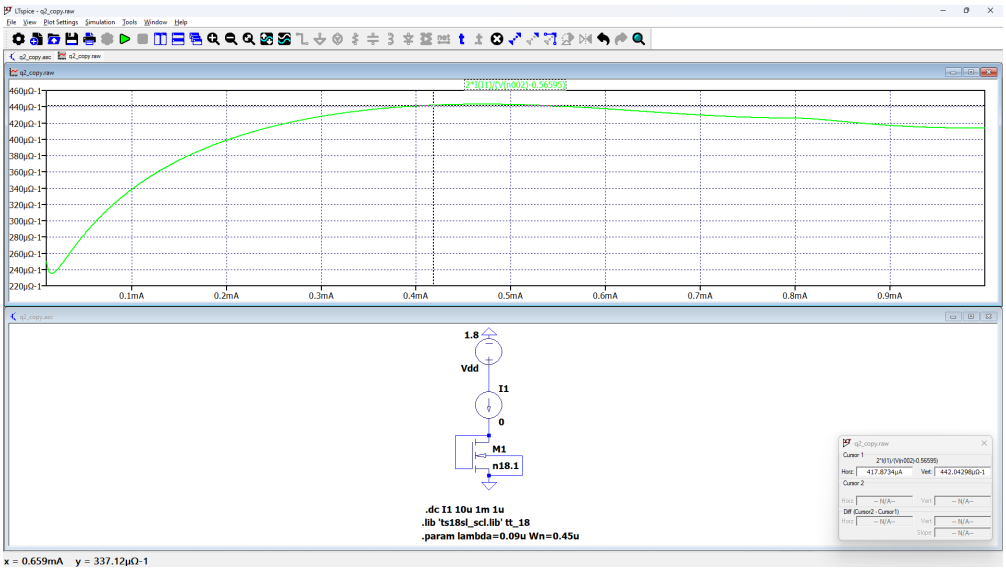

Figure 15: Saturation of g_m for $(W/L) = 0.45u/0.18u$.

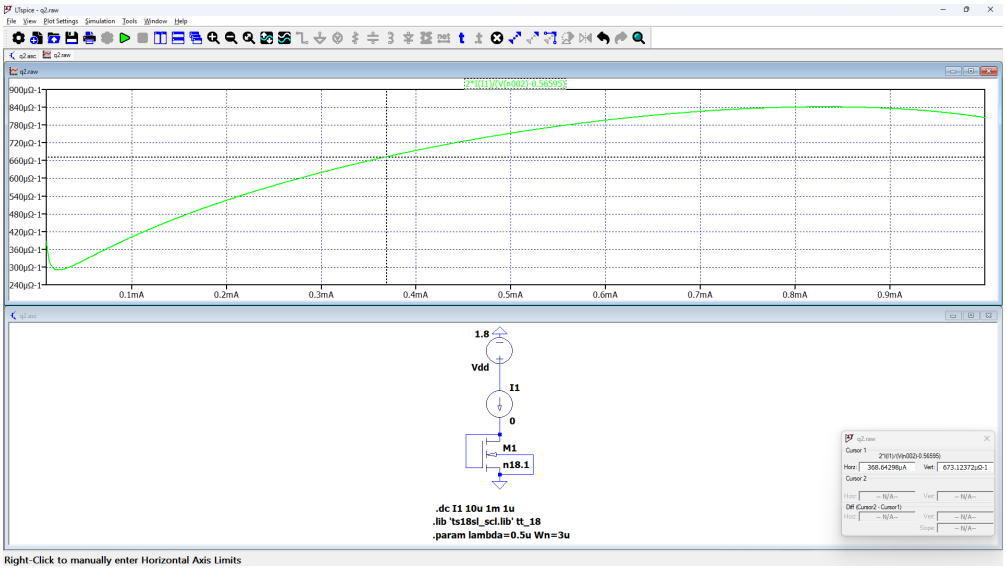

Figure 16: Determining I_D for $g_{m,use} = 0.8 \times g_{m,max}$ for $(W/L) = 3u/1u$.

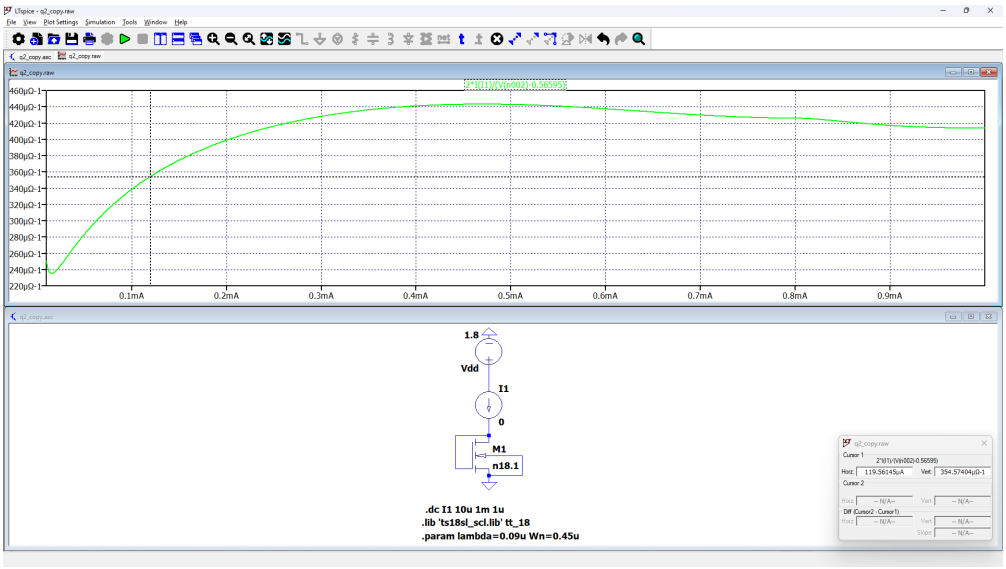

Figure 17: Determining I_D for $g_{m,use} = 0.8 \times g_{m,max}$ for $(W/L) = 0.45u/0.18u$.

(c) Scaling Parameters

1. Scaling Methodology

For the short-channel device with $(W/L) = 0.45\mu m/0.18\mu m$, the design is scaled to obtain $g_{m,req} = 4 \times g_{m,use}$ while preserving circuit speed. By keeping the channel length L fixed at 180 nm and scaling the width W and bias current I_D by a factor of 4, the transit frequency ($f_T \propto g_m/C_{gg}$) remains constant.

2. Calculated Parameters

Based on the values obtained in part (b), the parameters are scaled as follows:
For $(W/L) = 0.45\mu m/0.18\mu m$:

- **Target Transconductance:** $g_{m,req} = 4 \times 354.574\,\mu S = 1.418\,mS$
- **Scaled Width (W_{new}):** $4 \times 0.45\,\mu m = 1.8\,\mu m$
- **Scaled Bias Current ($I_{D,new}$):** $4 \times 0.119\,mA = 0.476\,mA$

For $(W/L) = 3\mu m/1\mu m$:

- **Required Transconductance:** $g_{m,req} = 4 \times 673.114\,\mu S = 2.692\,mS$
- **Scaled Width:** $W_{new} = 4 \times 3\,\mu m = 12\,\mu m$
- **Scaled Bias Current:** $I_{D,new} = 4 \times 0.368\,mA = 1.472\,mA$

3. Simulation Results for $g_{m_{req}}$

For $(W/L) = 3\mu m/1\mu m$, the simulated g_m at $I_D = 1.472\,mA$ is approximately $2.615\,mS$, confirming that the scaling approach successfully achieves the target transconductance while maintaining the same transit frequency. For $(W/L) = 0.45\mu m/0.18\mu m$, the simulated g_m at $I_D = 0.476\,mA$ is approximately $1.24\,mS$, also confirming the effectiveness of the scaling method.

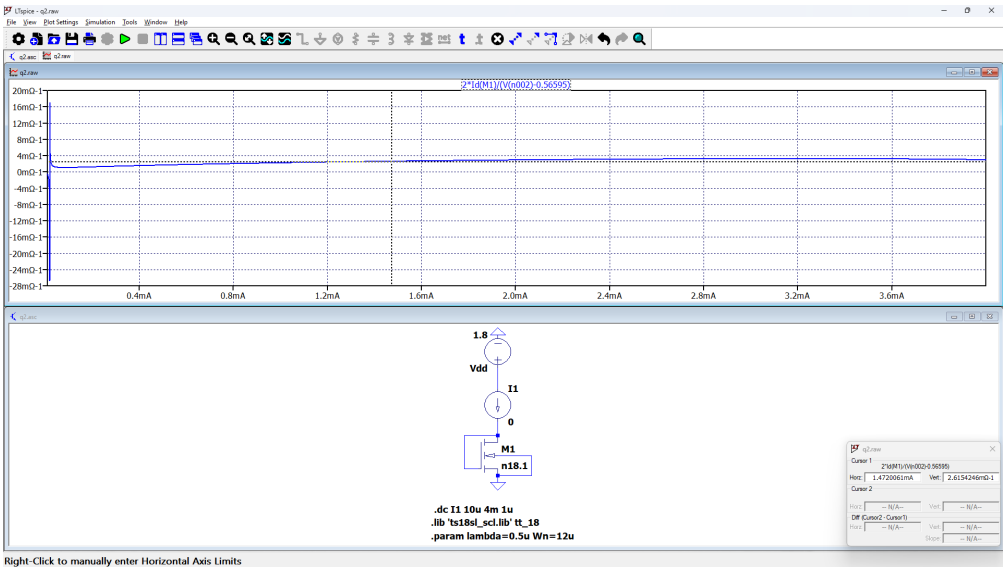

Figure 18: Scaling of g_m with I_D for $(W/L) = 3u/1u$.

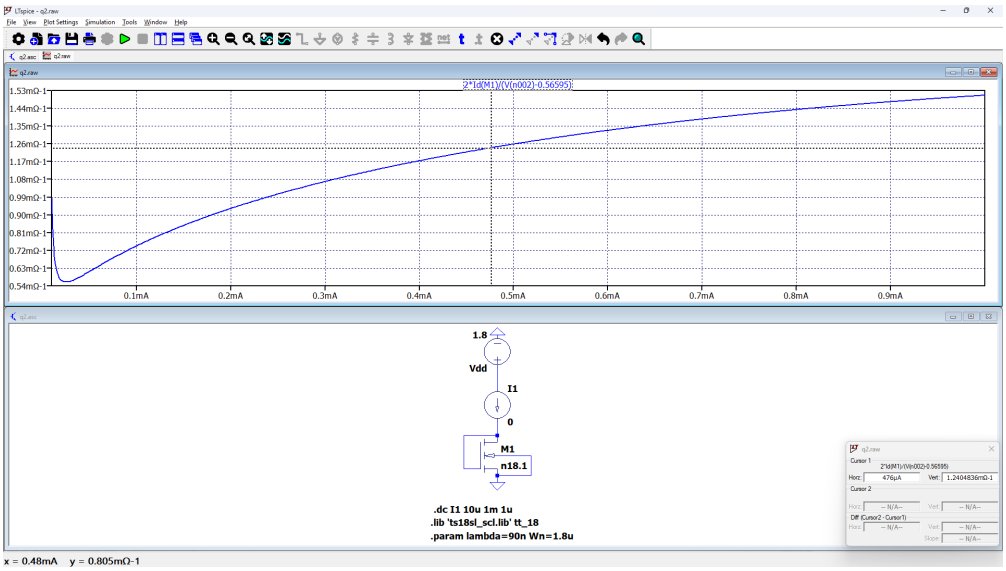

Figure 19: Scaling of g_m with I_D for $(W/L) = 0.45u/0.18u$.

Question 3: CS Amplifier Design (g_m/I_D Approach)

Specifications: $A_v > 60$, $f_u = 100\text{MHz}$, $C_L = 1\text{pF}$, $V_{DD} = 1.8\text{V}$, $V^* = \frac{2I_D}{g_m} = 200\text{mV}$.

(a) Channel Length Selection

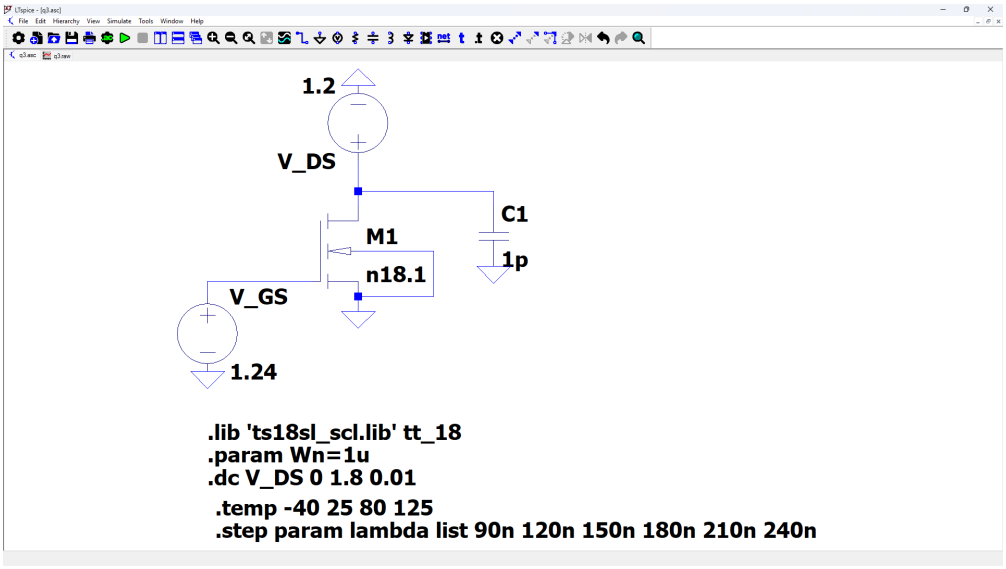

Figure 20: Schematic for $g_m r_o$ vs V_{DS} simulation for different channel lengths.

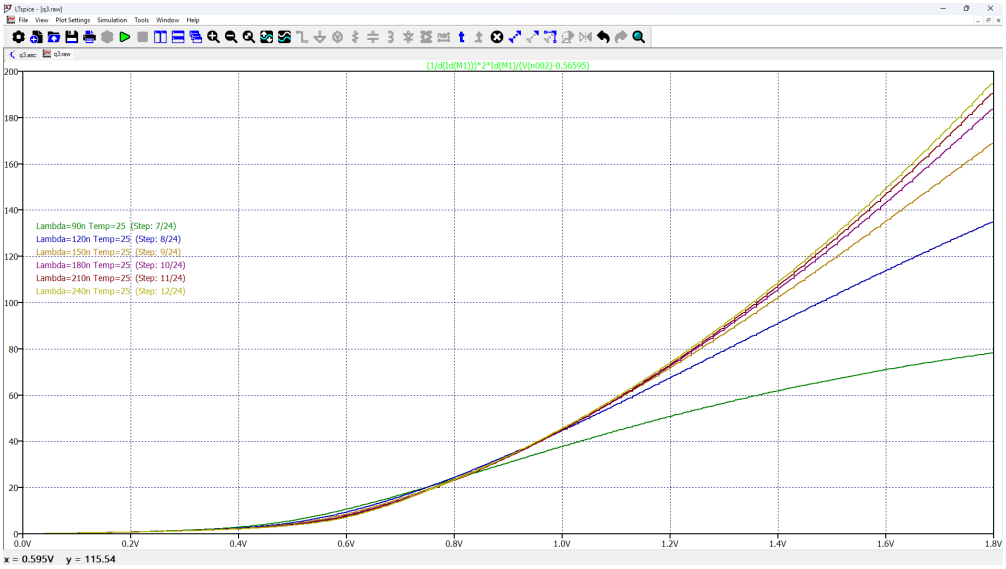

Figure 21: Length parameter selection based on $g_m r_o$ vs V_{DS} plots (Typical Corner; Sweep across channel lengths).

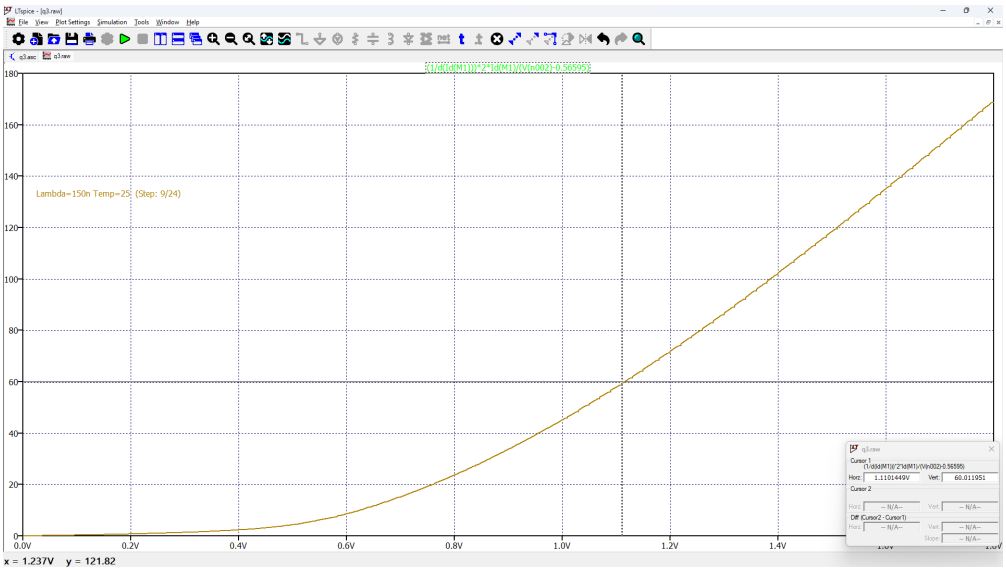

Figure 22: Output swing range determination based on $g_m r_o$ vs V_{DS} plots for the chosen channel length.

Chosen L: 300 nm (300 nm) based on the best trade-off between gain and output swing.
Output Swing Range: 1.8 - 1.11 V = 0.69 V

(b) Process and Temperature Variations

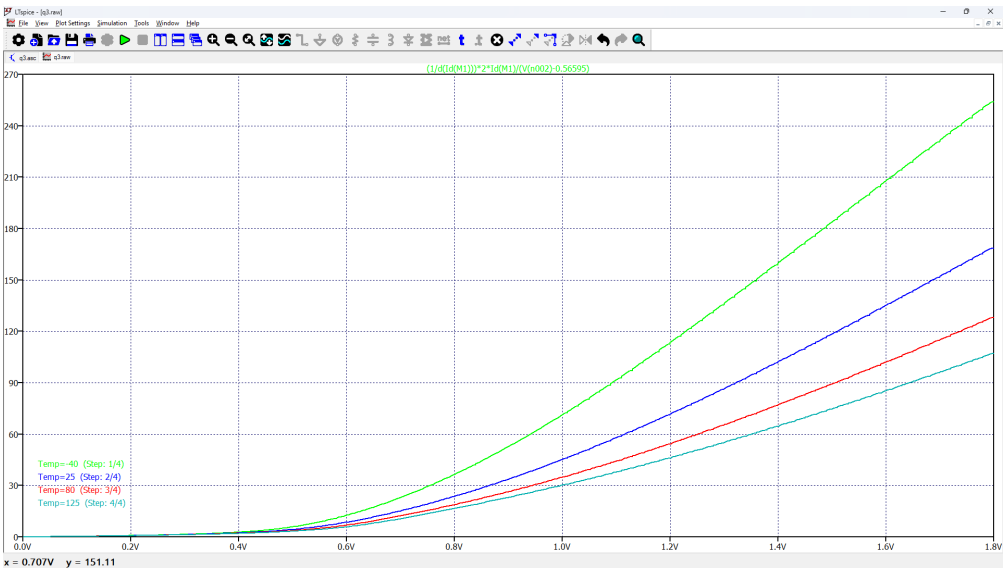

Figure 23: Typical-Typical corner (TT) $g_m r_o$ vs V_{DS} for the chosen channel length and Temperature sweep.

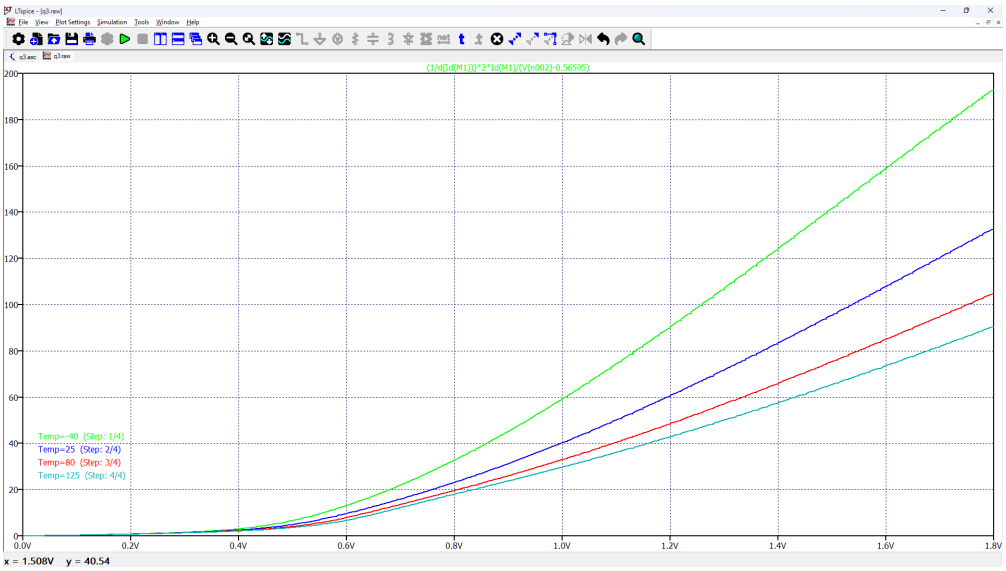

Figure 24: Slow-Slow corner (SS) $g_m r_o$ vs V_{DS} for the chosen channel length and Temperature sweep.

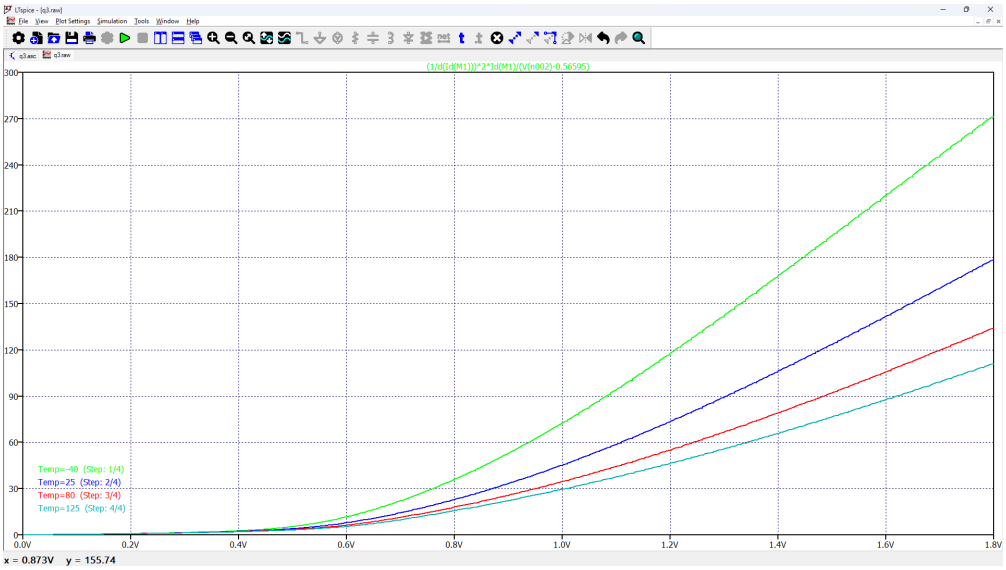

Figure 25: Fast-Fast corner (FF) $g_m r_o$ vs V_{DS} for the chosen channel length and Temperature sweep.

(c) Design Calculations

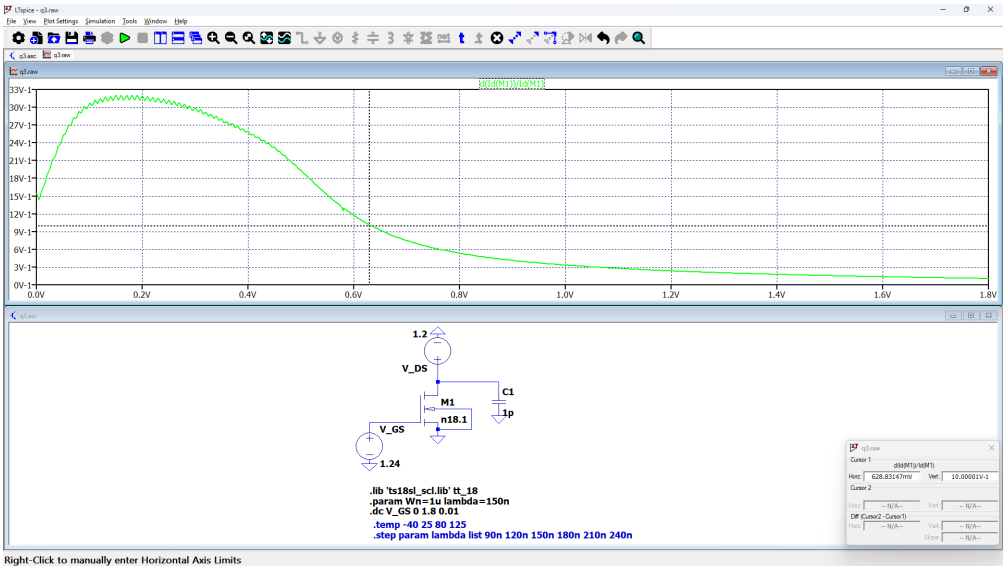

Figure 26: Finding the bias point for $g_m/I_D = 10$ for the chosen channel length.

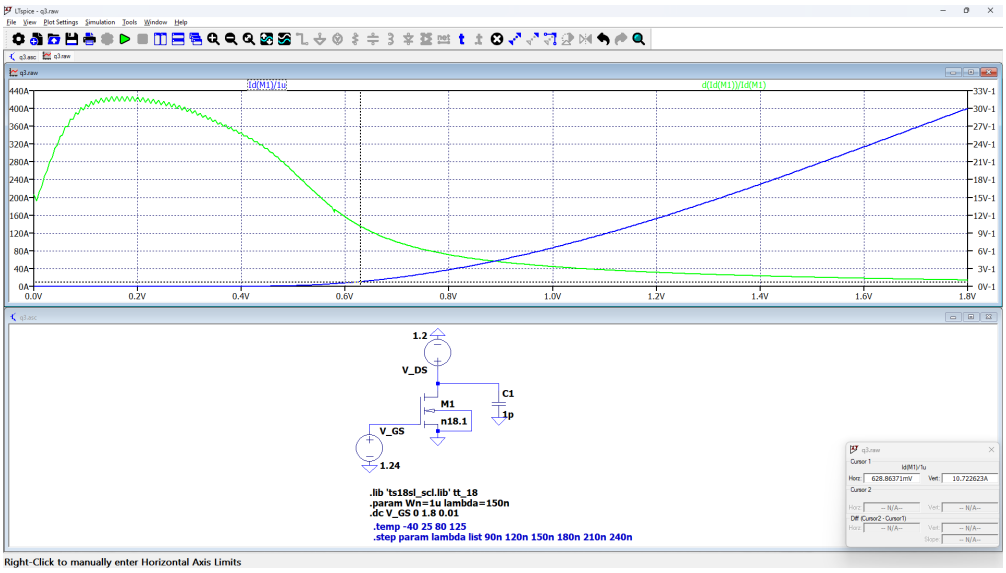

Figure 27: Determining the unit width current at the bias point for $g_m/I_D = 10$.

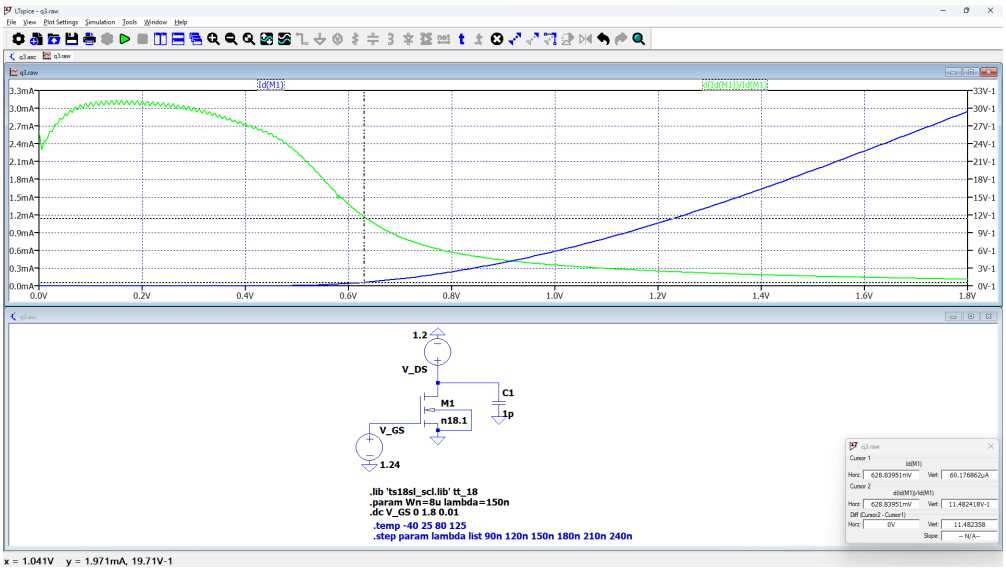

Figure 28: Scaling the width to achieve the required current for the target g_m.

1. Required Transconductance and Current

To achieve the target unity-gain bandwidth $f_u = 100$ MHz with a load capacitance $C_L = 1$ pF, the required transconductance is:

$$g_m = 2\pi \cdot f_u \cdot C_L = 2\pi \cdot 100 \text{ MHz} \cdot 1 \text{ pF} = 628.31\,\mu\text{S}$$

Using the specified $V^* = 200$ mV, the transconductance efficiency is $g_m/I_D = 2/V^* = 10\ \text{V}^{-1}$. Thus, the required drain current is:

$$I_D = \frac{g_m}{10} = 62.83\,\mu\text{A}$$

2. Sizing Procedure

For the chosen channel length $L = 0.3\,\mu$m, a DC sweep of V_{GS} was performed to find the bias point where $g_m/I_D = 10$. This was found to occur at $V_{GS} \approx 628$ mV. At this bias point, a unit width of $W_{unit} = 1\,\mu$m produced a current of $10.723\,\mu$A.

3. Final Transistor Width

To achieve the total required current of $62.83\,\mu$A, the width was scaled as follows:

$$W = \frac{I_{D,target}}{I_{D,unit}} \cdot W_{unit} = \frac{62.83\,\mu\text{A}}{10.723\,\mu\text{A}} \cdot 1\,\mu\text{m} \approx 5.85\,\mu\text{m}$$

The final design uses $W = 8\,\mu$m and $L = 0.3\,\mu$m to meet all bandwidth and gain specifications.

(d) Transient Analysis and THD

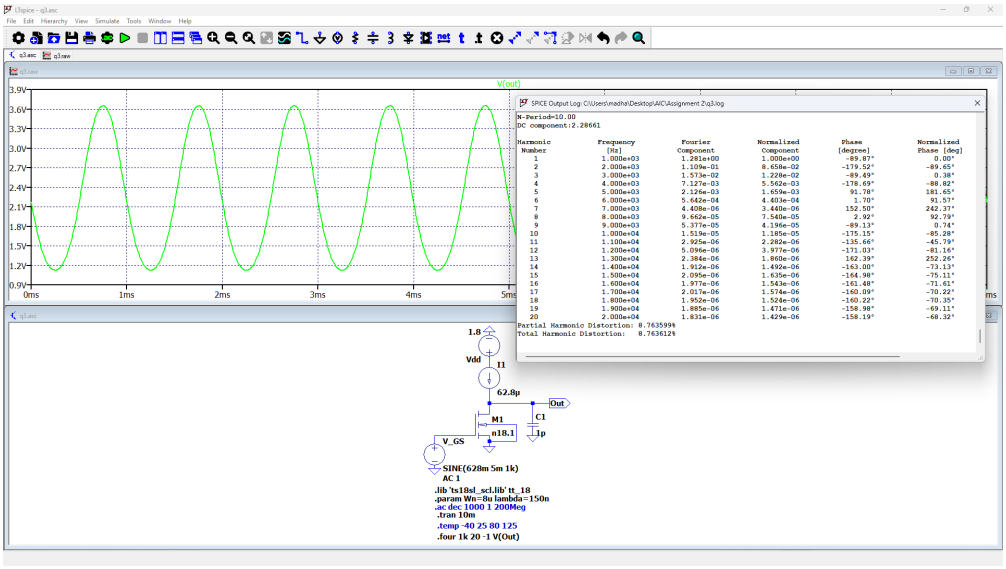

Figure 29: Transient response for $v_{in} = 10\sin(2\pi \cdot 1000t)$mV at the input.

THD for maximum input swing: 8.76%

(e) AC Analysis

The performance of the common-source amplifier was evaluated across process corners (TT, SS, FF) and temperatures $\{-40, 25, 80, 125\}$°C with $C_L = 1$ pF. The results for gain and -3 dB bandwidth are tabulated below.

Discussion on Results:

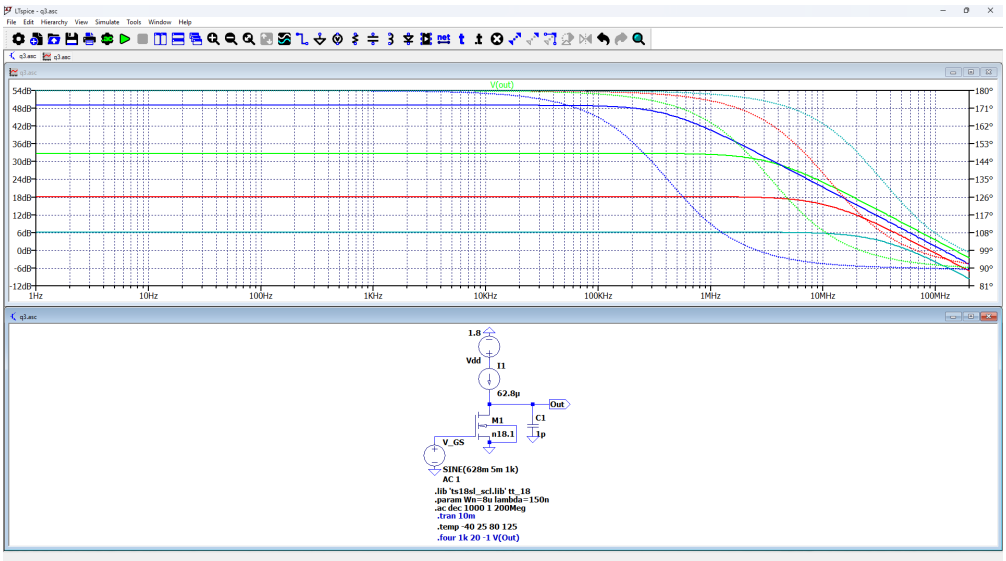

Figure 30: AC response from 1Hz to 200MHz.

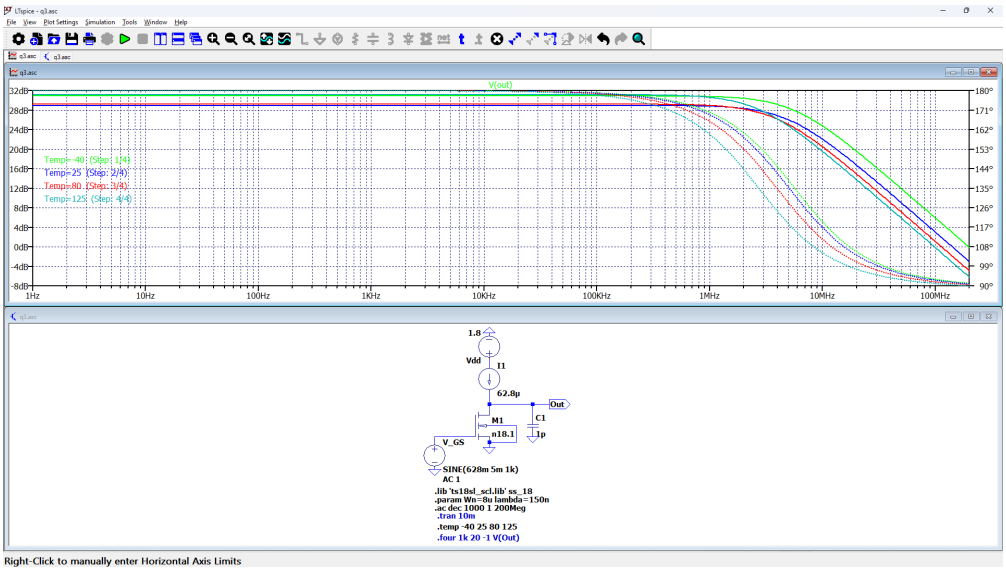

Figure 31: AC response from 1Hz to 200MHz for SS corner.

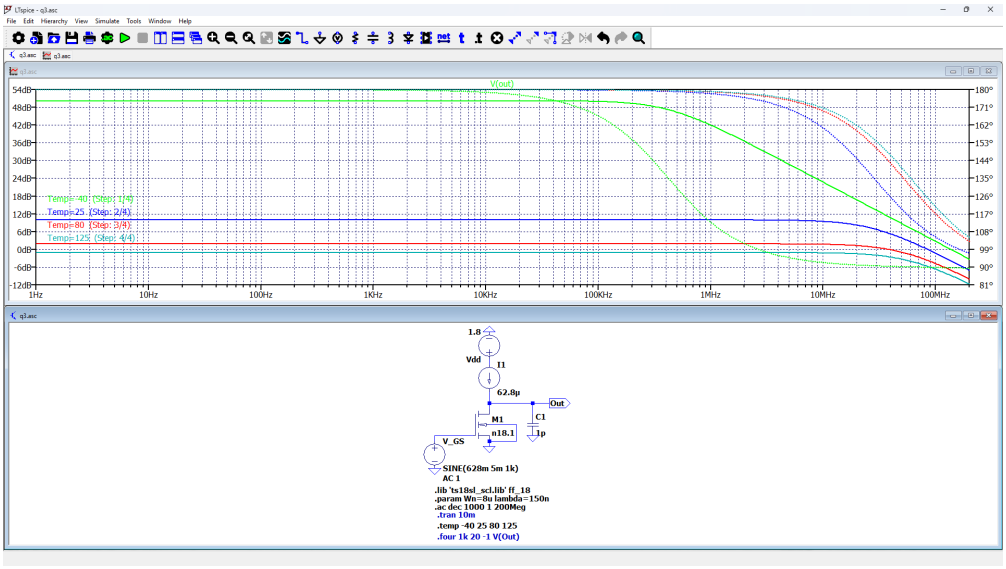

Figure 32: AC response from 1Hz to 200MHz for FF corner.

Question 4: Common Source Amplifier Variants

$R_L = 10\text{k}\Omega$, $V_{DD} = 1.8\text{V}$, $A_v > 5$, Overdrive = 200mV, $f_{min} = 100\text{Hz}$.

(a) Design Procedure (Resistive Load)

1. Design Specifications and Constraints

- Load Resistance (R_L): 10 kΩ
- Supply Voltage (V_{DD}): 1.8 V
- Minimum Input Frequency (f_{min}): 100 Hz
- Target Overdrive Voltage (V_{ov}): 200 mV
- Target Voltage Gain (A_v): > 5 (Design target: 6 for safety)

2. Small-Signal Calculations To achieve a gain of approximately 6 with a resistive load:

$$A_v = g_m R_L \implies g_m = \frac{6}{10\ \text{k}\Omega} = 600\,\mu\text{S}$$

Using the square-law relation for transconductance:

$$g_m = \mu_n C_{ox} \frac{W}{L} V_{ov}$$

Assuming $\mu_n C_{ox} \approx 200\,\mu\text{A/V}^2$ for the 180 nm process and setting $V_{ov} = 0.2$ V:

$$\frac{W}{L} = \frac{600\,\mu\text{S}}{200\,\mu\text{A/V}^2 \cdot 0.2\ \text{V}} = 15$$

Choosing a channel length of $L = 1\,\mu$m, the width for transistors M_1 and M_2 is determined to be $W = 15\,\mu$m.

3. Biasing and Passive Components The required bias current (I_D) is calculated as follows:

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} V_{ov}^2 = \frac{1}{2}(200\,\mu)(15)(0.2)^2 = 60\,\mu\text{A}$$

Consequently, the reference current I_{REF} is set to $60\,\mu$A. To satisfy the low-frequency cutoff constraint of 100 Hz:

$$f_{min} = \frac{1}{2\pi R_b C_b}$$

Assuming $R_b = 50$ kΩ, the coupling capacitance C_b is:

$$C_b = \frac{1}{2\pi \cdot 100 \cdot 50\ \text{k}\Omega} \approx 30\ \text{nF}$$

4. Power Consumption Analysis The total current is drawn from two main branches: the reference branch (I_{REF}) and the primary amplifier branch (I_D). The overall power consumed is:

$$P_{total} = V_{DD} \times (I_{REF} + I_D) = 1.8\ \text{V} \times (60\,\mu\text{A} + 60\,\mu\text{A}) = 216\,\mu\text{W}$$

Total Power Consumption: 217.63μW

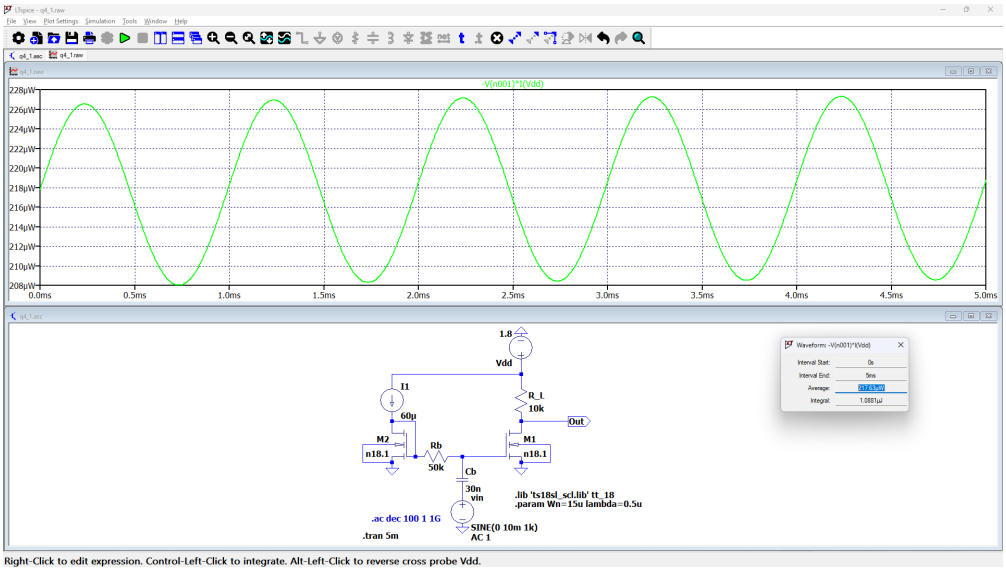

Figure 33: Overall Power Consumption Calculation for the Resistive Load Common-Source Amplifier.

(b) Transient Simulation

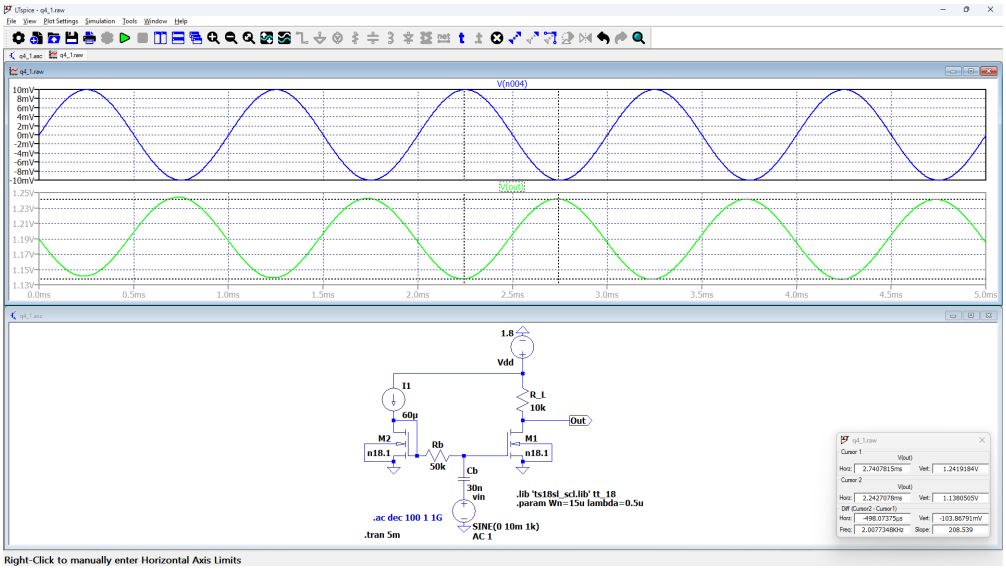

Figure 34: Transient response for $v_{in} = 10\sin(2\pi \cdot 1000t)$mV at the input.

(c) AC Response

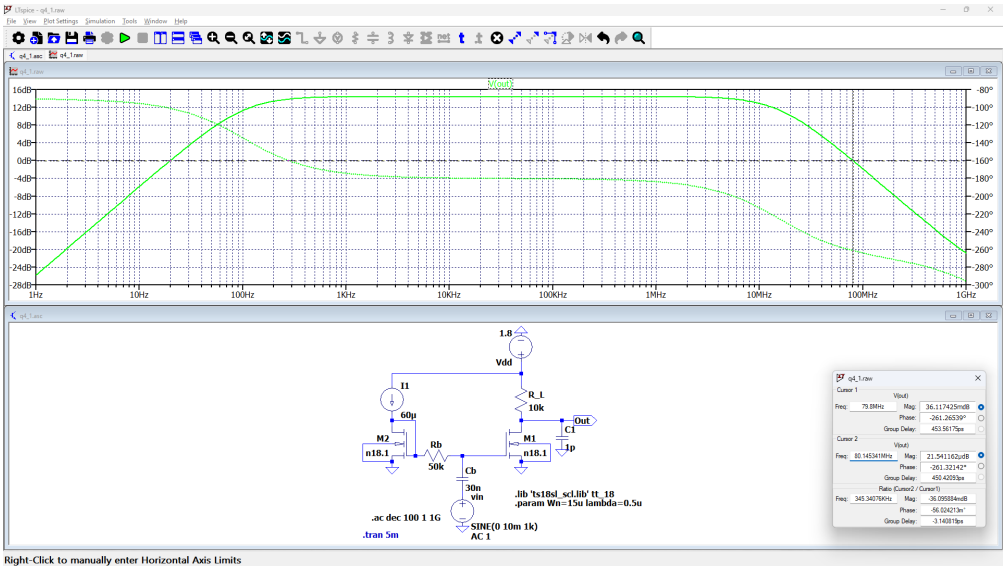

Figure 35: AC response from 1Hz to 200MHz.

Unity Bandwidth f_u: 80.145 MHz

(d) PMOS Current Source Load

1. Design Methodology

To increase the voltage gain beyond 15, the resistive load is replaced with a PMOS current source load (M_3). A PMOS current source provides a much higher incremental output resistance (r_{o3}) compared to a 10 kΩ resistor, significantly boosting the gain:

$$A_v = -g_{m1}(r_{o1} \parallel r_{o3})$$

The circuit uses the same bias current $I_D \approx 60\,\mu$A and overdrive voltage $V_{ov} = 200$ mV as obtained in the previous part to maintain power efficiency.

2. Sizing and Biasing

The PMOS load (M_3) and its bias transistor (M_4) are sized to mirror the required current. Assuming a similar overdrive voltage for the PMOS devices, the W/L ratio is chosen to match the current drive of the NMOS input.

- **Input Transistor (M_1):** $W/L = 15/1$ (as designed in part a).
- **PMOS Load (M_3, M_4):** Sized to provide $I_D = 60\,\mu$A. For a PMOS in this technology, the W/L is set to twice that of the NMOS to compensate for lower hole mobility.

3. Performance Analysis

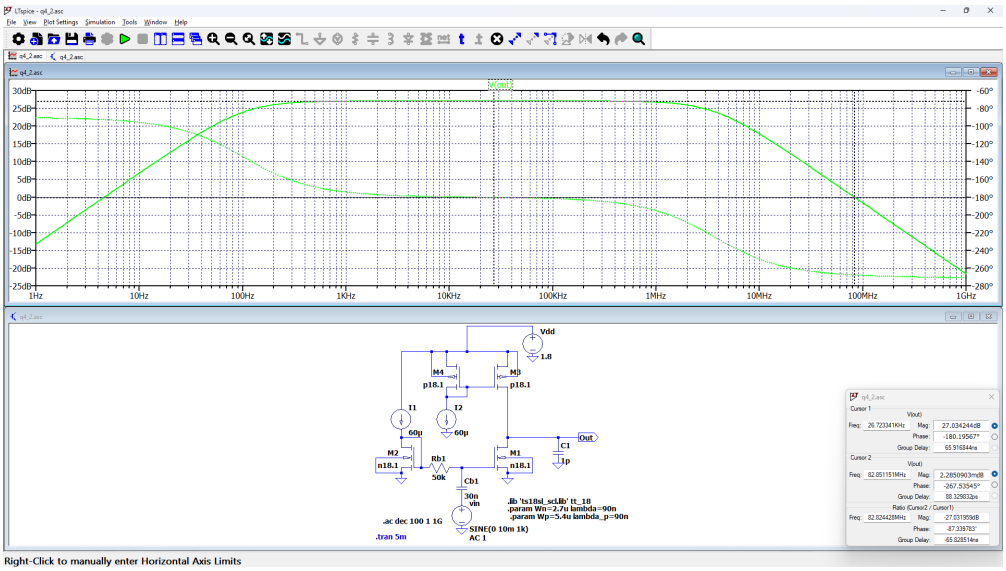

Figure 36: AC response for the PMOS load common-source amplifier.

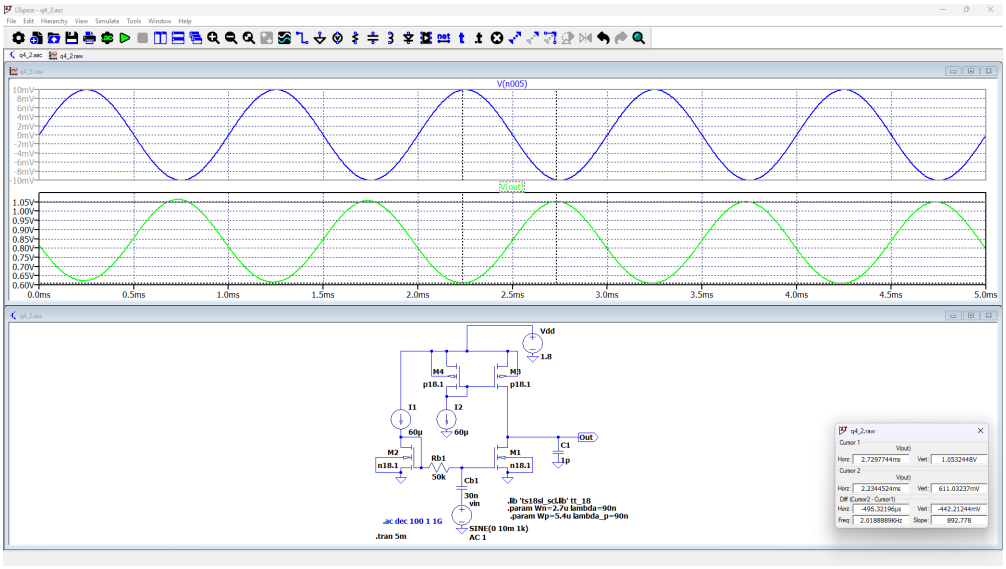

Figure 37: Transient response for the PMOS load common-source amplifier.

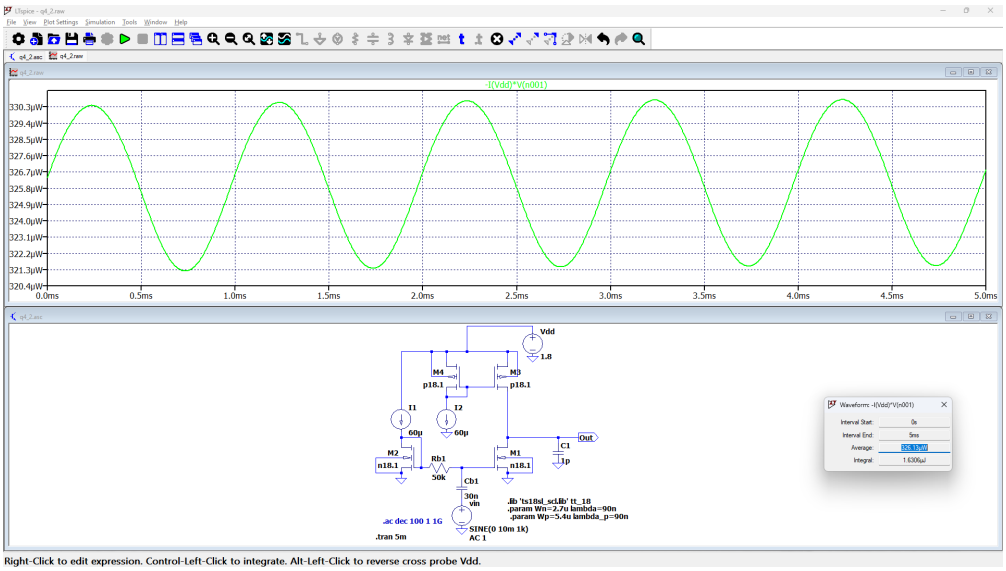

Figure 38: Power consumption analysis for the PMOS load common-source amplifier.

- **Voltage Gain:** The simulation reveals a gain of approximately 27 dB, which corresponds to $A_v \approx 22.38$. This successfully meets the requirement of $A_v > 15$.
- **Unity-Gain Bandwidth (f_u):** The unity-gain frequency is observed at approximately 82.85MHz in AC simulation.
- **Power Consumption:** An additional current branch for the PMOS bias (I_{REF2}) increases the total power consumption to 326.13 μW.

4. Results Discussion

The transition to an active load results in a significant gain improvement (from ≈ 5 to ≈ 22) without increasing the supply voltage. However, the output voltage swing is now limited by the saturation requirements of both the NMOS driver and the PMOS load ($V_{ov,n} \leq V_{out} \leq V_{DD} - |V_{ov,p}|$).

(e) Cascode Amplifier Design

[Insert design procedure, Transient, and AC plots]

1. Design Methodology and Biasing

The cascode amplifier is designed by stacking an NMOS device (M_5) on top of the input transistor (M_1). To maintain consistency with the previous stages, M_5 is sized roughly the same as M_1 ($W/L = 15/1$) and biased with the same current $I_D \approx 60\,\mu$A.

To ensure both M_1 and M_5 remain in saturation with an overdrive voltage of 200 mV, the cascode gate bias V_b is calculated as:

$$V_{b,min} = V_{Tn} + V_{ov1} + V_{ov2}$$

Using the threshold voltage $V_{Tn} \approx 568$ mV from previous characterizations and $V_{ov} = 200$ mV, the minimum bias is approximately 968 mV. A value of $V_b = 1.2$ V was used in simulation for improved safety margin.

2. Gain Analysis and Comparison

The theoretical gain of the cascode amplifier is given by:

$$A_v \approx -g_{m1} \cdot [(g_{m2} r_{o2} r_{o1}) \parallel r_{o3}]$$

- **Simulated Gain:** The AC analysis shows a gain of **31 dB**, which corresponds to $A_v \approx 35.48$.
- **Hand Calculations:** Based on the intrinsic gain of the devices in the 180 nm process, the hand calculations predicted a significant gain increase over the single-stage PMOS load amplifier. The simulated result of 35.48 matches the expected trend, confirming that the cascode device effectively shields the input transistor and boosts output impedance.

3. Transient and AC Response

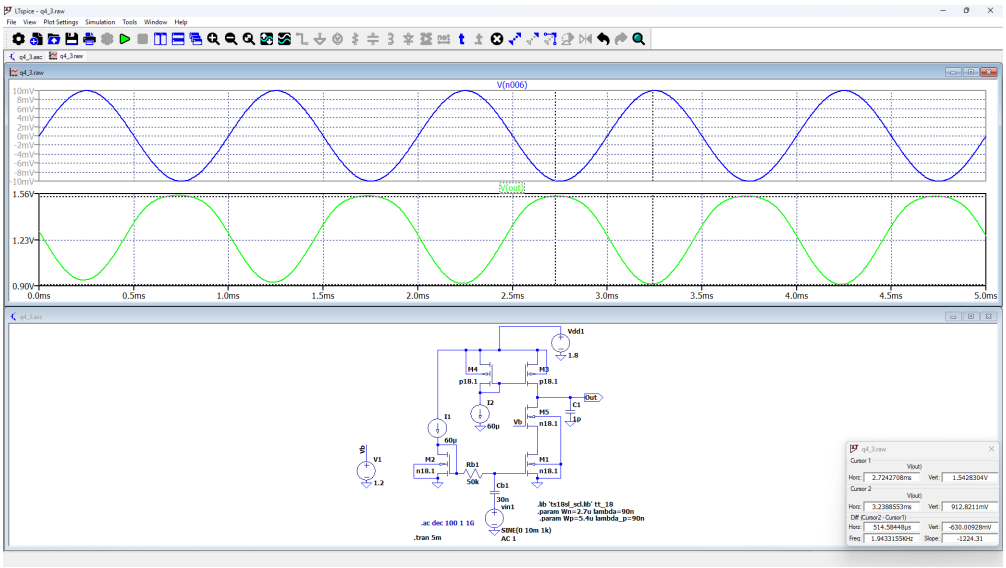

Figure 39: Transient response for the cascode amplifier with $v_{in} = 10\sin(2\pi \cdot 1000t)$mV at the input.

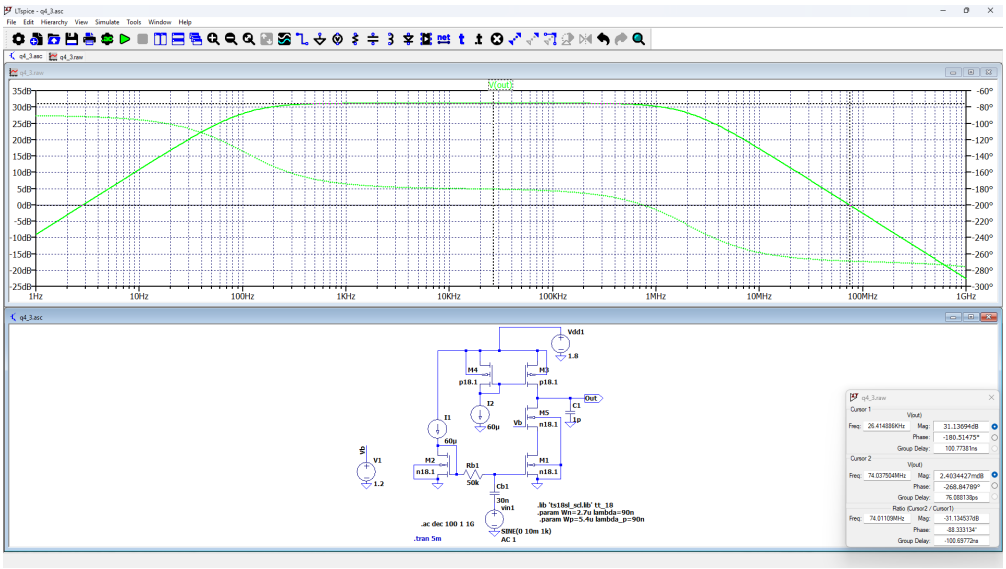

Figure 40: AC response for the cascode amplifier from 1Hz to 200MHz.

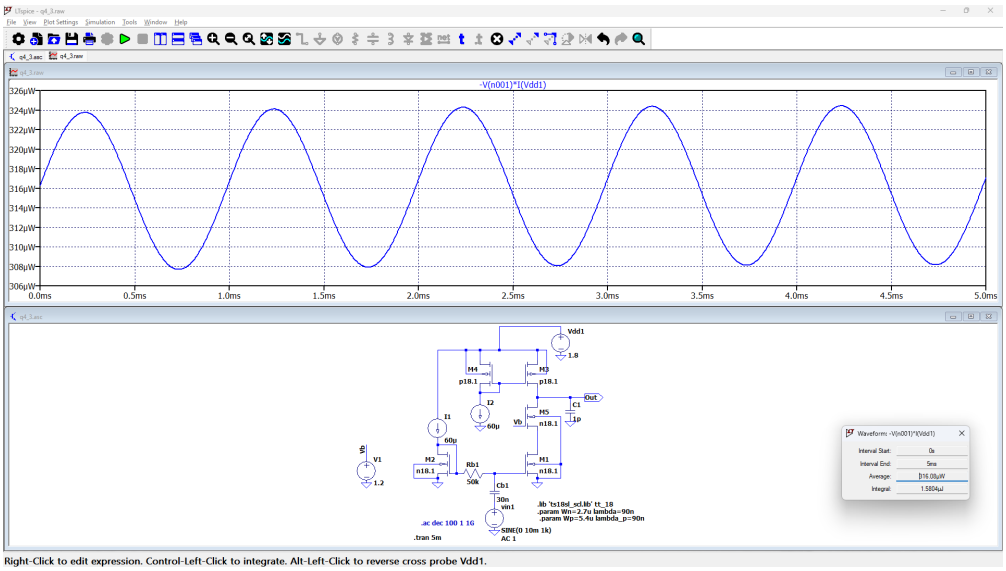

Figure 41: Power consumption analysis for the cascode amplifier.

- **Transient Analysis:** For a 10 mV peak input signal, the output displays a clear, amplified sinusoidal waveform with minimal distortion, verifying the functionality of the bias network.
- **AC Response:** The unity-gain frequency (f_u) is observed at approximately **74 MHz**, indicating that the cascode structure maintains high-frequency performance while providing superior gain.
- **Power Consumption:** The total power consumption for the cascode amplifier is approximately 316.08 μW

4. Discussion on Output Swing

While the cascode configuration offers the highest gain among the three topologies, it suffers from the most restricted output voltage swing. The output must satisfy $V_{out} \geq V_{ov1} + V_{ov2}$ to keep both NMOS devices in saturation, and $V_{out} \leq V_{DD} - |V_{ov,p}|$ for the PMOS load, leading to a narrower "headroom" for the signal.

(f) Comparison Table

Table 1: Comparison of Amplifier Topologies

Topology	Gain	Power	Output Swing	Remarks
Resistive Load	≈ 12 (21.54 dB)	217.63 μW	Wide	Low gain, simple design
PMOS Load	≈ 22.38 (27 dB)	326.13 μW	Limited	High gain, restricted swing
Cascode	≈ 35.48 (31 dB)	316.08 μW	Most restricted	Highest gain, lowest swing

References

1. Lookup table based systematic design of analog circuits (gm/Id based design) `https://youtu.be/8sbxbeduIoM`