Analog IC Design

Assignment 1

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2023102030

January 19, 2026

Question 2

Use the given SCL model file and plot I_D vs V_{GS} for a $10\,\mu$m/$1\,\mu$m NMOS transistor and estimate its V_T from the graph for the following cases (Suggested reading: *Operation and Modeling of the MOS Transistor*, second ed., by Tsividis, Sections 10.4 and 4.10):

(a) $V_{DS} = 50$ mV and V_{GS} is swept from 0 to 1.8 V in steps of 0.1 V.

(b) $V_{DS} = 1.8$ V and V_{GS} is swept from 0 to 1.8 V in steps of 0.1 V.

(c) Do you observe any difference in V_T values in cases (a) and (b)? If yes, explain why and indicate which one you will use for hand calculations with simple MOS models.

(d) Estimate the technology parameter μC_{ox} from simulations and simple MOS models.

(e) Plot I_D vs V_{GS} for $V_{DS} = 50$ mV and $V_{DS} = 1.8$ V. Clearly mark the subthreshold region on the graphs. From the plots, and using the simple exponential relationship

$$I_D = I_0 \exp\left(\frac{V_{GS}}{\eta V_{\text{thermal}}}\right),$$

estimate the process parameter η.

Solution:

(a) Linear Region ($V_{DS} = 50$mV):

Since V_{DS} is very small ($V_{DS} << V_{GS} - V_{Th}$), the MOSFET is in the triode region. The current is approximately (neglecting the α parameter that's described in Tsividis) modeled as:

$$I_D = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T)V_{DS}$$

The transconductance $g_m = \frac{\partial I_D}{\partial V_{GS}}$ is maximum at the point of strongest inversion. A tangent line is drawn to the I_D curve at this maximum slope point. The x-axis intercept of this tangent ($V_{GS,int}$) is identified.

$$V_T = V_{GS,int}$$

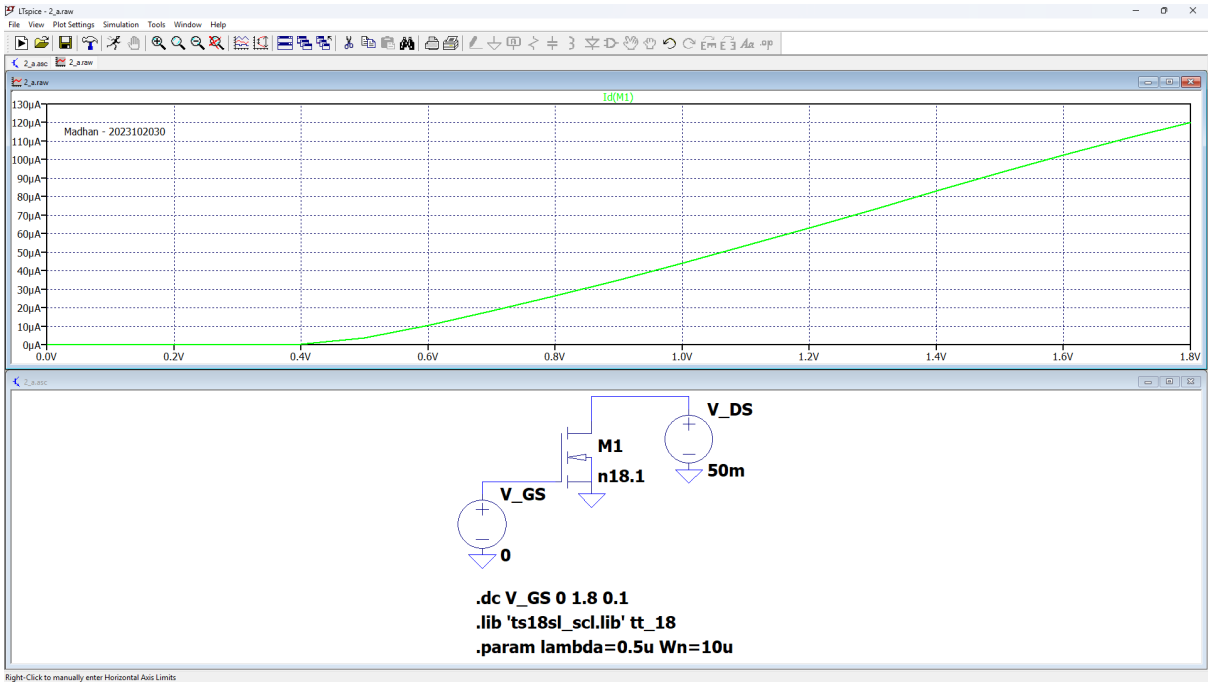

Figure 1: Plot of I_D vs. V_{GS} for $V_{DS} = 50mV$

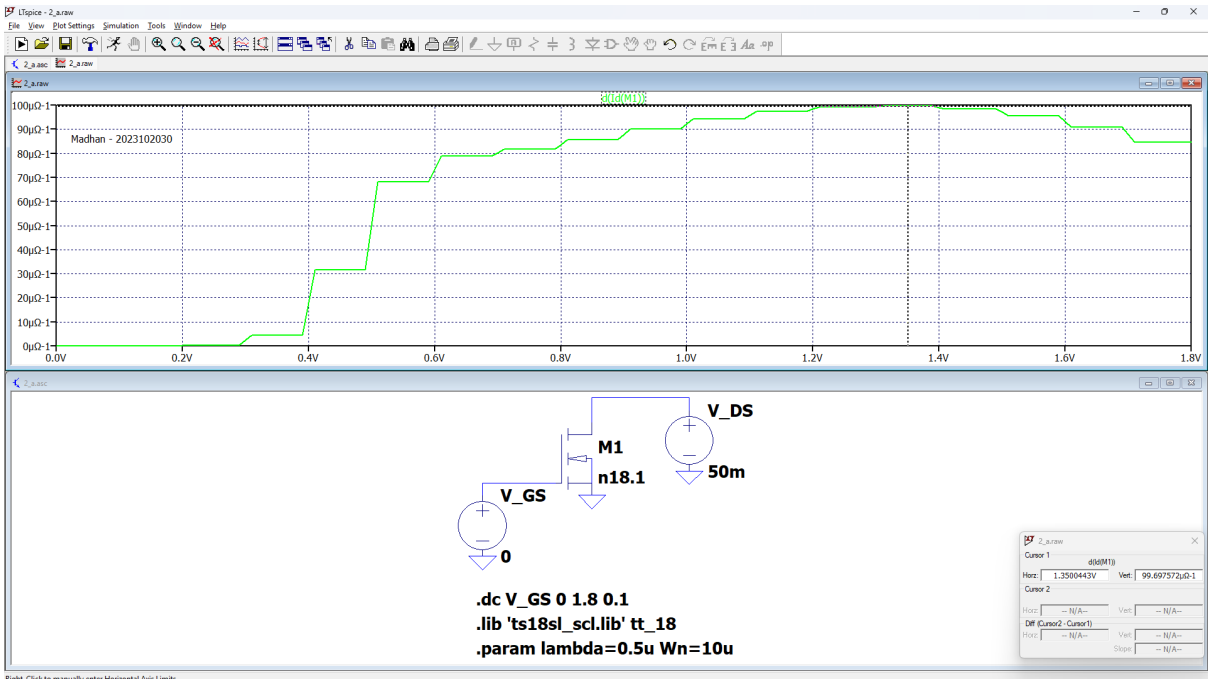

Figure 2: Plot of $\frac{dI_D}{dV_{GS}}$ vs. V_{GS} for $V_{DS} = 50mV$

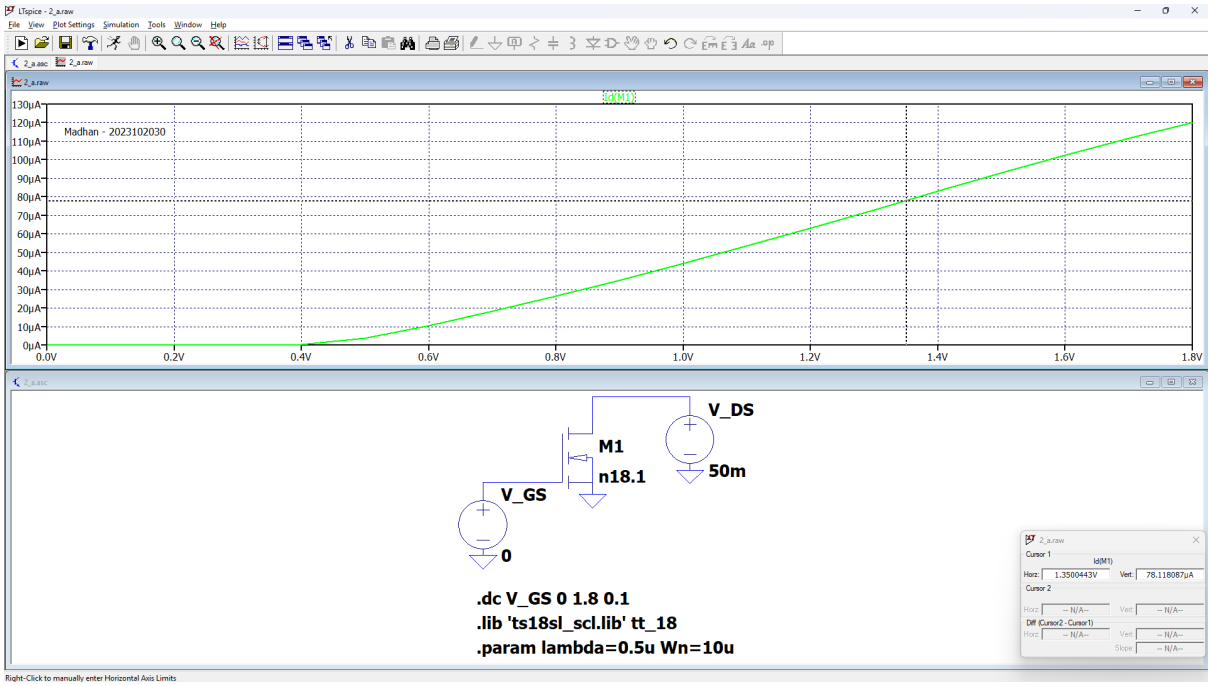

Figure 3: Tangent Line at Maximum Slope Point for $V_{DS} = 50mV$

Slope (m): 99.697572×10^{-6} S
Point (V_{GS0}, I_{D0}): $(1.35\text{ V}, 78.167927\ \mu\text{A})$
The equation of the line is given by:

$$y - y_0 = m(x - x_0)$$

Substituting your values (using μA for current):

$$I_D - 78.167927 = 99.697572(V_{GS} - 1.35)$$

$$V_{GS,int} = V_{Threshold} = \frac{56.423795}{99.697572}$$
$$V_{Threshold,linear} \approx \mathbf{0.56595}\text{ V}$$

(b) Saturation Region ($V_{DS} = 1.8$**V**):

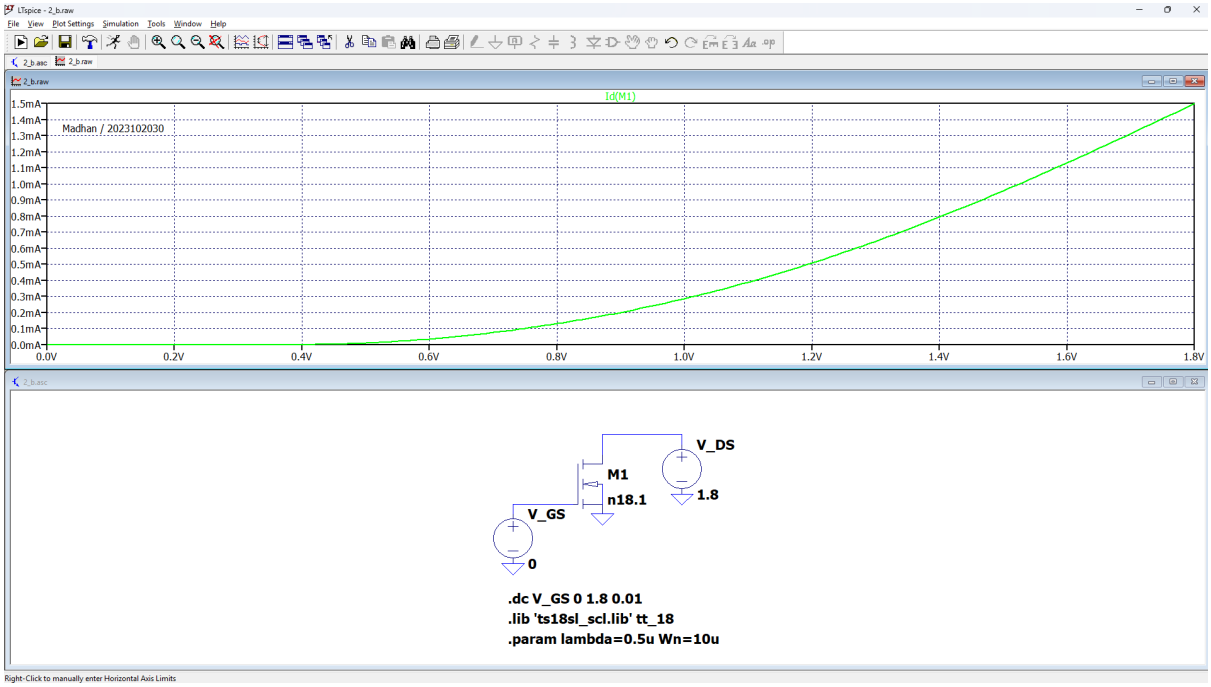

Figure 4: Plot of I_D vs. V_{GS} for $V_{DS} = 1.8V$

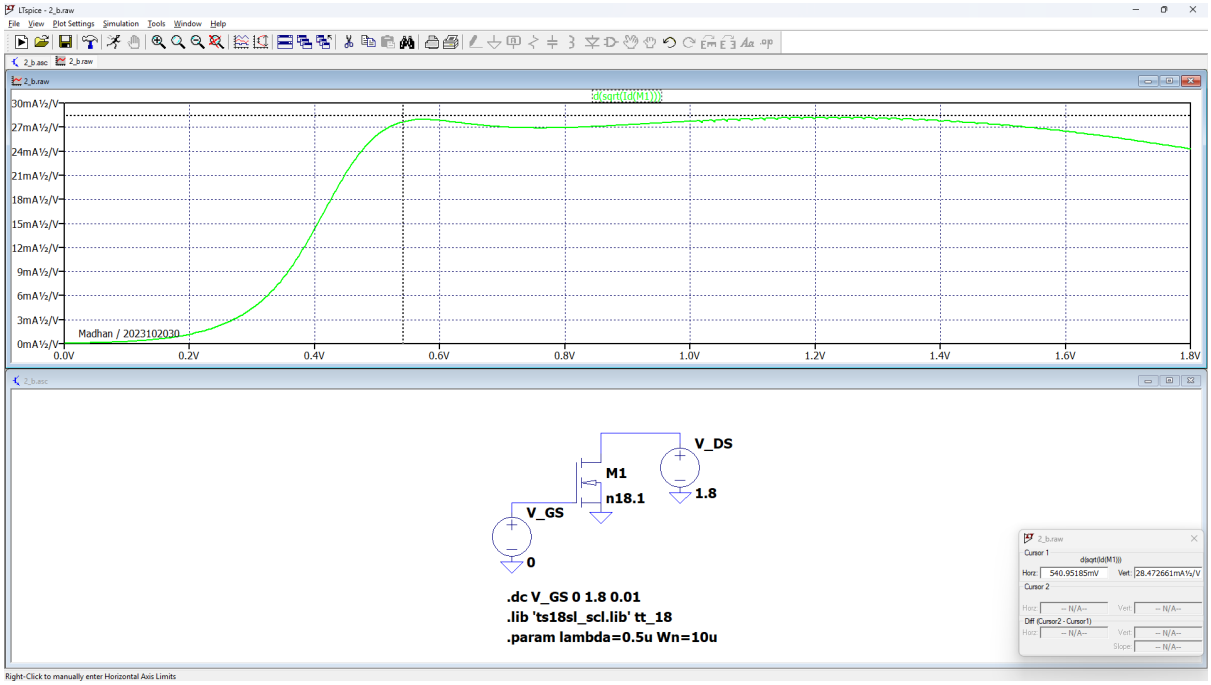

Figure 5: Plot of $\frac{d\sqrt{I_D}}{dV_{GS}}$ for $V_{DS} = 1.8V$

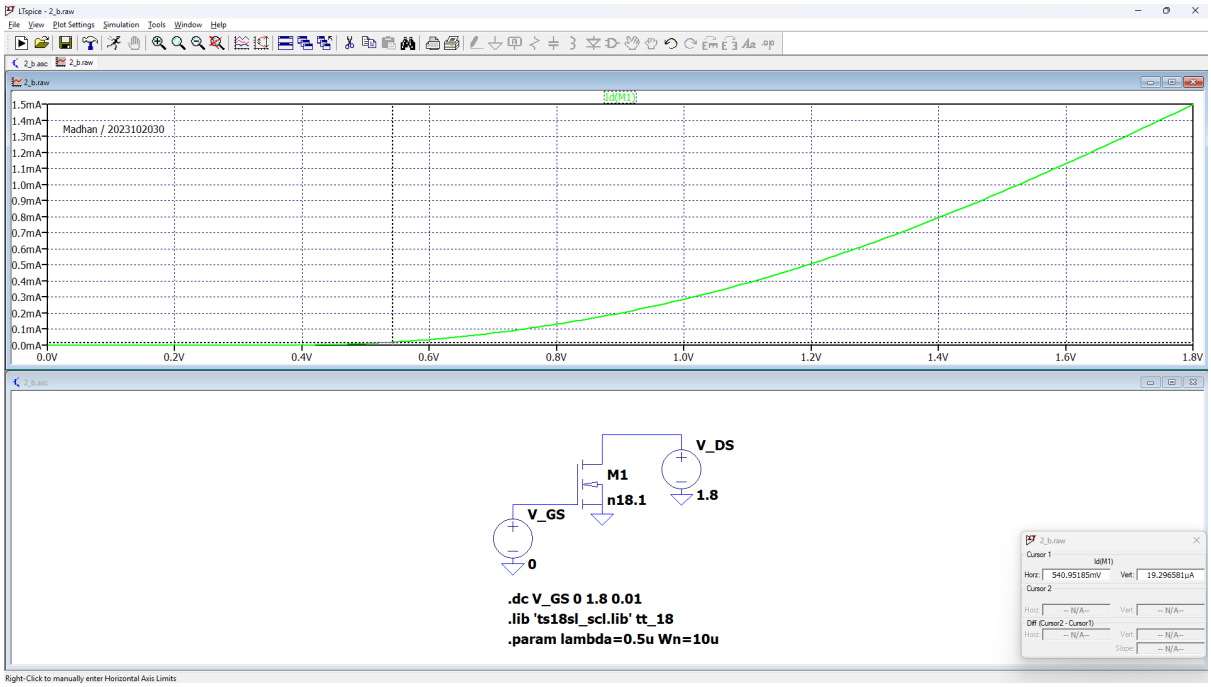

Figure 6: Tangent Line at Maximum Slope Point for $V_{DS} = 1.8V$

The standard square-law model for an NMOS in saturation ($V_{DS} \geq V_{GS} - V_T$) is:

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T)^2$$

To extract V_T through linear extrapolation, we take the square root of both sides of the saturation equation:

$$\sqrt{I_D} = \sqrt{\frac{1}{2}\mu_n C_{ox} \frac{W}{L}} \cdot (V_{GS} - V_T)$$

This matches the equation of a straight line, $y = mx + c$, where:
$y = \sqrt{I_D}$
$x = V_{GS}$
Slope $(m) = \sqrt{\frac{1}{2}\mu_n C_{ox} \frac{W}{L}}$
Constant $(c) = -m \cdot V_T$

Using the slope (m) and a point $(V_{GS0}, \sqrt{I_{D0}})$ from the linear region, we can find the intercept. The linear equation is: $\sqrt{I_D} = m \cdot V_{GS} + c$ The x-intercept occurs when $\sqrt{I_D} = 0$:

$$0 = m \cdot V_{GS,int} + c \implies V_{GS,int} = -\frac{c}{m}$$

Thus, $V_{T,sat} = V_{GS,int}$.

Slope (m): $28.472661\sqrt{\mu\text{A}}/\text{V}$
Point $(V_{GS0}, \sqrt{I_{D0}})$: $(0.54095185\ \text{V}, \sqrt{19.296581}\sqrt{\mu\text{A}})$
$\sqrt{I_{D0}} \approx 4.392787\sqrt{\mu\text{A}}$

Substituting these values into the point-slope form $y - y_0 = m(x - x_0)$ where $y = \sqrt{I_D}$ (in μA):

$$\sqrt{I_D} - 4.392787 = 28.472661(V_{GS} - 0.540952)$$

Expanding to find the intercept form:

$$\sqrt{I_D} = 28.472661 \cdot V_{GS} - (28.472661 \times 0.540952) + 4.392787$$

$$\sqrt{I_D} = 28.472661 \cdot V_{GS} - 15.402338 + 4.392787$$

$$\sqrt{I_D} = 28.472661 \cdot V_{GS} - 11.009551$$

$$V_{GS,int} = V_{Threshold,Saturation} \approx \mathbf{0.38667}\ \text{V}$$

(c) Comparison of V_T Values

Case (a) Linear Region ($V_{DS} = 50\text{mV}$): $V_{T,lin} \approx 0.541\text{V}$
Case (b) Saturation Region ($V_{DS} = 1.8\text{V}$): $V_{T,sat} \approx 0.387\text{V}$

The threshold voltage decreased by approximately 154mV as the drain-source voltage increased from 50mV to 1.8V.

This reduction is primarily due to Drain-Induced Barrier Lowering (DIBL). As V_{DS} increases, the high drain potential lowers the potential barrier at the source end of the channel found in these sub-micron devices. Consequently, a lower gate voltage is required to invert the channel, resulting in a lower effective threshold voltage in saturation.

For hand calculations using simple MOS models, I will use the threshold voltage extracted from Case (a) ($V_{DS} = 50\text{mV}$), i.e., $V_T \approx 0.541\text{V}$. The simple square-law models assume V_T is a constant parameter and do not account for DIBL. Therefore, the value extracted at low V_{DS} represents the intrinsic threshold voltage of the process and is the appropriate choice for basic hand calculations.

(d) Estimation of Technology Parameter $\mu_n C_{ox}$

To estimate the technology parameter $\mu_n C_{ox}$ (also known as the process transconductance parameter k'_n), we use the slopes extracted from the simulation data and relate them to the simple MOS models for both the linear and saturation regions.

1. Estimation from the Linear Region ($V_{DS} = 50\textbf{mV}$)

In the linear region, the simple MOS model for drain current is:

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

The transconductance (g_m), which is the slope of the I_D vs. V_{GS} curve, is:

$$g_{m,lin} = \frac{\partial I_D}{\partial V_{GS}} = \mu_n C_{ox} \frac{W}{L} V_{DS}$$

Using the simulated values: Slope ($g_{m,lin}$): 99.697572×10^{-6} A/V
Drain-Source Voltage (V_{DS}): 0.05 V
Aspect Ratio (W/L): $10\mu\text{m}/1\mu\text{m} = 10$

$$\mu_n C_{ox} = \frac{g_{m,lin}}{(W/L) \cdot V_{DS}} = \frac{99.697572 \times 10^{-6}}{10 \times 0.05}$$

$$\mu_n C_{ox} \approx \mathbf{199.40}\ \mu\text{A/V}^\mathbf{2}$$

2. Estimation from the Saturation Region ($V_{DS} = 1.8\mathbf{V}$)

In the saturation region, the square-law relationship is:

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_T)^2$$

Linearizing this by taking the square root gives:

$$\sqrt{I_D} = \sqrt{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}} \cdot (V_{GS} - V_T)$$

The slope of the $\sqrt{I_D}$ vs. V_{GS} curve is:

$$m_{sat} = \sqrt{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}}$$

Using the simulated values: Slope (m_{sat}): 28.472661 $\text{mA}^{1/2}/\text{V} = 0.028472661\ \text{A}^{1/2}/\text{V}$ Aspect Ratio (W/L): 10

$$\mu_n C_{ox} = \frac{2 \cdot m_{sat}^2}{W/L} = \frac{2 \cdot (0.028472661)^2}{10}$$

$$\mu_n C_{ox} \approx \frac{2 \cdot 0.00081069}{10} \approx 0.00016213$$

$$\mu_n C_{ox} \approx \mathbf{162.13}\ \mu\text{A/V}^\mathbf{2}$$

3. Explanation

The $\mu_n C_{ox}$ calculated from the linear region (199.4 $\mu\text{A/V}^2$) is significantly higher than that from the saturation region (162.1 $\mu\text{A/V}^2$).

Mobility Degradation: In saturation, the vertical electric field (from the gate) and the lateral electric field (from the drain) are much higher. This causes carriers to collide more frequently with the oxide interface, reducing the effective mobility (μ_{eff}) compared to the low-field linear case.

Velocity Saturation: At $V_{DS} = 1.8\text{V}$, the carriers reach their scattering-limited velocity, which prevents the current from increasing quadratically as the simple model predicts, leading to a lower "apparent" $\mu_n C_{ox}$ in saturation.

(e) Estimation of subthreshold process parameter η

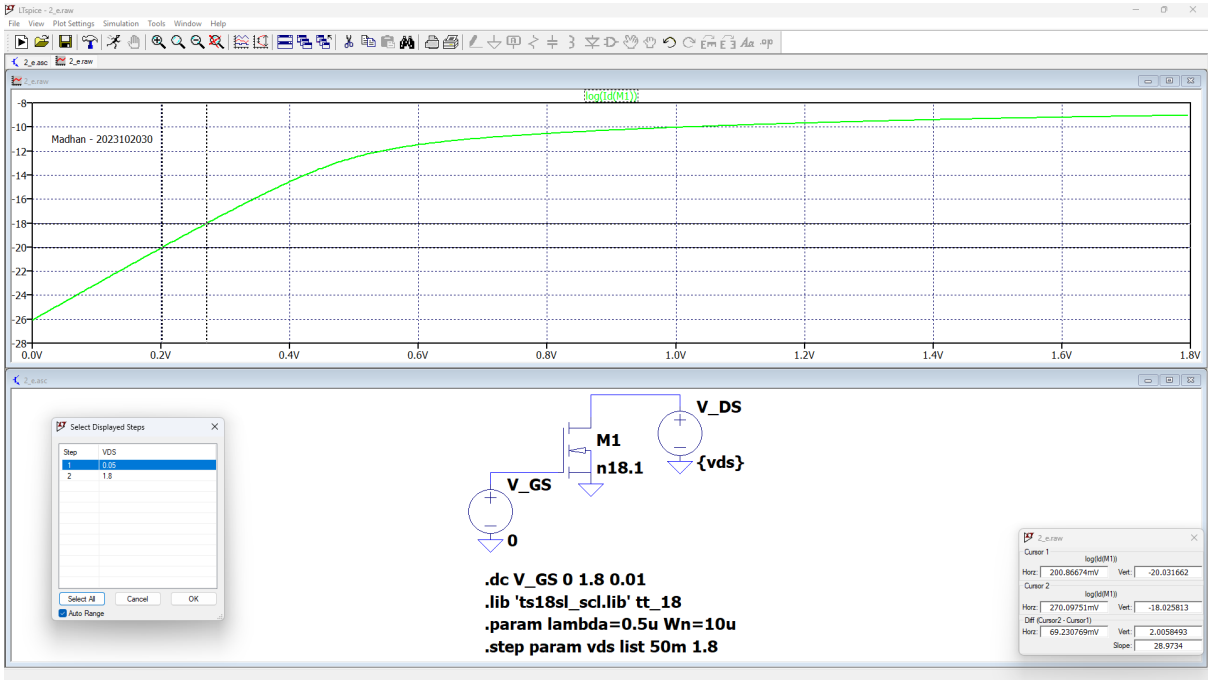

Figure 7: Plot of $\ln(I_D)$ vs. V_{GS} for $V_{DS} = 50mV$

Point 1: $(V_{GS1}, \ln(I_{D1})) = (200.867 \text{ mV}, -20.032)$
Point 2: $(V_{GS2}, \ln(I_{D2})) = (270.098 \text{ mV}, -18.026)$

The subthreshold current is given by:

$$I_D = I_0 \exp\left(\frac{V_{GS}}{\eta V_{thermal}}\right)$$

Taking the natural log:

$$\ln(I_D) = \ln(I_0) + \frac{1}{\eta V_{thermal}} \cdot V_{GS}$$

This takes the form of a line $y = mx + c$, where the slope m is:

$$m = \frac{\Delta \ln(I_D)}{\Delta V_{GS}} = \frac{1}{\eta V_{thermal}}$$

Rearranging for η:

$$\eta = \frac{1}{m \cdot V_{thermal}}$$

$$\Delta V_{GS} = 270.09751 \text{ mV} - 200.86674 \text{ mV} = 69.23077 \text{ mV} = 0.06923 \text{ V}$$

$$\Delta \ln(I_D) = -18.025813 - (-20.031662) = 2.005849$$

Slope (m):

$$m = \frac{2.005849}{0.06923} \approx 28.973 \text{ V}^{-1}$$

Using the standard thermal voltage at 27°C ($V_{thermal} \approx 25.86$ mV):

$$\eta = \frac{1}{28.973 \times 0.02586}$$

$$\eta \approx \mathbf{1.335}$$

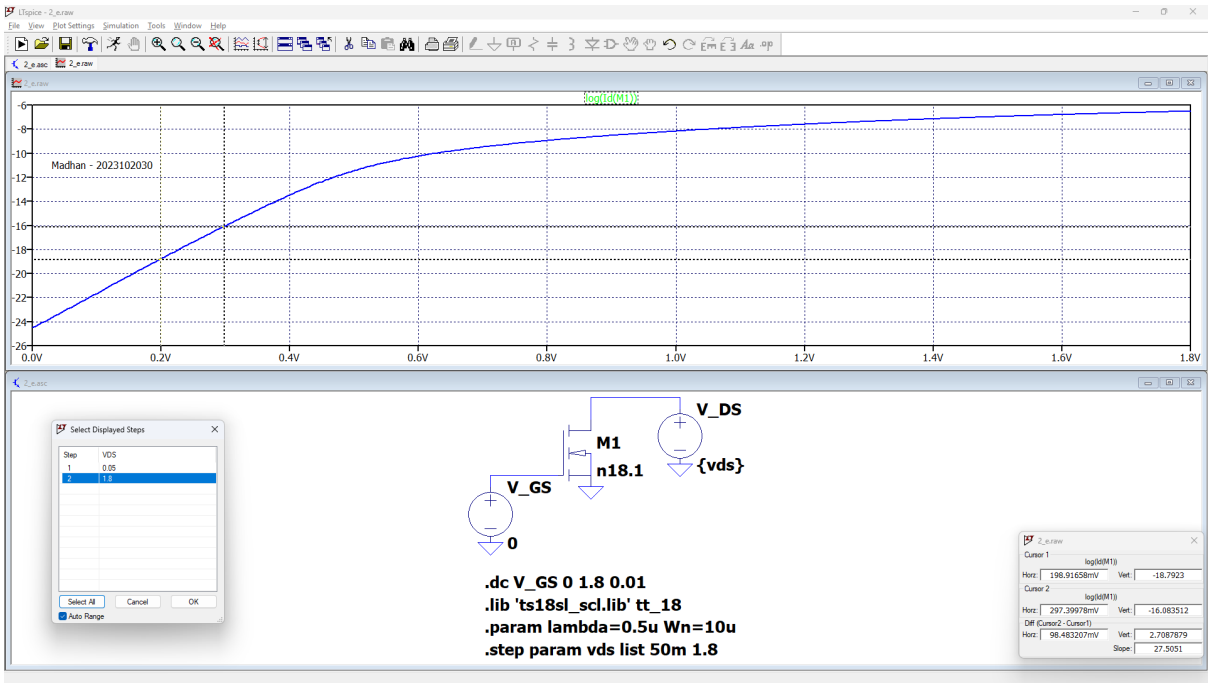

Figure 8: Plot of $\ln(I_D)$ vs. V_{GS} for $V_{DS} = 1.8V$

Point 1: $(V_{GS1}, \ln(I_{D1})) = (198.91658 \text{ mV}, -18.7923)$
Point 2: $(V_{GS2}, \ln(I_{D2})) = (297.39978 \text{ mV}, -16.083512)$

$$\Delta V_{GS} = 297.39978 \text{ mV} - 198.91658 \text{ mV} = 98.4832 \text{ mV} = 0.0984832 \text{ V}$$

$$\Delta \ln(I_D) = -16.083512 - (-18.7923) = 2.708788$$

Slope (m):

$$m = \frac{2.708788}{0.0984832} \approx 27.505 \text{ V}^{-1}$$

Using a standard thermal voltage at 27°C ($V_{thermal} \approx 25.86$ mV):

$$\eta = \frac{1}{27.505 \times 0.02586}$$

$$\eta \approx \mathbf{1.406}$$

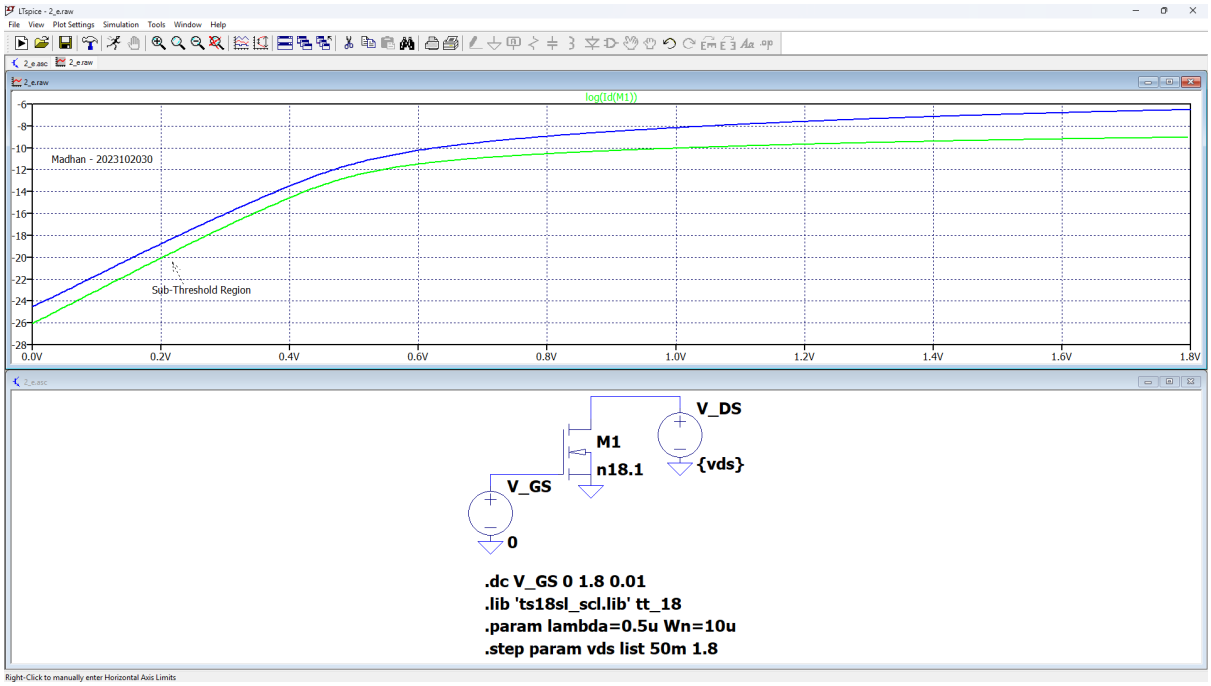

Figure 9: Subthreshold Region Marked on I_D vs. V_{GS} Plots

Question 3

Finding unity current gain frequency f_T of the technology node.

(a) Using minimum size NMOS, find the f_T (unity current gain frequency, where $|i_d/i_g| = 1$) for the 180 nm TSMC, 180 nm SCL, and 130 nm IBM technologies. You are expected to show the method, plots, and your explanation.

(b) Suggest a method to compare the intrinsic gains ($g_m r_o$) of minimum size transistors for the three model files given to you. Show the schematic, netlist, simulation results, and necessary discussions.

Hint: Useful commands: `lib 'tsl85_scl.lib' tt_18`, `include TSMC_180nm.txt`, `include IBM130nm.txt`, `use nmos4 and edmin model name as n18`, `CMOSN130, CMOSN180, ADSP/P` and substitute in MOS parameters.

Solution:

(a) Unity Current Gain Frequency (f_T) Comparison

Theoretically, $f_T \approx \frac{g_m}{2\pi(C_{gs}+C_{gd})}$. As technology scales from 180nm to 130nm, capacitances decrease significantly, and f_T increases. The simulation data even shows that 130nm node shas a much higher f_T than the 180nm nodes.

Table 1: Comparison of Unity Current Gain Frequency (f_T) for Minimum Size NMOS across Technology Nodes ($V_{GS} = 1.2\text{V}$, $V_{DS} = 1.8\text{V}$)

Technology Node	**Feature Size (L_{min})**	**Extracted f_T (GHz)**
SCL 180nm (Real PDK)	180 nm	64.90
TSMC 180nm (Spice model)	180 nm	43.26
IBM 130nm (Spice model)	130 nm	51.54

Note:
All reported frequencies were extracted at a gate-source voltage (V_{GS}) of 1.2 V to ensure the devices are biased in the strong inversion saturation region.

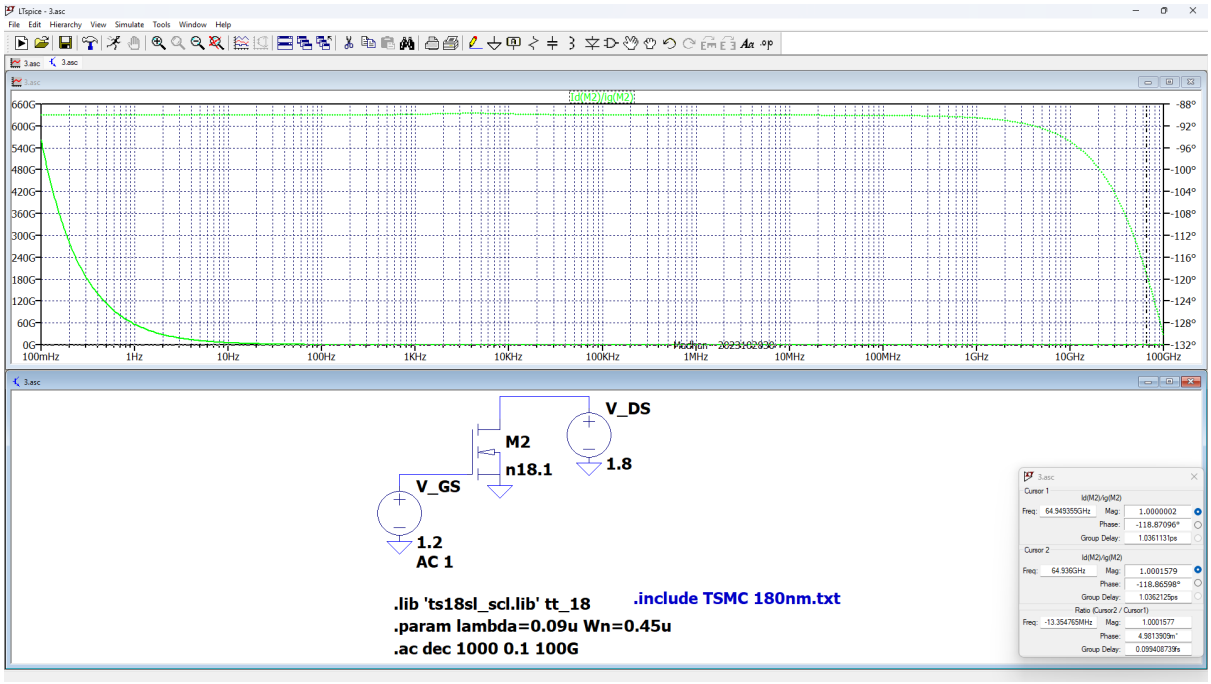

Figure 10: Plot of Gain vs. V_{GS} for SCL180nm technology node

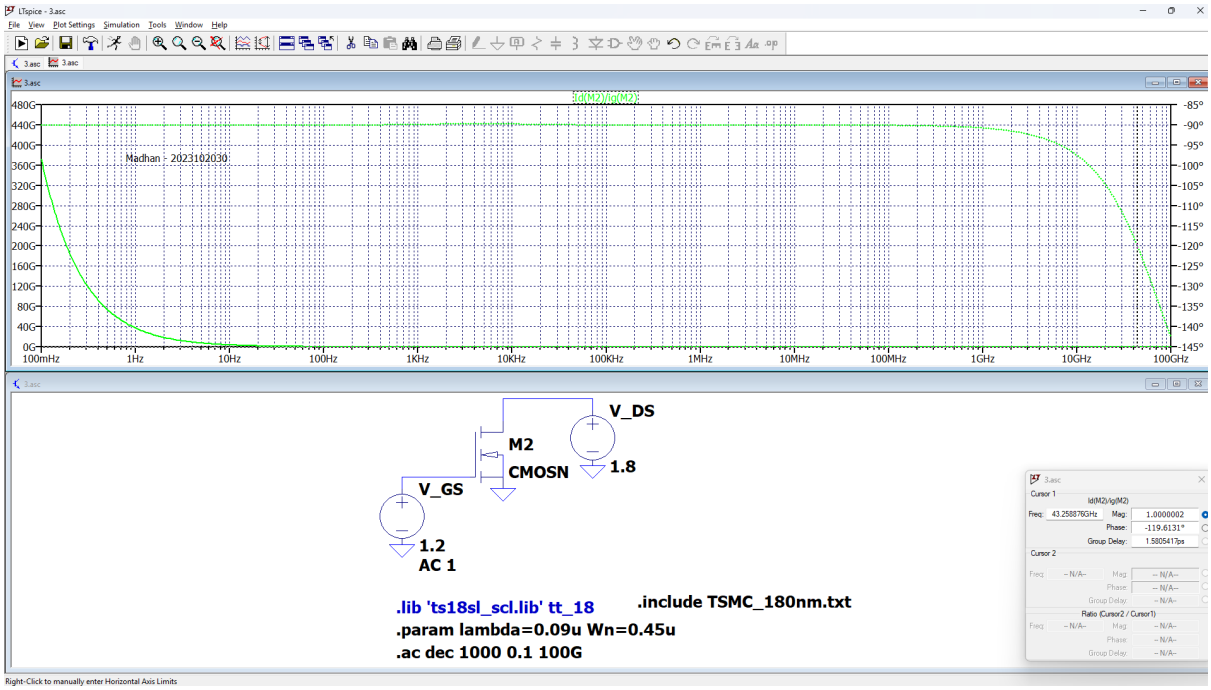

Figure 11: Plot of Gain vs. Frequency for TSMC180nm technology node

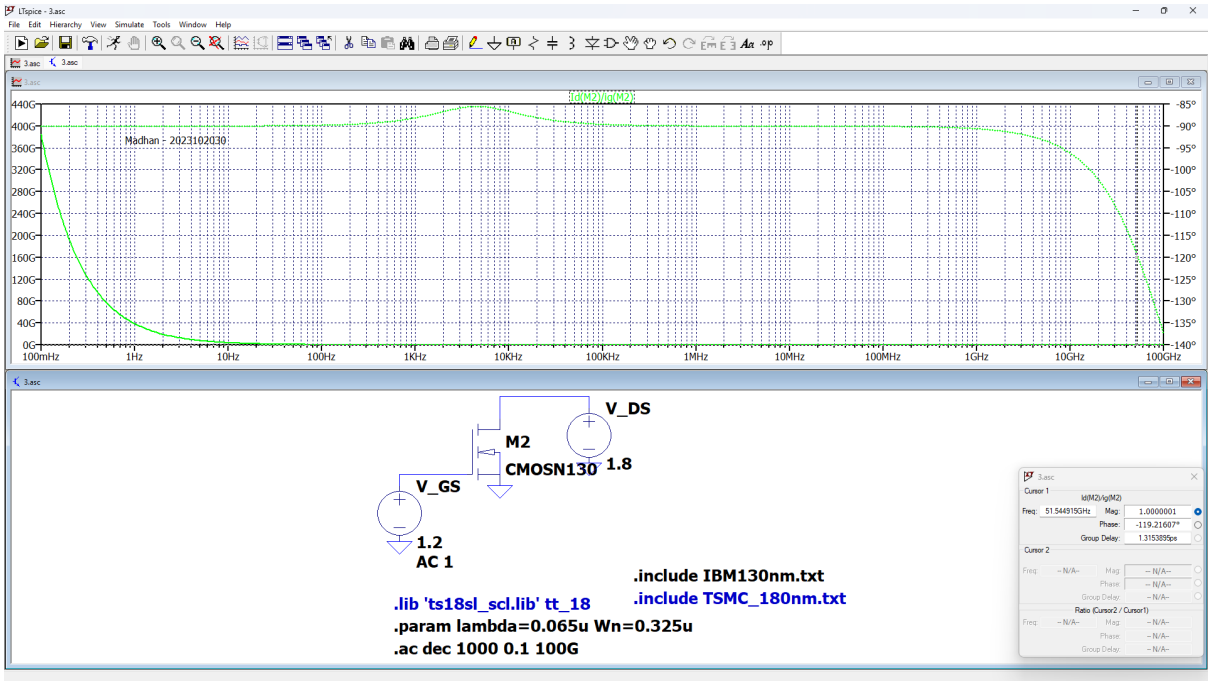

Figure 12: Plot of Gain vs. Frequency for IBM130nm technology node

SCL 180nm vs. TSMC 180nm

Even though both technologies share the same 180 nm feature size, the SCL 180 nm (64.9 GHz) significantly outperforms the TSMC 180 nm (43.26 GHz). This discrepancy is likely due to differences in the process parameters provided in their respective library files. SCL is a real PDK file whereas TSMC is a spice model file.

Scaling Trend (180nm vs. 130nm)

Theoretically, the transition frequency f_T is given by:

$$f_T \approx \frac{g_m}{2\pi C_{gs}} \approx \frac{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T)}{2\pi \cdot \frac{2}{3} W L C_{ox}} \propto \frac{\mu_n (V_{GS} - V_T)}{L^2}$$

As the channel length L scales down from 180nm to 130nm, f_T is expected to increase significantly due to the $1/L^2$ dependence. The carriers cross the channel faster, resulting in higher operating speeds. The general trend in semiconductor scaling dictates that smaller nodes (like 130nm) inherently offer higher intrinsic speed capabilities (f_T) compared to larger nodes (like 180nm), provided the device is not limited by velocity saturation or excessive parasitic capacitances.

(b) Intrinsic Gain ($g_m r_o$) Comparison Methodology

To compare the intrinsic gains ($g_m r_o$), I employed a simulation method using an ideal current source load.

Methodology: I biased the NMOS transistor in the saturation region using an ideal DC current source connected to the drain. The value of this current (I_{DS}) was chosen based on the I_D vs. V_{DS} characteristics to ensure saturation.

Since an ideal current source has infinite small-signal impedance ($r_{oc} \to \infty$), the effective load seen at the drain is solely the output resistance of the transistor (r_o).

Mathematical Justification: The small-signal voltage gain of a common-source amplifier is:

$$|A_v| = g_m(r_o || r_{oc})$$

With $r_{oc} \to \infty$, the equation simplifies to:

$$|A_v| = g_m r_o$$

Thus, the AC gain magnitude obtained from the simulation corresponds directly to the intrinsic gain of the transistor.

To normalize the comparison, each transistor was biased in the saturation region with $V_{DS} = 1.2$V and $V_{GS} = 1.2$V. The gains were extracted at a frequency of 1 GHz to capture the intrinsic performance.

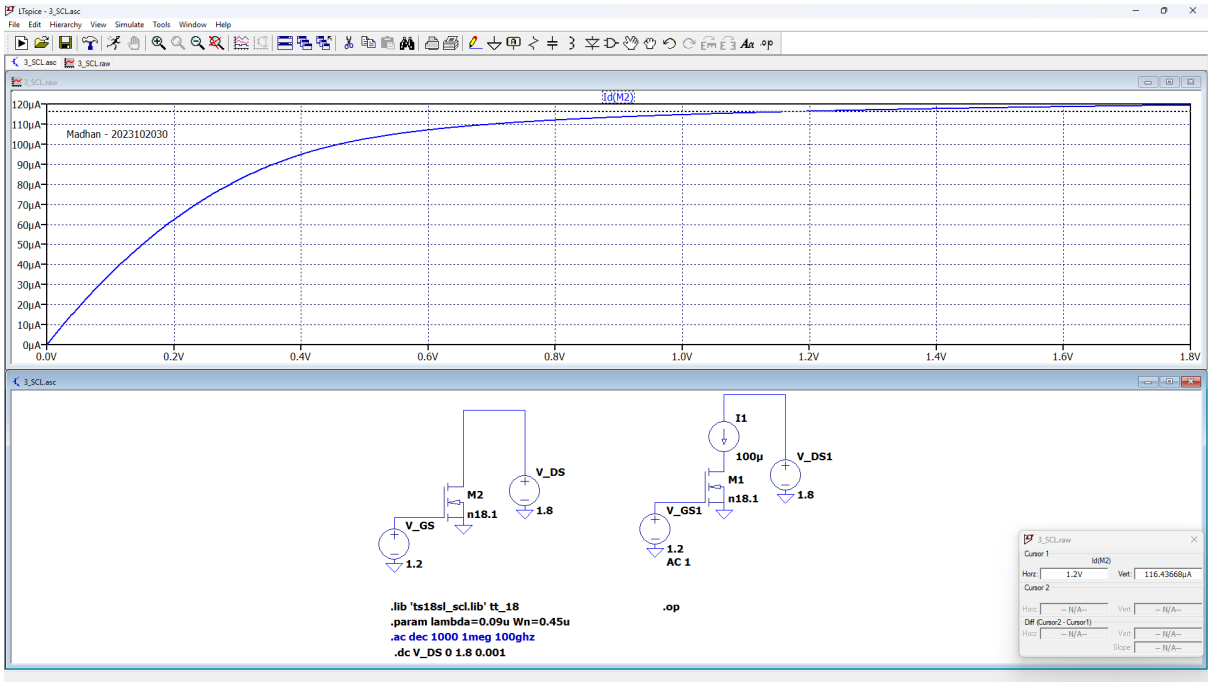

Figure 13: I_D vs. V_{DS} for SCL180nm technology node at $V_{DS} = 1.2V \& V_{GS} = 1.2V$

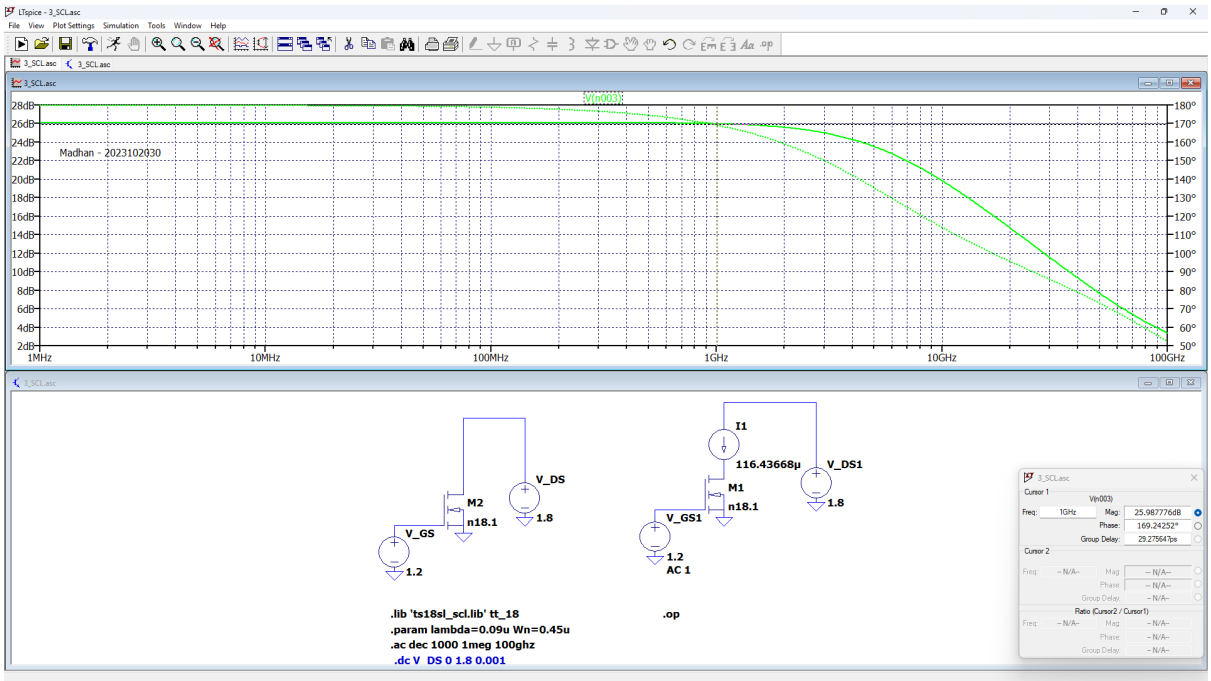

Figure 14: Intrinsic Gain ($g_m r_o$) for SCL180nm technology node at Midband Frequency 1GHz

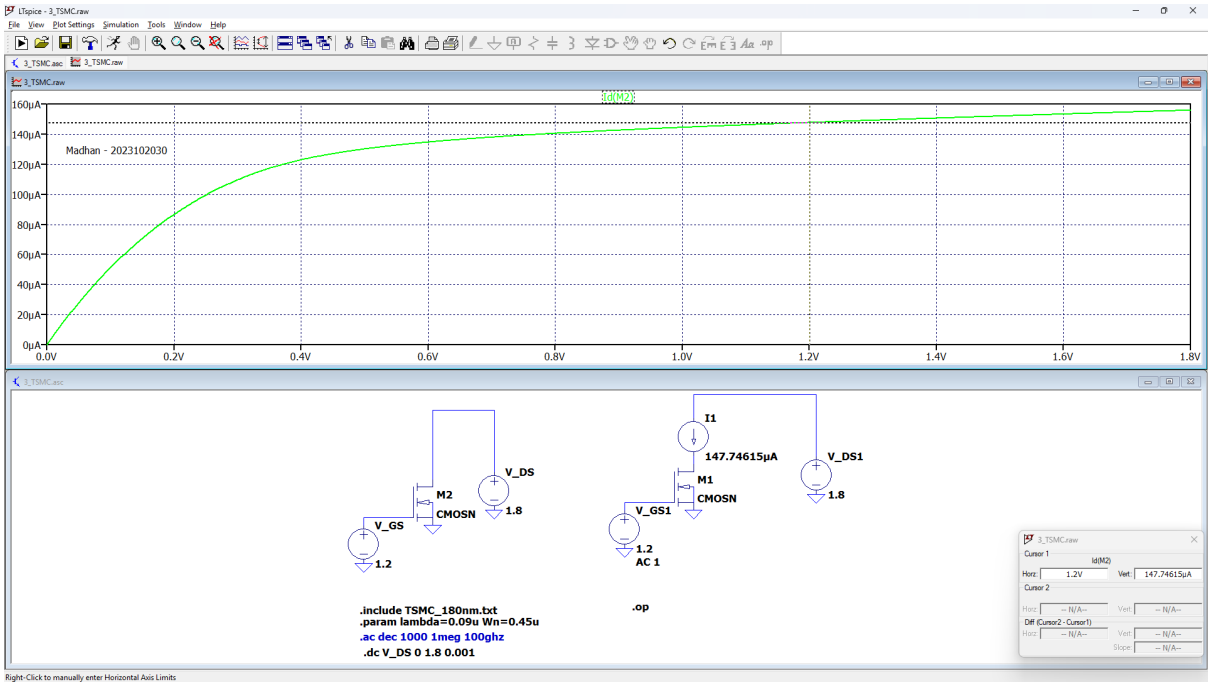

Figure 15: I_D vs. V_{DS} for TSMC180nm technology node at $V_{DS} = 1.2V \& V_{GS} = 1.2V$

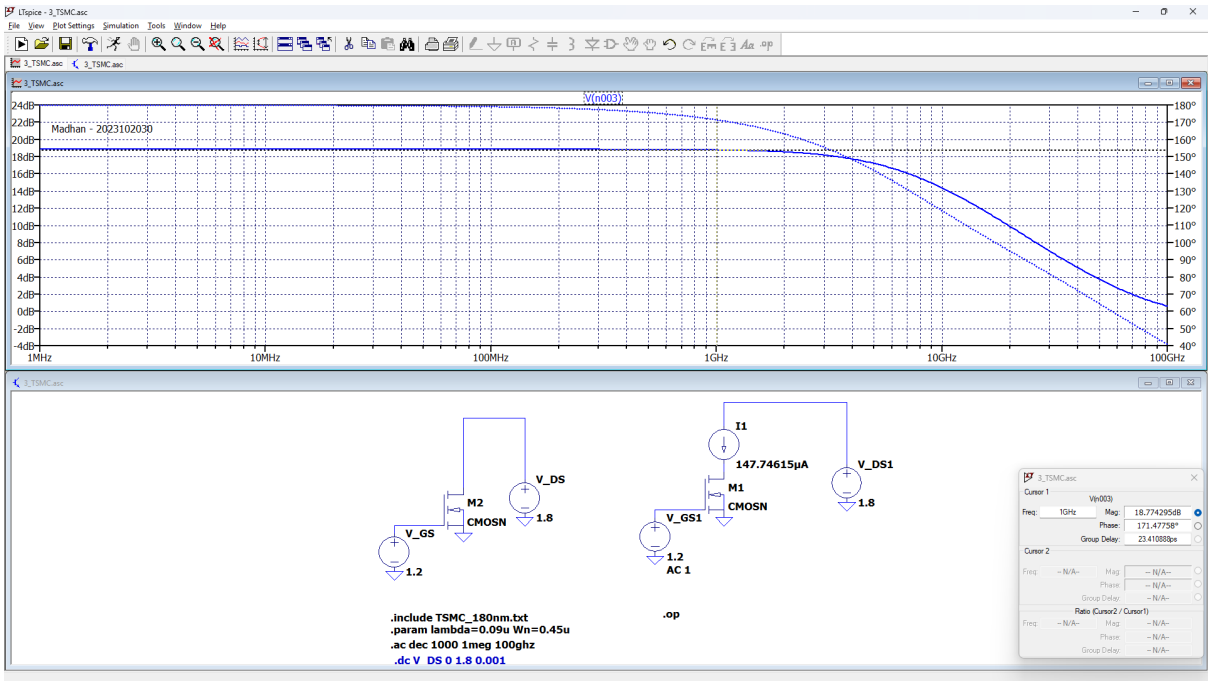

Figure 16: Intrinsic Gain ($g_m r_o$) for TSMC180nm technology node at Midband Frequency 1GHz

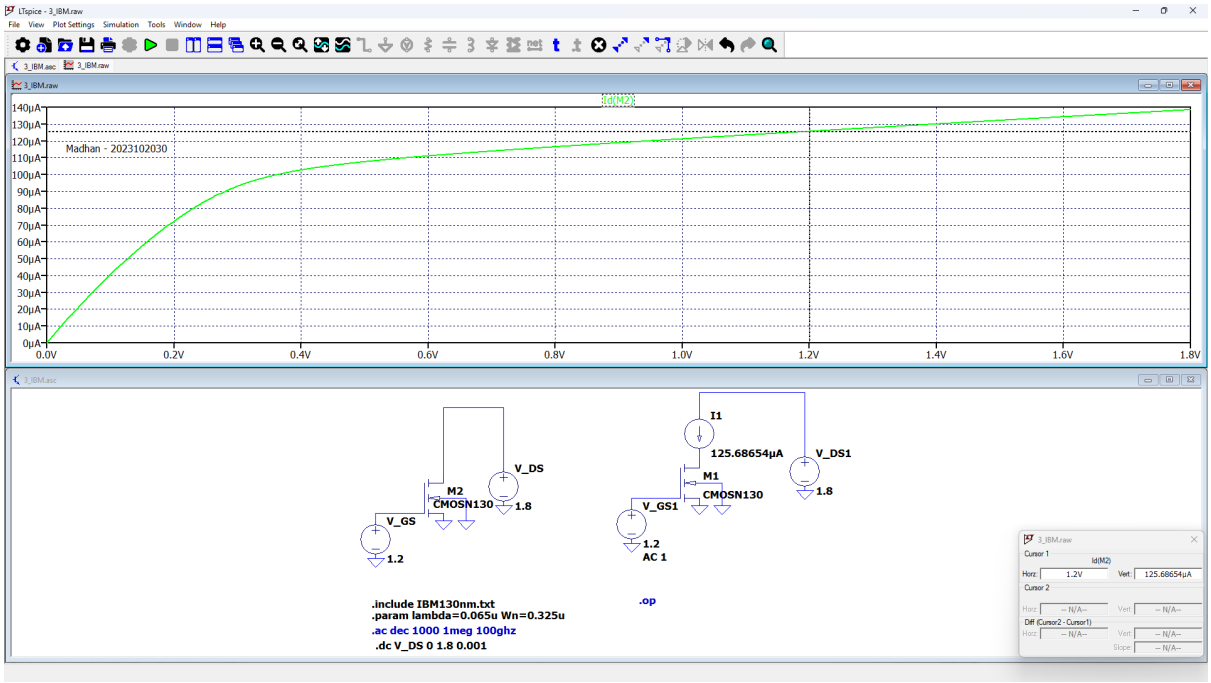

Figure 17: I_D vs. V_{DS} for IBM130nm technology node at $V_{DS} = 1.2V \& V_{GS} = 1.2V$

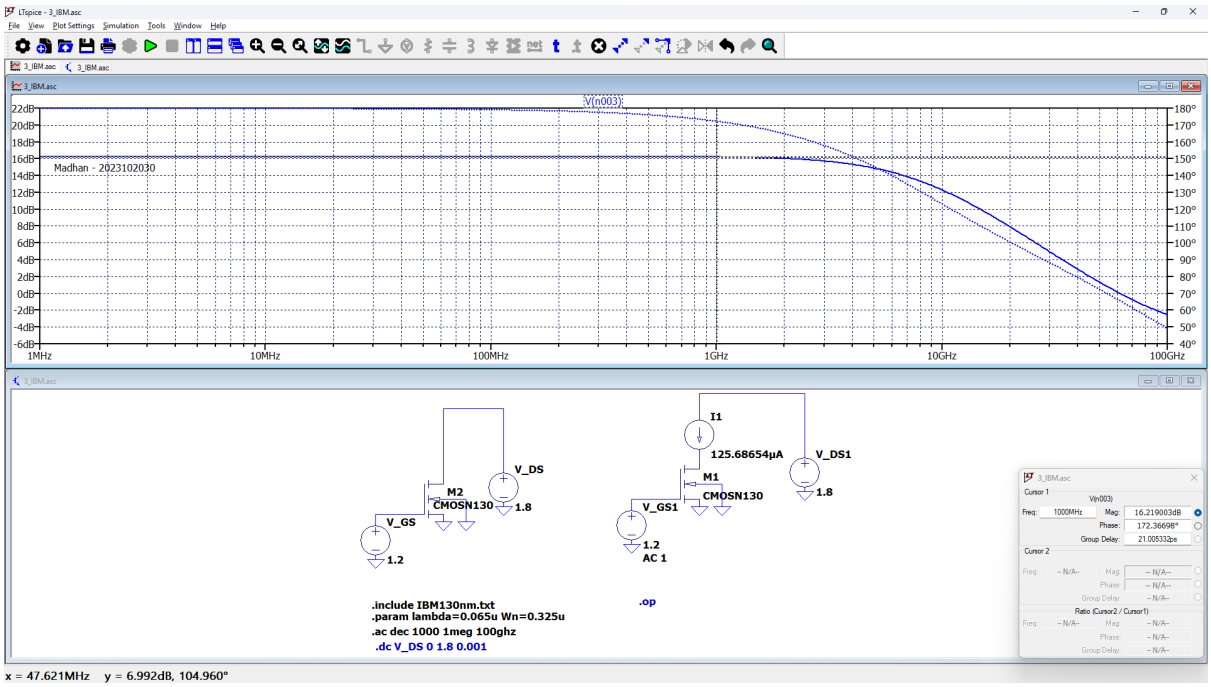

Figure 18: Intrinsic Gain ($g_m r_o$) for IBM130nm technology node at Midband Frequency 1GHz

Table 2: Intrinsic Gain Comparison Across Technology Nodes

Technology Node	$L_{\min}$	W **used**	**Bias Current** (I_D)	**Intrinsic Gain (dB)**	**Intrinsic Gain (V/V)**
SCL 180 nm	180 nm	0.45 μm	116.44 μA	25.99	$\approx$ 19.93
TSMC 180 nm	180 nm	0.45 μm	147.75 μA	18.77	$\approx$ 8.68
IBM 130 nm	130 nm	0.325 μm	125.69 μA	16.22	$\approx$ 6.47

Clearly, we can see that as the technology node decreases the intrinsic gain also decreases. This is primarily due to the increased short-channel effects and reduced output resistance (r_o) in smaller geometries, which negatively impact the intrinsic gain despite improvements in transconductance (g_m). Due to the reduction in parasitic capacitances, the transition frequency (f_T) improves with scaling, but the intrinsic gain ($g_m r_o$) tends to decrease.

We have proved the above statement with the simulation results shown above.

Question 4

Using TSMC model file, draw a circuit for an analog amplifier using complementary NMOS ($5\,\mu$m/$1\,\mu$m) and PMOS ($10\,\mu$m/$1\,\mu$m) configuration discussed in class. Use only one DC source $V_{DD} = 1.8$ V and generate other voltages using resistive dividers.
From simulations, find the DC bias point and maximum input amplitude ($A_{\max}$) for maximum gain and THD $< 10\%$. Report the bias point and the maximum gain. How will you cascade two such amplifiers? Show the schematic with the exact schematic and simulation results (gain and THD) for the cascaded amplifier at $A_{\max}$.

Solution:

The amplifier was designed using a complementary NMOS (5μm/1μm) and PMOS (10μm/1μm) configuration under a 1.8V supply. To determine the optimal bias point, a DC sweep of V_{GS} was performed, and the derivative of the transfer characteristic (dV_{out}/dV_{in}) was analyzed to identify the region of maximum slope. The peak gain was found at an input bias of approximately 811.65mV. This was implemented using a resistive divider with $R_3 = 16.2\text{k}\Omega$ and $R_4 = 13.3\text{k}\Omega$

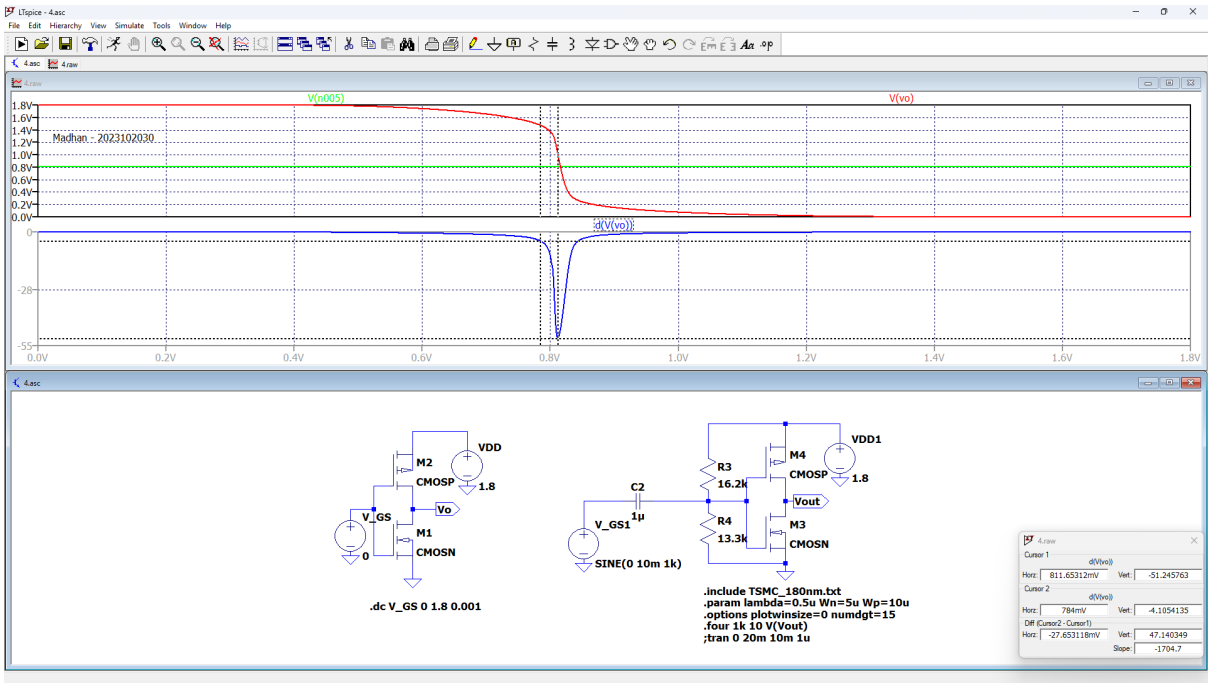

Figure 19: Biasing Circuit for Single Stage CMOS Amplifier in TSMC 180nm Technology Node

The single-stage configuration achieved a maximum small-signal gain of 20.54dB (≈ 10.64V/V) at 1kHz.

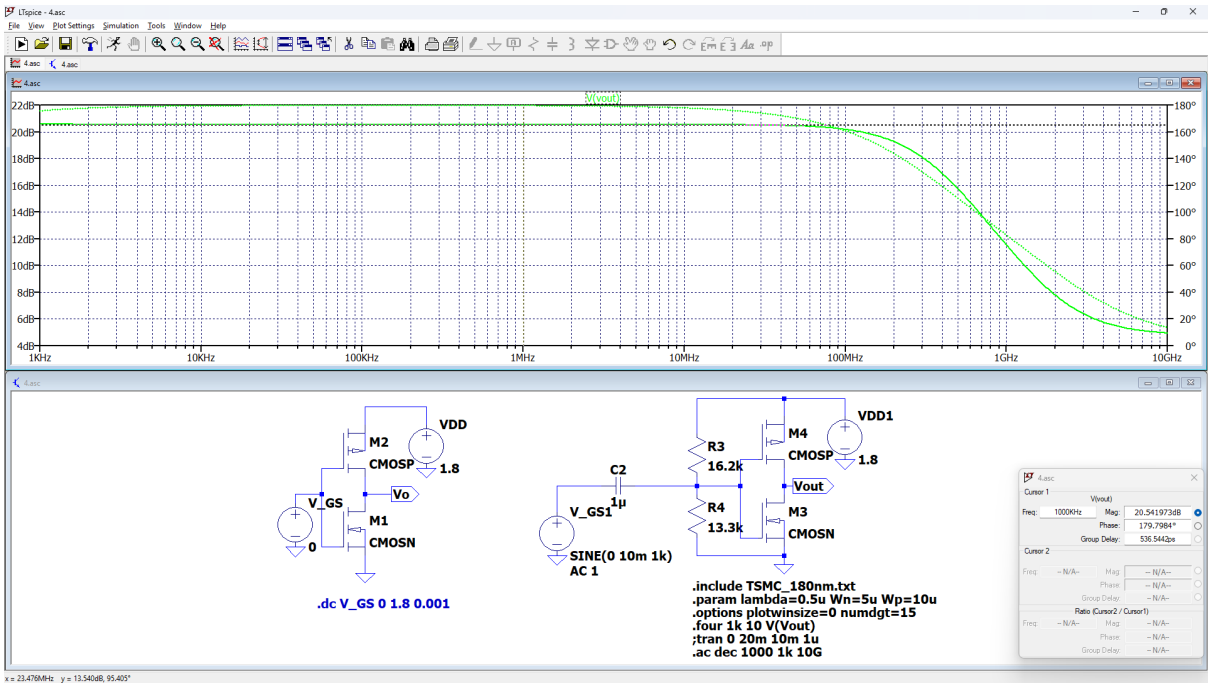

Figure 20: AC Small Signal Gain for Single Stage CMOS Amplifier in TSMC 180nm Technology Node

Transient analysis showed that for a 10mV input sine wave, the Total Harmonic Distortion (THD) remained low at 0.37%. The maximum input amplitude (A_{max}) for a single stage was identified as 90mV, yielding a THD of 9.97%, effectively meeting the $< 10\%$ requirement.

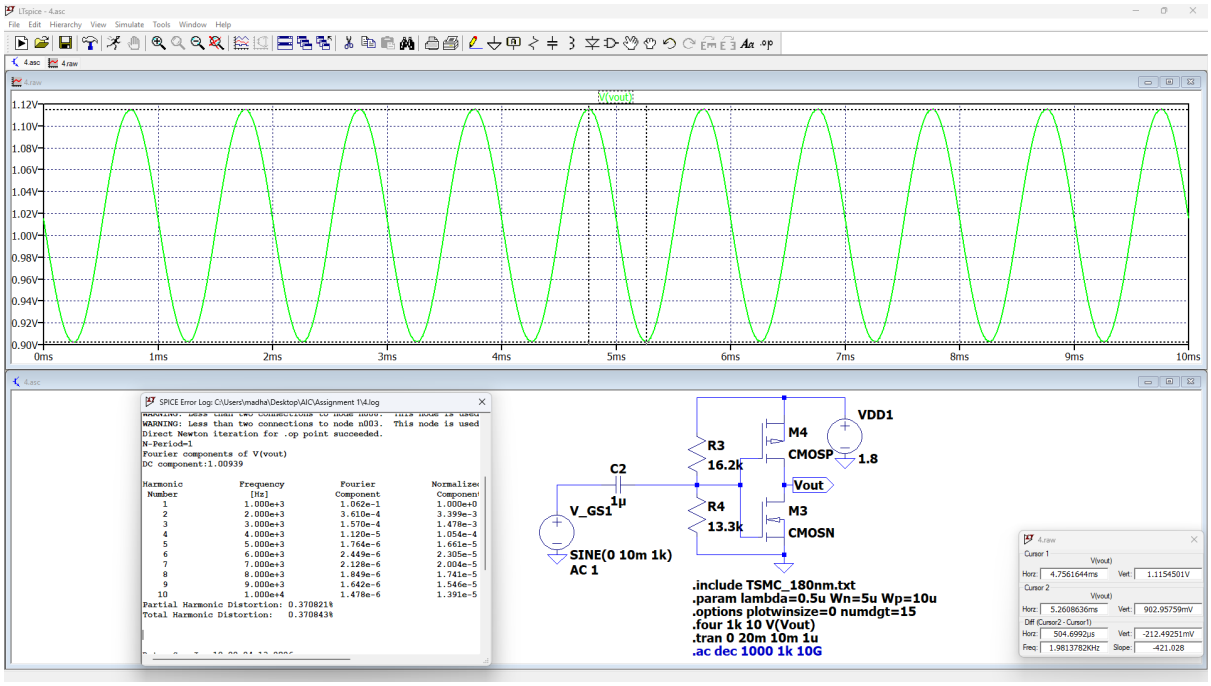

Figure 21: Maximum Input Amplitude for Maximum Gain Point for Single Stage CMOS Amplifier in TSMC 180nm Technology Node

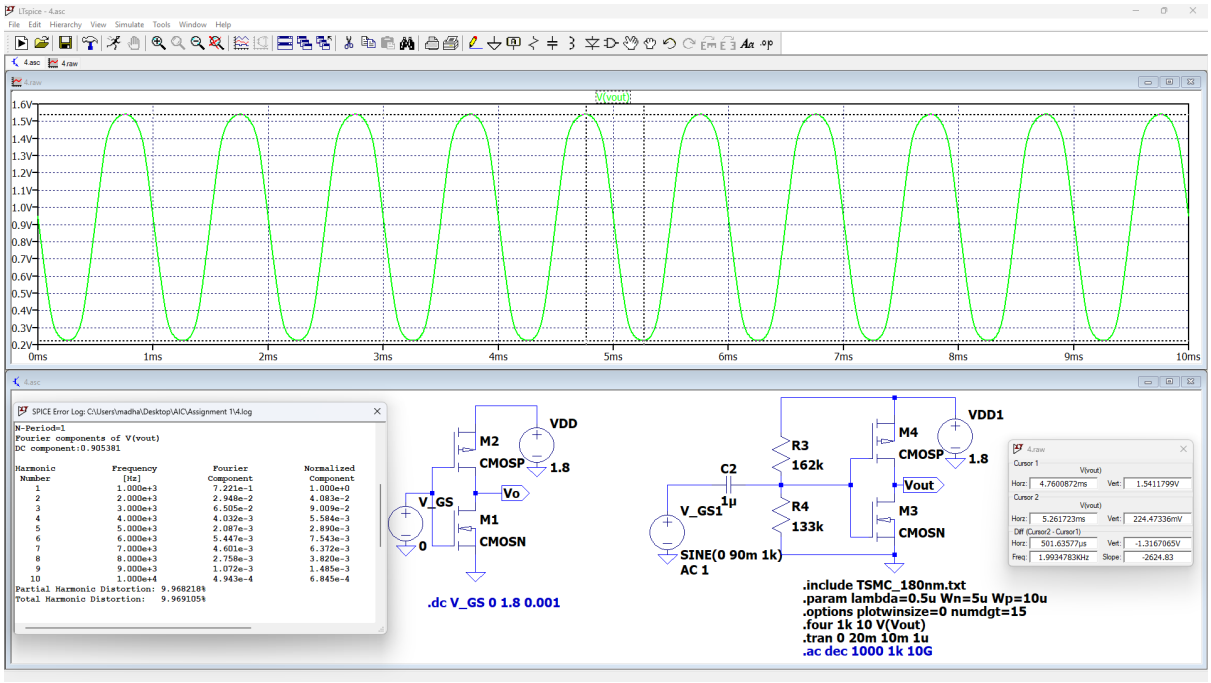

Figure 22: Maximum Input Amplitude for THD $< 10\%$ in Single Stage CMOS Amplifier in TSMC 180nm Technology Node

Two identical stages were cascaded using a 1μF AC coupling capacitor to ensure DC isolation between stages while allowing the signal to pass. To mitigate the loading effect—where the second stage's input impedance reduces the gain of the first stage—the resistive divider values were scaled by a factor of 10 to 162kΩ and 133kΩ. This increased

the input impedance of the second stage to approximately 73kΩ, preserving the overall gain.

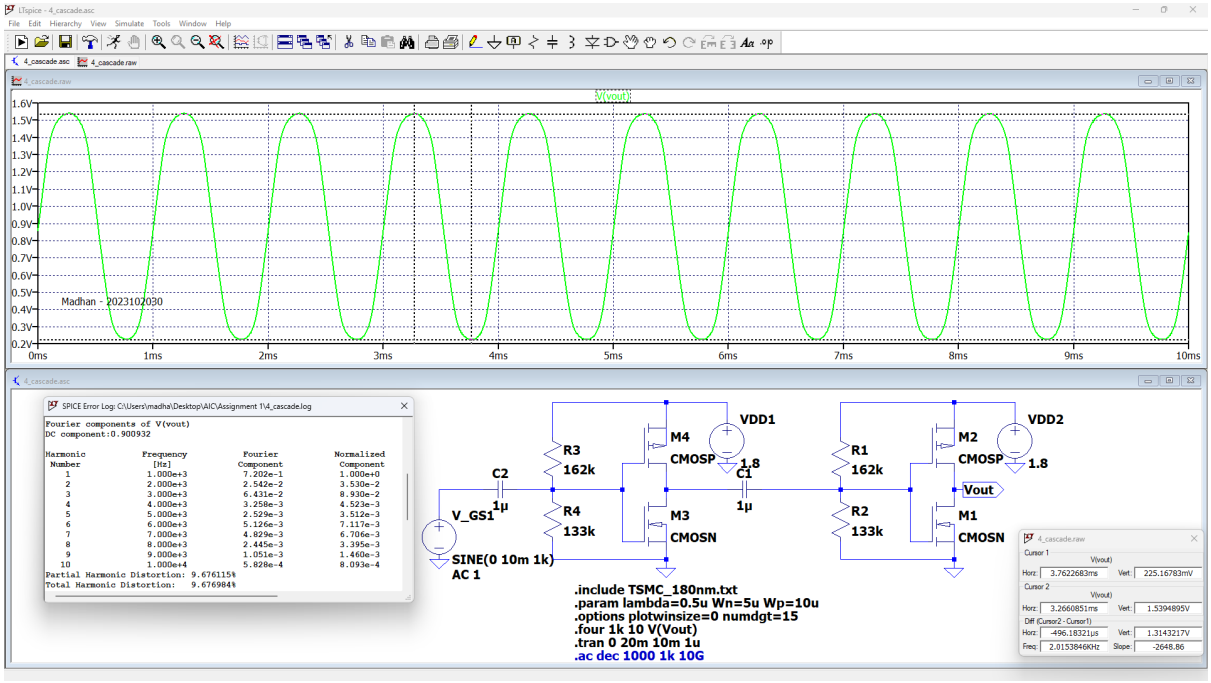

Figure 23: Maximum input amplitude for Maximum gain for Cascaded Two Stage CMOS Amplifier Schematic in TSMC 180nm Technology Node

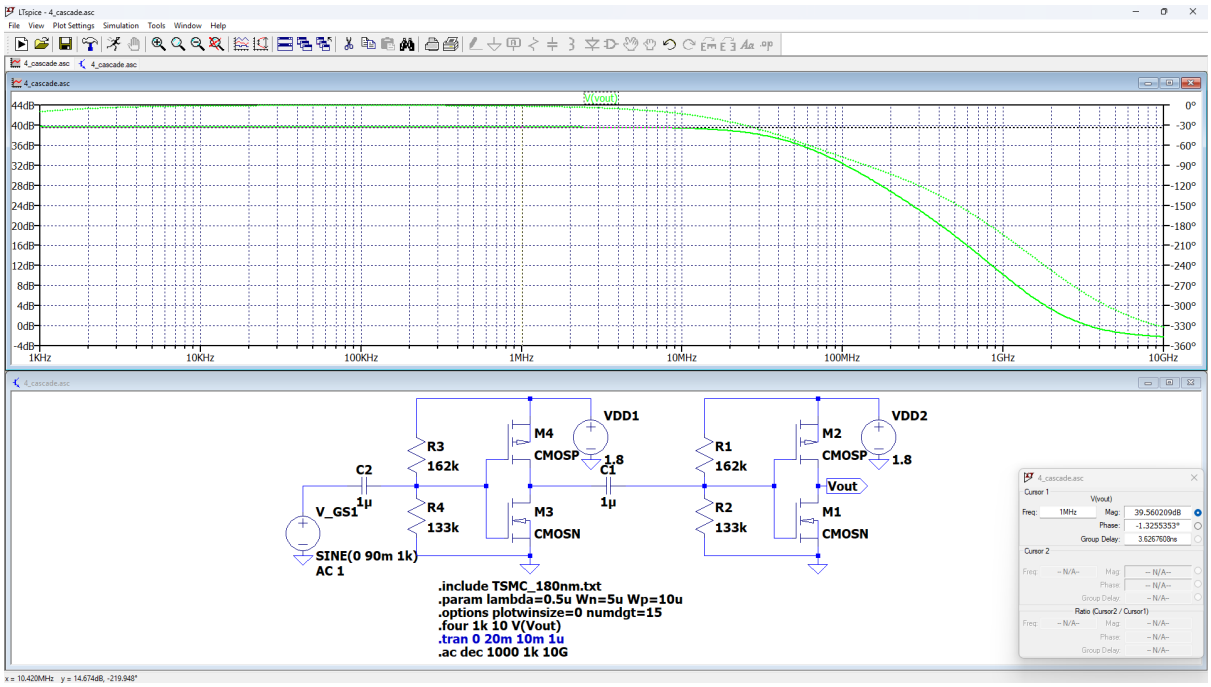

Figure 24: AC Small Signal Gain for Cascaded Two Stage CMOS Amplifier in TSMC 180nm Technology Node

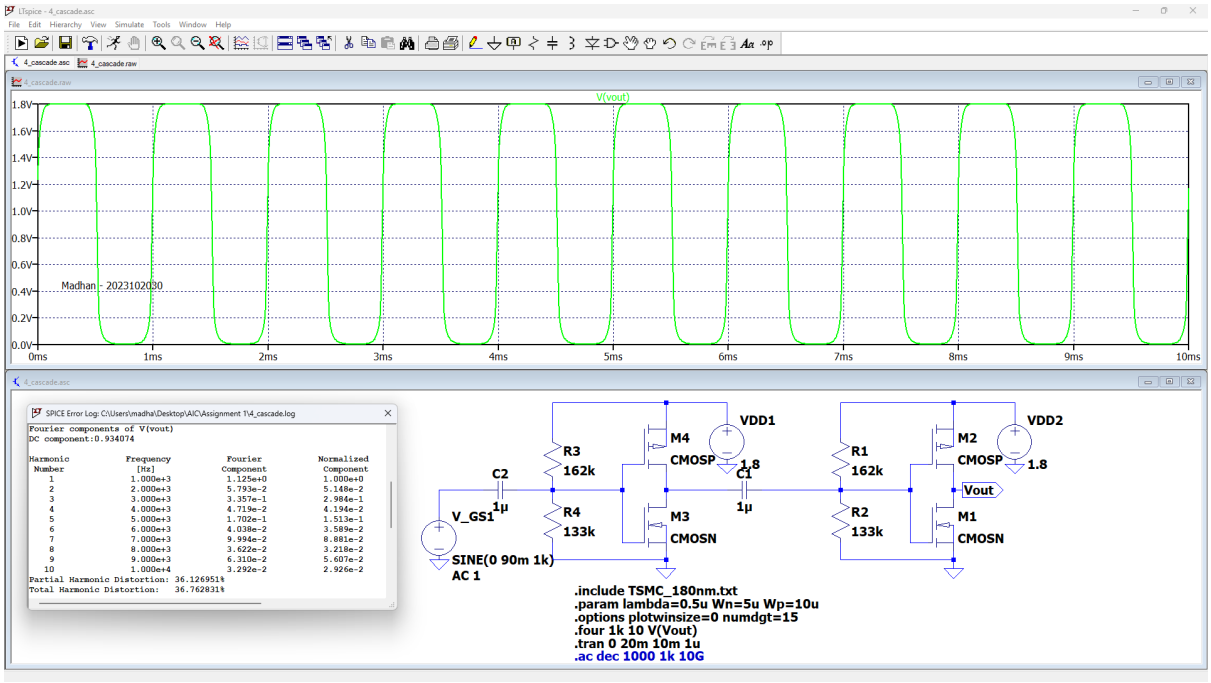

Figure 25: Maximum Input Amplitude for THD $< 10\%$ in Cascaded Two Stage CMOS Amplifier in TSMC 180nm Technology Node

The cascaded system provided a significantly higher gain of 39.56dB ($\approx$ 95V/V). However, it was observed that the 90mV input signal (A_{max} of a single stage) caused severe output clipping in the cascaded setup, resulting in a THD of 36.76%. Consequently, for the cascaded amplifier to operate within the 10% THD limit, the input amplitude must be scaled down to accommodate the increased gain.

Table 3: Performance Comparison at Different Input Amplitudes

Parameter	**Value at 10 mV Input**	**Value at 90 mV Input**
Output Swing	Unclipped (approx. 1.32 V_{pp})	Severely Clipped (1.8 V flat peaks)
Total Harmonic Distortion	9.68% (Success)	36.76% (Fail)
Cascaded Gain	39.56 dB	N/A (Non-linear due to clipping)