

Audio Amplifier

Electronic Workshop 2 Project 1

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2023102030

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2023102013

Abstract—This document is a detailed report on our Electronics Workshop 2 course project in the first half of the semester. The goal was to design and build an audio amplifier that can drive a $10\ \Omega$ speaker while maintaining good signal quality. We analyzed key performance metrics such as Common-Mode Rejection Ratio (CMRR), Total Harmonic Distortion (THD), and Slew Rate to ensure minimal distortion and effective amplification.

Testing in the laboratory confirmed that our final design achieved excellent audio performance across the entire hearing range, successfully meeting all project requirements. Throughout this process, we gained practical experience dealing with real-world amplifier design challenges, especially in managing heat issues and reducing interference from the power supply.

I. INTRODUCTION

The **Aim** of the project is to build an audio amplifier with the following specifications:

- Supply Voltage: $\pm 5V$ and $12V$ rail
- Input small signal voltage: $10 - 20\text{ mV}$ peak-to-peak
- Gain: $G_1 \times G_2 \geq 400$ (Pre-amp & Gain Stage)
- Frequency Range: Audible Range (20 Hz to 20 kHz)
- Power: $\geq 1.5W$
- The filter **should not** attenuate the input signal.
- The Power Amplifier **should not** provide voltage gain.
- Load: 10Ω

II. STAGES

A. Pre-Amplifier

The pre-amp stage is required for initial amplification. Ideally, the input resistance should not be low as this will cause the amplifier to draw high current, which the microphone cannot supply, leading to ineffective operation.

For this reason, the common-emitter differential amplifier is used as it has high input impedance, low output impedance, and good noise performance. If the noise performance is poor, the already weak signal ($10mV - 40mV$) could be completely overpowered by noise.

For proper operation, the two NPN BJTs must be in active mode:

- Base-Emitter junction: Forward Bias
- Base-Collector junction: Reverse Bias

The input can be applied to either transistor's base, with the choice of either grounding the other transistor's base or

applying an equal and opposite input to the other transistor's base (effectively doubling the amplification).

In our circuit simulation and hardware we've grounded the other transistor's base since we didn't want to deal with the phase offset issues due to the inverting circuit design. We made sure that the CMRR of the differential amplifier is high enough to suppress the noise.

1) *Circuit Design*: Pre-Amp stage circuit is a BJT differential amplifier. We've used a voltage source to generate the required tail current and R_{E_1} and R_{E_2} to model the differences in the NPN transistors to equalize the emitter currents.

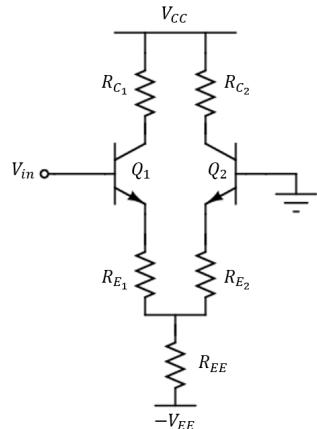


Fig. 1. BJT Differential Amplifier Circuit Design

2) *Circuit Analysis*: For simpler calculations, we've used the T-Model of a BJT for small signal model. Differential Mode,

Using KCL,

$$\frac{1}{r_e + R_{E_1}} \left[\frac{v_{id}}{2} - v_e \right] + \frac{1}{r_e + R_{E_2}} \left[\frac{-v_{id}}{2} - v_e \right] - \frac{v_e}{R_{ee}} = 0$$

To make the circuit symmetric, R_{E_1}, R_{E_2} and R_{C_1}, R_{C_2} are equalized. From the symmetry of the circuit it is clear that, $i_{e_1} = -i_{e_2}$ and $v_e = 0$

$$\Rightarrow i_{e_1} = -i_{e_2} = \frac{v_{id}}{2(r_e + R_{ee})}$$

$$\Rightarrow V_{C_1} = -\alpha i_{e_1} R_{C_1}$$

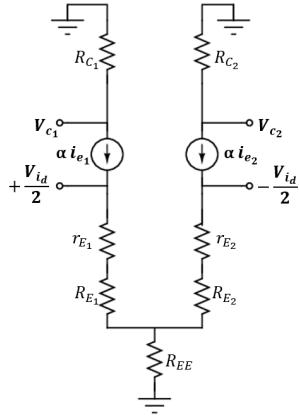


Fig. 2. Small Signal model of Pre-Amp Stage in Differential Mode

Considering, $\alpha \approx 1$ We get,

$$v_{c1} = \frac{v_{id}R_C}{2(r_e) + R_{EE}}$$

$$\left| \frac{v_{c1}}{v_{id}} \right| = \frac{R_c}{2(r_e + R_{EE})}$$

$$|A_d| = \frac{R_c}{2(r_e + R_{EE})}$$

Common - Mode,

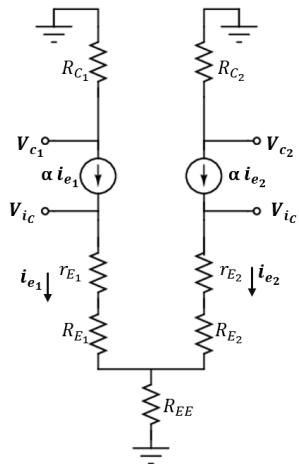


Fig. 3. Small Signal Model of Pre-Amp Stage in Common Mode

Considering the plane of symmetry, we get $v_e = 0$
Using KVL,

$$v_{ic} - i_e(r_e + R_e) - 2i_eR_{EE} = 0$$

$$\Rightarrow i_e = \frac{v_{ic}}{r_e + R_e + 2R_{EE}}$$

$$v_{c1} = v_{c2} = -\alpha i_e R_c = -\alpha \frac{v_{ic}}{r_e + R_e + 2R_{EE}} R_C$$

$$\Rightarrow A_c = \frac{v_c}{v_{ic}} = \frac{-\alpha R_C}{r_e + R_e + 2R_{EE}}$$

Considering, $\alpha \approx 1$ and $r_e \ll R_e + 2R_{EE}$

$$A_C = \frac{-R_C}{R_e + 2R_{EE}}$$

Using the Differential gain A_d and Common Mode gain A_c derived above, we can find the Common-Mode Rejection Ratio(CMRR) of the differential amplifier,

$$CMRR = \left| \frac{A_d}{A_c} \right| = \frac{2R_{EE} + R_e}{2(R_e + r_e)} \approx \frac{2R_{EE} + R_e}{2R_e}$$

3) *Simulation:* The simulated Pre-Amp stage gives a gain of about 440 times the input.

$$\left| \frac{V_{out}}{V_{in}} \right| \approx 44$$

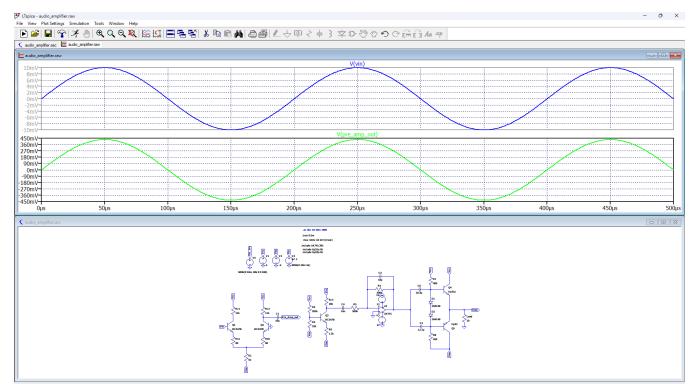


Fig. 4. Pre-Amp LTSpice Simulation Results

4) *Hardware:* The hardware design of the Pre-Amp stage is about 42 times.

$$\left| \frac{V_{out}}{V_{in}} \right| \approx 42$$

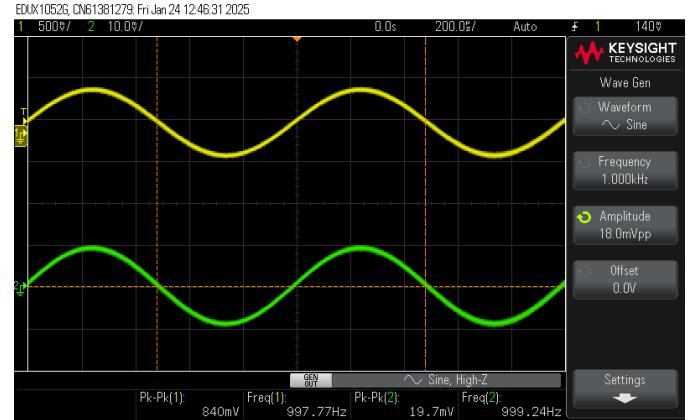


Fig. 5. Hardware Result of the Pre-Amp Stage

B. Gain Stage

A Common-Emitter (CE) amplifier is used for this stage due to its high input impedance, low output impedance, and high current and voltage gain.

1) *Circuit Design:* The gain stage uses a BJT amplifier in Common Emitter configuration (CE Amplifier). The input capacitor (C_1) and the output capacitor (C_2) serves to block DC components of the input signal and contributes a pole to the system. The frequency lies between 20Hz and 20kHz .

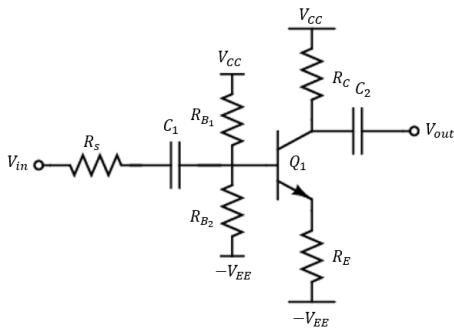


Fig. 6. CE Amplifier design

2) *Circuit Analysis:* We've used the T-Model of BJT to analyse the CE amplifier in its small signal model.

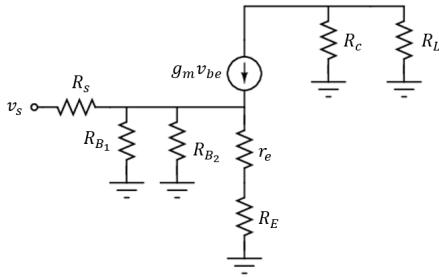


Fig. 7. Small Signal model using T Model of a BJT

$$v_{be} = \frac{v_i r_e}{r_e + R_e} = \frac{v_i \frac{\alpha}{g_m}}{\frac{\alpha}{g_m} + R_e} = \frac{v_i \alpha}{\alpha + g_m R_e}$$

$$v_o = -g_m v_{be} R_o = -g_m \frac{v_i \alpha}{\alpha + g_m R_e} R_o$$

$$A_v = -g_m \frac{\alpha}{\alpha + g_m R_e} R_o$$

Considering, $\alpha \approx 1$ and $g_m R_E \gg 1$

$$A_V \approx \frac{-R_o}{R_E}$$

3) *Simulation:* The simulated design results show a gain of around 10 times.

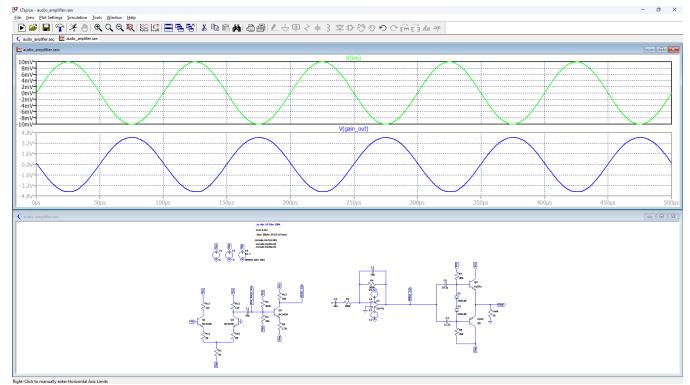


Fig. 8. Simulation result after the gain stage + Pre-Amp Stage Combined

4) *Hardware:* The hardware results almost match the simulated results. The output of the final gain stage is inverted and amplified by around 420 times as expected from the simulations.

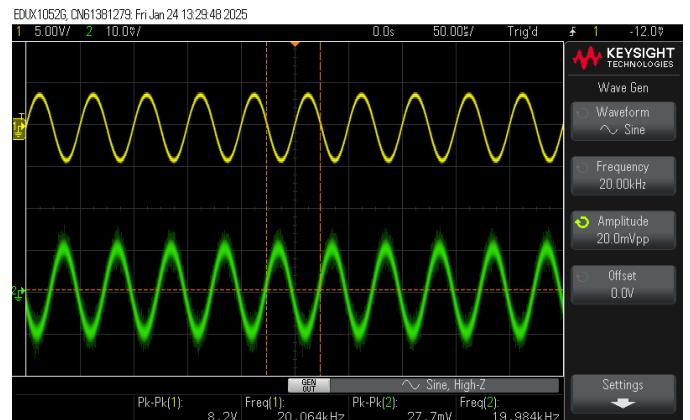


Fig. 9. Hardware output result after the gain stage + Pre-Amp Stage combined

C. Filter Stage

We're using an active band-pass filter to filter out the frequencies outside the range of (20Hz to 20KHz).

1) *Circuit Design:* Below is the configuration of op-amp band pass filter we're using for this project.

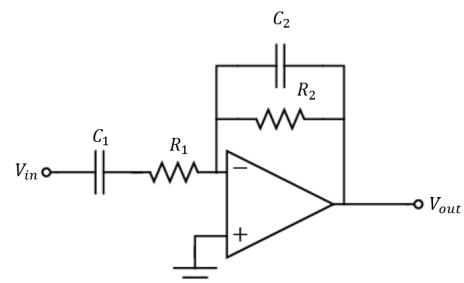


Fig. 10. Active Band Pass filter circuit design

2) *Circuit Analysis:* Using KCL at the non-inverting terminal node,

$$\frac{0 - V_{in}}{R_1 + \frac{1}{SC_1}} + \frac{0 - V_o}{R_2} + \frac{0 - V_o}{\frac{1}{SC_2}} = 0$$

$$V_o \left(\frac{1}{R_2} + SC_2 \right) = \frac{-V_{in}}{R_1 + \frac{1}{SC_1}}$$

$$\Rightarrow H(s) = \frac{-S(\frac{1}{R_1 C_2})}{S^2 + S(\frac{1}{R_1 C_1} + \frac{1}{R_2 C_2}) + (\frac{1}{R_1 C_1})(R_2 C_2)}$$

3) *Simulation:* The frequency cut-off values are close to the required 20Hz and 20KHz.

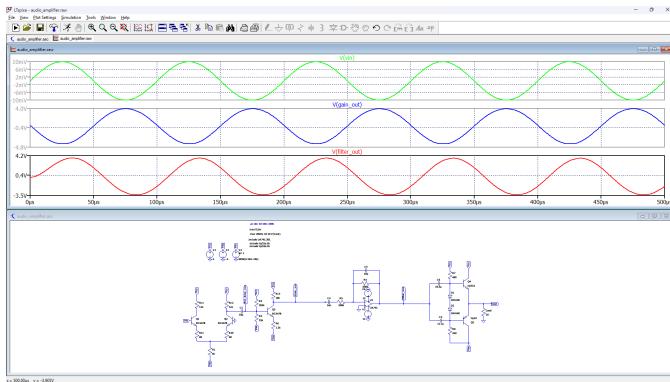


Fig. 11. Simulation Result of pre-amp + gain + filter

4) *Hardware:* The hardware results showed a cut-off of around 20.6GHz at -2.89dB and around 23.31KHz at -2.96dB.

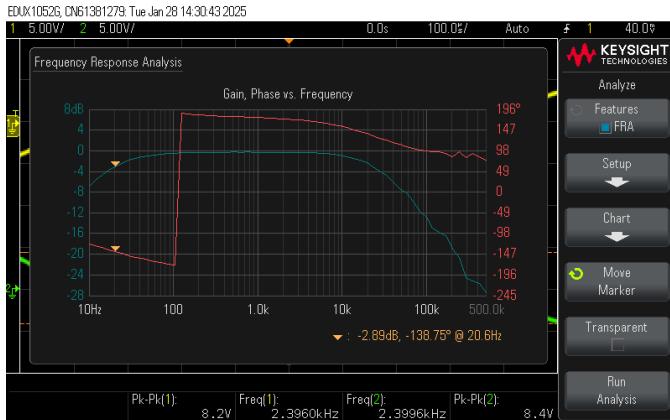


Fig. 12. Bode Plot of the bandpass filter for lower frequency cutoff

D. Power Amplifier

A class AB power amplifier is recommended, as it improves upon class A and class B designs. Class A amplifiers are inefficient, requiring higher DC supply and leading to excessive power dissipation. Class B amplifiers introduce crossover distortion, which can negatively affect audio quality. Class AB amplifiers reduce crossover distortion while maintaining efficiency.



Fig. 13. Bode Plot of the bandpass filter for higher frequency cutoff

1) *Circuit Design:* Below figure shows the configuration of class AB amplifier we've used for our project.

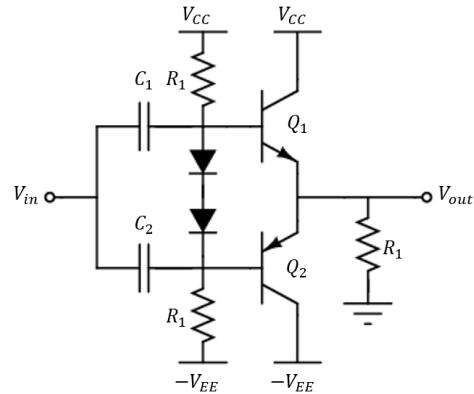


Fig. 14. Class AB Power Amplifier Circuit Design

2) *Simulation:* Below is the simulation result of the power amplifier design used in the project

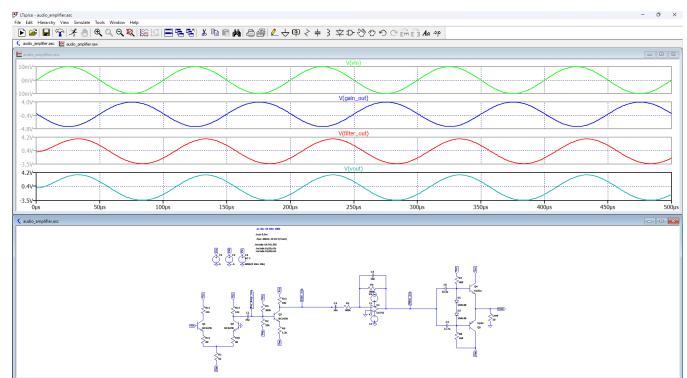


Fig. 15. Simulation result after power amplifier

3) *Hardware:* The hardware results followed the simulation results.

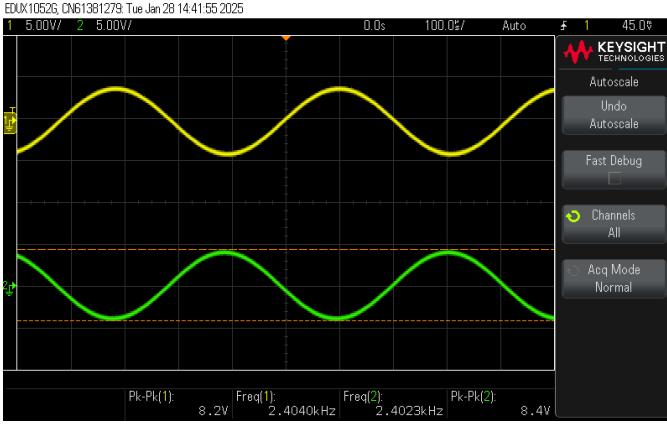


Fig. 16. Output waveform of the power amplifier for the filter stage input

E. Mic Biasing

The given mic works at a certain voltage and current specifications. We've used voltage dividers to bring down the input signal voltage to the desired range for the pre-amp stage and a capacitor to block the dc component from the mic.

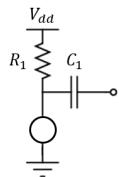


Fig. 17. Mic Circuit

F. Voltage Regulator

The Op-Amps need a voltage rail of $> 7V$. So we've used a voltage regulator ic (LM7805 & LM7905) to down convert the 12V input supply to the required 5V and -5V.

III. FULL CIRCUIT

A. SPICE Circuit

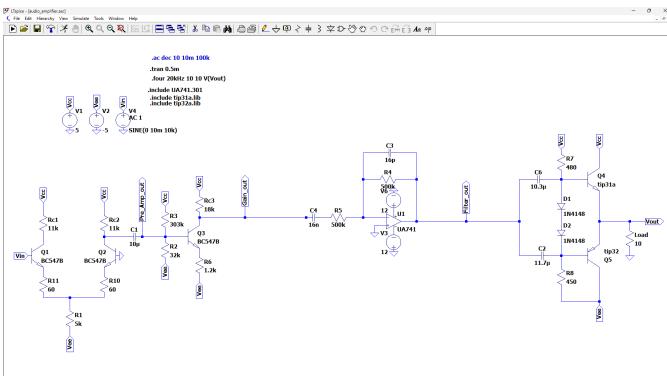


Fig. 18. Simulation design of the final circuit design of the audio amplifier

1) Final Simulated design:

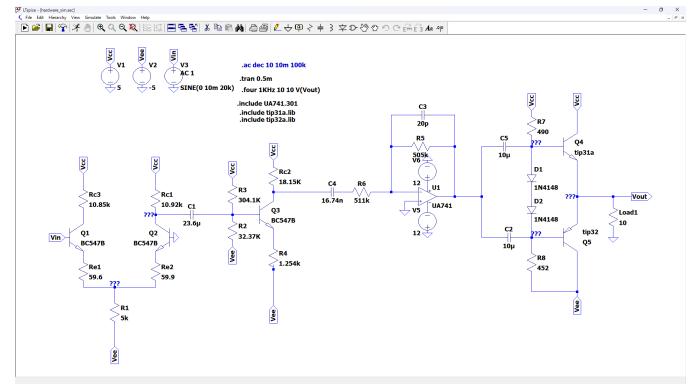


Fig. 19. Hardware simulated design of the final assembled circuit

2) Final Hardware implementation modeled design:

Final Hardware Implementation: Below is the labeled image of the final hardware implementation of our audio amplifier design.

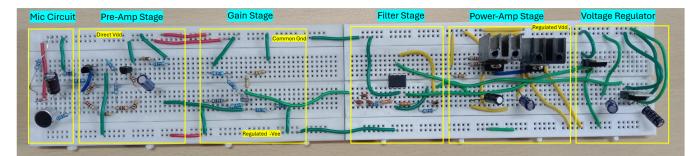


Fig. 20. Full Hardware Implementation

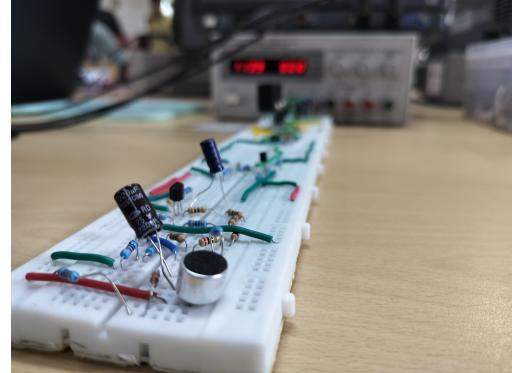


Fig. 21. Final Hardware assembly 1

IV. DISTORTION ANALYSIS

Distortion analysis helps quantify unwanted harmonic content in the output signal. The Total Harmonic Distortion (THD) is given by:

$$\text{THD} = \sqrt{\frac{\sum_{n=2}^{\infty} V_{n\text{RMS}}^2}{V_{f\text{RMS}}^2}}$$

where:

- $V_{n\text{RMS}}$ is the RMS voltage of the n th harmonic.
- $V_{f\text{RMS}}$ is the RMS voltage of the fundamental frequency.

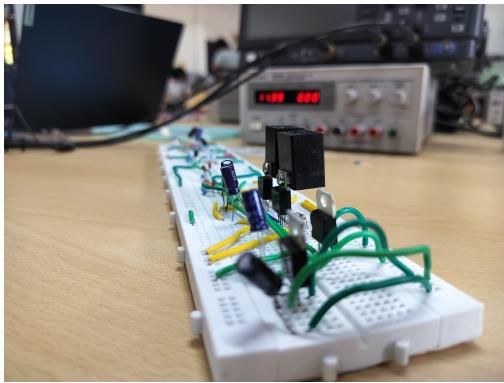


Fig. 22. Final Hardware assembly 2

High THD leads to significant distortion, affecting the quality of audio output. Lower THD values result in better audio fidelity. THD can be improved by minimizing circuit interference and using filters to eliminate unwanted harmonics.

For an input signal frequency of 20Hz.

Harmonic Number	Frequency [Hz]	Fourier Component	Normalized Component	Phase [deg]	Normalized Phase [deg]
1	20	1.291	1.000	-17.36	0.00
2	40	0.05607	0.04341	103.70	121.06
3	60	0.02239	0.01734	55.80	73.16
4	80	0.008619	0.006674	-37.29	-19.92
5	100	0.002781	0.002153	-44.74	-27.38
6	120	0.001058	0.0008193	145.69	163.05
7	140	0.0006570	0.0005087	39.26	56.62
8	160	0.0008463	0.0006553	8.93	26.29
9	180	0.0003079	0.0002384	-127.60	-110.24
10	200	0.0002432	0.0001883	8.67	26.03

Partial Harmonic Distortion: 4.728816%
Total Harmonic Distortion: 4.741400%

For an input signal frequency of 20KHz.

Harmonic Number	Frequency [Hz]	Fourier Component	Normalized Component	Phase [deg]	Normalized Phase [deg]
1	20000	2.590	1.000	143.75	0.00
2	40000	0.03947	0.01524	-71.13	-214.88
3	60000	0.07911	0.03054	34.39	-109.36
4	80000	0.01156	0.004465	179.12	35.37
5	100000	0.01425	0.005503	-140.39	-284.14
6	120000	0.003107	0.001200	33.57	-110.18
7	140000	0.007627	0.002945	48.78	-94.97
8	160000	0.001641	0.0006336	-147.82	-291.57
9	180000	0.003692	0.001426	-87.40	-231.15
10	200000	0.001920	0.0007411	66.77	-76.98

Partial Harmonic Distortion: 3.504799%
Total Harmonic Distortion: 3.514212%

A. Slew Rate

The slew rate (S.R.) is defined as:

$$S.R. = \max \left(\frac{\delta V_{out}}{\delta t} \right)$$

Ideally, the slew rate should be infinitely high so that high-frequency signals are accurately amplified without distortion. A low slew rate causes the circuit to lag behind the input signal, resulting in distortion. The slew rate can be increased by:

- Increasing the maximum operating voltage.
- Reducing the capacitive impedance of subcircuits to allow higher-frequency operation.

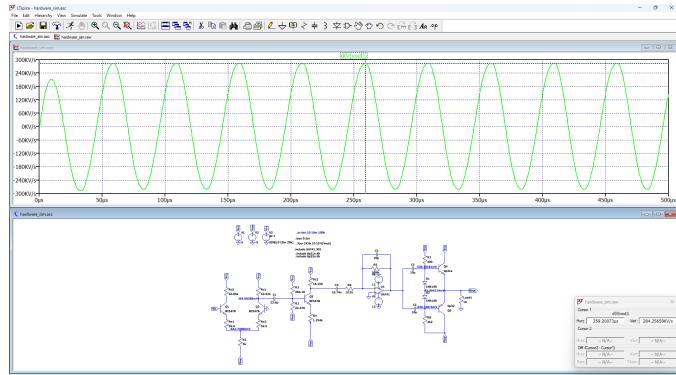


Fig. 23. Time derivative plot of output voltage V_{out}

From the above LTSpice simulation, the slew rate of our audio amplifier is found out to be around $284.3KV/s$ at $20KHz$ input frequency.

V. CONCLUSION

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