

CMOS References and Regulators: Homework

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1 Lecture 1

1.1 Proving Resistance: Current is proportional to Voltage

Do the 'DC Analysis' for the following circuits. Plot V vs I & write expression for the slope. Prove that its a resistance.

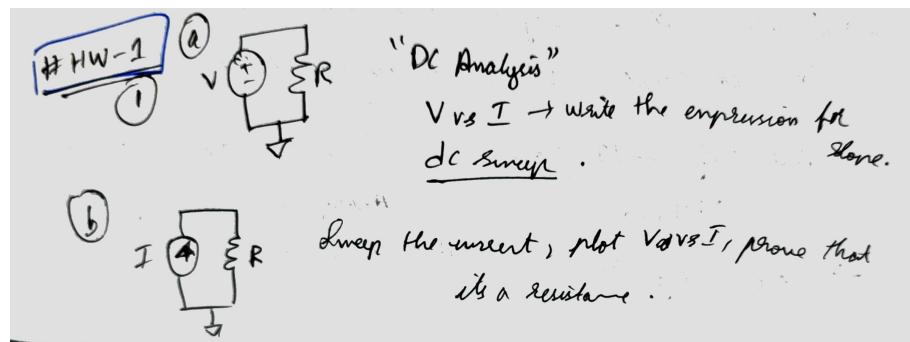


Figure 1: Lecture 1 - Question 1 - (a) and (b)

Answer:

Left graph shows the I - V characteristics of the device. Clearly, $I \propto V$. The right graph shows the expression for the slope.

Plot for (a) : Using a Voltage source

Plot for (b) : Using a Current source

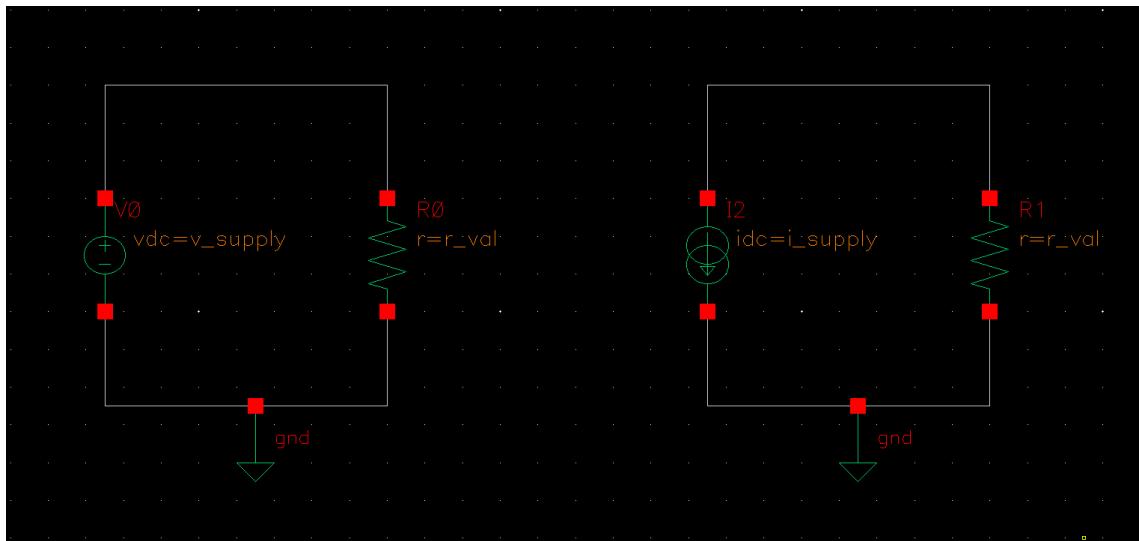


Figure 2: Lec 1: Q1: Testbench for (a) and (b)

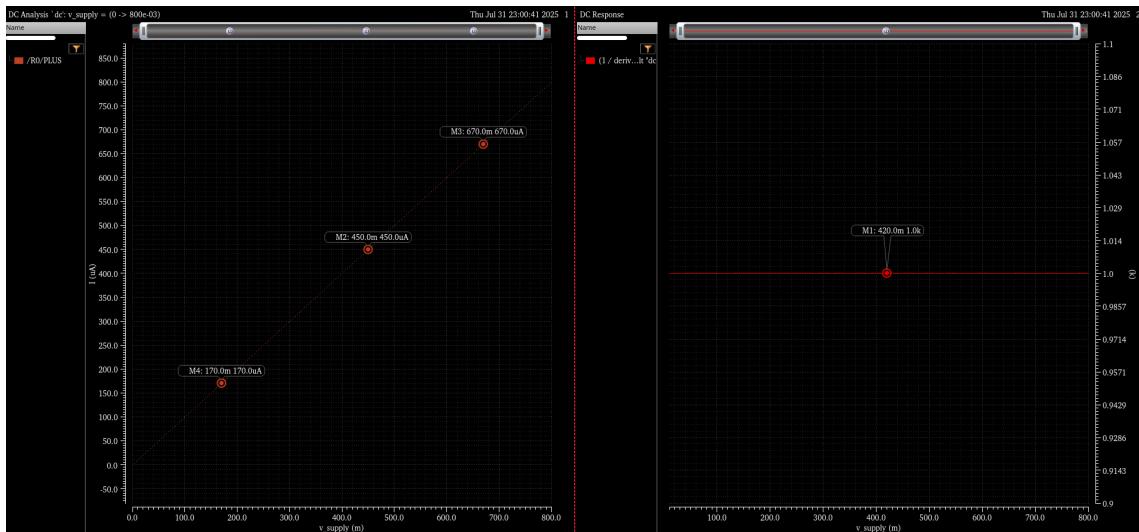


Figure 3: Lec 1: Q1: Plot for (a)

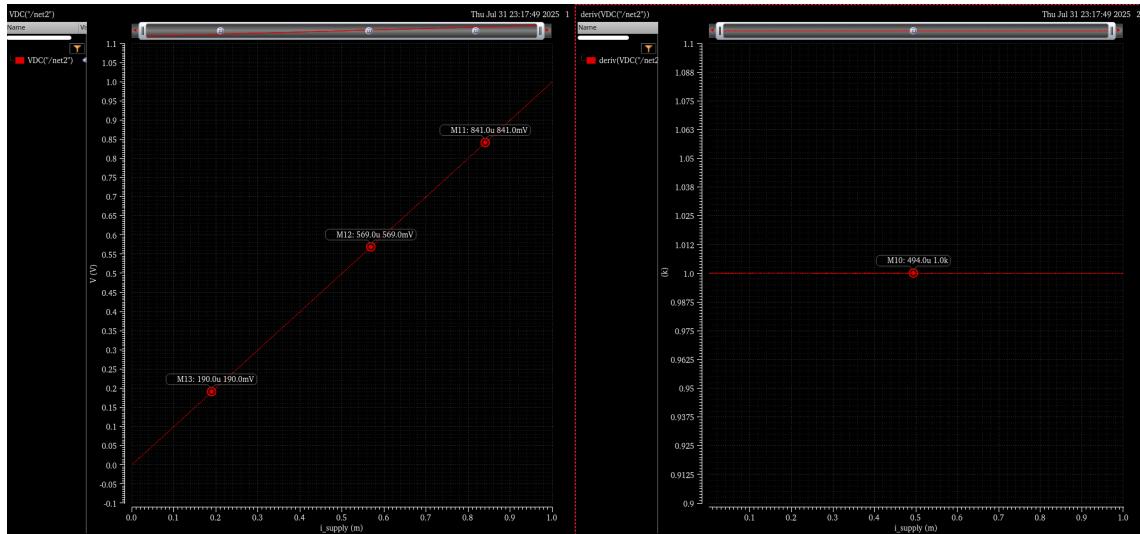


Figure 4: Lec 1: Q1: Plot for (b)

1.2 Capacitance Amplifier using Controlled Sources

Design a capacitance amplifier using controlled sources.

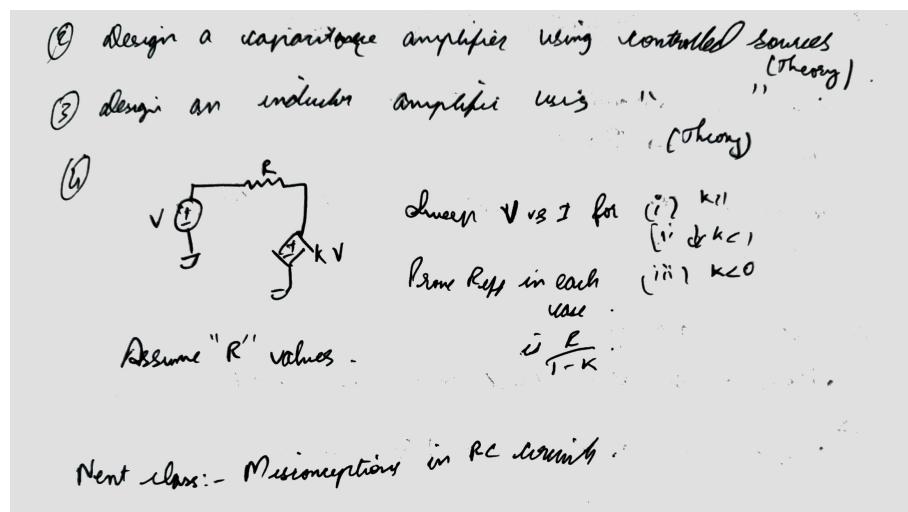
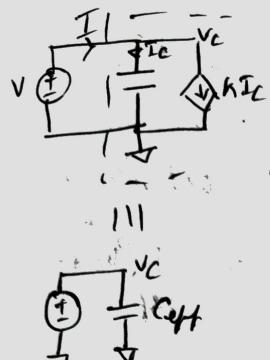


Figure 5: Lecture 1 - Question 2, 3, 4

Answer:

Capacitance Amplifier using controlled sources

CCCS:



$$I = I_{ct} + k \cdot I_c$$

$$= I_c(1+k)$$

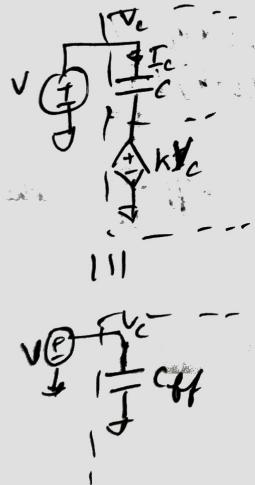
$$I = C \cdot \frac{dV_c}{dt} \cdot (1+k)$$

$$I = C(1+k) \cdot \frac{dV_c}{dt}$$

$$I \propto \frac{dV_c}{dt} \rightarrow \text{Capacitance.}$$

$$I = C_{eff} \cdot \frac{dV_c}{dt} \quad \text{where } C_{eff} = C(1+k)$$

VCVS:



$$I_c = C \cdot \frac{d}{dt}(V_c - kV_c)$$

$$I_c = C \frac{dV_c}{dt} \cdot (1-k)$$

$$I_c \propto \frac{dV_c}{dt} \Rightarrow C_{eff} = (1-k) \cdot C$$

Figure 6: Lecture 1 - Question 2 - Solution

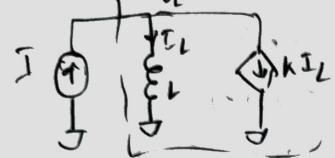
1.3 Inductance Amplifier using Controlled Sources

Design a inductance amplifier using controlled sources.

Answer:

Inductance Amplifier using controlled sources

CCS

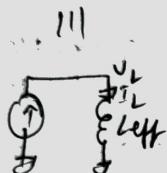


$$I = I_L + kI_L$$

$$= I_L(1+k)$$

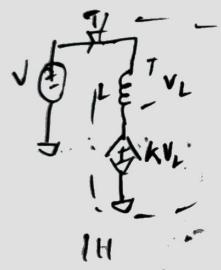
$$I = L \frac{dI}{dt} \cdot (1+k)$$

$$V_L = L \frac{dI_L}{dt}$$



$$I = \frac{1}{L_{eff}} \int V_L dt \Rightarrow L_{eff} = \frac{L}{1+k}$$

JCVS



$$V = V_L + kV_L$$

$$= (1+k) L \frac{dI}{dt}$$

$$V = L_{eff} \frac{dI}{dt} \quad \text{where } L_{eff} = L(1+k)$$

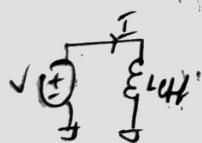
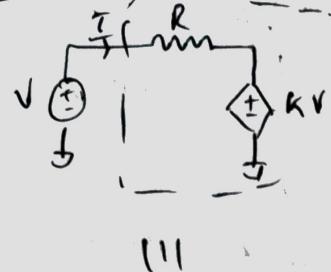


Figure 7: Lecture 1 - Question 3 - Solution

1.4 Resistance Amplifier using Controlled Sources

Sweep V vs I for (i) $k > 1$ (ii) $0 < k < 1$ (iii) $K < 0$ Prove R_{eff} in each case is $\frac{R}{1-k}$.
Answer:

Resistance Amplified using controlled sources



$$(V - kV) = I \cdot R$$

$$V(1-k) = I \cdot R$$

$$V = \frac{I \cdot R}{1-k}$$

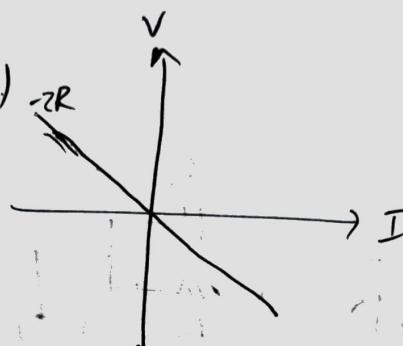
$$V = I \cdot R_{eff}$$



$$\text{where } R_{eff} = \frac{R}{1-k}$$

(i) $k > 1 \Rightarrow R_{eff} < 0$
(Neg. resistance)

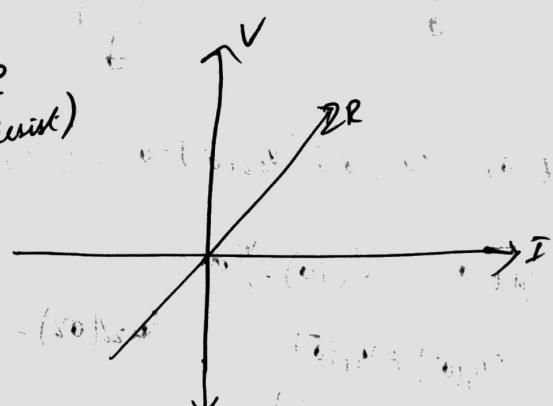
$$k=1.5 \Rightarrow R_{eff} = -2R$$



(ii) $0 < k < 1 \Rightarrow R_{eff} < \infty$

$$k=0.5 \rightarrow R_{eff} = 2R$$

(Amplified resist)



(iii) $k < 0 \Rightarrow R_{eff} < R$

$$k=-0.5 \rightarrow R_{eff} = \frac{R}{1.5} = \frac{2R}{3}$$

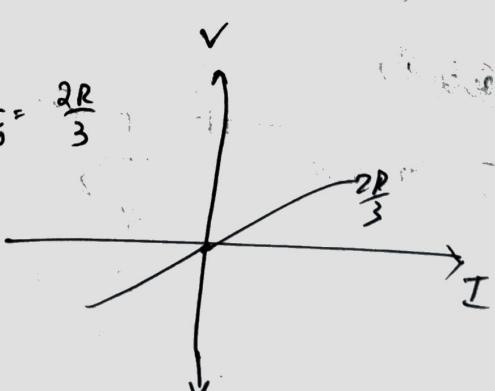


Figure 8: Lecture 1 - Question 4 - Solution

2 Lecture 2

2.1 Output Resistance

find the effective output resistance at V_{out} i.e., $R_{out} = ?$

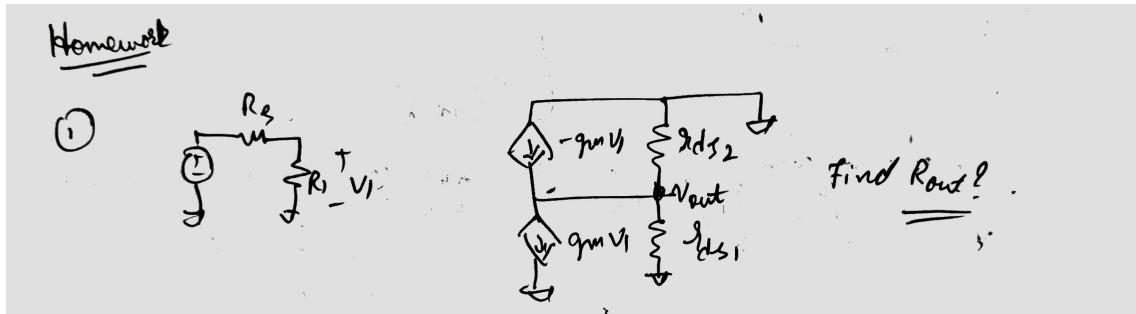


Figure 9: Lec 2: Question 1

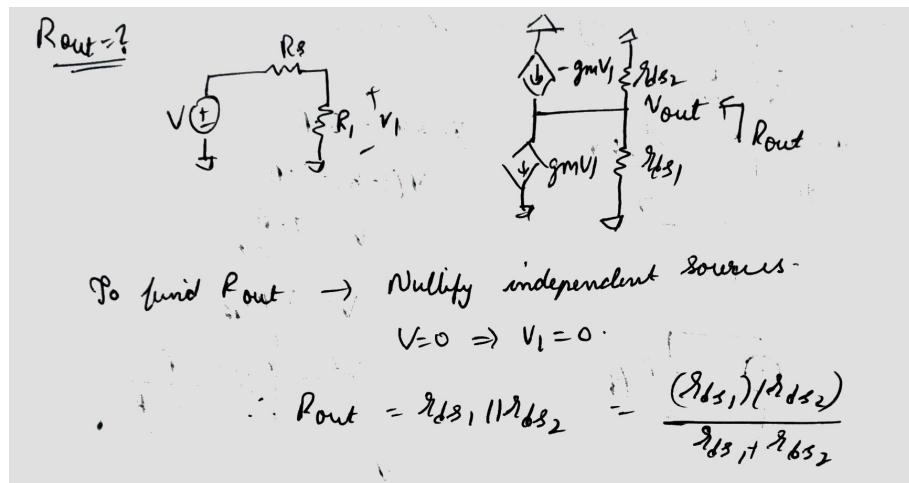


Figure 10: Lecture 2 - Question 1 - Solution

Answer:

When we nullify the V_1 , the vccs vanish and the effective output resistance at v_{out} node is $R_{out} = r_{ds_1} \parallel r_{ds_2}$.

Proved this using the plot with values.

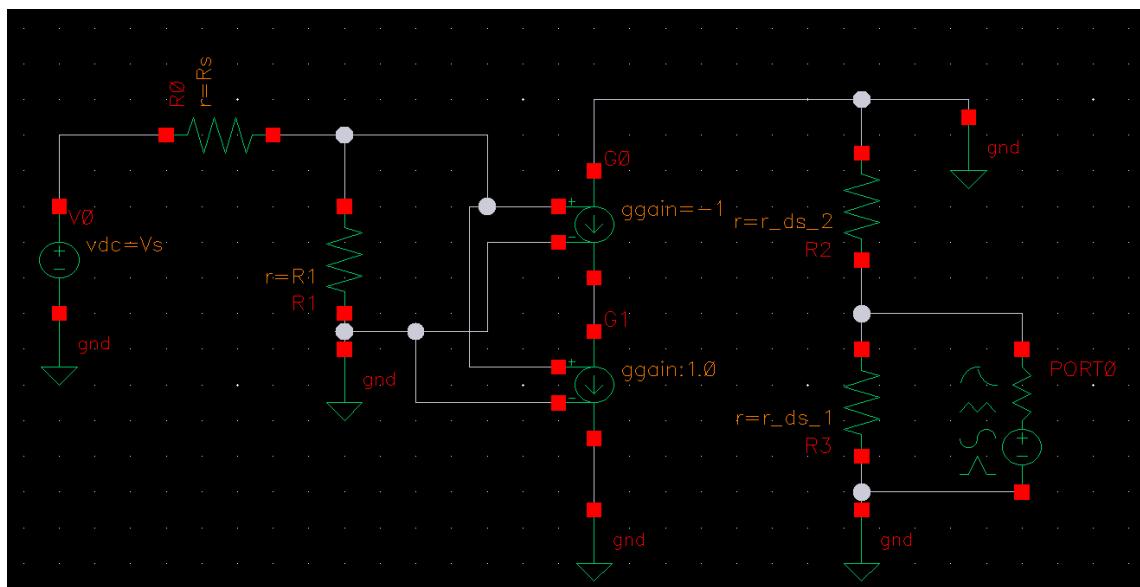


Figure 11: Lec 2: Q1: Testbench

2.2 Step Response for RC Circuit

Plot V_{out} vs time in Cadence. Prove Theory.

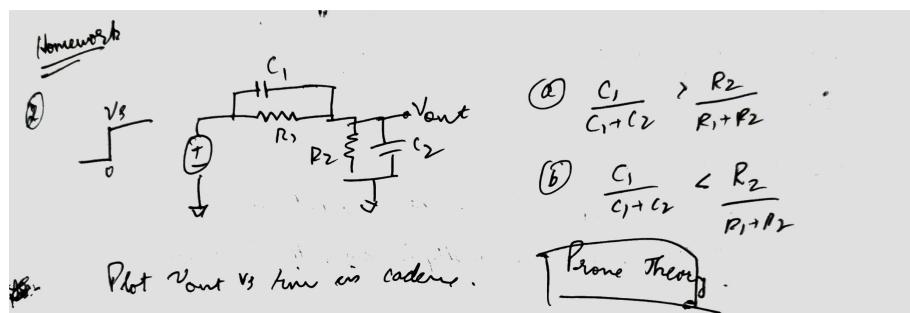
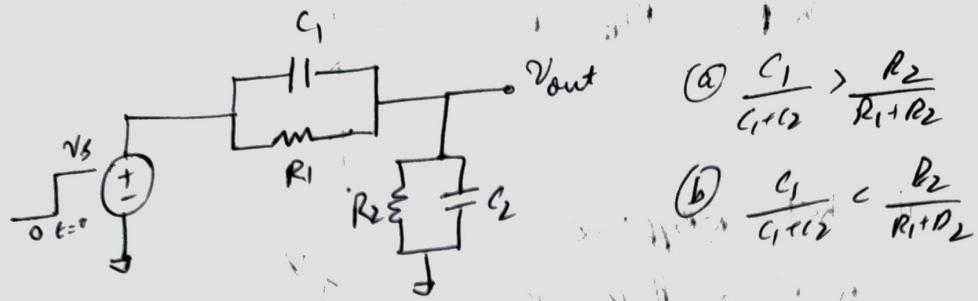


Figure 12: Lecture 2 - Question 2

Answer:

Copy this from the notes



$$(a) \frac{C_1}{C_1+C_2} > \frac{R_2}{R_1+R_2}$$

$$(b) \frac{C_1}{C_1+C_2} < \frac{R_2}{R_1+R_2}$$

$$@ t=0, \quad v_{c1}(0^+) = v_{c2}(0^-) = 0 \Rightarrow v_o(0^+) = 0$$

$$@ t=0, \quad i_c(0) = \frac{v_s}{R_2}$$

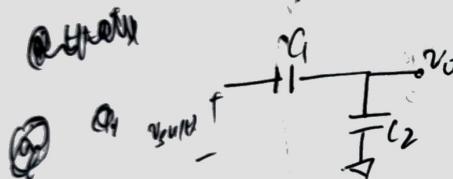
$$v_{c1}(0^+) \neq v_{c1}(0^-)$$

$$v_{c2}(0^-) \neq v_{c2}(0^+)$$

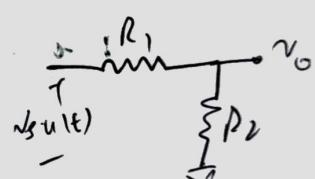
$$v_{c2}(0^+) =$$

$$\begin{aligned} v_o &= (R_{\text{eq}})([c_1]) \\ &\approx (R_1 R_2) / (C_1 C_2) \end{aligned}$$

@ t=0th



(b)



$$v_o(0^+) = \frac{C_1}{C_1+C_2} \cdot v_s$$

$$v_o(0^+) = \frac{R_2}{R_1+R_2} \cdot v_s$$

Figure 13: Lec 2: Solution for Question 2

$$(a) V_o(0^+) = \frac{R_2}{R_1+R_2} \cdot V_s$$

$$V_o(\infty) = \frac{C_1}{C_1+C_2} \cdot V_s$$

$$V_o(t) = \left\{ \frac{V_s C_1}{C_1+C_2} + \left(\frac{V_s R_2}{R_1+R_2} - \frac{V_s C_1}{C_1+C_2} \right) e^{-\frac{t}{\tau}} \right\} u(t)$$

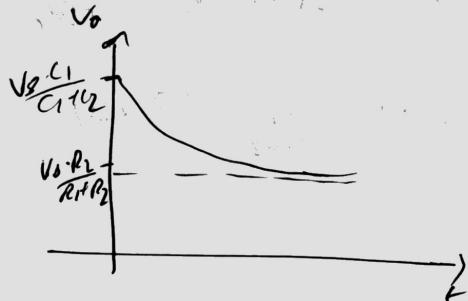
$$C_1 = 2n$$

$$C_2 = 1n$$

$$R_1 = 100\Omega$$

$$R_2 = 100\Omega$$

$$\gamma = 150nS$$



$$V_o(t) = 0.5 + (0.66 - 0.5)e^{-\frac{t}{\tau}}$$

$$V_o(\infty) = 0.5 + 0.37 \times 10^{-16} \\ = 560 \text{ mV}$$

$$(b) V_o(0^+) = \frac{C_1}{C_1+C_2} \cdot V_s \quad V_o(\infty) = \frac{R_2}{R_1+R_2} \cdot V_s$$

$$V_o(t) = \left\{ \frac{V_s R_2}{R_1+R_2} + \left(\frac{V_s C_1}{C_1+C_2} - \frac{V_s R_2}{R_1+R_2} \right) e^{-\frac{t}{\tau}} \right\} u(t)$$

Figure 14: Lec 2: Solution for Question 2

$$C_1 = 1n$$

$$C_2 = 1n$$

$$R_1 = 100\Omega$$

$$R_2 = 100\Omega$$

$$\gamma = 133nS$$

$$V_o(t) = 0.67 + (0.5 - 0.67)0.37$$

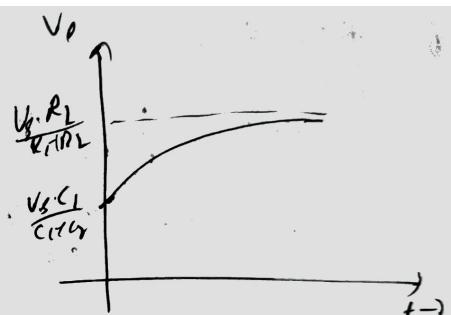


Figure 15: Lec 2: Solution for Question 2

Proved this using theory and from the simulations by finding the output voltage after 1 time constant.

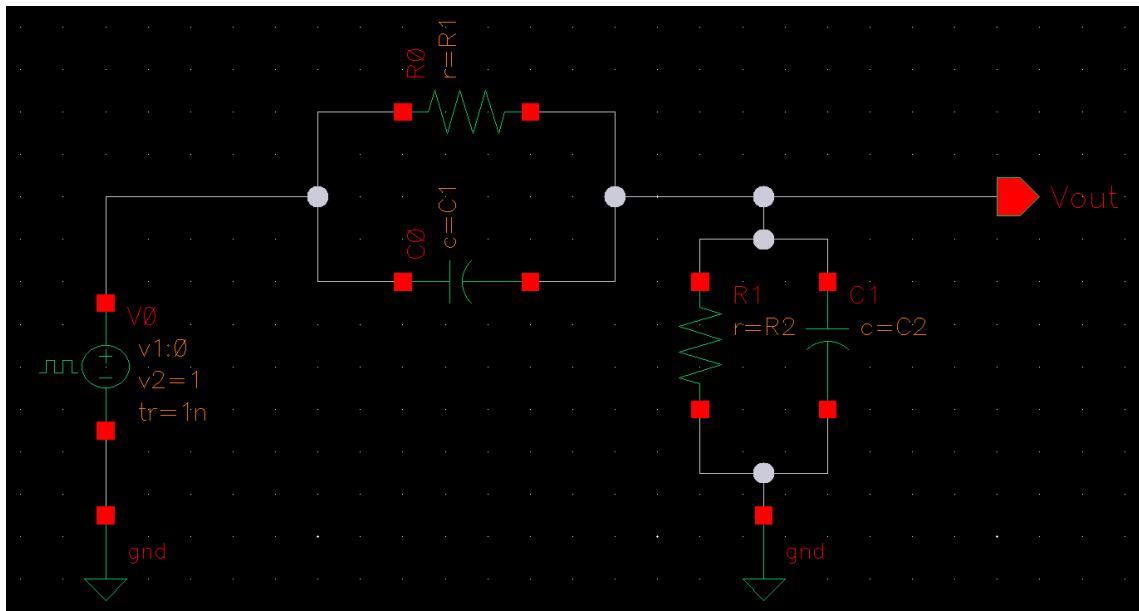


Figure 16: Lec 2: question 2 Testbench

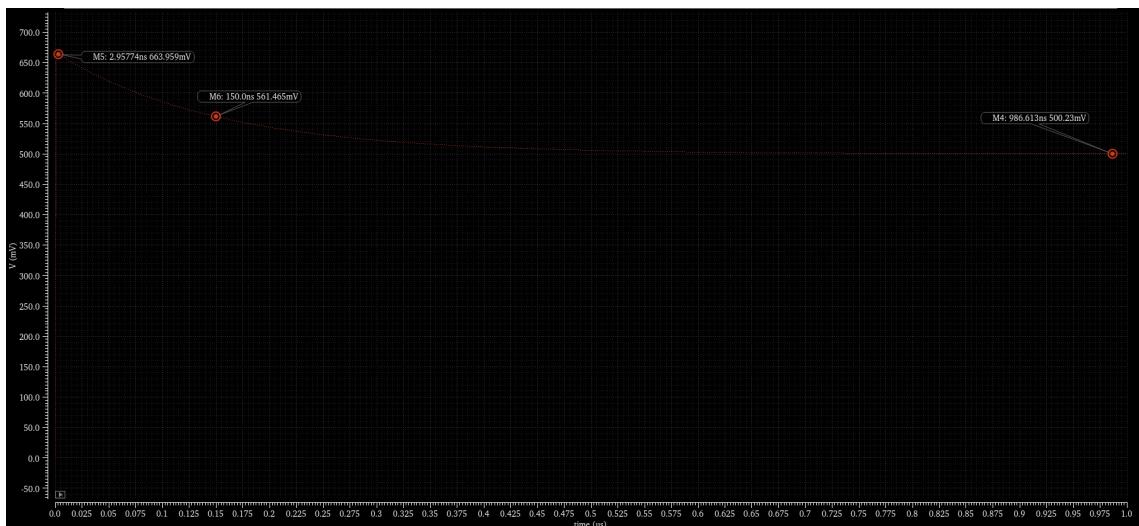


Figure 17: Lec 2: Q2: Soln - Part (a)

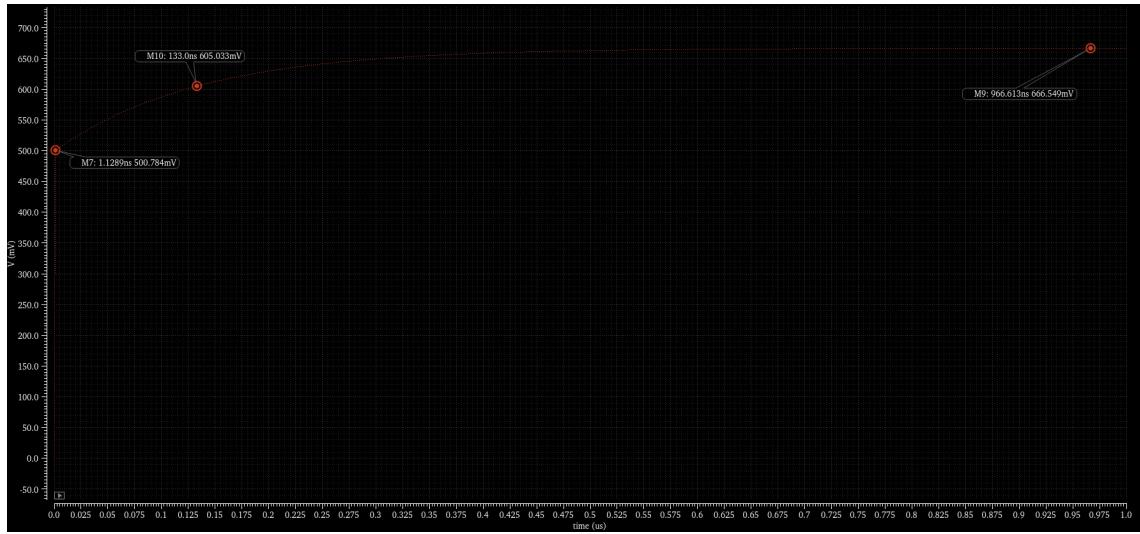


Figure 18: Lec 2 : Q2: Soln - Part (b)

3 Lecture 3

3.1 Step Response for passive RLC circuit Combinations

Plot V_{out} vs time and I_{out} vs time

-
-
-

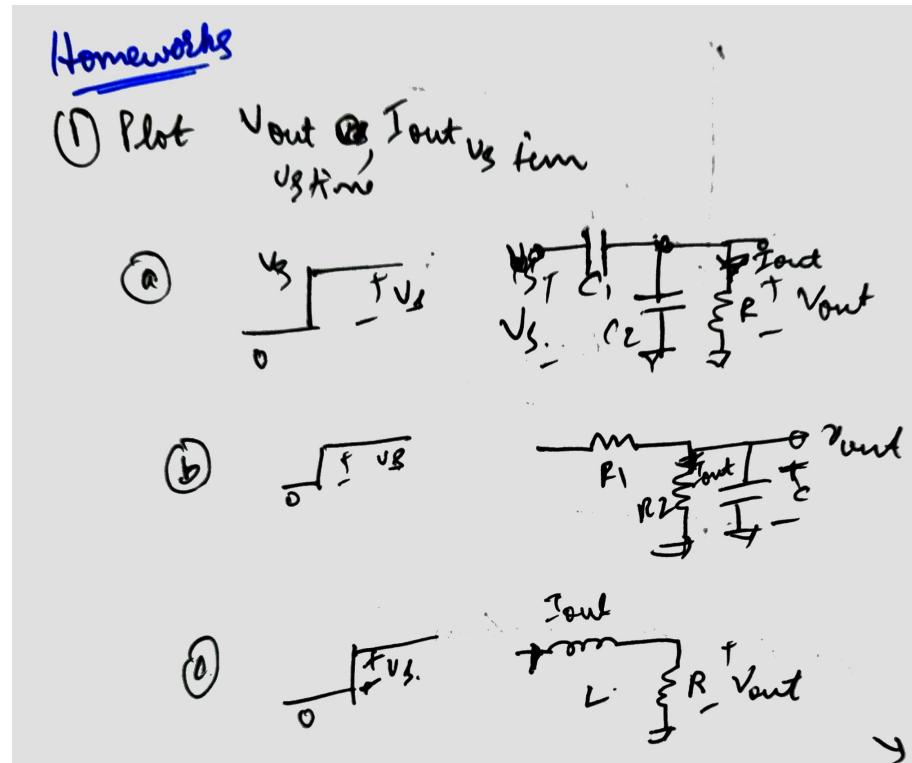


Figure 19: Lecture 3 - Question 1

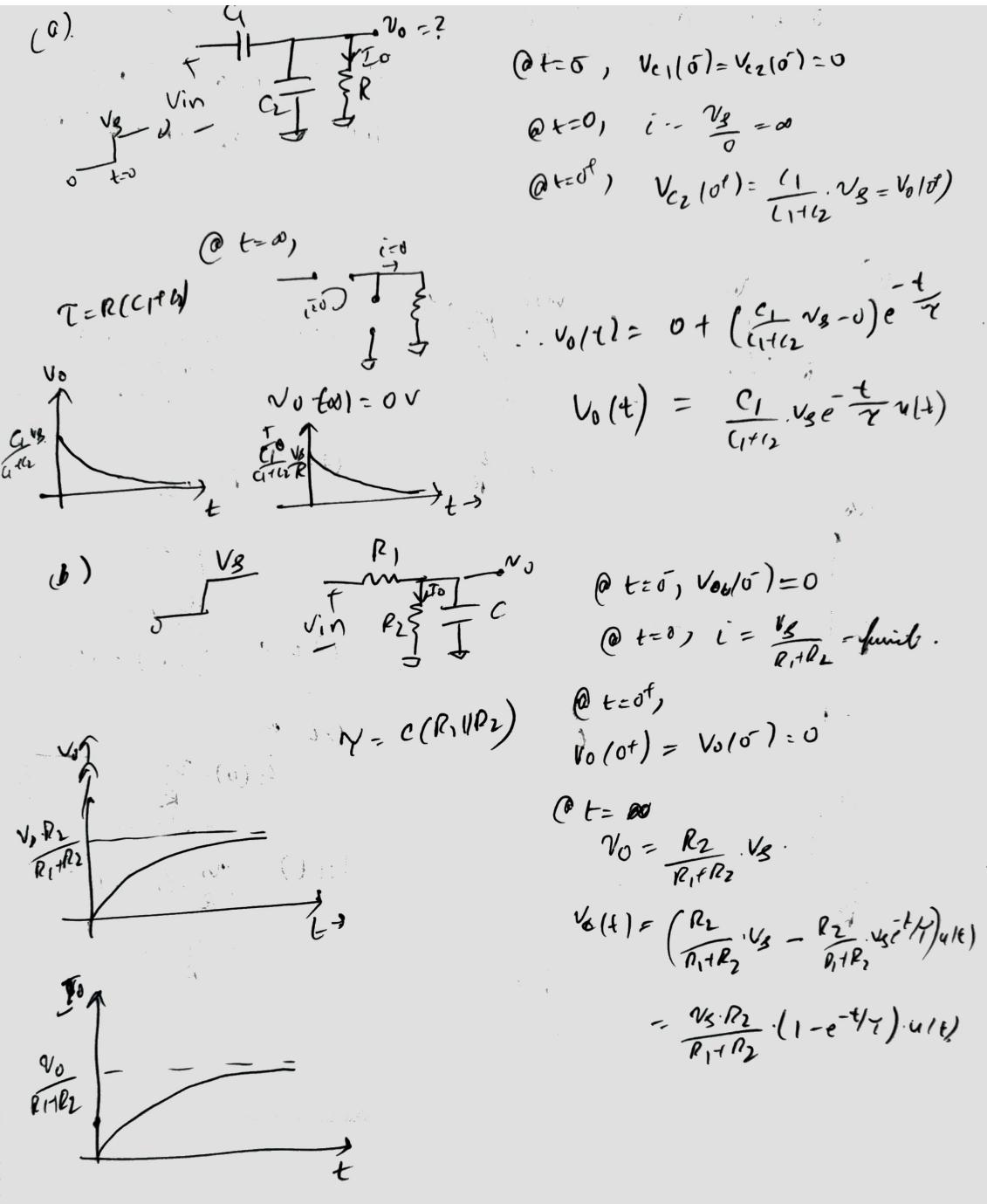


Figure 20: Lec 3: Solution for Question 1

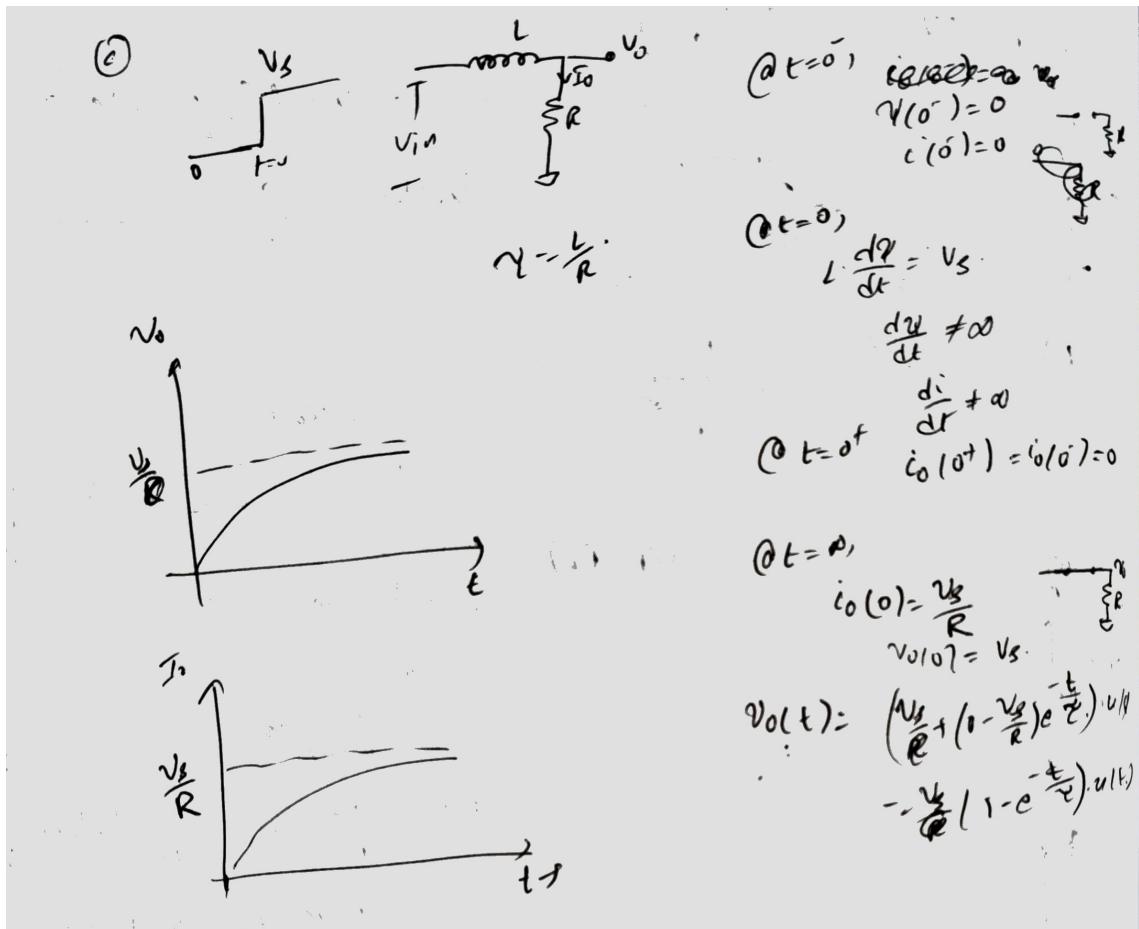


Figure 21: Lec 3: Solution for Question 1

3.2 Pulse Response for RC Circuit with varying Duty Cycle and Time Period

Plot V_{out} vs time (a) $D = 10\%$ (b) $D = 90\%$ (i) $T = 0.1RC$ (ii) $T = 10RC$ where $D = \frac{T_{ON}}{T}$

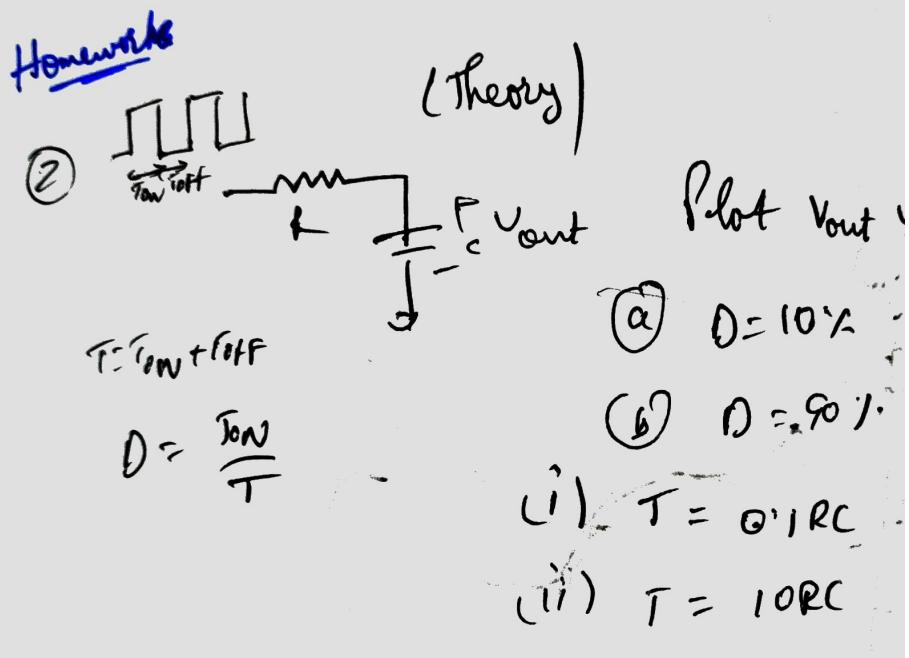
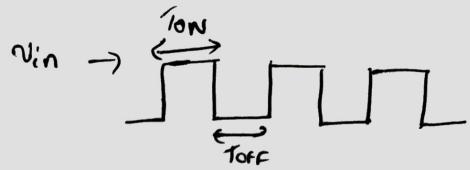
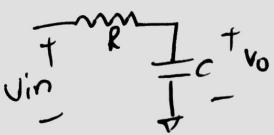


Figure 22: Lecture 3 - Question 2



$$(a) D = 10\%$$

$$(i) T = 0.1RC$$

$$(b) D = 90\%$$

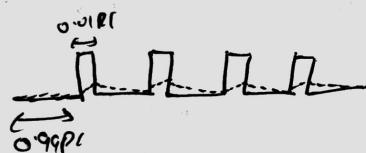
$$(ii) T = 10RC$$

$$(i) T = 0.1RC$$

$$(a) \frac{T_{ON}}{T} = 10\%$$

$$T_{ON} = 0.01RC$$

$$T_{OFF} = 0.99RC$$

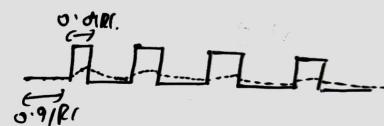


(ii)

$$(b) \frac{T_{ON}}{T} = 90\%$$

$$T_{ON} = 0.9RC$$

$$T_{OFF} = 0.1RC$$



$$(ii) T = 10RC$$

$$(a) \frac{T_{ON}}{T} = 10\%$$

$$T_{ON} = RC$$

$$T_{OFF} = 9RC$$



$$(b) \frac{T_{ON}}{T} = 90\%$$

$$T_{ON} = 9RC$$

$$T_{OFF} = RC$$

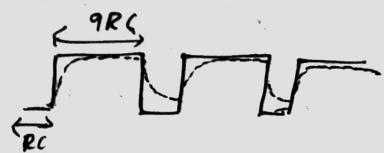


Figure 23: Lec 3: Solution for Question 2

3.3 Bode Plot for a given Transfer Function

Draw Bode plot for $H(s) = \frac{(s-z_1)(s+z_2)}{(s+p_1)(s+p_2)(s+p_3)}$ where (i) $z_2 \ll p_1 \ll p_2 \ll p_3 \ll z_1$ (ii) $p_3 \ll p_2 \ll p_1 \ll z_1 \ll z_2$

Homework

$$\textcircled{3} \quad H(s) = \frac{(s-p_1)(s-p_2)}{(s+p_1)(s+p_2)s^2+p_3 s}$$

(i) $s_2 < p_1 < p_2 < p_3 < s_1$
(ii) $p_3 < p_2 < p_1 < s_1 < s_2$
Draw bode plot:

Figure 24: Lecture 3 - Question 3

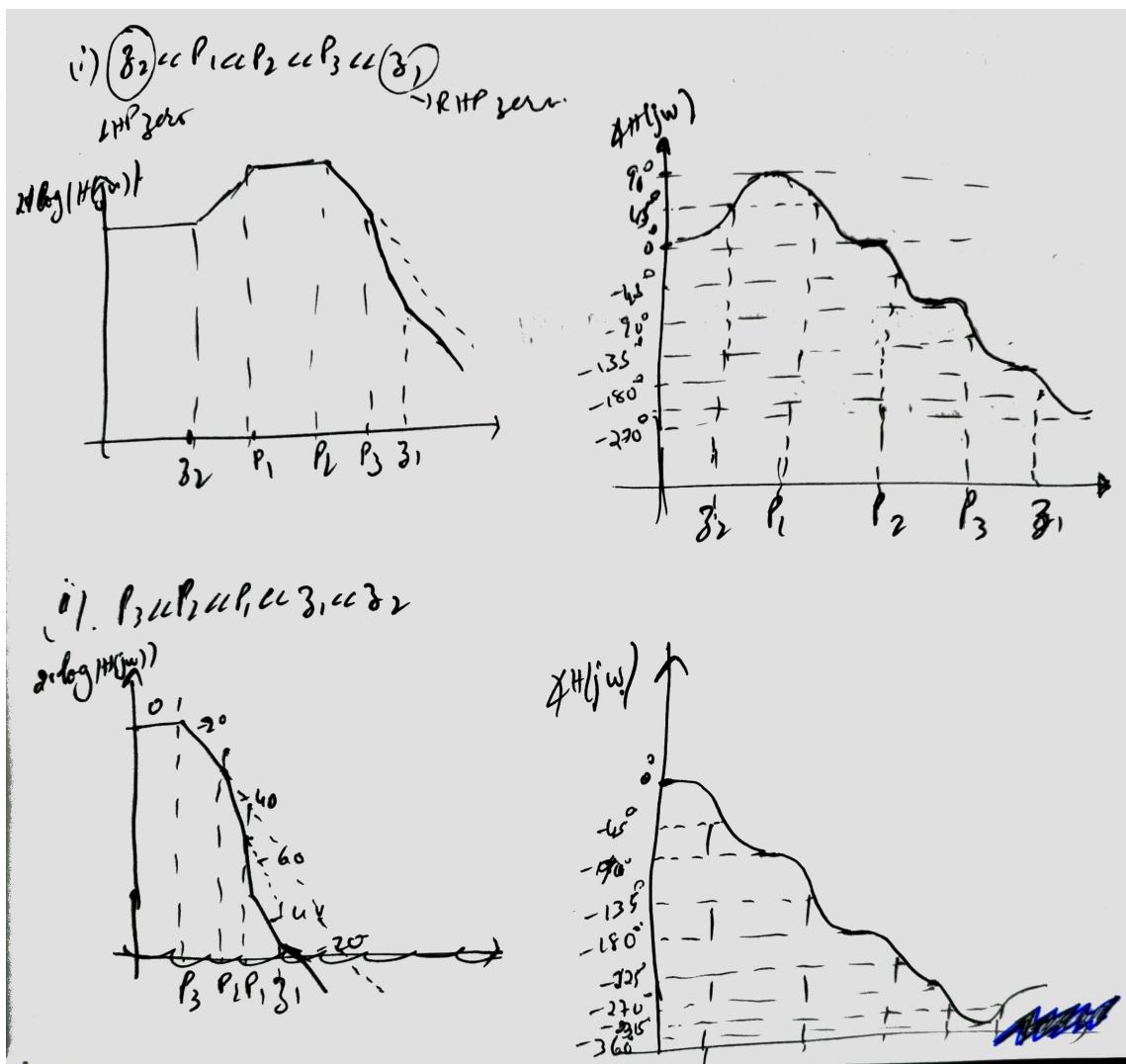


Figure 25: Lec 3: Solution for Question 3

4 Lecture 4

4.1 Non-inverting Schmitt Trigger

Design a non-inverting schmitt trigger using opamp based circuits.

Homework

① Design a non-inverting Schmitt Trigger using op-amp based circuits -

Figure 26: Lecture 4 - Question 1

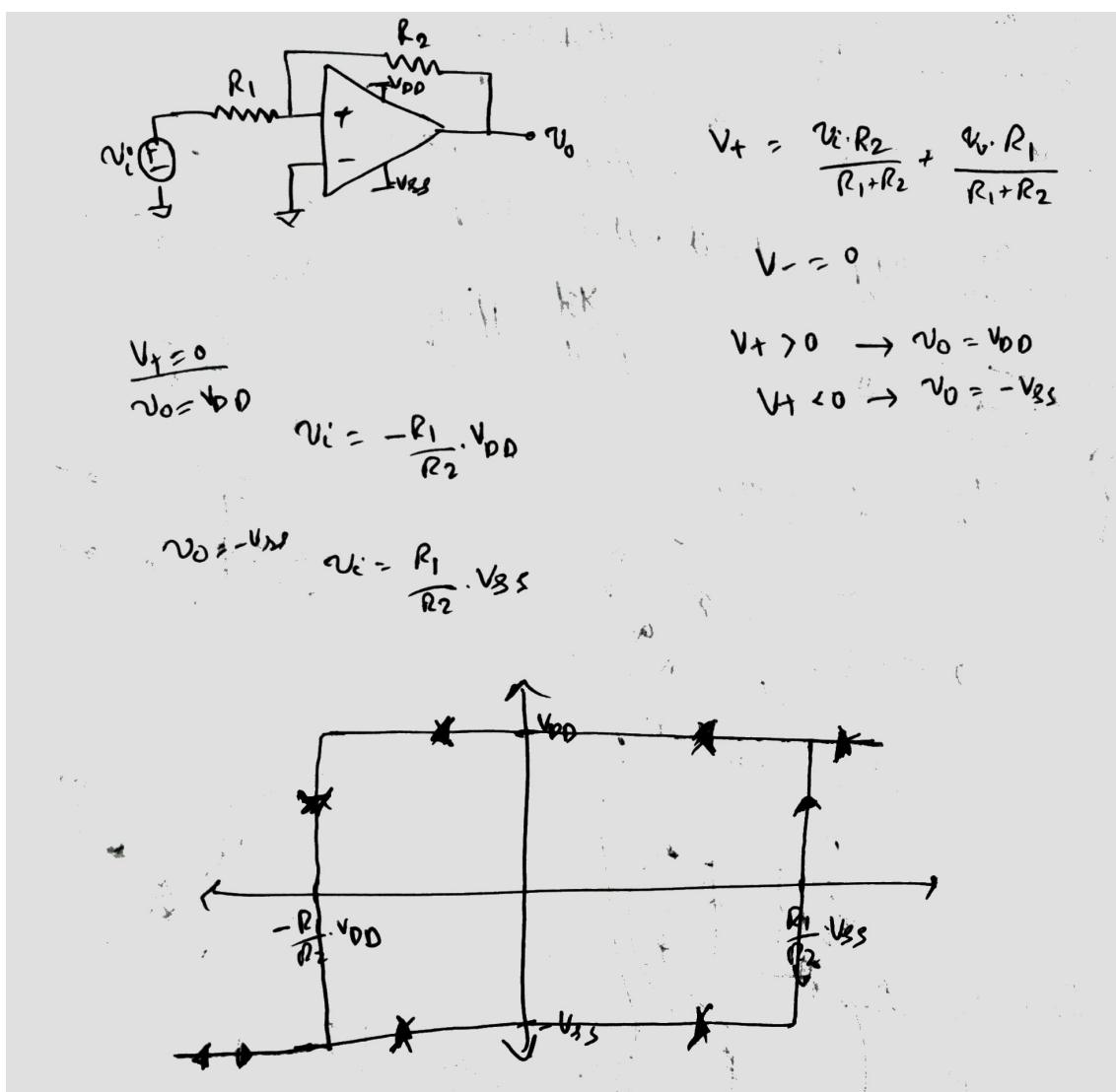


Figure 27: Lec 4: Solution for Question 1

4.2 Expression for Closed loop Unity gain bandwidth

Find the expression for Closed loop Unity gain bandwidth.

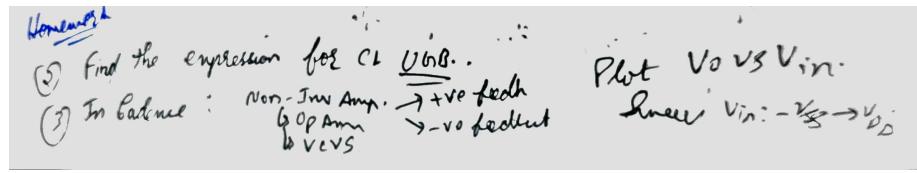


Figure 28: Lecture 4 - Question 2,3

Answer:

Assuming a single pole system, the below image shows the closed loop unity gain bandwidth.

$$V_o(s) = \frac{A}{1 + \frac{s}{(1+A\beta)W_p}} \cdot V_{in}(s)$$

$$W_p = \frac{1}{R_{out} \cdot C}$$

$$A = G_m R_{out}$$

$$\omega_{VnB} \rightarrow \omega @ |V_o/V_i(j\omega)| = 1$$

$$(1+A\beta) \cdot W_p \approx \frac{G_m \beta}{C}$$

$$\Rightarrow \left| \frac{A}{1 + \frac{j\omega}{\frac{G_m \beta}{C}}} \right| = 1$$

$$\Rightarrow A^2 = 1 + \frac{\omega^2}{\frac{G_m^2 \beta^2}{C^2}}$$

$$\Rightarrow A \gg 1$$

$$\Rightarrow A \frac{G_m \beta}{C} = \omega_{VnB}$$

$$\Rightarrow A v_o \cdot W_p = \omega_{VnB}$$

Figure 29: Lec 4: Solution for Question 2

4.3 Non-Inverting Amplifier using VCVS

In cadence, Plot V_o vs V_{in} (Sweep V_{in} from $-V_{ss}$ to V_{DD}) for non-inverting amplifier using Opamp and VCVS for both positive and -ve feedback.

Answer:

A non-inverting amplifier using positive feedback is not possible. Due to positive feedback, the output will saturate to either V_{DD} or V_{SS} for any non-zero input.

For negative feedback, the output voltage is given by

$$V_{out} = V_{in} \cdot \left(1 + \frac{R_2}{R_1}\right).$$

For the non-inverting amplifier we can use either an opamp or a VCVS.

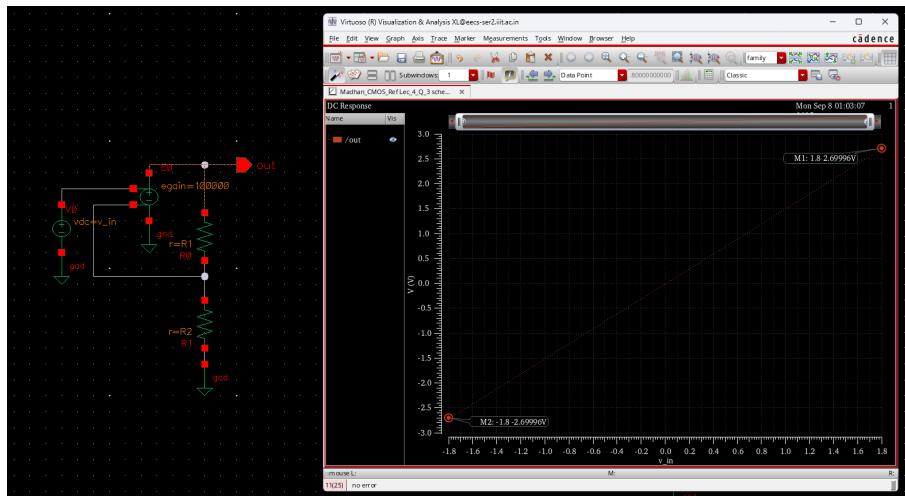


Figure 30: Lecture 4 - Question 3 Solution: Non-inverting Amplifier using VCVS

5 Lecture 5

5.1 Single Pole Opamp with Feedback - Bode Plot

In Cadence, Bode Plot for

1. $A = 100$, check V_x (offset) [DC]
2. $A = 1000$, check V_x (offset) [DC]
3. UGB = 1MHz, Gain = 1000, Design G_m , R_{out} , R_1 , R_2 , C , $V_{Ref} = 0.6V$, $V_{out} = 1.2V$

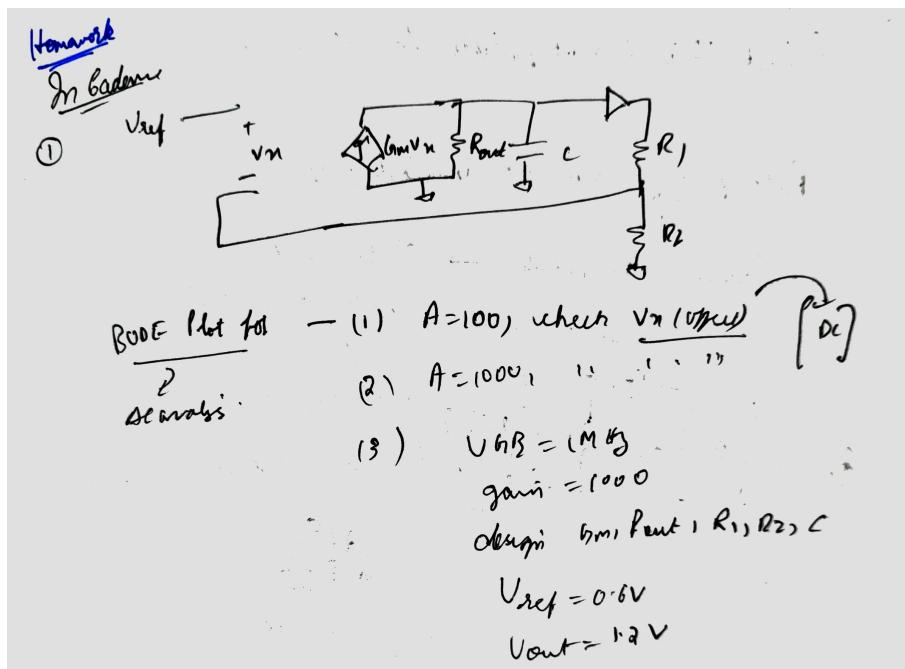


Figure 31: Lecture 5 - Question 1

Answer:

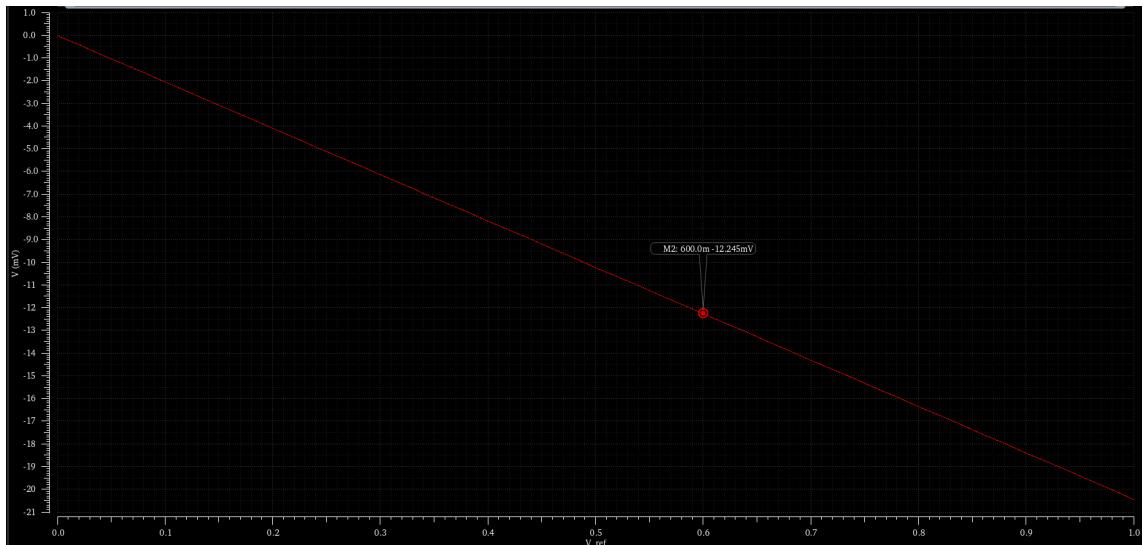


Figure 32: Lec 5: Solution for Question 1_1)

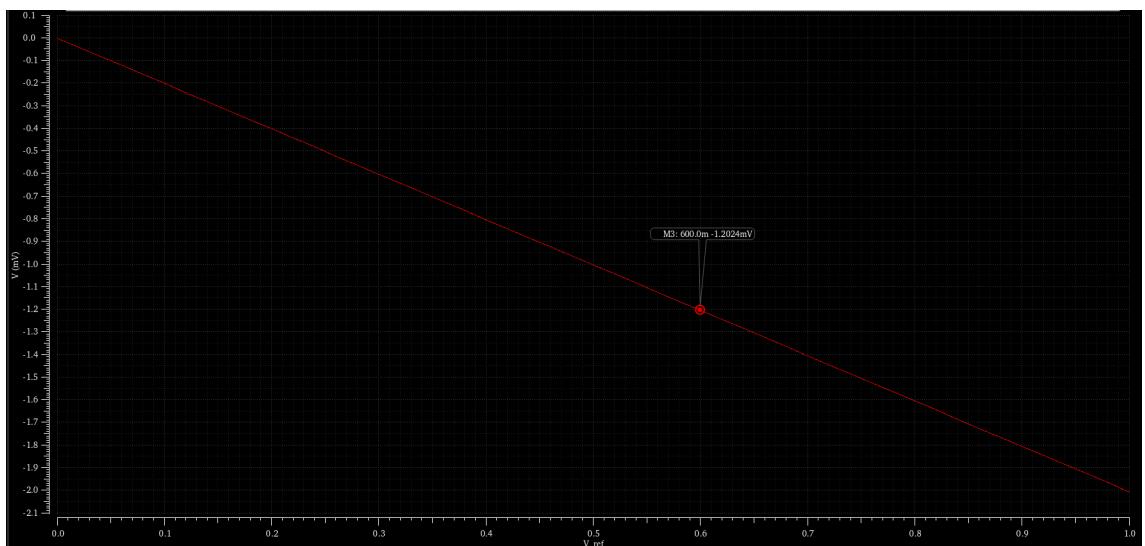


Figure 33: Lec 5: Solution for Question 1_2

5.2 Bode Plot for a 2 Pole System

In cadence, AC analysis. Bode Plot for $\frac{V_{out}}{V_{in}}$

1. $G_{m1} = G_{m2} = 10\mu F$, $R_1 = R_2 = 10M\Omega$, $C_1 = 10fF$, $C_2 = 2fF$
2. add $C_{effective}$ at C_1 and get phase margin = 45°

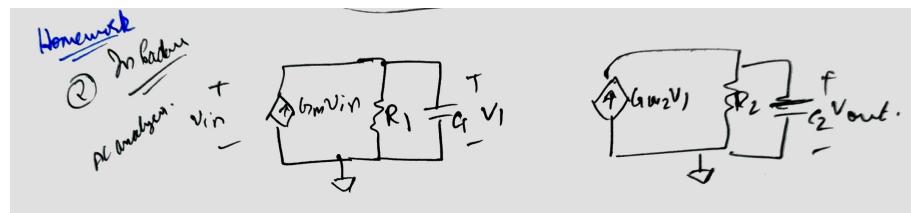


Figure 34: Lecture 5 - Question 2 - circuit

\rightarrow Bode Plot for $\frac{V_{out}}{V_{in}}$

$$\textcircled{1} \quad G_{m1} = G_{m2} = 10\mu S$$

$$R_1 = R_2 = 10 M\Omega$$

$$C_1 = 10 fF \quad C_2 = 2 fF$$

$\textcircled{2}$ Add Cap at $C_1 \rightarrow$ get Phase Margin = 45° .

Figure 35: Lecture 5 - Question 2 - Question

6 Lecture 6

6.1 Miller compensation - Bode Plot

Draw Bode plot for miller compensated circuit.

$$G_{m1} = G_{m2} = 10\mu S, R_1 = R_2 = 10M\Omega, C_1 = 10fF, C_2 = 2fF$$

Find Phase Margin, Unity Gain Bandwidth and DC Gain. (Theory + Cadence) (AC analysis/STB)

Homework

$\textcircled{1}$ Draw bode plot for miller compensated circuit.

$$R_1 = R_2 = 10M\Omega, G_{m1} = G_{m2} = 10\mu S, C_1 = 10fF, C_2 = 2fF$$

find PM, UGB, DC gain

Theory + Cadence (AG/STB)

$$\begin{aligned} \text{DC gain} &= 10^4 \\ wP_1 &= 10M\Omega \\ wP_2 &= 50M\Omega \end{aligned}$$

Figure 36: Lecture 6 - Question 1

6.2 Adding a zero to a system

Simulate in cadence.

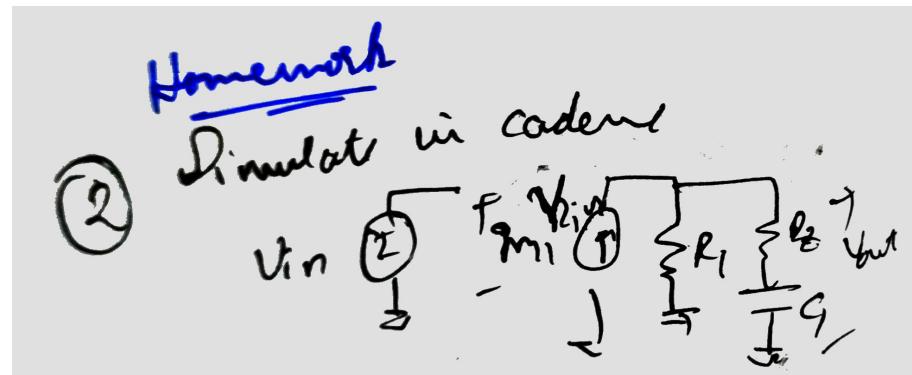


Figure 37: Lecture 6 - Question 2

7 Lecture 7

7.1 Characterization of Resistors in TSMC 180nm

TSMC 18 lib, Simulate all the resistors -40° to 125° (SS, TT, FF) TSMC 18 lib, Simulate all the resistors -40° to 125° (SS, TT, FF)

Resistor	Temperature Coefficient	Type	Process Spread	Linearity	Area
R1	Value	TypeA	Spread1	Linear1	Area1
R2	Value	TypeB	Spread2	Linear2	Area2
R3	Value	TypeC	Spread3	Linear3	Area3

Table 1: Resistor characteristics under different conditions

Homework

Q. ① TSMC - 18 bit
Simulate all the resistors
• $100\Omega \rightarrow 125\Omega \left(\frac{33}{ff} \right)$

Resistor	TC	Type	Process spread	Linearity	Area

Which is better in terms of
 (i) Linearity
 (ii) Temp Coeff. (least)
 (iii) Process spread (least)
 (iv) Area (least)

Q. ② Repeat ① for capacitor.

$I_{ref} = \frac{V_{PTAT}}{R_{PTAT}}, \frac{V_{CTAT}}{R_{CTAT}}, \frac{V_{Ref}}{R_{Ref}}$

$$\frac{V_{PTAT}}{R_{PTAT}} \times R_{Ref} = V_{ref}$$

Q. ③

$V_{PTAT}, V_{CTAT}, V_{Ref}$
 $I_{PTAT}, I_{CTAT}, I_{Ref}$
 $R_{PTAT}, R_{CTAT}, R_{Ref}$

All P & C for 9 values

Figure 38: Lecture 7 - Question 1,2,3

7.2 Characterization of Capacitors in TSMC 180nm

Repeate Question 1 with a capacitor.

Capacitor	Temperature Coefficient	Type	Process Spread	Linearity	Area
C1	Value	TypeA	Spread1	Linear1	Area1
C2	Value	TypeB	Spread2	Linear2	Area2
C3	Value	TypeC	Spread3	Linear3	Area3

Table 2: Resistor characteristics under different conditions

7.3 PTAT, CTAT, Ref - Voltage, Current and Resistance Design Combinations

$V_{PTAT}, V_{CTAT}, V_{Ref}$

$I_{PTAT}, I_{CTAT}, I_{Ref}$

$R_{PTAT}, R_{CTAT}, R_{Ref}$

All P and C for 9 values.

Solution:

Formulas for V_{PTAT} :

$$\begin{aligned}
 V_{PTAT} &= I_{PTAT} \cdot R_{Ref} \\
 V_{PTAT} &= I_{Ref} \cdot R_{PTAT} \\
 V_{PTAT} &= \frac{V_{CTAT}}{R_{CTAT}} \cdot R_{PTAT} \\
 V_{PTAT} &= \frac{V_{PTAT}}{R_{PTAT}} \cdot R_{PTAT} \\
 V_{PTAT} &= (I_{PTAT} + I_{CTAT}) \cdot R_{PTAT} \\
 V_{PTAT} &= V_{Ref} - V_{CTAT} \\
 V_{PTAT} &= I_{CTAT}(\text{small slope}) \cdot R_{PTAT} \text{ (Non-linear)}
 \end{aligned}$$

Formulas for V_{CTAT} :

$$\begin{aligned}
 V_{CTAT} &= I_{CTAT} \cdot R_{Ref} \\
 V_{CTAT} &= I_{Ref} \cdot R_{CTAT} \\
 V_{CTAT} &= \frac{V_{PTAT}}{R_{PTAT}} \cdot R_{CTAT} \\
 V_{CTAT} &= \frac{V_{CTAT}}{R_{CTAT}} \cdot R_{CTAT} \\
 V_{CTAT} &= (I_{PTAT} + I_{CTAT}) \cdot R_{CTAT} \\
 V_{CTAT} &= V_{Ref} - V_{PTAT} \\
 V_{CTAT} &= I_{PTAT}(\text{small slope}) \cdot R_{CTAT} \text{ (Non-linear)}
 \end{aligned}$$

Formulas for V_{Ref} :

$$\begin{aligned}
 V_{Ref} &= I_{Ref} \cdot R_{Ref} \\
 V_{Ref} &= (I_{PTAT} + I_{CTAT}) \cdot R_{Ref} \\
 V_{Ref} &= \frac{V_{PTAT}}{R_{PTAT}} \cdot R_{Ref} \\
 V_{Ref} &= \frac{V_{CTAT}}{R_{CTAT}} \cdot R_{Ref} \\
 V_{Ref} &= \frac{V_{PTAT} + V_{CTAT}}{R_{Ref}} \cdot R_{Ref} \\
 V_{Ref} &= V_{PTAT_1} - V_{PTAT_2} \\
 V_{Ref} &= V_{CTAT_1} - V_{CTAT_2}
 \end{aligned}$$

Formulas for I_{PTAT} , I_{CTAT} , I_{Ref} :

$$\begin{aligned}
 I_{PTAT} &= \frac{V_{PTAT}}{R_{Ref}} \\
 I_{PTAT} &= \frac{I_{PTAT} \cdot R_{PTAT}}{R_{Ref}} \\
 I_{CTAT} &= \frac{V_{CTAT}}{R_{Ref}} \\
 I_{CTAT} &= \frac{I_{CTAT} \cdot R_{CTAT}}{R_{Ref}} \\
 I_{CTAT} &= \frac{V_{CTAT}}{R_{CTAT}} \\
 I_{Ref} &= \frac{V_{Ref}}{R_{Ref}} \\
 I_{Ref} &= \frac{V_{CTAT}}{R_{CTAT}} \\
 I_{Ref} &= \frac{V_{PTAT}}{R_{PTAT}} \\
 I_{Ref} &= \frac{V_{PTAT} + V_{CTAT}}{R_{Ref}} \\
 I_{Ref} &= \frac{I_{CTAT} \cdot R_{Ref}}{R_{CTAT}} \\
 I_{Ref} &= \frac{I_{PTAT} \cdot R_{Ref}}{R_{PTAT}}
 \end{aligned}$$

Formulas for R_{PTAT} , R_{CTAT} , R_{Ref} :

$$\begin{aligned}
 R_{PTAT} &= \frac{V_{PTAT}}{I_{Ref}} \\
 R_{PTAT} &= \frac{V_{Ref} - V_{CTAT}}{I_{Ref}} \\
 R_{PTAT} &= \frac{V_{PTAT} \cdot R_{PTAT}}{V_{CTAT}} \\
 R_{PTAT} &= \frac{V_{PTAT} \cdot R_{CTAT}}{V_{CTAT}} \\
 R_{CTAT} &= \frac{V_{CTAT}}{I_{Ref}} \\
 R_{CTAT} &= \frac{V_{Ref} - V_{PTAT}}{I_{Ref}} \\
 R_{Ref} &= \frac{V_{Ref}}{I_{Ref}} \\
 R_{CTAT} &= \frac{V_{CTAT} \cdot R_{PTAT}}{V_{PTAT}} \\
 R_{CTAT} &= \frac{V_{CTAT} \cdot R_{CTAT}}{V_{CTAT}} \\
 R_{Ref} &= \frac{V_{PTAT}}{I_{PTAT}}
 \end{aligned}$$

8 Lecture 8 - Part of MidSem Project

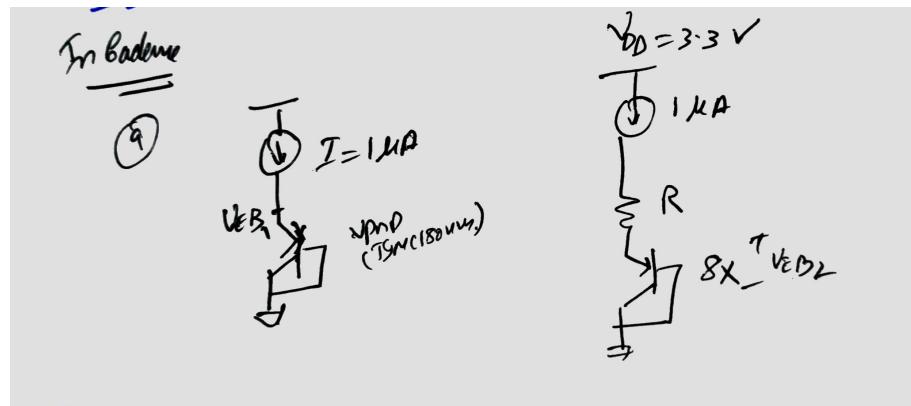


Figure 39: Lecture 8 - Question 1: Circuit

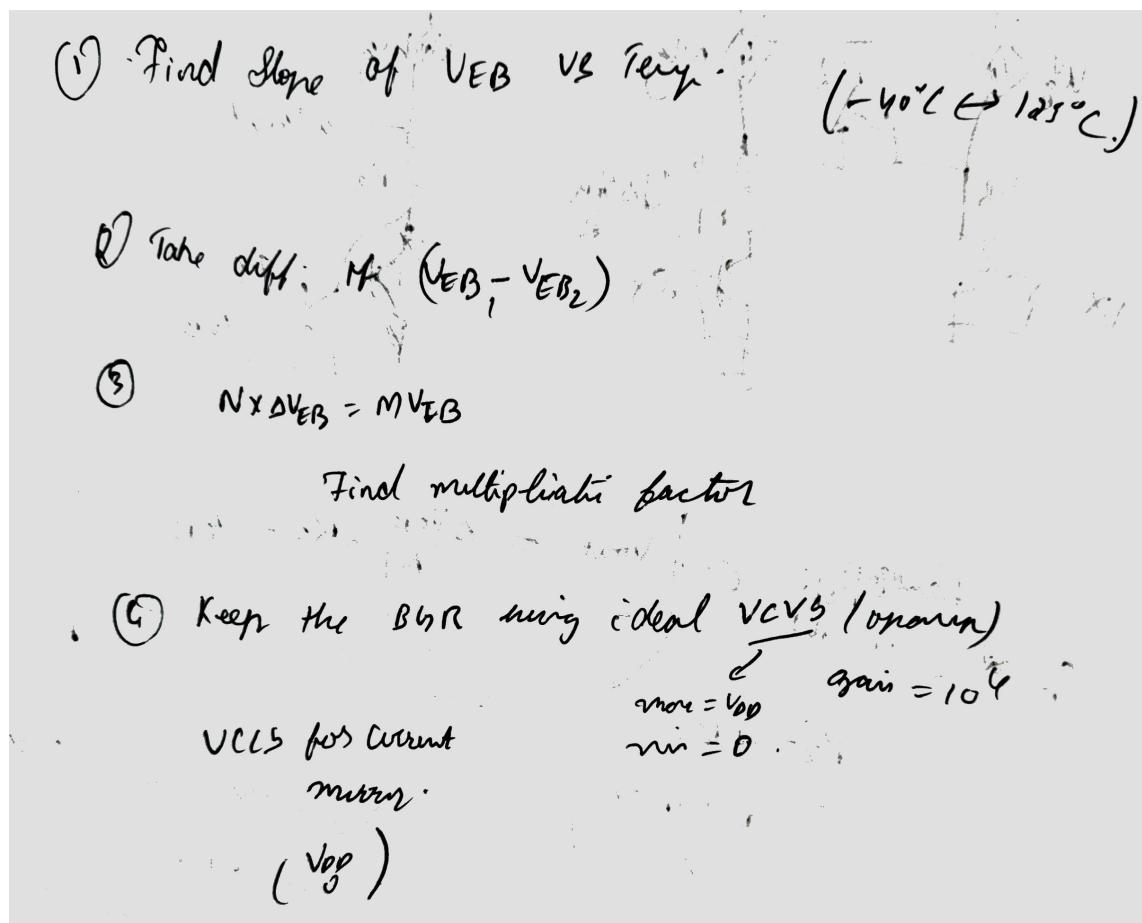


Figure 40: Lec 8: Question 1

- 8.1 Slope of V_{EB} vs Temperature curve of a BJT
- 8.2 Difference of V_{EB} of two BJTs
- 8.3 Find the multiplication factor to equate PTAT and CTAT voltages
- 8.4 Simulate the BGR using ideal VCVS, VCVS for current mirror

9 Lecture 9 - MOSFET

9.1 NMOS I-V characteristics

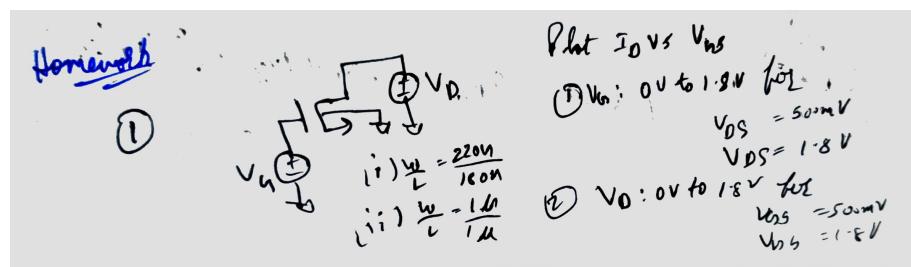


Figure 41: Lecture 9 - Question 1

9.2 PMOS I-V characteristics

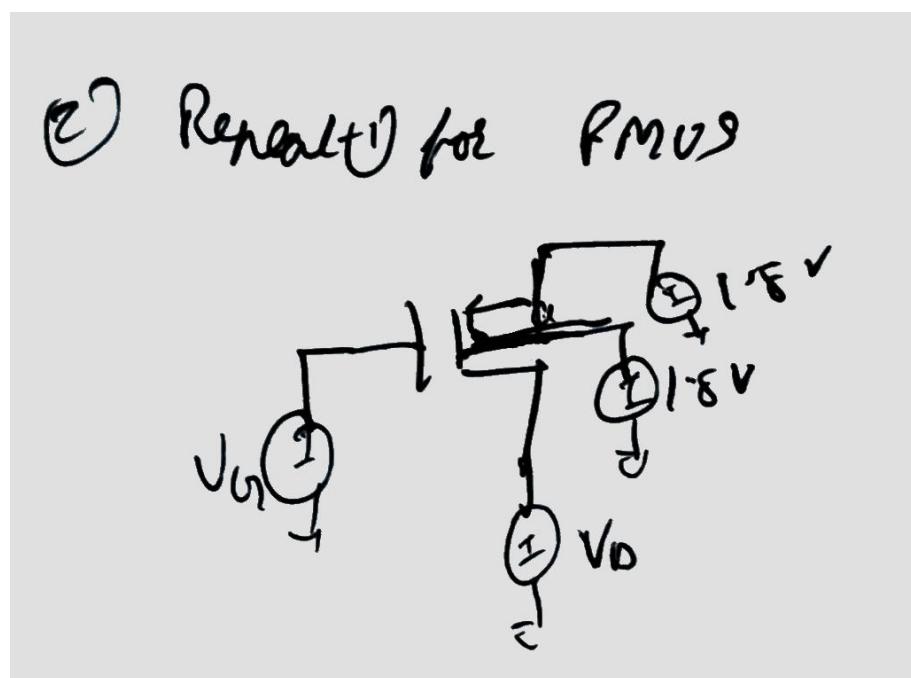


Figure 42: Lecture 9 - Question 2

10 Lecture 10 - Current Mirrors

10.1 Prove that Threshold voltage is linear and CTAT

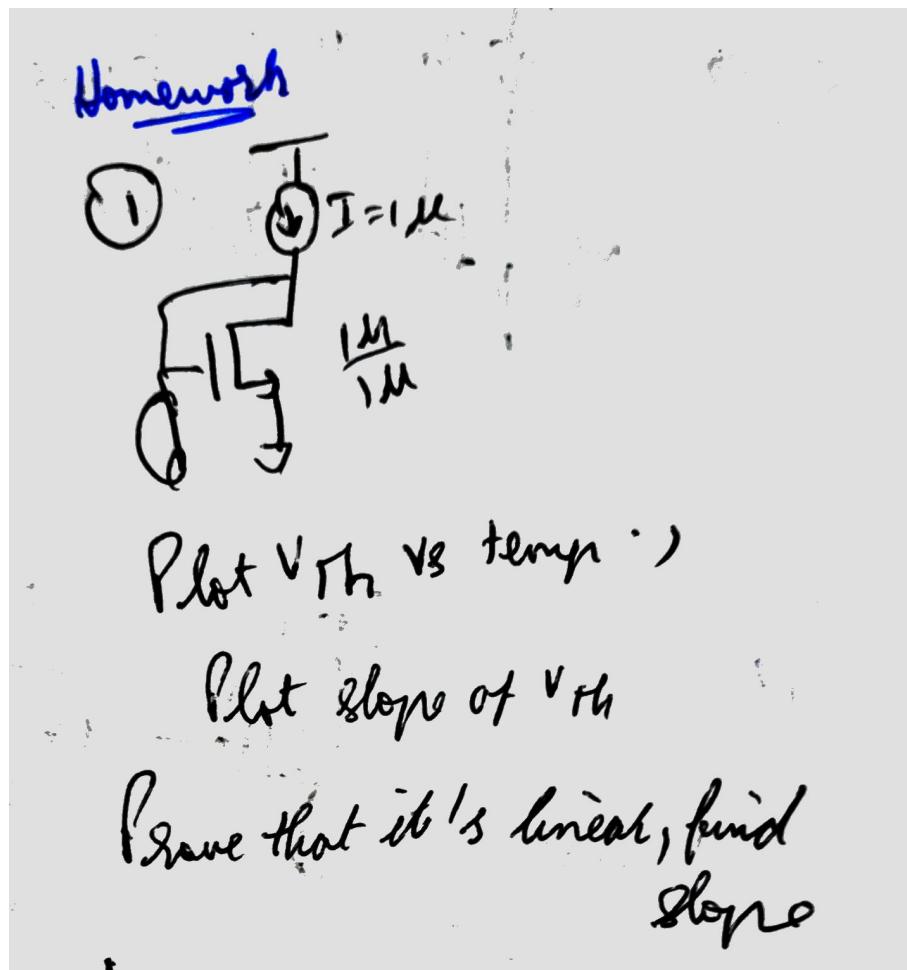


Figure 43: Lecture 10 - Question 1

10.2 Finding the current and size of the mosfet required to make V_{GS} as Reference

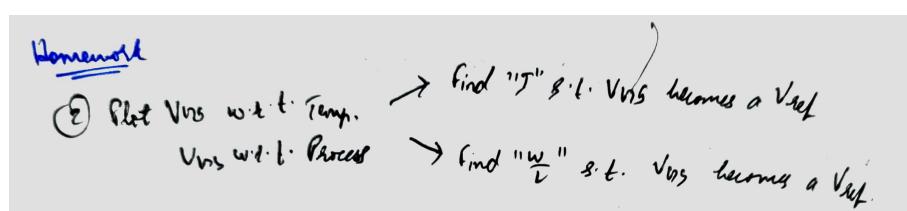


Figure 44: Lecture 10 - Question 2

10.3 PMOS Current Mirror - Simple, Widlar, Low swing, High swing

(3) Draw PMOS simple, widlar, low swing, high V cascode current mirror.

Figure 45: Lecture 10 - Question 3

10.4 Plot V_{EB} w.r.t Process

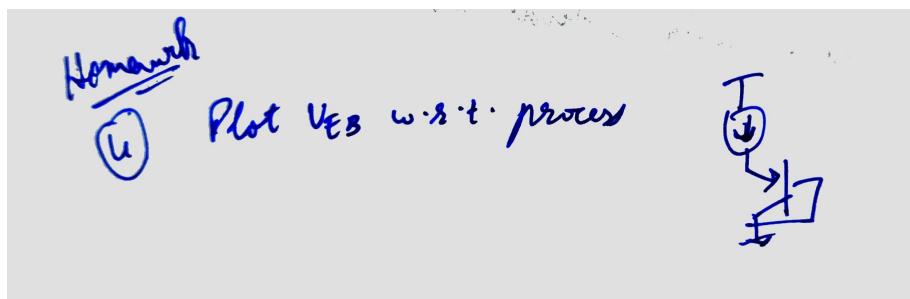


Figure 46: Lecture 10 - Question 4

11 Lecture 11 - Startup Condition, Power Down Signal, Random Mismatch

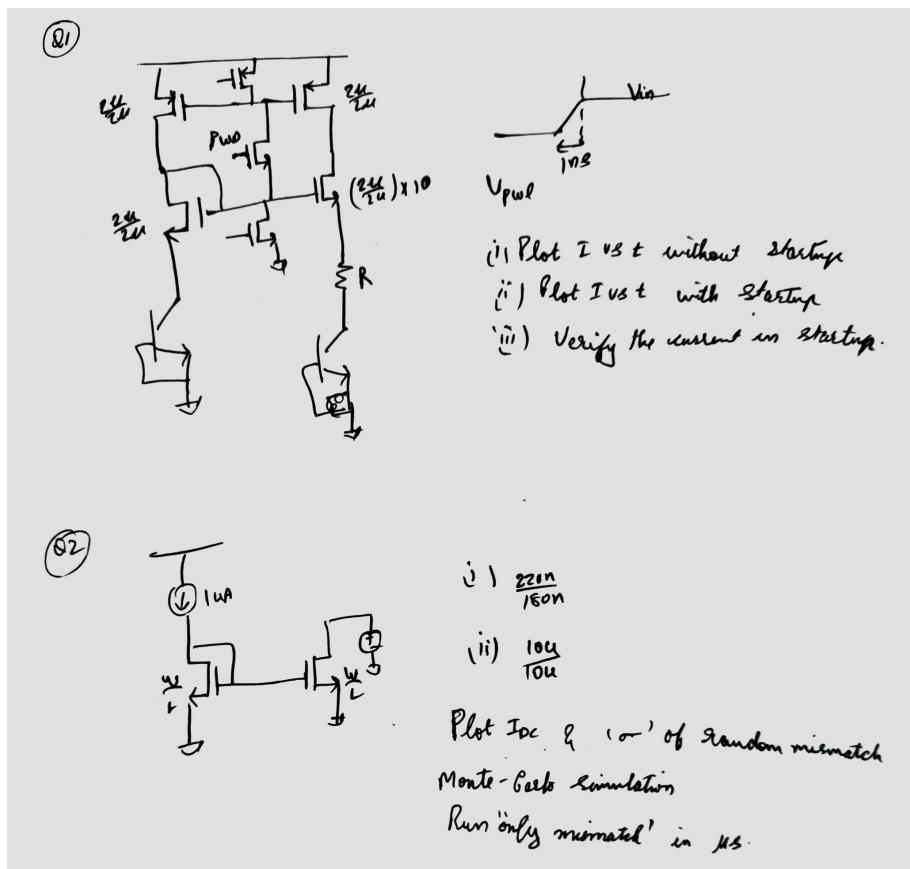


Figure 47: Lecture 11 - Question 1 and Question 2

11.1 Question 1

11.2 Question 2

12 Lecture 12 - Small Signal Analysis of Current Mirrors

12.1 Derivation of small signal equivalent

Homework

Q1 $V_1 = f(I_1, I_2)$
 $V_2 = g(I_1, I_2)$
Derive small signal circuit equivalent.

Figure 48: Lecture 12 - Question 1

12.2 Finding the output resistance of the current mirror

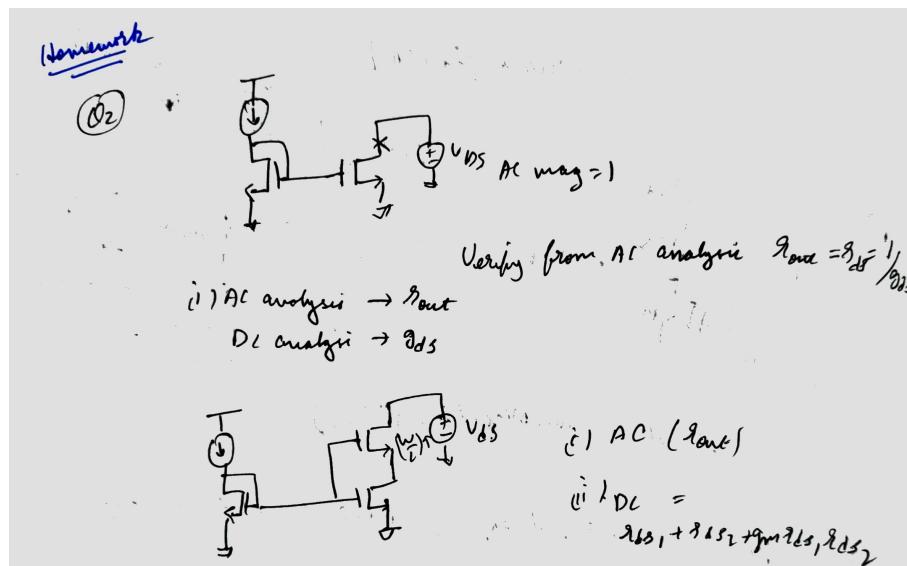


Figure 49: Lecture 12 - Question 2

13 Lecture 13 - Amplifiers

13.1 CS Amplifier with resistive load

Design a CS amplifier with resistive load to get a gain of 20dB, $V_{DD} = 1.8V$, $I_Q = 1\mu A$

14 Lecture 14 - Single Stage Amplifiers

14.1 Drain feedback CS Amplifier

Find conditions for C_1, C_2 to be short circuit in a drain feedback CS amplifier(NMOS based).

14.2 Source feedback CS Amplifier

Find conditions on R_G, C_1, C_2 in source feedback bias CS Amplifier(NMOS based).

14.3 PMOS equivalent of CS Amplifiers

Draw PMOS equivalent of voltage mode CS Amplifier (6), Current Mode CS Amplifier(3), CD and CG amplifier.

15 Lecture 15 - Differential Amplifiers

15.1 ICMR and OCMR of PMOS differential pair

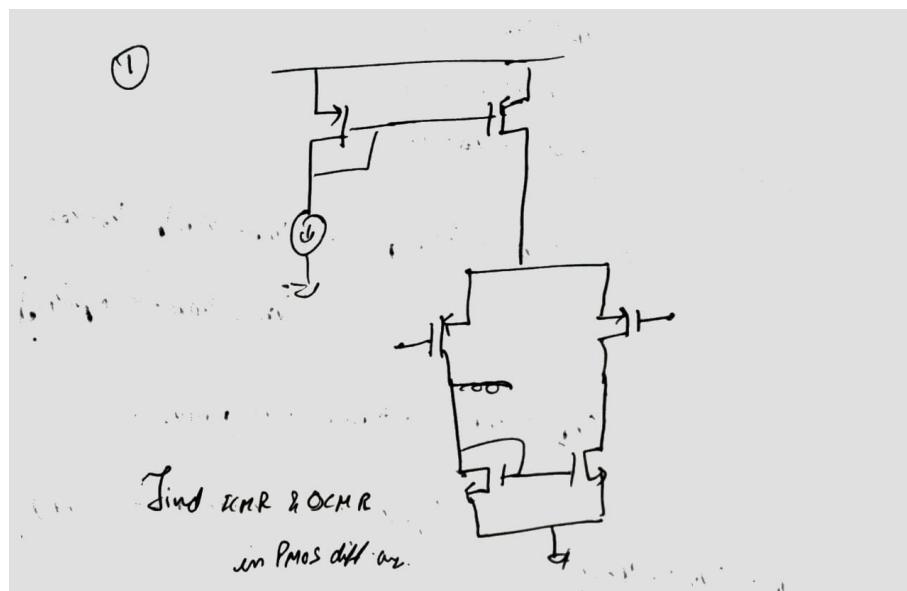


Figure 50: Lecture 15 - Question 1

16 Lecture 16 - Parasitic Capacitances and Poles

16.1 Bode Plot of NMOS CS Amp with capacitive load

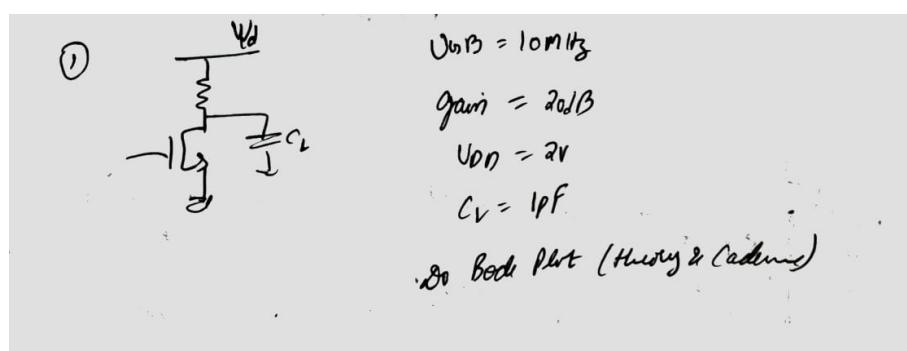


Figure 51: Lecture 16 - Question 1

17 Lecture 17