

# CMOS References and Regulators: Homework

Chamarthy Madhan Sai Krishna  
2023102030

November 11, 2025

## Contents

<b>1 Lecture 1</b>	<b>2</b>
1.1 Proving Resistance: Current is proportional to Voltage . . . . .	2
1.2 Capacitance Amplifier using Controlled Sources . . . . .	4
1.3 Inductance Amplifier using Controlled Sources . . . . .	5
1.4 Resistance Amplifier using Controlled Sources . . . . .	6
<b>2 Lecture 2</b>	<b>8</b>
2.1 Output Resistance . . . . .	8
2.2 Step Response for RC Circuit . . . . .	9
<b>3 Lecture 3</b>	<b>13</b>
3.1 Step Response for passive RLC circuit Combinations . . . . .	13
3.2 Pulse Response for RC Circuit with varying Duty Cycle and Time Period . . . . .	15
3.3 Bode Plot for a given Transfer Function . . . . .	17
<b>4 Lecture 4</b>	<b>18</b>
4.1 Non-inverting Schmitt Trigger . . . . .	18
4.2 Expression for Closed loop Unity gain bandwidth . . . . .	19
4.3 Non-Inverting Amplifier using VCVS . . . . .	20
<b>5 Lecture 5</b>	<b>21</b>
5.1 Single Pole Opamp with Feedback - Bode Plot . . . . .	21
5.2 Bode Plot for a 2 Pole System . . . . .	24
<b>6 Lecture 6</b>	<b>25</b>
6.1 Miller compensation - Bode Plot . . . . .	25
6.2 Adding a zero to a system . . . . .	25
<b>7 Lecture 7</b>	<b>25</b>
7.1 Characterization of Resistors in TSMC 180nm . . . . .	25
7.2 Characterization of Capacitors in TSMC 180nm . . . . .	27
7.3 PTAT, CTAT, Ref - Voltage, Current and Resistance Design Combinations . . . . .	27
<b>8 Lecture 8 - Part of MidSem Project</b>	<b>29</b>
8.1 Slope of $V_{EB}$ vs Temperature curve of a BJT . . . . .	30
8.2 Difference of $V_{EB}$ of two BJTs . . . . .	31
8.3 Find the multiplication factor to equate PTAT and CTAT voltages . . . . .	31
8.4 Simulate the BGR using ideal VCVS, VCVS for current mirror . . . . .	32
<b>9 Lecture 9 - MOSFET</b>	<b>32</b>
9.1 NMOS I-V characteristics . . . . .	32
9.2 PMOS I-V characteristics . . . . .	36

<b>10 Lecture 10 - Current Mirrors</b>	<b>41</b>
10.1 Prove that Threshold voltage is linear and CTAT . . . . .	41
10.2 Finding the current and sizing of the mosfet required to make $V_{GS}$ as Reference . . . . .	43
10.3 PMOS Current Mirror - Simple, Widlar, Low swing, High swing . . . . .	45
10.4 Plot $V_{EB}$ w.r.t Process . . . . .	47
<b>11 Lecture 11 - Startup Condition, Power Down Signal, Random Mismatch</b>	<b>48</b>
11.1 Question 1 . . . . .	48
11.2 Question 2 . . . . .	51
<b>12 Lecture 12 - Small Signal Analysis of Current Mirrors</b>	<b>52</b>
12.1 Derivation of small signal equivalent . . . . .	52
12.2 Finding the output resistance of the current mirror . . . . .	53
<b>13 Lecture 13 - Amplifiers</b>	<b>54</b>
13.1 CS Amplifier with resistive load . . . . .	54
<b>14 Lecture 14 - Single Stage Amplifiers</b>	<b>56</b>
14.1 Drain feedback CS Amplifier . . . . .	56
14.2 Source feedback CS Amplifier . . . . .	56
14.3 PMOS equivalent of CS Amplifiers . . . . .	57
<b>15 Lecture 15 - Differential Amplifiers</b>	<b>59</b>
15.1 ICMR and OCMR of PMOS differential pair . . . . .	59
<b>16 Lecture 16 - Parasitic Capacitances and Poles</b>	<b>61</b>
16.1 Bode Plot of NMOS CS Amp with capacitive load . . . . .	61
<b>17 Lecture 17</b>	<b>62</b>

## 1 Lecture 1

### 1.1 Proving Resistance: Current is proportional to Voltage

Do the 'DC Analysis' for the following circuits. Plot V vs I & write expression for the slope. Prove that its a resistance.

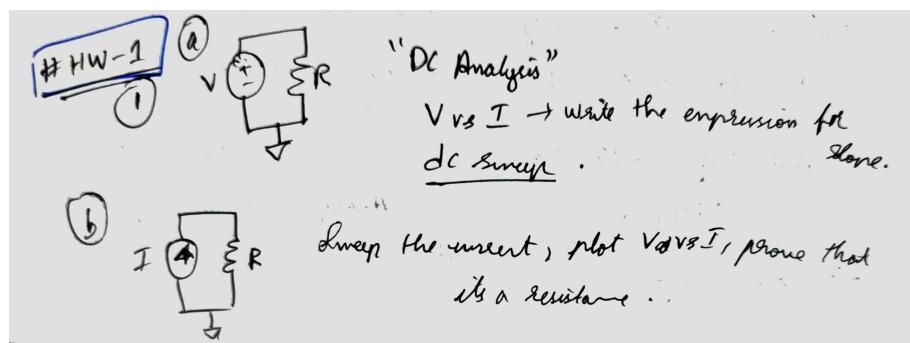


Figure 1: Lecture 1 - Question 1 - (a) and (b)

*Answer:*

Left graph shows the I - V characteristics of the device. Clearly,  $I \propto V$ . The right graph shows the expression for the slope.

Plot for (a) : Using a Voltage source

Plot for (b) : Using a Current source

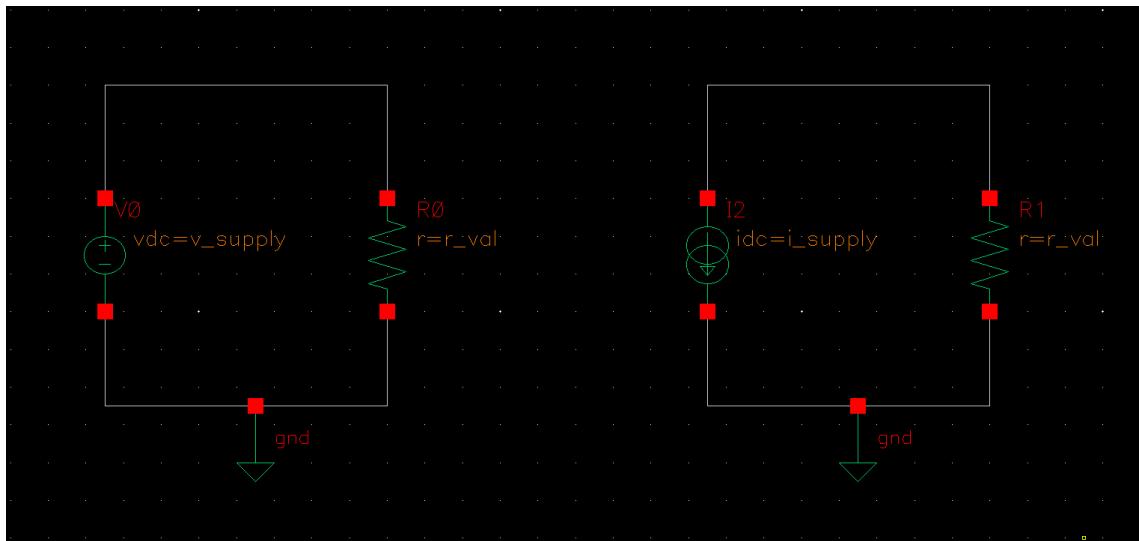


Figure 2: Lec 1: Q1: Testbench for (a) and (b)

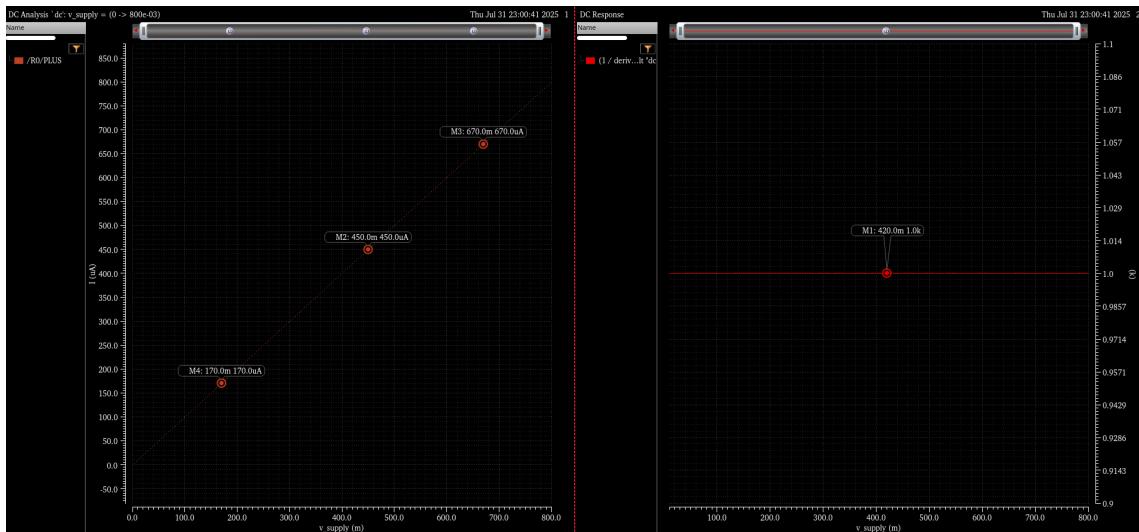


Figure 3: Lec 1: Q1: Plot for (a)

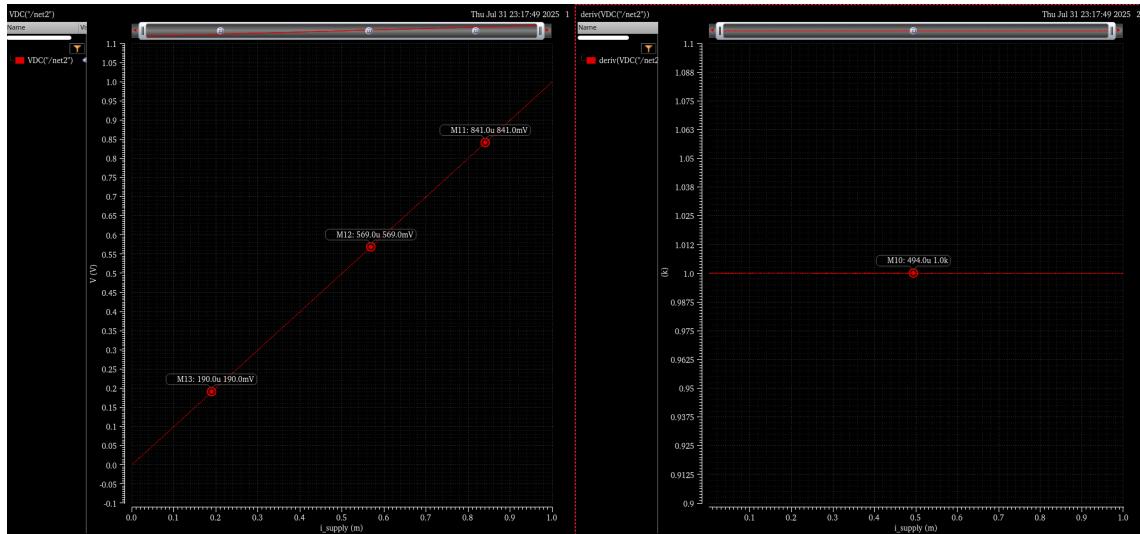


Figure 4: Lec 1: Q1: Plot for (b)

## 1.2 Capacitance Amplifier using Controlled Sources

Design a capacitance amplifier using controlled sources.

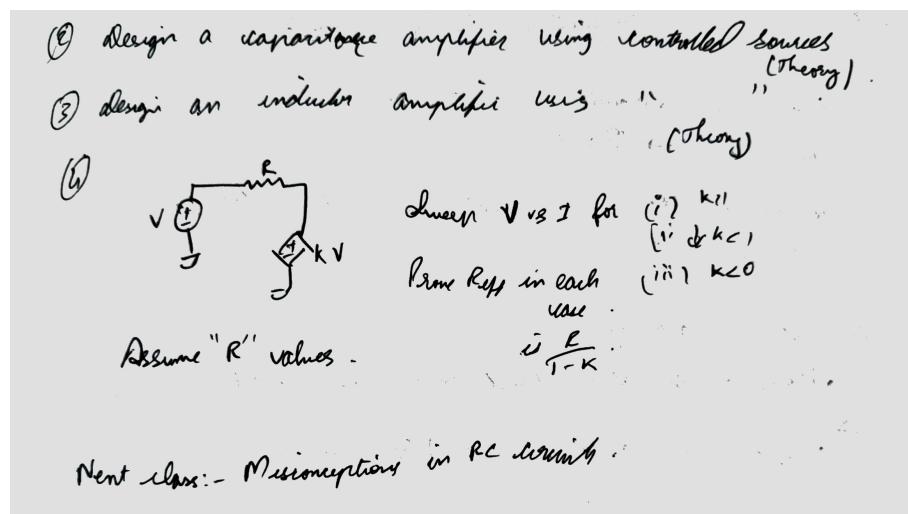
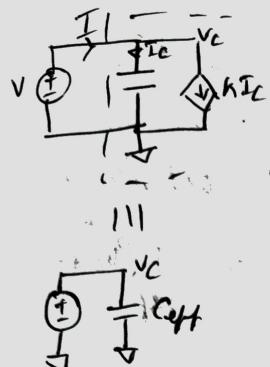


Figure 5: Lecture 1 - Question 2, 3, 4

Answer:

## Capacitance Amplifier using controlled sources

CCCS



$$I = I_{C1} + k \cdot I_c$$

$$= I_{C1}(1+k)$$

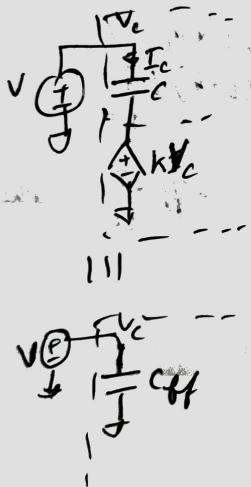
$$I = C \cdot \frac{dV_c}{dt} \cdot (1+k)$$

$$I = C(1+k) \cdot \frac{dV_c}{dt}$$

$$I \propto \frac{dV_c}{dt} \rightarrow \text{Capacitance.}$$

$$I = C_{eff} \cdot \frac{dV_c}{dt} \quad \text{where } C_{eff} = C(1+k)$$

V<sub>CVS</sub>



$$I_c = C \cdot \frac{d}{dt} (V_c - kV_c)$$

$$I_c = C \frac{dV_c}{dt} \cdot (1-k)$$

$$I_c \propto \frac{dV_c}{dt} \Rightarrow C_{eff} = (1-k) \cdot C$$

Figure 6: Lecture 1 - Question 2 - Solution

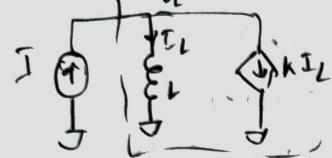
### 1.3 Inductance Amplifier using Controlled Sources

Design a inductance amplifier using controlled sources.

Answer:

Inductance Amplifier using controlled sources

CCS



$$I = I_L + kI_L$$

$$= I_L(1+k)$$

$$I = L \frac{dI}{dt} \cdot (1+k)$$

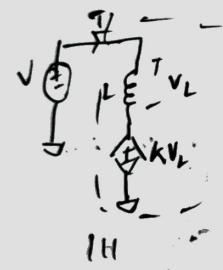
$$V_L = L \frac{dI_L}{dt}$$



$$I = \frac{1}{L_{eff}} \int V_L dt$$

$$L_{eff} = \frac{L}{1+k}$$

JCVS



$$V = V_L + kV_L$$

$$= (1+k) L \frac{dI}{dt}$$

$$V = L_{eff} \frac{dI}{dt} \quad \text{where } L_{eff} = L(1+k)$$

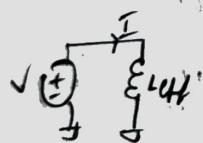
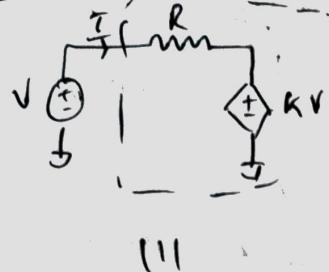


Figure 7: Lecture 1 - Question 3 - Solution

#### 1.4 Resistance Amplifier using Controlled Sources

Sweep V vs I for (i)  $k > 1$  (ii)  $0 < k < 1$  (iii)  $K < 0$  Prove  $R_{eff}$  in each case is  $\frac{R}{1-k}$ .  
Answer:

Resistance Amplified using controlled sources



$$(V - kV) = I \cdot R$$

$$V(1-k) = I \cdot R$$

$$V = \frac{I \cdot R}{1-k}$$

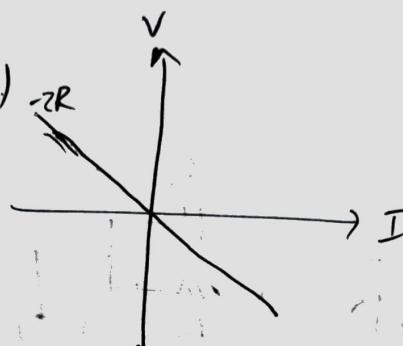
$$V = I \cdot R_{eff}$$



$$\text{where } R_{eff} = \frac{R}{1-k}$$

(i)  $k > 1 \Rightarrow R_{eff} < 0$   
(Neg. resistance)

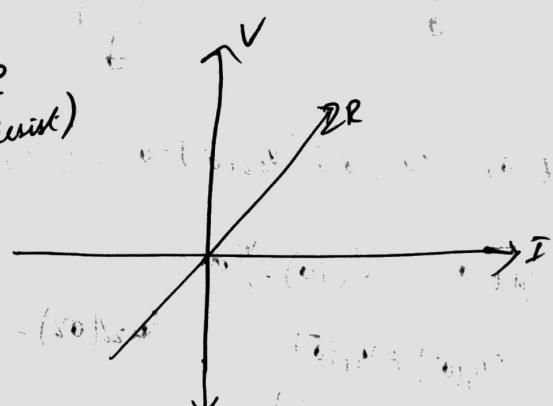
$$k=1.5 \Rightarrow R_{eff} = -2R$$



(ii)  $0 < k < 1 \Rightarrow R_{eff} < \infty$

$$k=0.5 \rightarrow R_{eff} = 2R$$

(Amplified resist)



(iii)  $k < 0 \Rightarrow R_{eff} < R$

$$k=-0.5 \rightarrow R_{eff} = \frac{R}{1.5} = \frac{2R}{3}$$

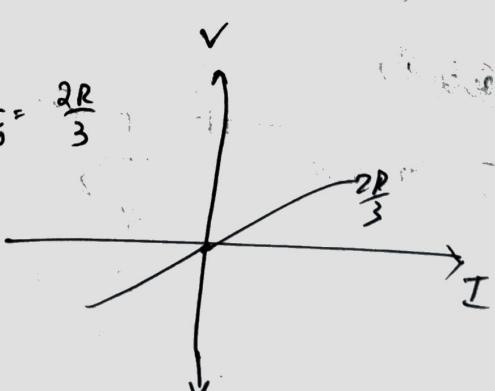


Figure 8: Lecture 1 - Question 4 - Solution

## 2 Lecture 2

### 2.1 Output Resistance

find the effective output resistance at  $V_{out}$  i.e.,  $R_{out} = ?$

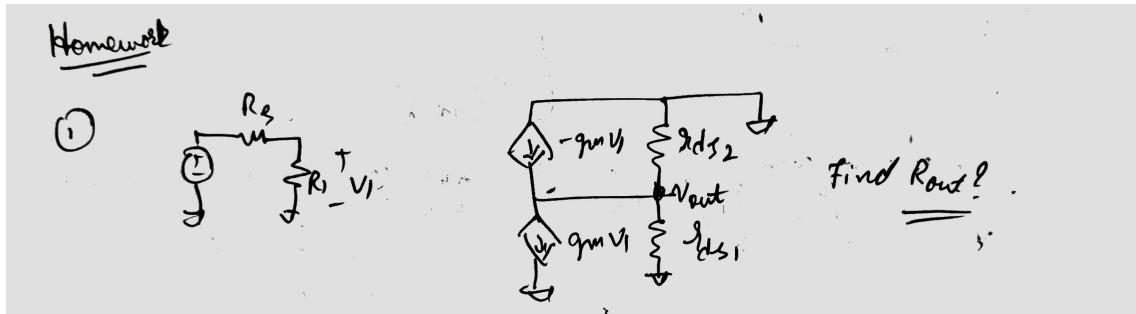


Figure 9: Lec 2: Question 1

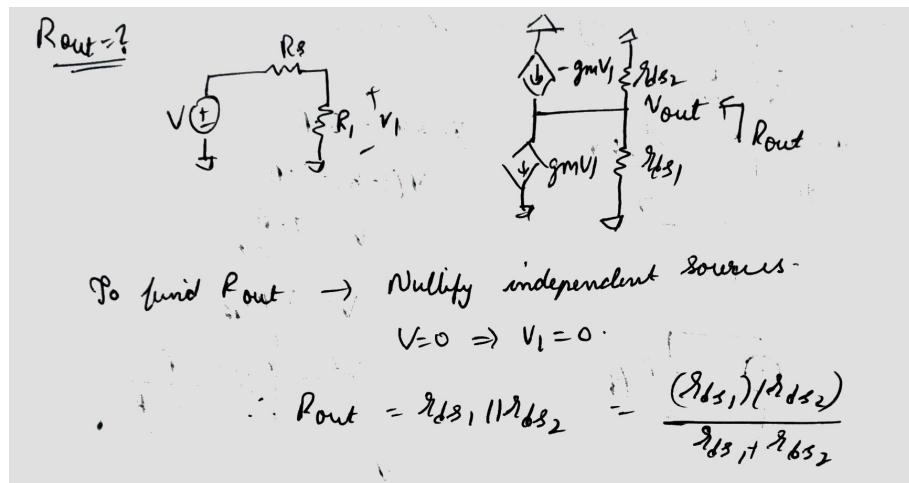


Figure 10: Lecture 2 - Question 1 - Solution

*Answer:*

When we nullify the  $V_1$ , the vccs vanish and the effective output resistance at  $v_{out}$  node is  $R_{out} = r_{ds_1} \parallel r_{ds_2}$ .

Proved this using the plot with values.

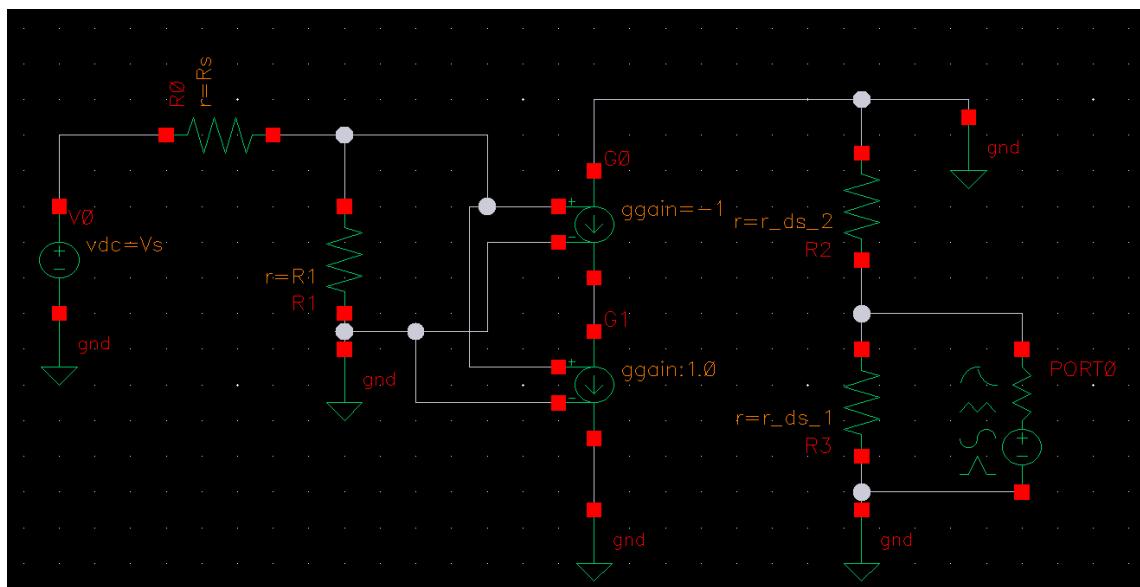


Figure 11: Lec 2: Q1: Testbench

## 2.2 Step Response for RC Circuit

Plot  $V_{out}$  vs time in Cadence. Prove Theory.

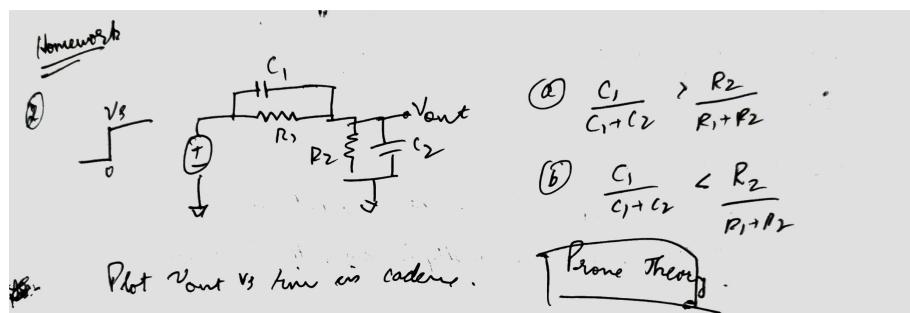
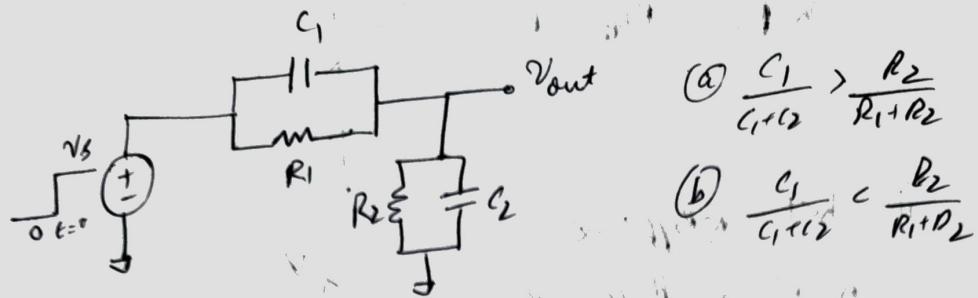


Figure 12: Lecture 2 - Question 2

*Answer:*  
Copy this from the notes



$$(a) \frac{C_1}{C_1+C_2} > \frac{R_2}{R_1+R_2}$$

$$(b) \frac{C_1}{C_1+C_2} < \frac{R_2}{R_1+R_2}$$

$$@ t=0, \quad v_{c_1}(0^+) = v_{c_2}(0^-) = 0 \Rightarrow v_o(0^+) = 0$$

$$@ t=0, \quad i_c(0) = \frac{v_s}{R_1}$$

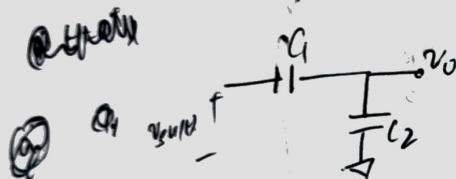
$$v_{c_1}(0^+) \neq v_{c_1}(0^-)$$

$$v_{c_2}(0^-) \neq v_{c_2}(0^+)$$

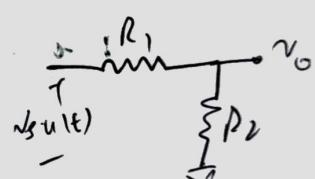
$$v_{c_2}(0^+) =$$

$$\begin{aligned} v_o &= (R_{in})([c_1]) \\ &\sim (R_1 R_2)(C_1 C_2) \end{aligned}$$

@ t=0<sup>th</sup>



(b)



$$v_o(0^+) = \frac{C_1}{C_1+C_2} \cdot v_s$$

$$v_o(0^+) = \frac{R_2}{R_1+R_2} \cdot v_s$$

Figure 13: Lec 2: Solution for Question 2

$$(a) V_o(0^+) = \frac{R_2}{R_1+R_2} \cdot V_s$$

$$V_o(\infty) = \frac{C_1}{C_1+C_2} \cdot V_s$$

$$V_o(t) = \left\{ \frac{V_s C_1}{C_1+C_2} + \left( \frac{V_s R_2}{R_1+R_2} - \frac{V_s C_1}{C_1+C_2} \right) e^{-\frac{t}{\tau}} \right\} u(t)$$

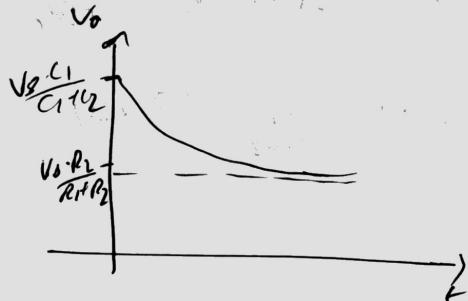
$$\text{Given: } C_1 = 2n$$

$$C_2 = 1n$$

$$R_1 = 100\Omega$$

$$R_2 = 100\Omega$$

$$\gamma = 150nS$$



$$\begin{aligned} V_o(t) &= 0.5 + (0.66 - 0.5)e^{-\frac{t}{\tau}} \\ V_o(\infty) &= 0.5 + 0.37 \times 0.16 \\ &= 56 \text{ mV} \end{aligned}$$

$$(b) V_o(0^+) = \frac{C_1}{C_1+C_2} \cdot V_s \quad V_o(\infty) = \frac{R_2}{R_1+R_2} \cdot V_s$$

$$V_o(t) = \left\{ \frac{V_s R_2}{R_1+R_2} + \left( \frac{V_s C_1}{C_1+C_2} - \frac{V_s R_2}{R_1+R_2} \right) e^{-\frac{t}{\tau}} \right\} u(t)$$

Figure 14: Lec 2: Solution for Question 2

$$\text{Given: } C_1 = 1n$$

$$C_2 = 1n$$

$$R_1 = 100\Omega$$

$$R_2 = 100\Omega$$

$$\gamma = 133nS$$

$$V_o(t) = 0.67 + (0.5 - 0.67)0.37$$

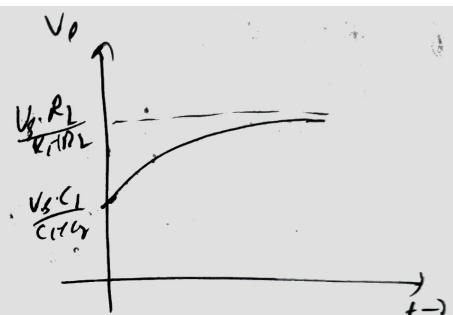


Figure 15: Lec 2: Solution for Question 2

Proved this using theory and from the simulations by finding the output voltage after 1 time constant.

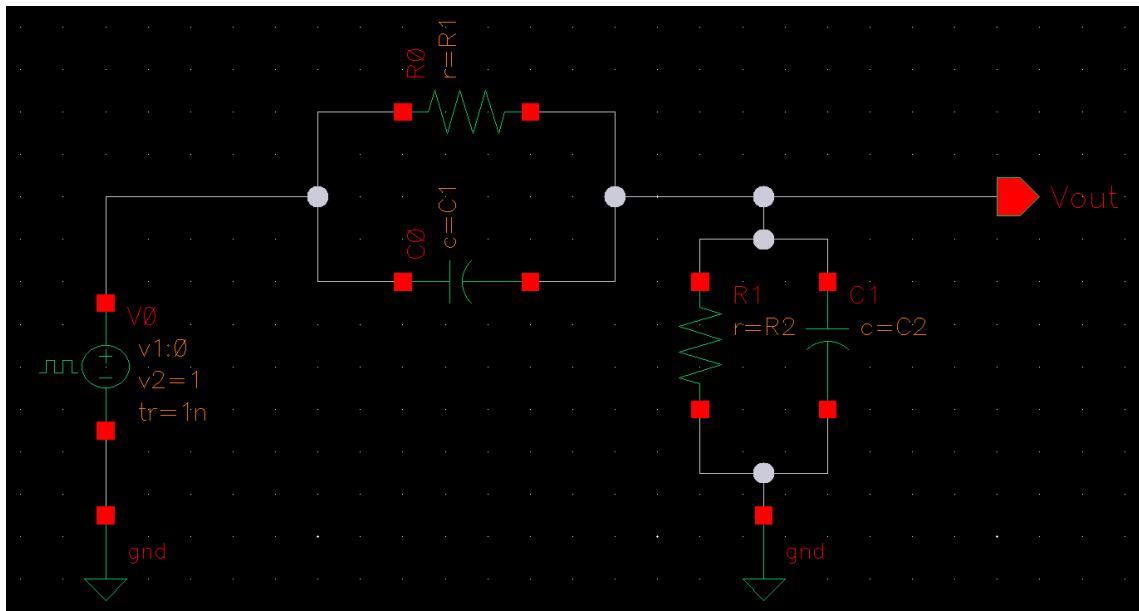


Figure 16: Lec 2: question 2 Testbench

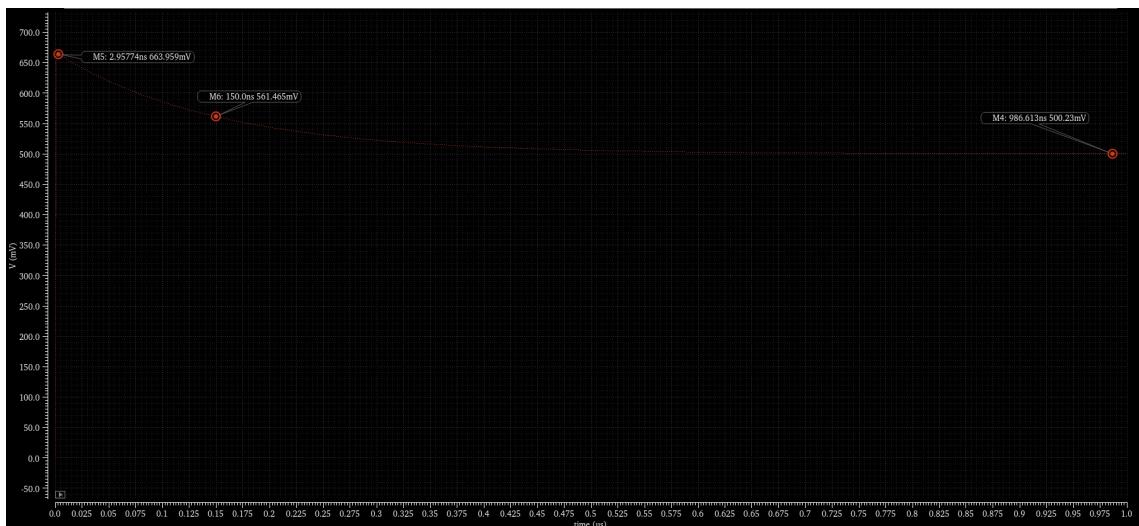


Figure 17: Lec 2: Q2: Soln - Part (a)

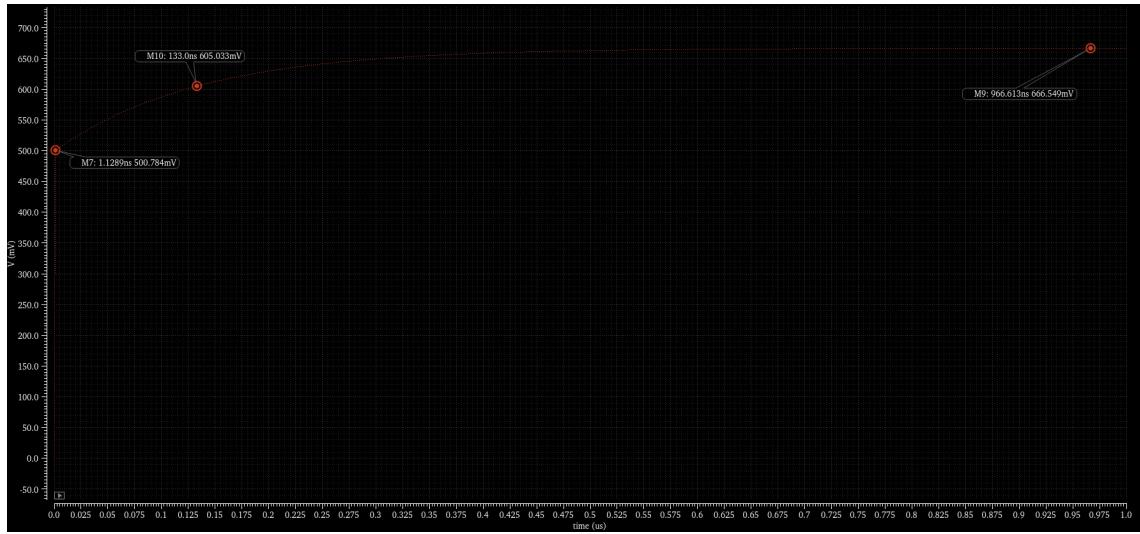


Figure 18: Lec 2 : Q2: Soln - Part (b)

### 3 Lecture 3

#### 3.1 Step Response for passive RLC circuit Combinations

Plot  $V_{out}$  vs time and  $I_{out}$  vs time

- 
- 
- 

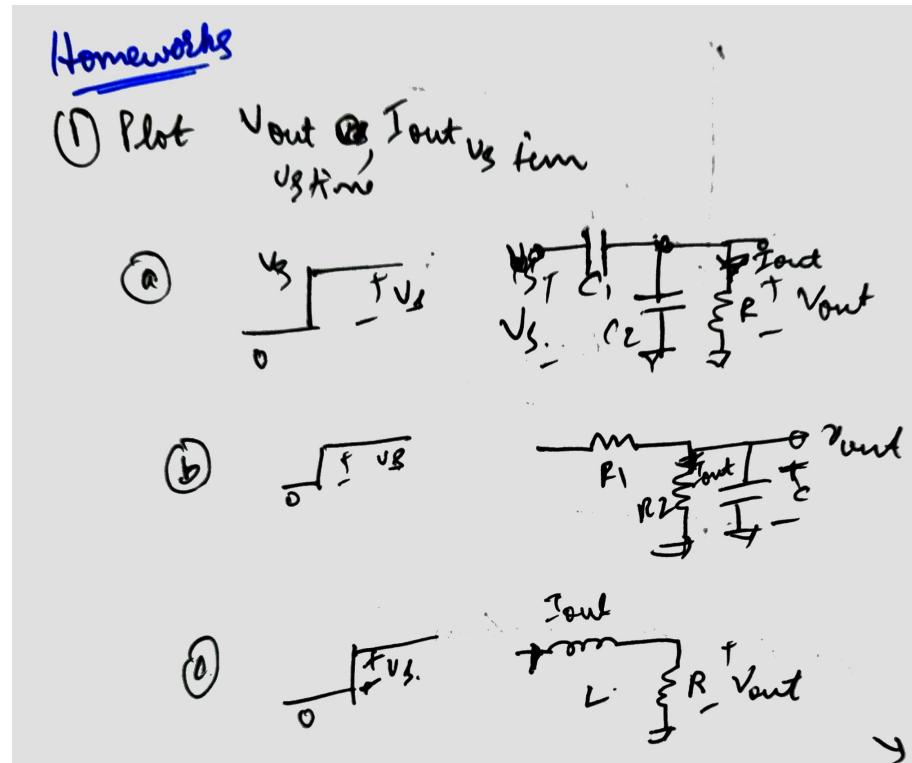
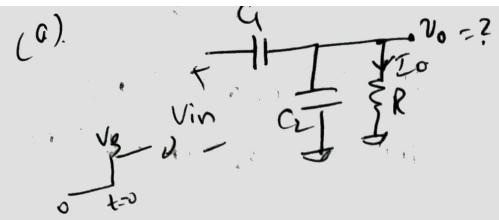


Figure 19: Lecture 3 - Question 1

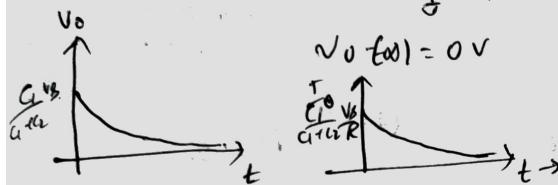


$$@ t=0^-, V_{C1}(0^-) = V_{C2}(0^-) = 0$$

$$@ t=0^+, i = \frac{V_B}{R} = \infty$$

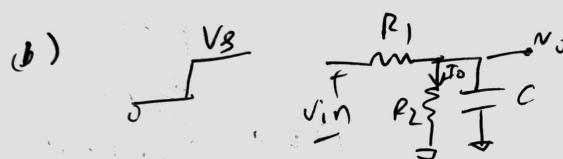
$$@ t=\infty, V_{C2}(\infty) = \frac{C_1}{C_1+C_2} V_B = V_0(\infty)$$

$$T = R(C_1 + C_2)$$



$$\therefore V_0(t) = 0 + \left( \frac{C_1}{C_1+C_2} V_B - 0 \right) e^{-\frac{t}{T}}$$

$$V_0(t) = \frac{C_1}{C_1+C_2} V_B e^{-\frac{t}{T}} u(t)$$



$$@ t=0^-, V_{00}(0^-) = 0$$

$$@ t=0^+, i = \frac{V_B}{R_1+R_2} - \text{initial}$$

$$@ t=\infty,$$

$$V_0(\infty) = V_0(0^+) = 0$$

$$@ t=\infty$$

$$V_0 = \frac{R_2}{R_1+R_2} \cdot V_B$$

$$V_0(t) = \left( \frac{R_2}{R_1+R_2} \cdot V_B - \frac{R_2}{R_1+R_2} \cdot V_B e^{-\frac{t}{T}} \right) u(t)$$

$$= \frac{V_B \cdot R_2}{R_1+R_2} \cdot (1 - e^{-\frac{t}{T}}) \cdot u(t)$$

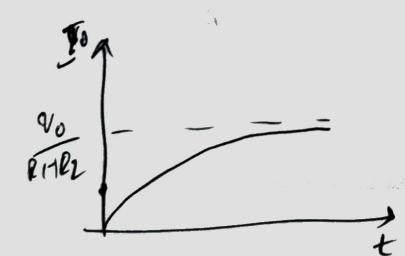


Figure 20: Lec 3: Solution for Question 1

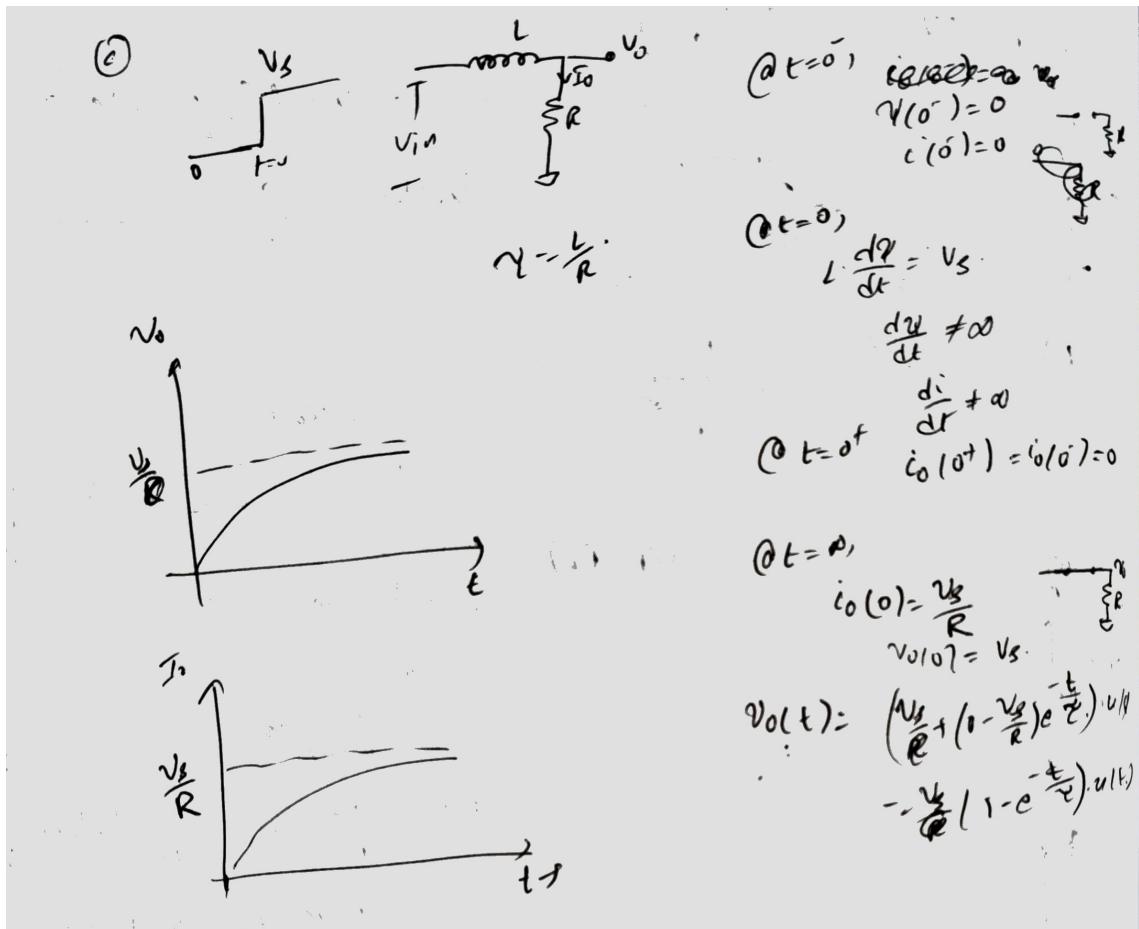


Figure 21: Lec 3: Solution for Question 1

### 3.2 Pulse Response for RC Circuit with varying Duty Cycle and Time Period

Plot  $V_{out}$  vs time (a)  $D = 10\%$  (b)  $D = 90\%$  (i)  $T = 0.1RC$  (ii)  $T = 10RC$  where  $D = \frac{T_{ON}}{T}$

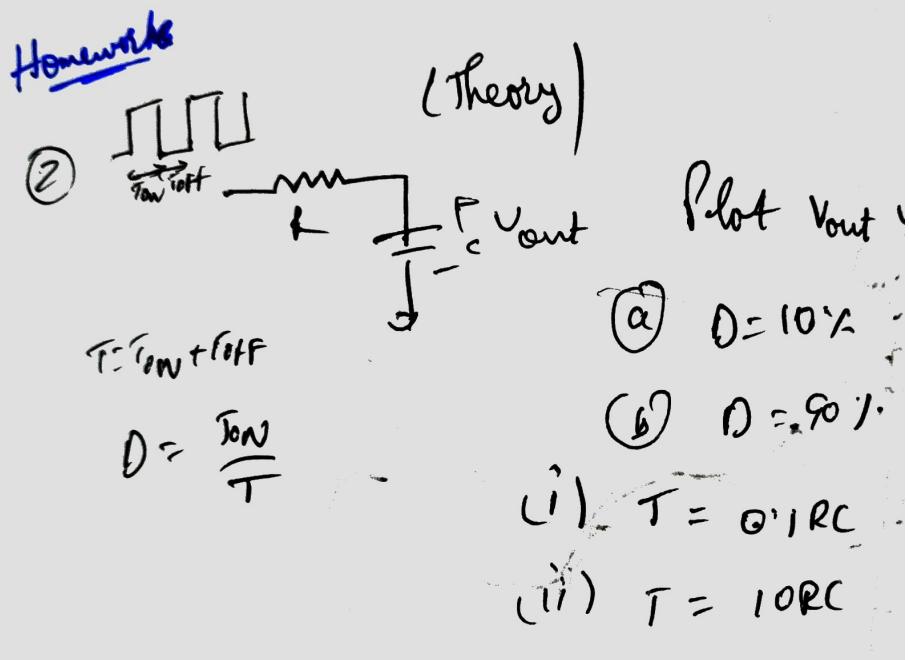
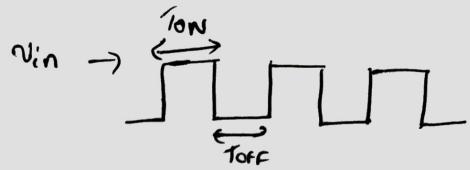
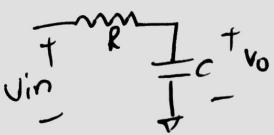


Figure 22: Lecture 3 - Question 2



$$(a) D = 10\%$$

$$(i) T = 0.1RC$$

$$(b) D = 90\%$$

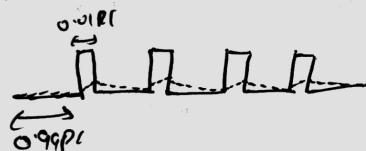
$$(ii) T = 10RC$$

$$(i) T = 0.1RC$$

$$(a) \frac{T_{on}}{T} = 10\%$$

$$T_{on} = 0.01RC$$

$$T_{off} = 0.99RC$$



(ii)

$$(b) \frac{T_{on}}{T} = 90\%$$

$$T_{on} = 0.9RC$$

$$T_{off} = 0.1RC$$



$$(ii) T = 10RC$$

$$(a) \frac{T_{on}}{T} = 10\%$$

$$T_{on} = RC$$

$$T_{off} = 9RC$$



$$(b) \frac{T_{on}}{T} = 90\%$$

$$T_{on} = 9RC$$

$$T_{off} = RC$$

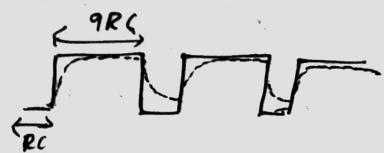


Figure 23: Lec 3: Solution for Question 2

### 3.3 Bode Plot for a given Transfer Function

Draw Bode plot for  $H(s) = \frac{(s-z_1)(s+z_2)}{(s+p_1)(s+p_2)(s+p_3)}$  where (i)  $z_2 \ll p_1 \ll p_2 \ll p_3 \ll z_1$  (ii)  $p_3 \ll p_2 \ll p_1 \ll z_1 \ll z_2$

Homework

$$\textcircled{3} \quad H(s) = \frac{(s-p_1)(s-p_2)}{(s+p_1)(s+p_2)s^2 + p_3 s}$$

(i)  $s_2 < p_1 < p_2 < p_3 < s_1$   
(ii)  $p_3 < p_2 < p_1 < s_1 < s_2$   
Draw bode plot:

Figure 24: Lecture 3 - Question 3

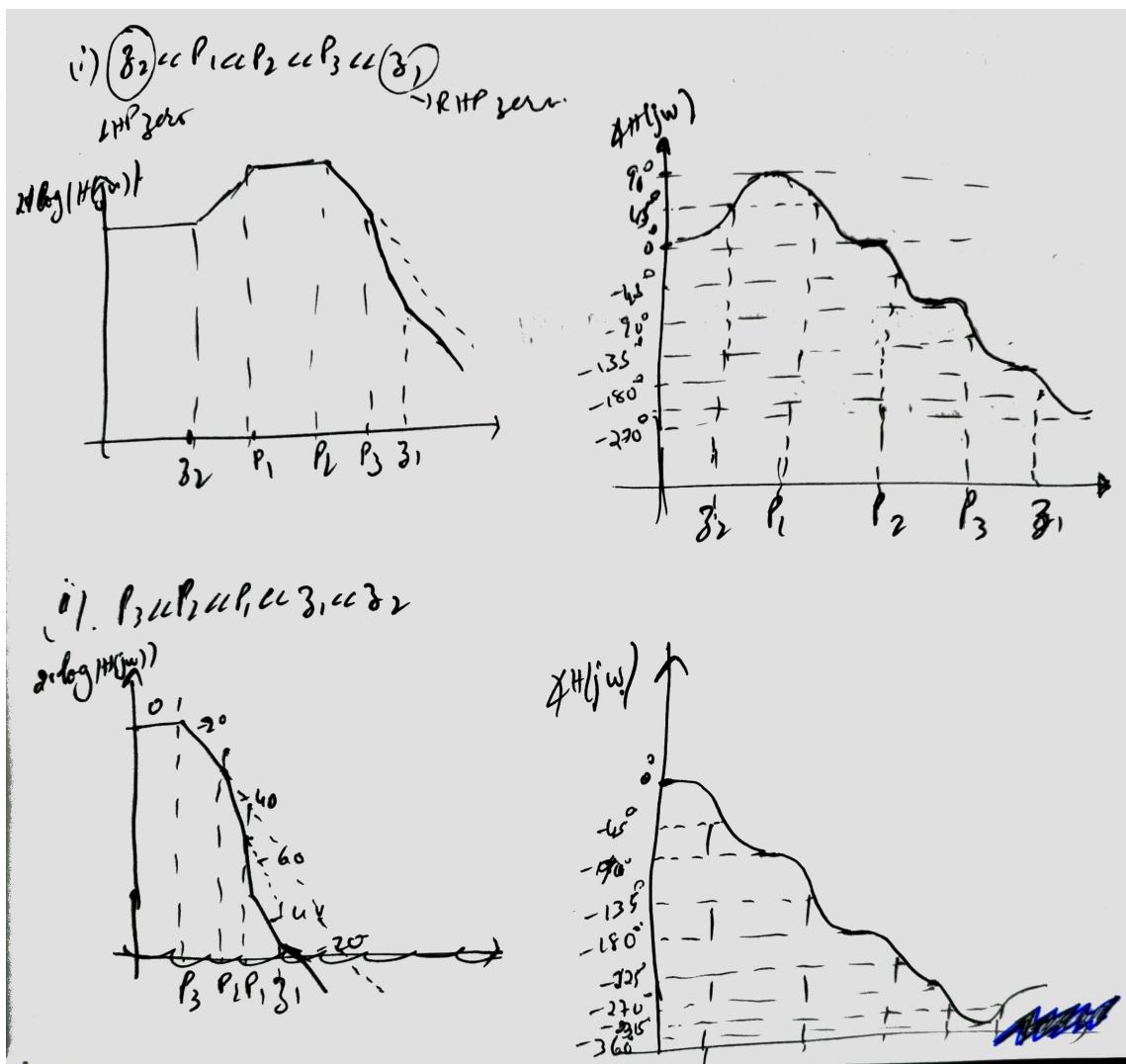


Figure 25: Lec 3: Solution for Question 3

## 4 Lecture 4

### 4.1 Non-inverting Schmitt Trigger

Design a non-inverting schmitt trigger using opamp based circuits.

# Homework

① Design a non-inverting Schmitt Trigger using op-amp based circuits -

Figure 26: Lecture 4 - Question 1

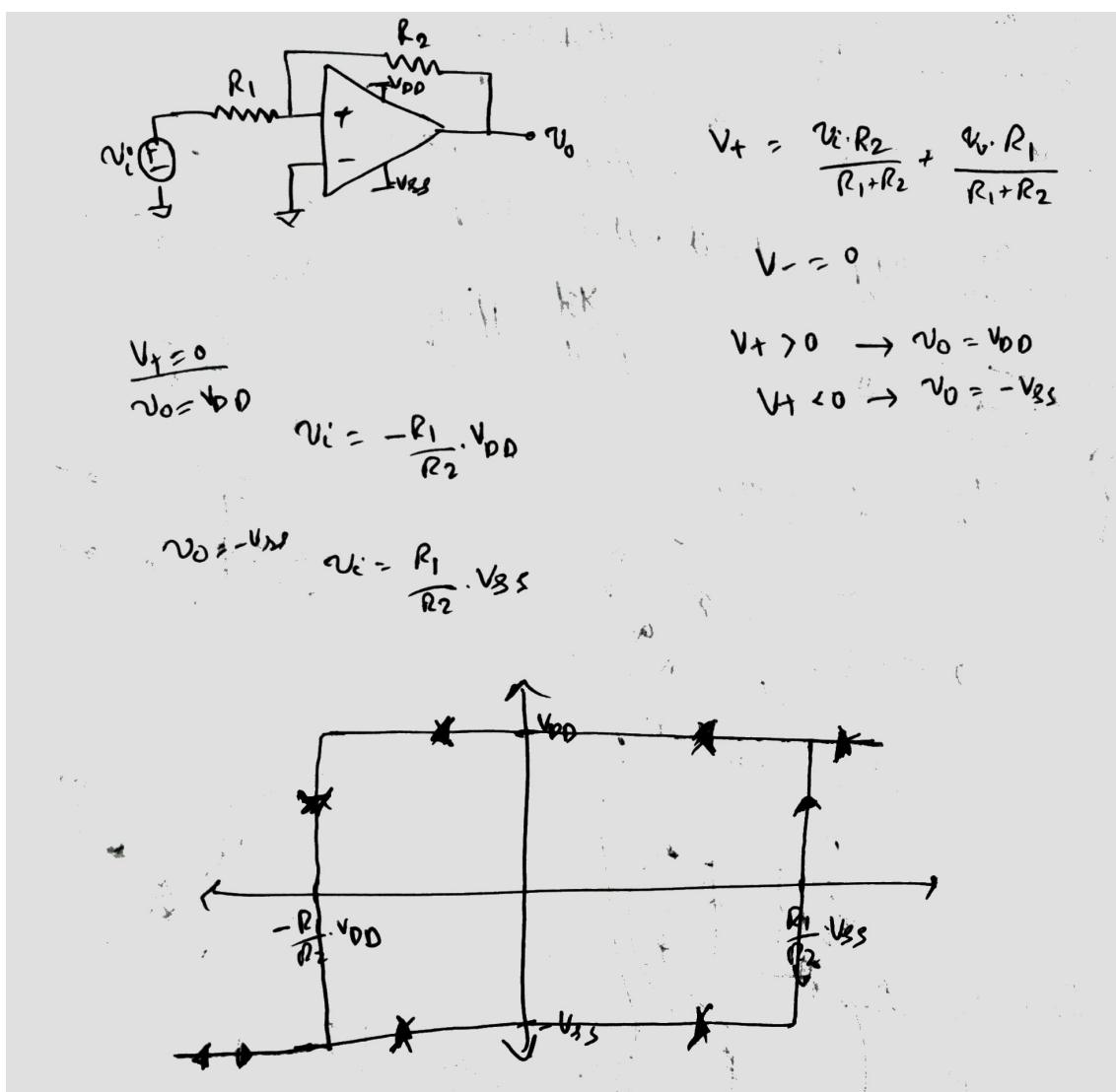


Figure 27: Lec 4: Solution for Question 1

## 4.2 Expression for Closed loop Unity gain bandwidth

Find the expression for Closed loop Unity gain bandwidth.

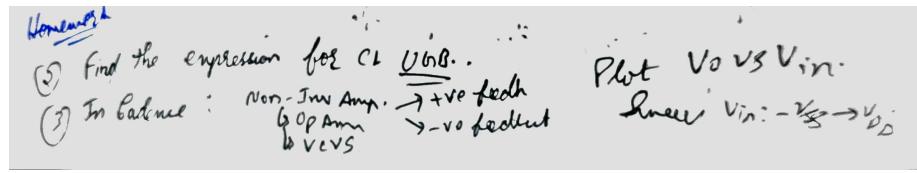


Figure 28: Lecture 4 - Question 2,3

**Answer:**

Assuming a single pole system, the below image shows the closed loop unity gain bandwidth.

$$V_o(s) = \frac{A}{1 + \frac{s}{(1+A\beta)W_p}} \cdot V_{in}(s)$$

$$W_p = \frac{1}{R_{out} \cdot C}$$

$$A = G_m R_{out}$$

$$\omega_{VnB} \rightarrow \omega @ |V_o/V_i(j\omega)| = 1$$

$$(1+A\beta) \cdot W_p \approx \frac{G_m \beta}{C}$$

$$\Rightarrow \left| \frac{A}{1 + \frac{j\omega}{\frac{G_m \beta}{C}}} \right| = 1$$

$$\Rightarrow A^2 = 1 + \frac{\omega^2}{\frac{G_m^2 \beta^2}{C^2}}$$

$$\Rightarrow A \gg 1$$

$$\Rightarrow A \frac{G_m \beta}{C} = \omega_{VnB}$$

$$\Rightarrow A v_o \cdot W_p = \omega_{VnB}$$

Figure 29: Lec 4: Solution for Question 2

### 4.3 Non-Inverting Amplifier using VCVS

In cadence, Plot  $V_o$  vs  $V_{in}$  (Sweep  $V_{in}$  from  $-V_{ss}$  to  $V_{DD}$ ) for non-inverting amplifier using Opamp and VCVS for both positive and -ve feedback.

**Answer:**

A non-inverting amplifier using positive feedback is not possible. Due to positive feedback, the output will saturate to either  $V_{DD}$  or  $V_{SS}$  for any non-zero input.

For negative feedback, the output voltage is given by

$$V_{out} = V_{in} \cdot \left(1 + \frac{R_2}{R_1}\right).$$

For the non-inverting amplifier we can use either an opamp or a VCVS.

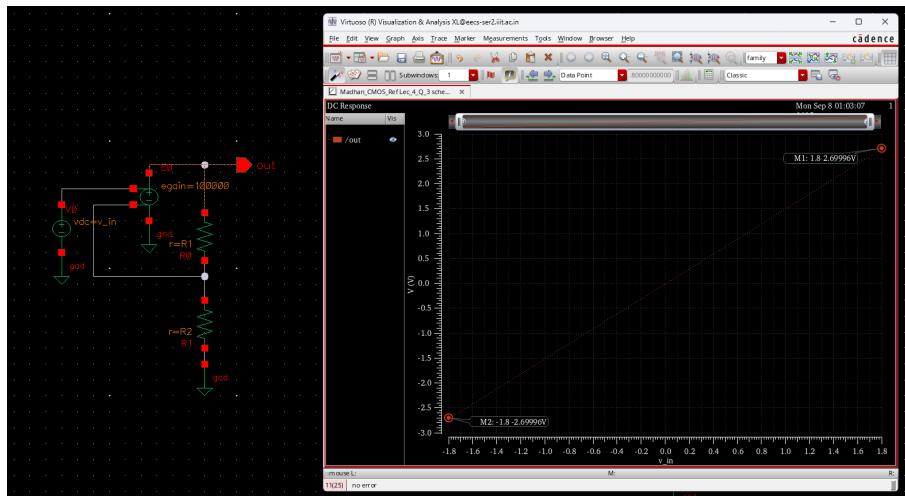


Figure 30: Lecture 4 - Question 3 Solution: Non-inverting Amplifier using VCVS

## 5 Lecture 5

### 5.1 Single Pole Opamp with Feedback - Bode Plot

In Cadence, Bode Plot for

1.  $A = 100$ , check  $V_x$  (offset) [DC]
2.  $A = 1000$ , check  $V_x$  (offset) [DC]
3. UGB = 1MHz, Gain = 1000, Design  $G_m$ ,  $R_{out}$ ,  $R_1$ ,  $R_2$ ,  $C$ ,  $V_{Ref} = 0.6V$ ,  $V_{out} = 1.2V$

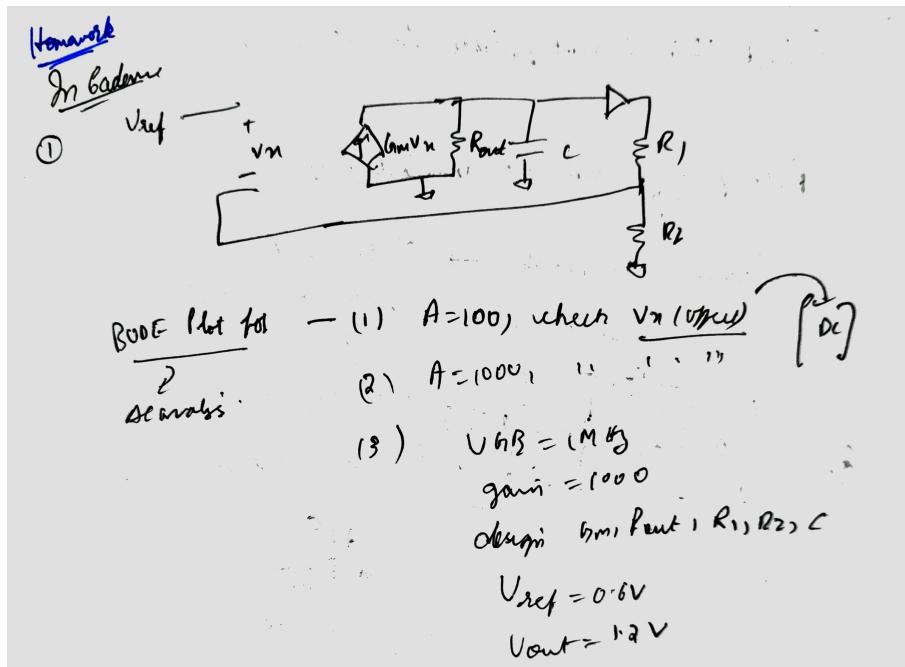


Figure 31: Lecture 5 - Question 1

**Answer:**

$$V_{eff} = V_{ref} - V_{fb}$$

$$\text{Open-loop TF}, \quad A(s) = \frac{g_m \cdot R_{out}}{1 + sC_{out}}, \quad \beta = \frac{R_2}{R_1 + R_2}$$

$$\text{Closed-loop TF}, \quad H(s) = \frac{A(s)}{1 + A(s) \cdot \beta} = \frac{g_m \cdot R_{out}}{1 + sC_{out} + \beta g_m R_{out}} = \frac{V_{out}}{V_{ref}}$$

$$V_{eff} = V_{ref} - V_{fb}$$

$$-V_{ref} - \beta V_{out} = \frac{V_{ref}}{1 + A_0 \beta} \quad A_0 = g_m R_{out}$$

$$WP = \frac{1}{R_{out} C}$$

$$\omega_{WP} = A_0 WP = \frac{g_m \cdot R_{out}}{R_{out} C}$$

$$f_{WP} = \frac{\omega_{WP}}{2\pi} = \frac{g_m}{2\pi C}$$

$$\text{given, } V_{ref} = 0.6V$$

$$H(s)|_{s=0} = \frac{1 \cdot 2}{0.6} = 2$$

$$V_{out} = 1.2V$$

$$\beta = \frac{1}{2} \rightarrow \begin{cases} R_1 = 1k\Omega \\ R_2 = 1k\Omega \end{cases}$$

$$\text{Let } C = 10\text{pf}$$

$$g_m = \frac{2\pi f_a}{2\pi \times 10^6 \times 10 \times 10^{-12}} = 62.83 \mu S$$

Figure 32: Lecture 5 - Question 1 - Theory

$$A_0 = 100 - g_m \cdot R_{out}$$

$$A_0 \beta = 50$$

$$V_{err} = \frac{V_{ref}}{1 + A_0 \beta} - \frac{0.6}{1 + 50} \times 11.76 \text{ mV}$$

$$V_{fb} = V_{ref} - V_{err} = 0.568$$

$$V_{out} = \frac{A_0}{1 + A_0 \beta} \cdot V_{ref} = \frac{100}{51} \times 0.6 = 1.17 \text{ V}$$

$$R_{out} = 1.59 \text{ M}\Omega$$

ii)  $A_0 = 2000$

$$V_{err} = \frac{0.6}{501} \approx 1.19 \text{ mV}$$

$$V_x = 0.598 \text{ V} \quad R_{out} = \frac{A_0}{g_m} = 15.92 \mu\Omega$$

$$V_{out} = 1.192 \text{ V}$$

Figure 33: Lecture 5 - Question 2 - Theory

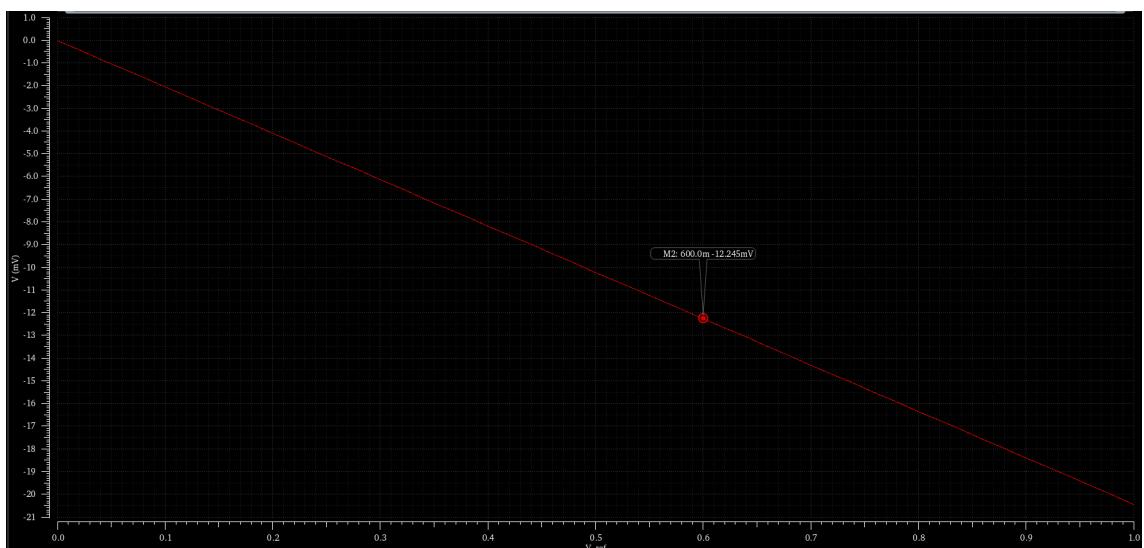


Figure 34: Lec 5: Solution for Question 1\_1)

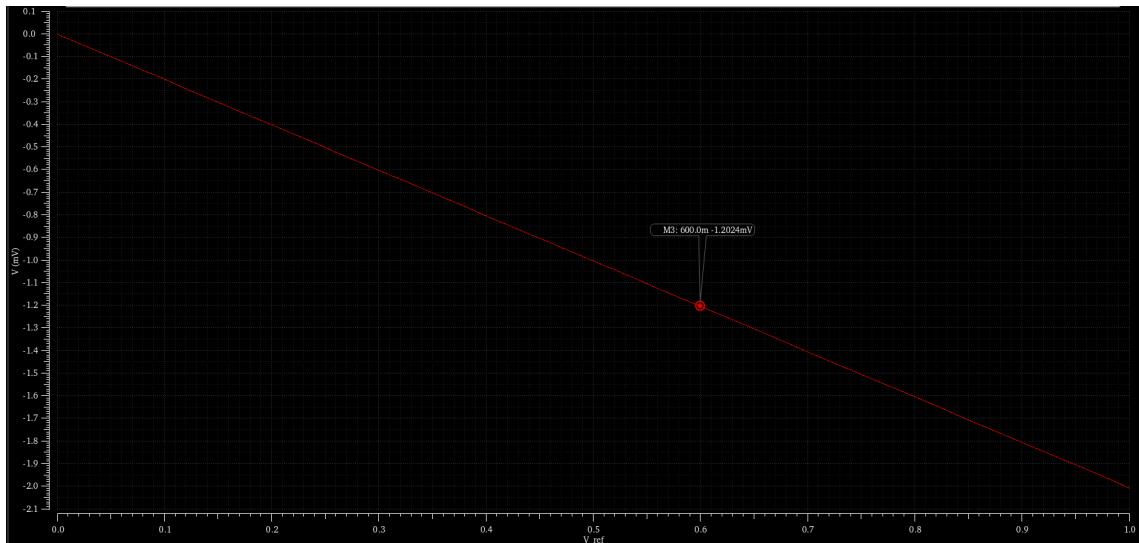


Figure 35: Lec 5: Solution for Question 1\_2

## 5.2 Bode Plot for a 2 Pole System

In cadence, AC analysis. Bode Plot for  $\frac{V_{out}}{V_{in}}$

1.  $G_{m1} = G_{m2} = 10\mu F$ ,  $R_1 = R_2 = 10M\Omega$ ,  $C_1 = 10fF$ ,  $C_2 = 2fF$
2. add  $C_{effective}$  at  $C_1$  and get phase margin =  $45^\circ$

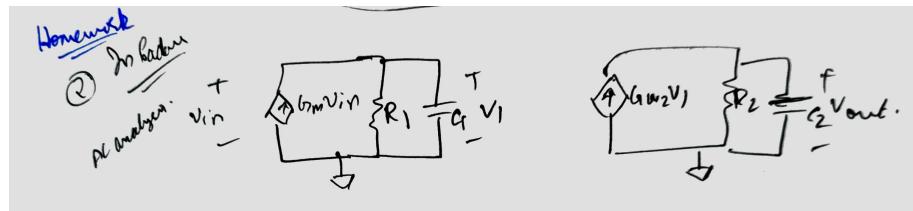


Figure 36: Lecture 5 - Question 2 - circuit

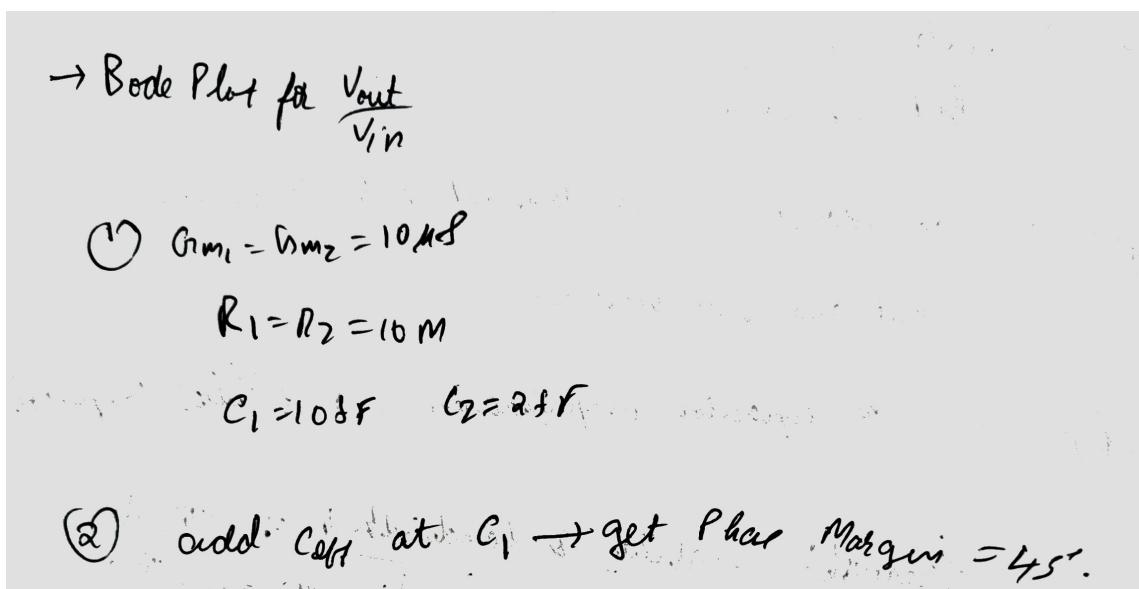


Figure 37: Lecture 5 - Question 2 - Question

**Answer:**

**Given:**

$$g_m = 10 \mu S, \quad R_1 = R_2 = 10 M\Omega, \quad C_1 = 10 fF, \quad C_2 = 2 fF$$

**(1) DC Gain and Pole Locations:**

$$A_1 = A_2 = g_m R = 10 \times 10^{-6} \times 10 \times 10^6 = 100$$

$$A_0 = A_1 A_2 = 100 \times 100 = 10^4 = 80 \text{ dB}$$

$$\omega_{p1} = \frac{1}{R_1 C_1} = 1 \times 10^7 \text{ rad/s}, \quad \omega_{p2} = \frac{1}{R_2 C_2} = 5 \times 10^7 \text{ rad/s}$$

$$f_{p1} = 1.59 \text{ MHz}, \quad f_{p2} = 7.96 \text{ MHz}$$

## 6 Lecture 6

### 6.1 Miller compensation - Bode Plot

Draw Bode plot for miller compensated circuit.

$$G_{m1} = G_{m2} = 10 \mu S, \quad R_1 = R_2 = 10 M\Omega, \quad C_1 = 10 fF, \quad C_2 = 2 fF$$

Find Phase Margin, Unity Gain Bandwidth and DC Gain. (Theory + Cadence) (AC analysis/STB)

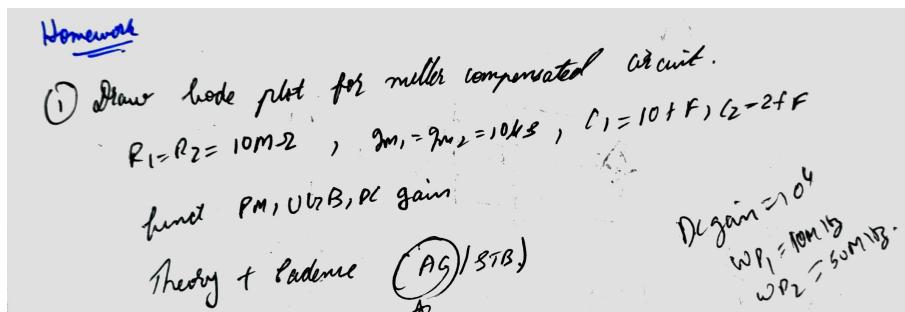


Figure 38: Lecture 6 - Question 1

### 6.2 Adding a zero to a system

Simulate in cadence.

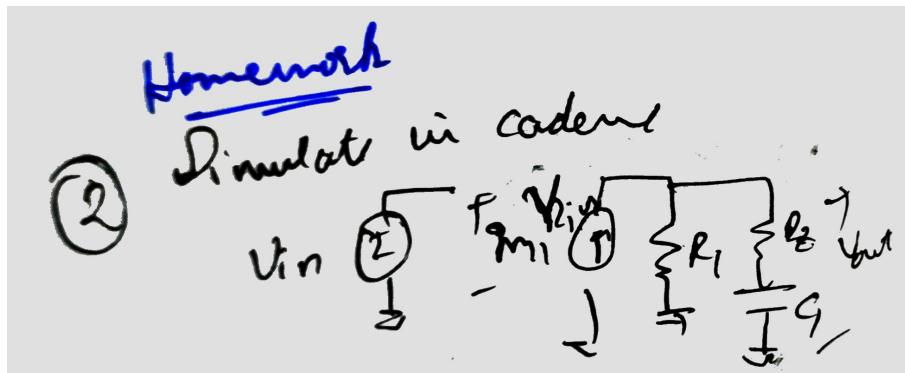


Figure 39: Lecture 6 - Question 2

## 7 Lecture 7

### 7.1 Characterization of Resistors in TSMC 180nm

TSMC 18 lib, Simulate all the resistors  $-40^\circ$  to  $125^\circ$  (SS, TT, FF) TSMC 18 lib, Simulate all the resistors  $-40^\circ$  to  $125^\circ$  (SS, TT, FF)

Resistor	Temperature Coefficient	Type	Process Spread	Linearity	Area
R1	Value	TypeA	Spread1	Linear1	Area1
R2	Value	TypeB	Spread2	Linear2	Area2
R3	Value	TypeC	Spread3	Linear3	Area3

Table 1: Resistor characteristics under different conditions

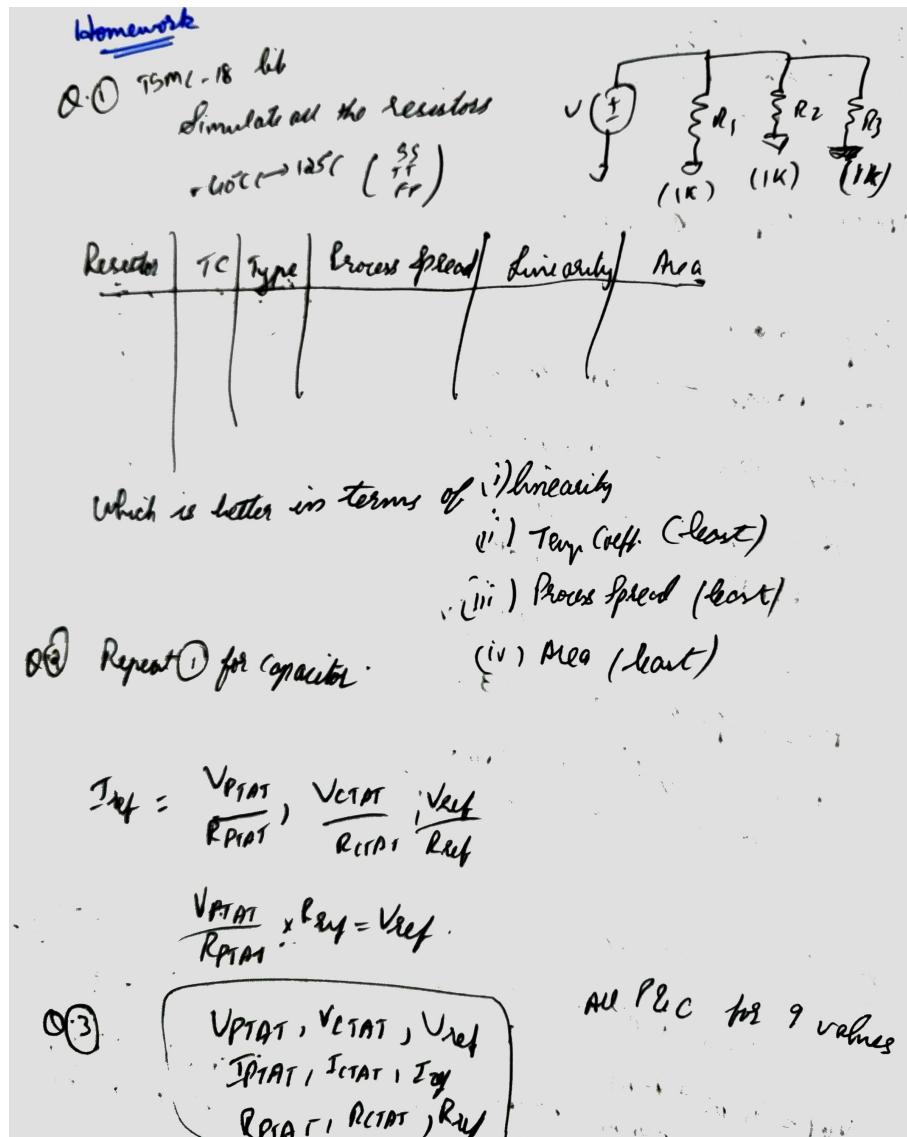


Figure 40: Lecture 7 - Question 1,2,3

All the resistors are adjusted to a resistance of  $1k\Omega$ .

Table 2: Comparison of Different Resistors

extbfResistor	TC (ppm/ $^{\circ}\text{C}$ )	Type	Process Spread (%)	Linearity	Area ( $\mu\text{m}^2$ )
res (analogLib)	0	Ideal resistor		0	
rphpoly	-297.56	p+ polysilicon resistor	4.9	0.28	27.116
rphpoly_dis	-297.56	p+ polysilicon	4.9	0.28	27.116
rphpoly_rf	-270.033	p+ polysilicon RF resistor	4.4	0.27	12.6
rnhpoly	-1375.19	n+ polysilicon resistor	22.68	0.81	24.7084
rnwell	3324.13	n-well resistor	54.8	3.31	50.37

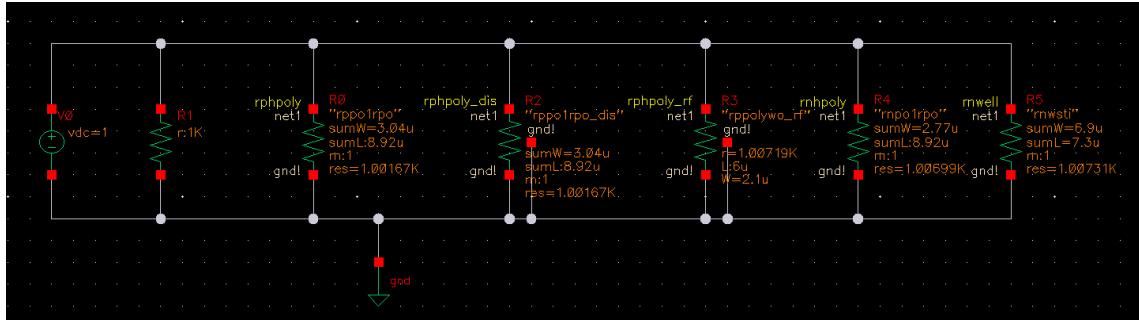


Figure 41: Lec 7 : Question 1: Testbench

## 7.2 Characterization of Capacitors in TSMC 180nm

Repeate Question 1 with a capacitor.

Capacitor	Temperature Coefficient	Type	Process Spread	Linearity	Area
C1	Value	TypeA	Spread1	Linear1	Area1
C2	Value	TypeB	Spread2	Linear2	Area2
C3	Value	TypeC	Spread3	Linear3	Area3

Table 3: Resistor characteristics under different conditions

## 7.3 PTAT, CTAT, Ref - Voltage, Current and Resistance Design Combinations

$$V_{PTAT}, V_{CTAT}, V_{Ref}$$

$$I_{PTAT}, I_{CTAT}, I_{Ref}$$

$$R_{PTAT}, R_{CTAT}, R_{Ref}$$

All P and C for 9 values.

**Solution:**

**Formulas for  $V_{PTAT}$ :**

$$\begin{aligned} V_{PTAT} &= I_{PTAT} \cdot R_{Ref} \\ V_{PTAT} &= I_{Ref} \cdot R_{PTAT} \\ V_{PTAT} &= \frac{V_{CTAT}}{R_{CTAT}} \cdot R_{PTAT} \\ V_{PTAT} &= \frac{V_{PTAT}}{R_{PTAT}} \cdot R_{PTAT} \\ V_{PTAT} &= (I_{PTAT} + I_{CTAT}) \cdot R_{PTAT} \\ V_{PTAT} &= V_{Ref} - V_{CTAT} \\ V_{PTAT} &= I_{CTAT}(\text{small slope}) \cdot R_{PTAT} \text{ (Non-linear)} \end{aligned}$$

**Formulas for  $V_{CTAT}$ :**

$$\begin{aligned} V_{CTAT} &= I_{CTAT} \cdot R_{Ref} \\ V_{CTAT} &= I_{Ref} \cdot R_{CTAT} \\ V_{CTAT} &= \frac{V_{PTAT}}{R_{PTAT}} \cdot R_{CTAT} \\ V_{CTAT} &= \frac{V_{CTAT}}{R_{CTAT}} \cdot R_{CTAT} \\ V_{CTAT} &= (I_{PTAT} + I_{CTAT}) \cdot R_{CTAT} \\ V_{CTAT} &= V_{Ref} - V_{PTAT} \\ V_{CTAT} &= I_{PTAT}(\text{small slope}) \cdot R_{CTAT} \text{ (Non-linear)} \end{aligned}$$

**Formulas for  $V_{Ref}$ :**

$$\begin{aligned}
 V_{Ref} &= I_{Ref} \cdot R_{Ref} \\
 V_{Ref} &= (I_{PTAT} + I_{CTAT}) \cdot R_{Ref} \\
 V_{Ref} &= \frac{V_{PTAT}}{R_{PTAT}} \cdot R_{Ref} \\
 V_{Ref} &= \frac{V_{CTAT}}{R_{CTAT}} \cdot R_{Ref} \\
 V_{Ref} &= \frac{V_{PTAT} + V_{CTAT}}{R_{Ref}} \cdot R_{Ref} \\
 V_{Ref} &= V_{PTAT_1} - V_{PTAT_2} \\
 V_{Ref} &= V_{CTAT_1} - V_{CTAT_2}
 \end{aligned}$$

**Formulas for  $I_{PTAT}$ ,  $I_{CTAT}$ ,  $I_{Ref}$ :**

$$\begin{aligned}
 I_{PTAT} &= \frac{V_{PTAT}}{R_{Ref}} \\
 I_{PTAT} &= \frac{I_{PTAT} \cdot R_{PTAT}}{R_{Ref}} \\
 I_{CTAT} &= \frac{V_{CTAT}}{R_{Ref}} \\
 I_{CTAT} &= \frac{I_{CTAT} \cdot R_{CTAT}}{R_{Ref}} \\
 I_{CTAT} &= \frac{V_{CTAT}}{R_{CTAT}} \\
 I_{Ref} &= \frac{V_{Ref}}{R_{Ref}} \\
 I_{Ref} &= \frac{V_{CTAT}}{R_{CTAT}} \\
 I_{Ref} &= \frac{V_{PTAT}}{R_{PTAT}} \\
 I_{Ref} &= \frac{V_{PTAT} + V_{CTAT}}{R_{Ref}} \\
 I_{Ref} &= \frac{I_{CTAT} \cdot R_{Ref}}{R_{CTAT}} \\
 I_{Ref} &= \frac{I_{PTAT} \cdot R_{Ref}}{R_{PTAT}}
 \end{aligned}$$

Formulas for  $R_{PTAT}$ ,  $R_{CTAT}$ ,  $R_{Ref}$ :

$$R_{PTAT} = \frac{V_{PTAT}}{I_{Ref}}$$

$$R_{PTAT} = \frac{V_{Ref} - V_{CTAT}}{I_{Ref}}$$

$$R_{PTAT} = \frac{V_{PTAT} \cdot R_{PTAT}}{V_{CTAT}}$$

$$R_{PTAT} = \frac{V_{PTAT} \cdot R_{CTAT}}{V_{CTAT}}$$

$$R_{CTAT} = \frac{V_{CTAT}}{I_{Ref}}$$

$$R_{CTAT} = \frac{V_{Ref} - V_{PTAT}}{I_{Ref}}$$

$$R_{Ref} = \frac{V_{Ref}}{I_{Ref}}$$

$$R_{CTAT} = \frac{V_{CTAT} \cdot R_{PTAT}}{V_{PTAT}}$$

$$R_{CTAT} = \frac{V_{CTAT} \cdot R_{CTAT}}{V_{CTAT}}$$

$$R_{Ref} = \frac{V_{PTAT}}{I_{PTAT}}$$

## 8 Lecture 8 - Part of MidSem Project

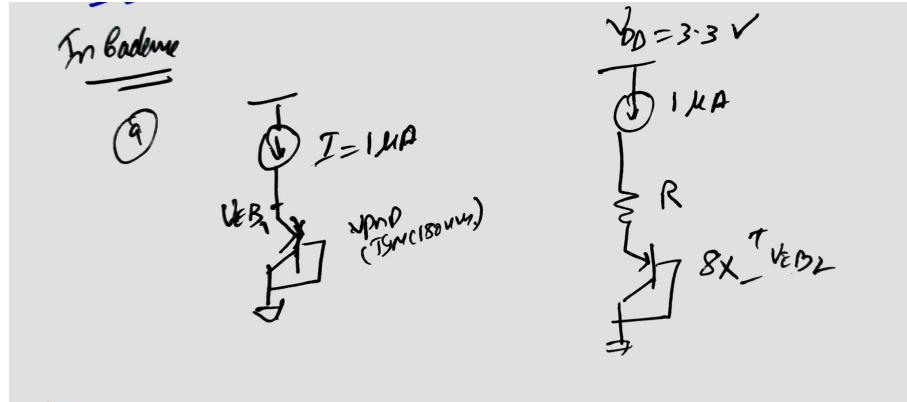


Figure 42: Lecture 8 - Question 1: Circuit

Answer:

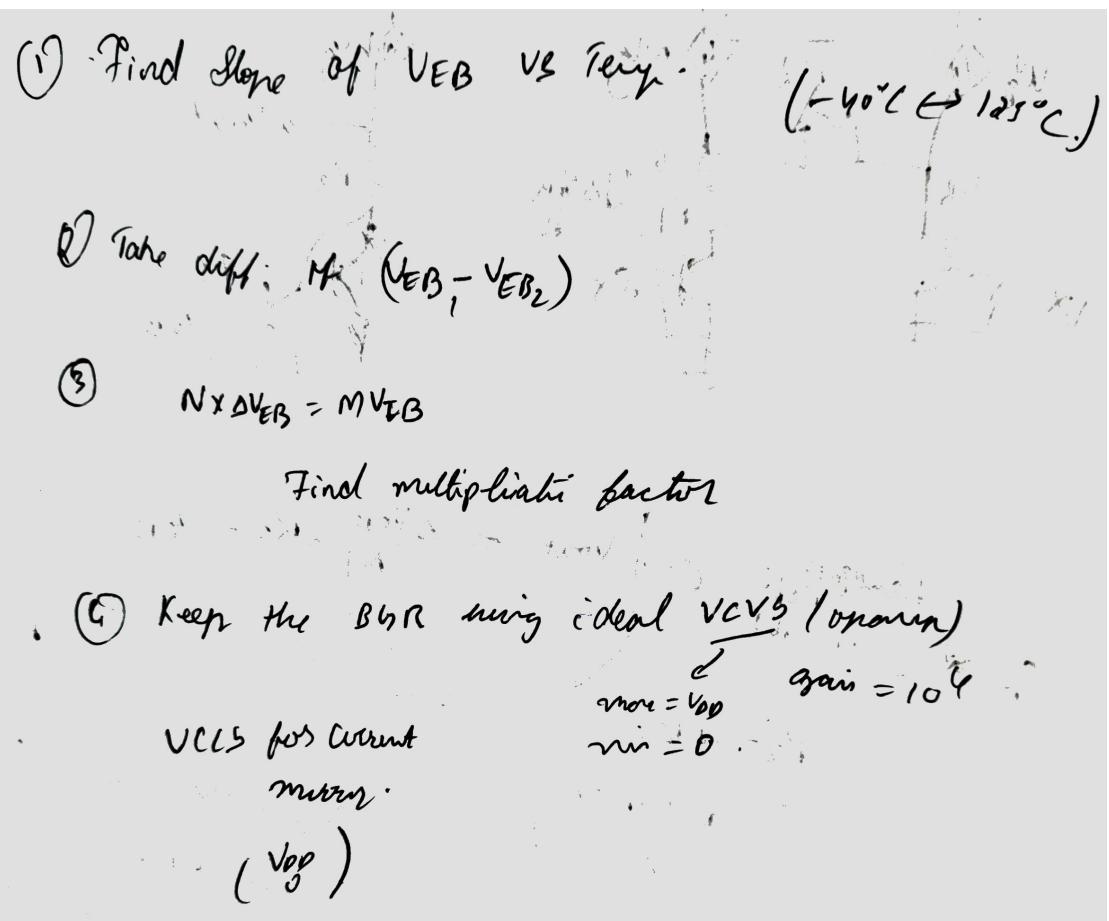


Figure 43: Lec 8: Question 1

### 8.1 Slope of $V_{EB}$ vs Temperature curve of a BJT

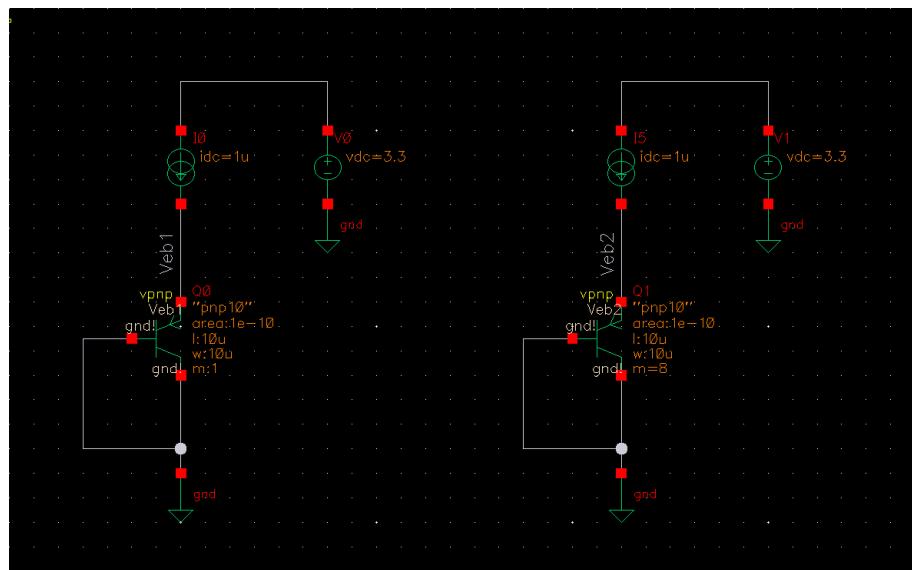


Figure 44: Lecture 8 - Question 1 - Testbench

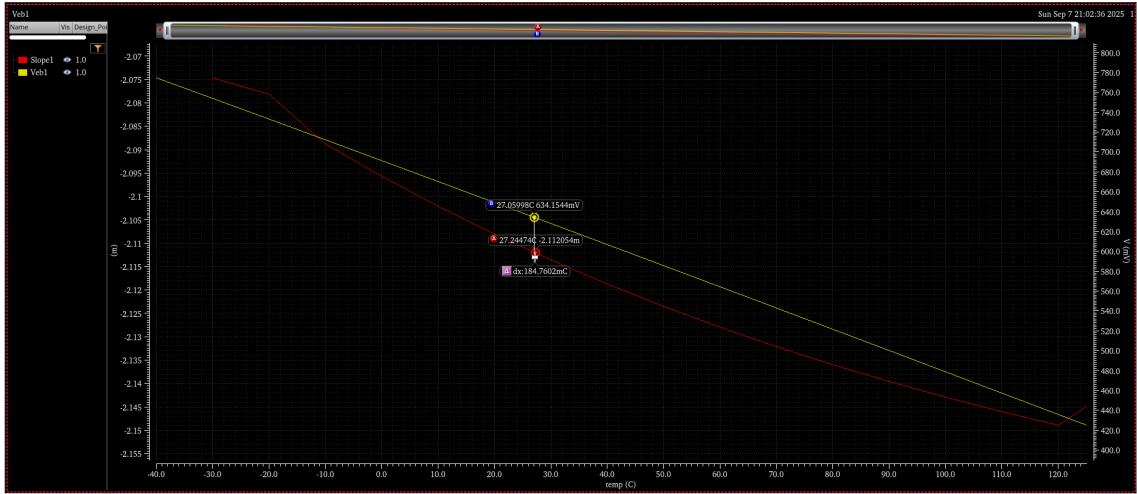


Figure 45: Lec 8: Q1:  $V_{EB}$  vs Temperature curve of a BJT

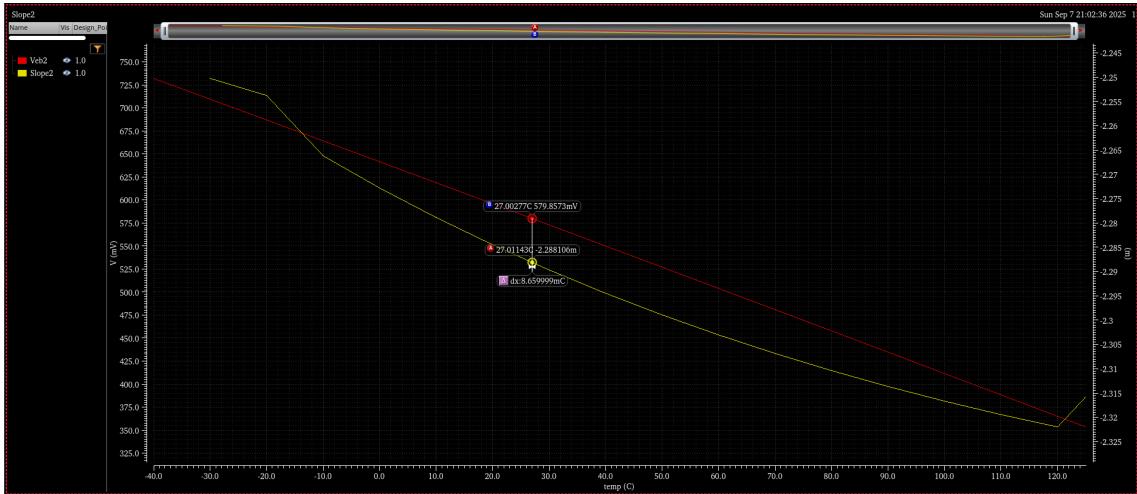


Figure 46: Lec 8: Q1: Slope Calculation of  $V_{EB}$  vs Temperature curve of a BJT

## 8.2 Difference of $V_{EB}$ of two BJTs

### 8.3 Find the multiplication factor to equate PTAT and CTAT voltages

At 27°C, the measured values are:

$$V_{BE1} = 634.2644 \text{ mV}, \quad \Delta V_{BE} = 54.42 \text{ mV}$$

The equality condition is given by:

$$N \cdot \Delta V_{BE} = M \cdot V_{BE1}$$

Rearranging,

$$\frac{M}{N} = \frac{\Delta V_{BE}}{V_{BE1}}$$

Substituting the values,

$$\frac{M}{N} = \frac{54.42}{634.2644} \approx 0.0858$$

Therefore,

$$\frac{M}{N} \approx 0.086 \quad \Rightarrow \quad \frac{R_2}{R_1} \approx 0.086$$

## 8.4 Simulate the BGR using ideal VCVS, VCVS for current mirror

### 9 Lecture 9 - MOSFET

#### 9.1 NMOS I-V characteristics

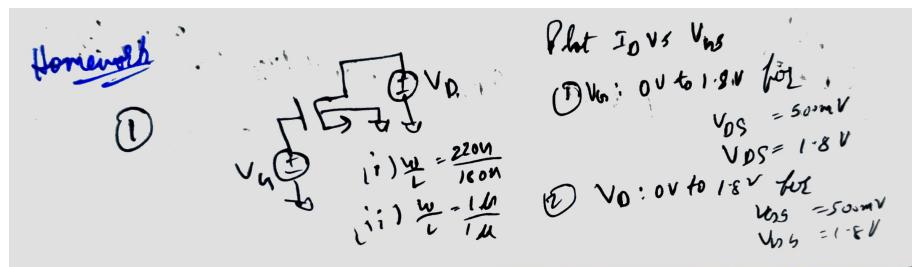
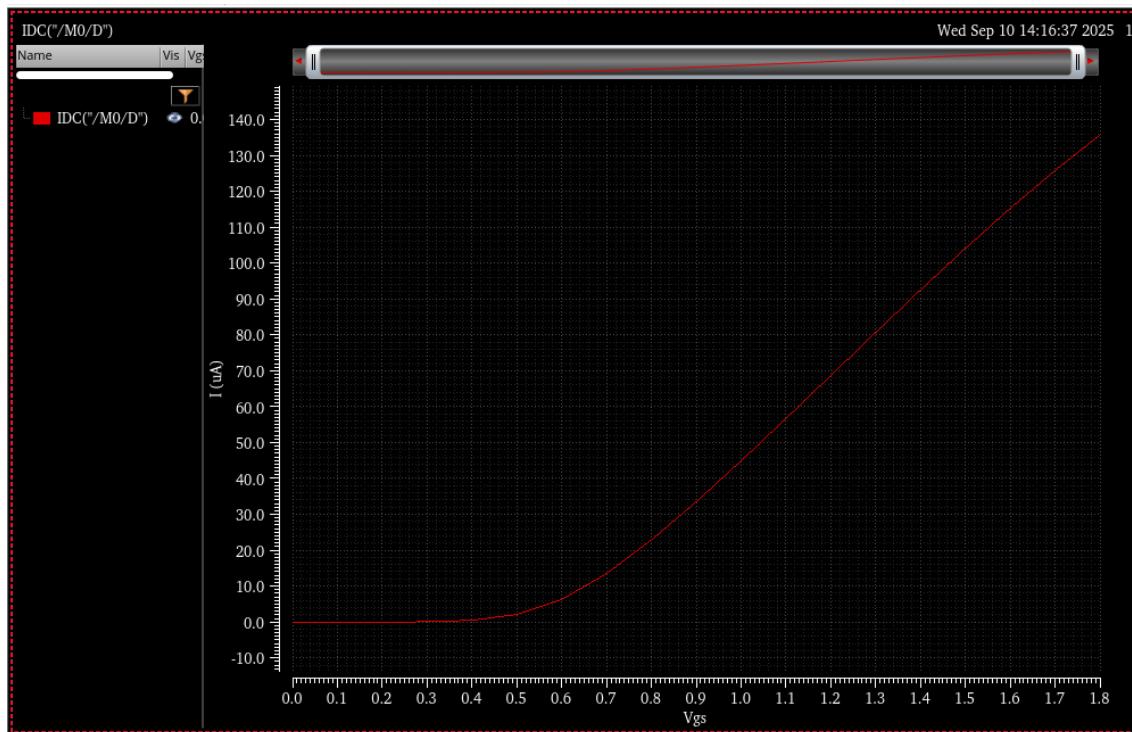


Figure 47: Lecture 9 - Question 1

**Vg: 0 to 1.8V**

(i)  $\frac{W}{L} = 220n/180n$

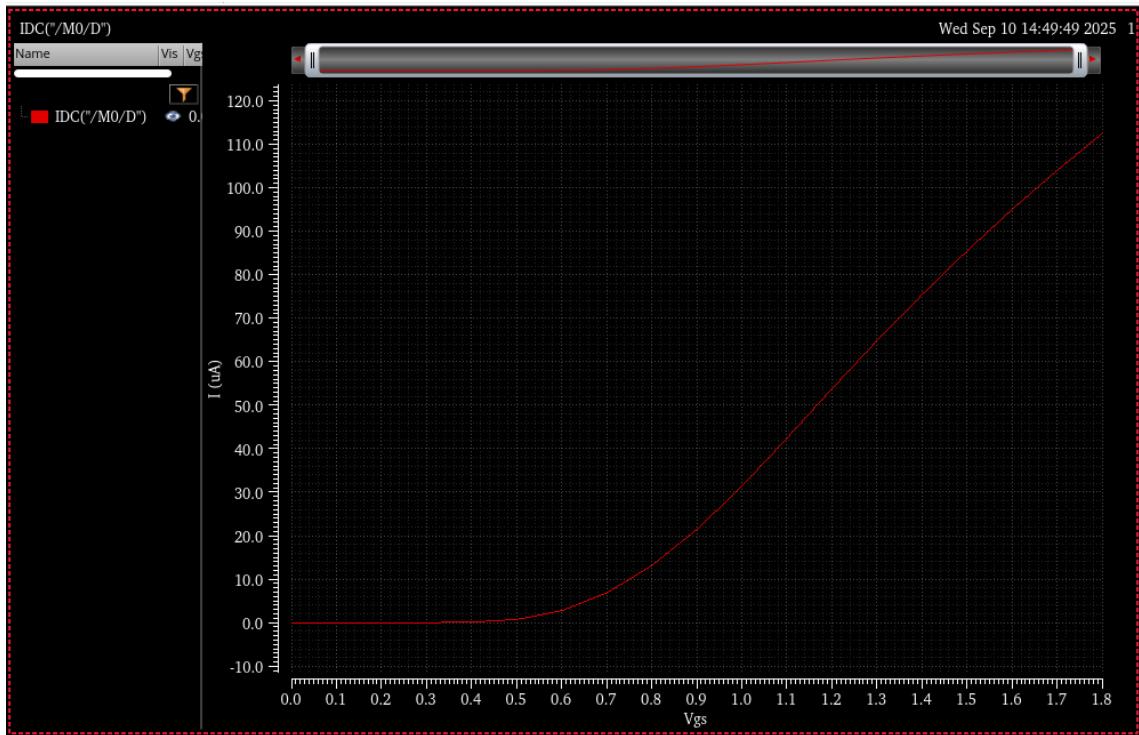
(a)  $V_{DS} = 500$  mV



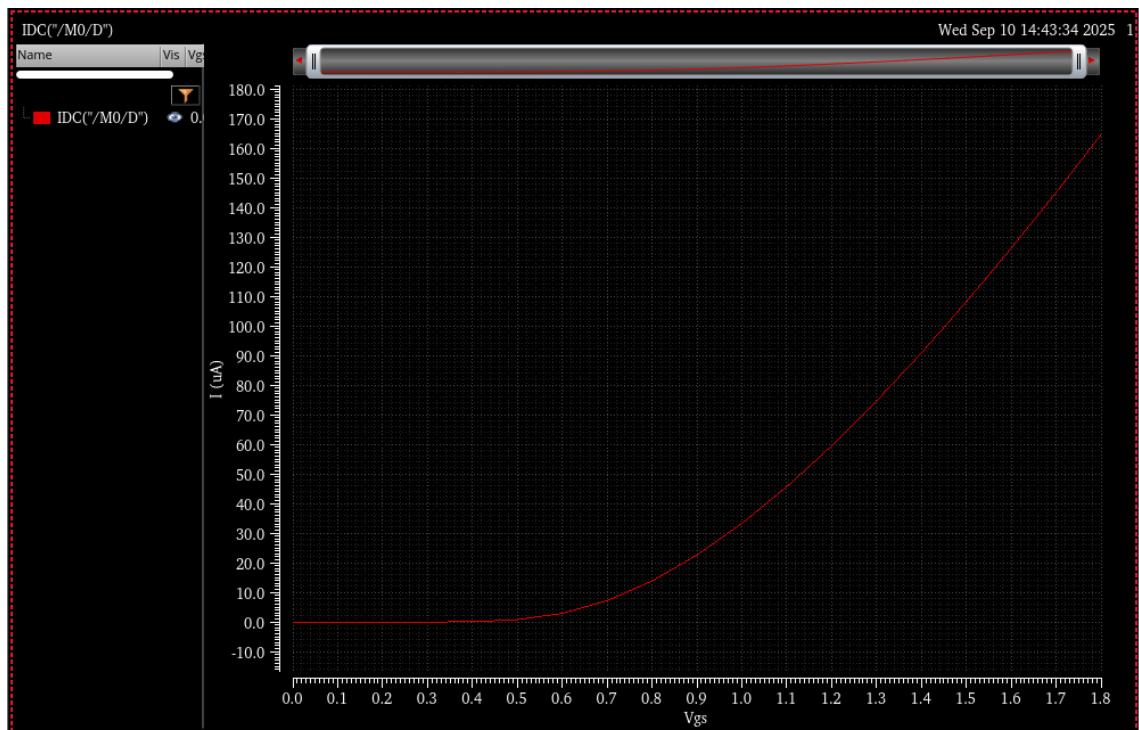
(b)  $V_{DS} = 1.8$  V

(ii)  $\frac{W}{L} = 1\mu/1\mu$

(a)  $V_{DS} = 500$  mV



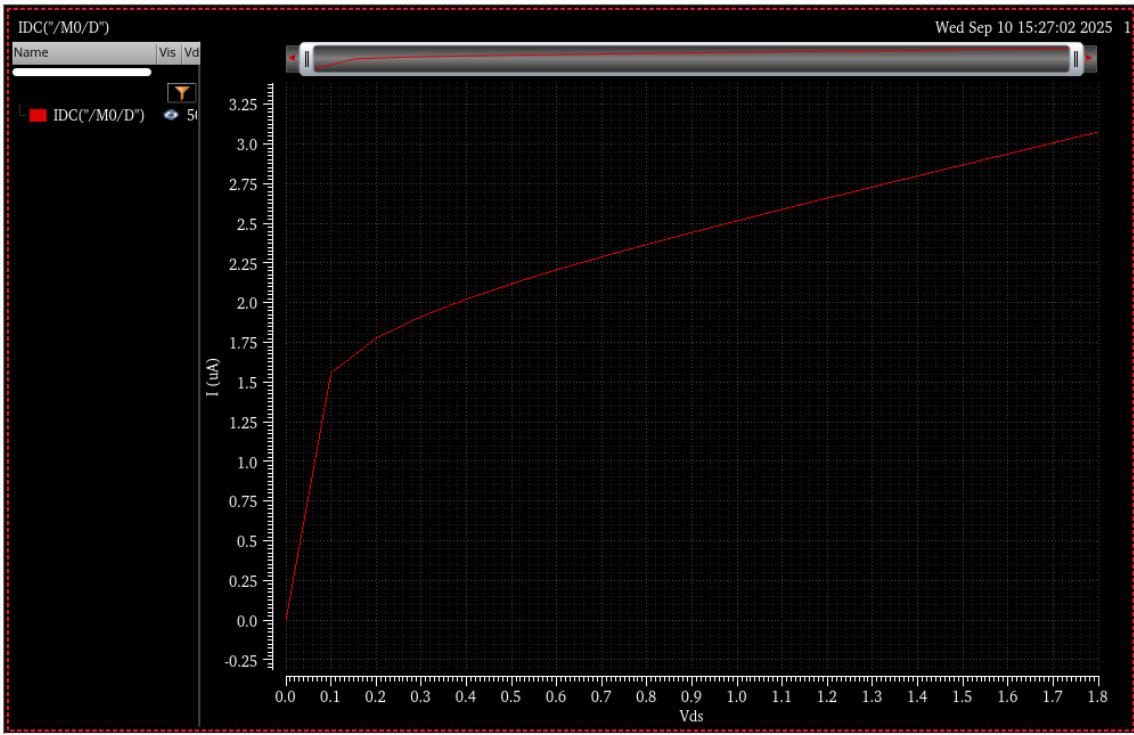
(b)  $V_{ds} = 1.8 \text{ V}$



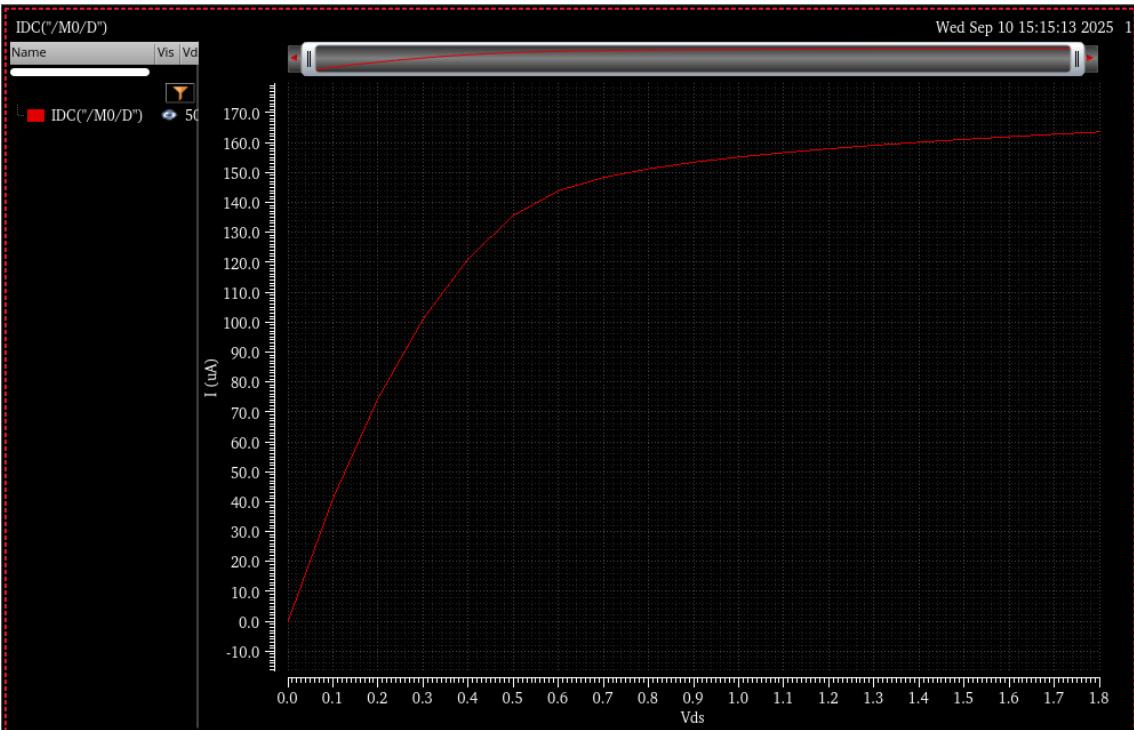
**Vd: 0 to 1.8V**

(i)  $W/L = 220\text{n}/180\text{n}$

(a)  $V_{gs} = 500 \text{ mV}$

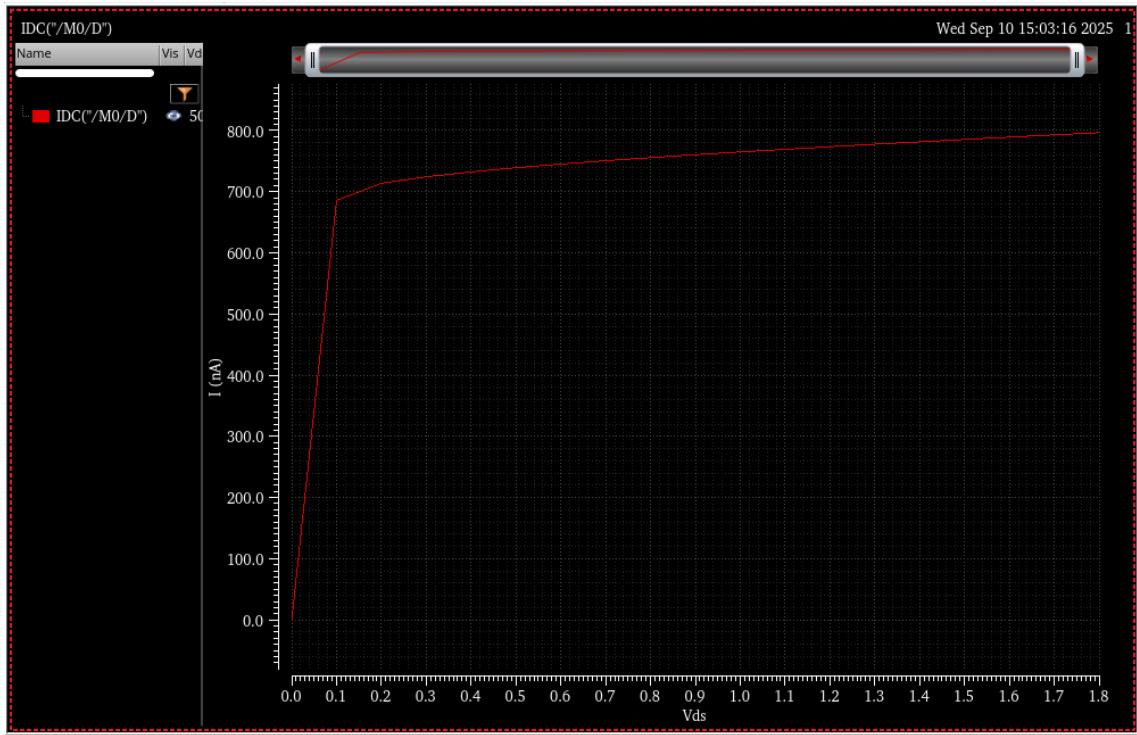


(b)  $V_{gs} = 1.8 \text{ V}$

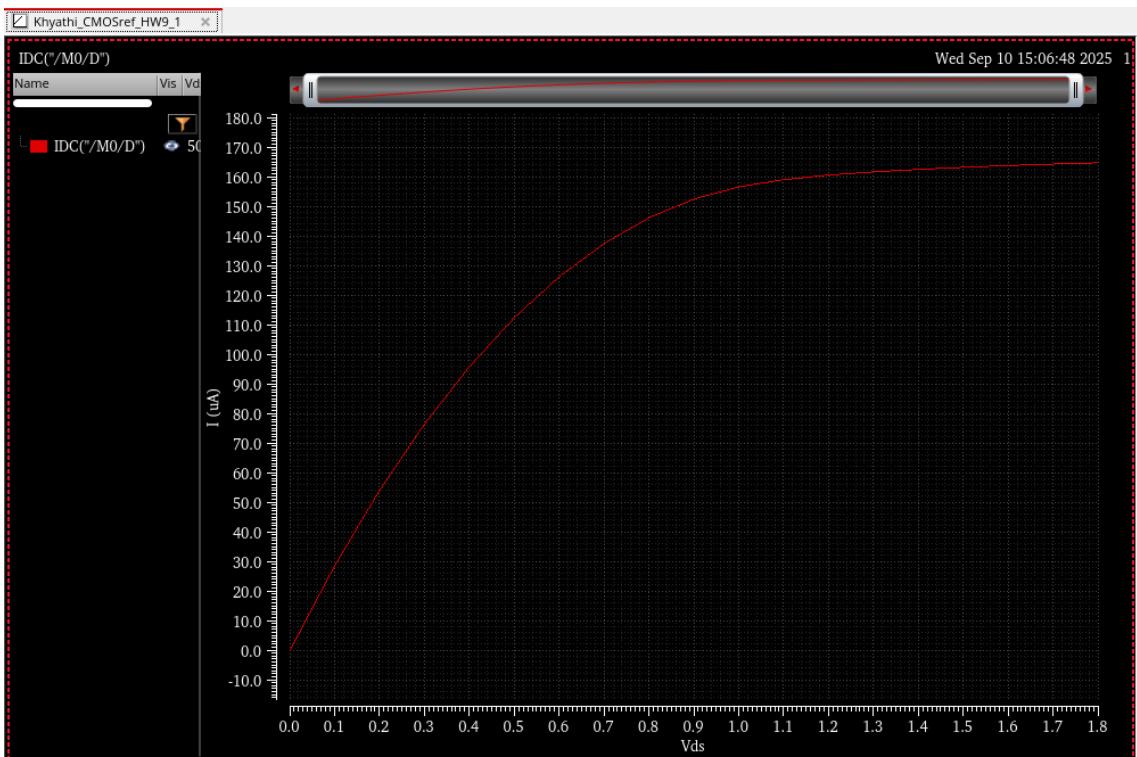


(ii)  $W/L = 1\mu/1\mu$

(a)  $V_{gs} = 500 \text{ mV}$



(b)  $V_{gs} = 1.8 \text{ V}$



## 9.2 PMOS I-V characteristics

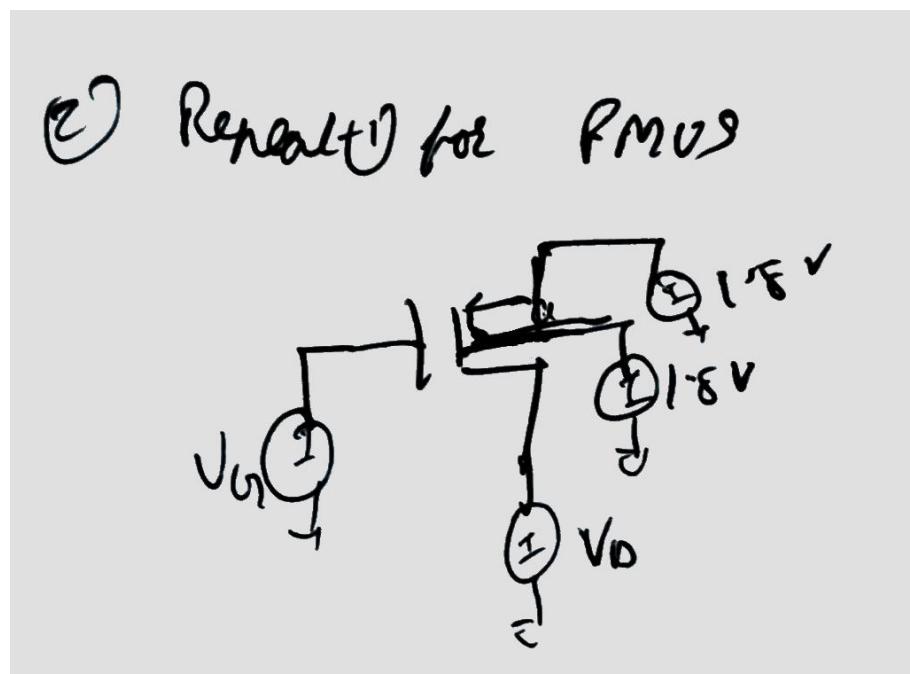
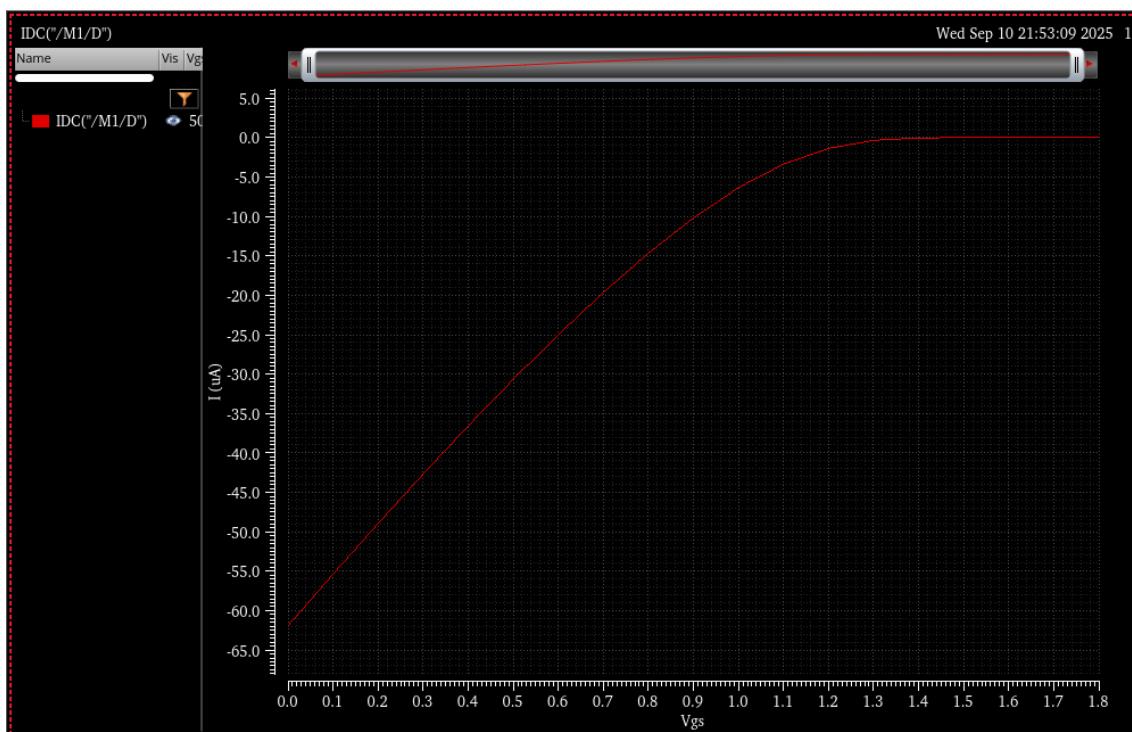


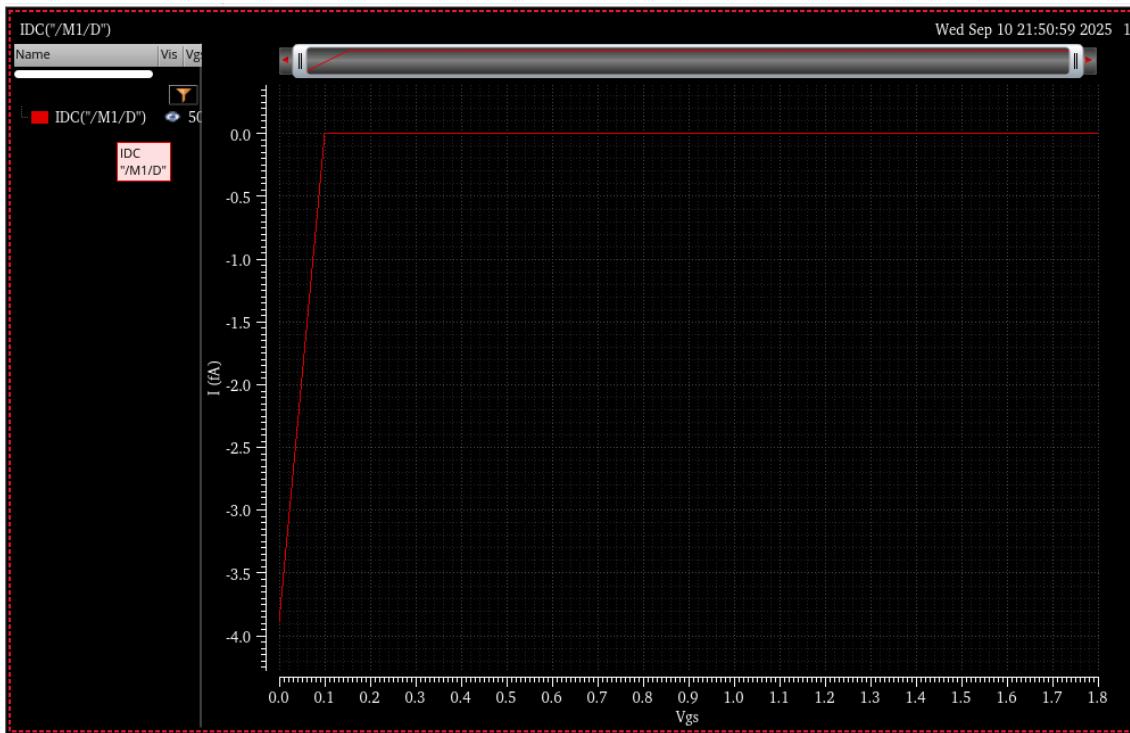
Figure 48: Lecture 9 - Question 2

$V_g$ : 0 to 1.8V

- (i)  $W/L = 220n/180n$
- (a)  $V_d = 500$  mV

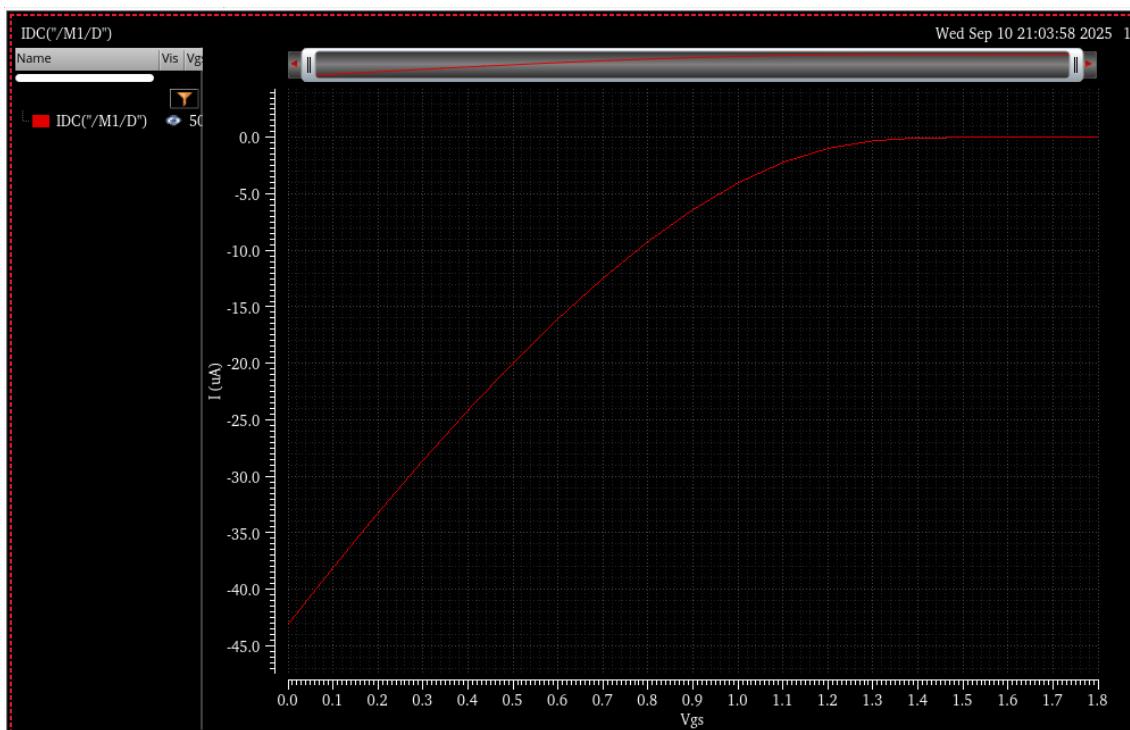


(b)  $V_d = 1.8$  V

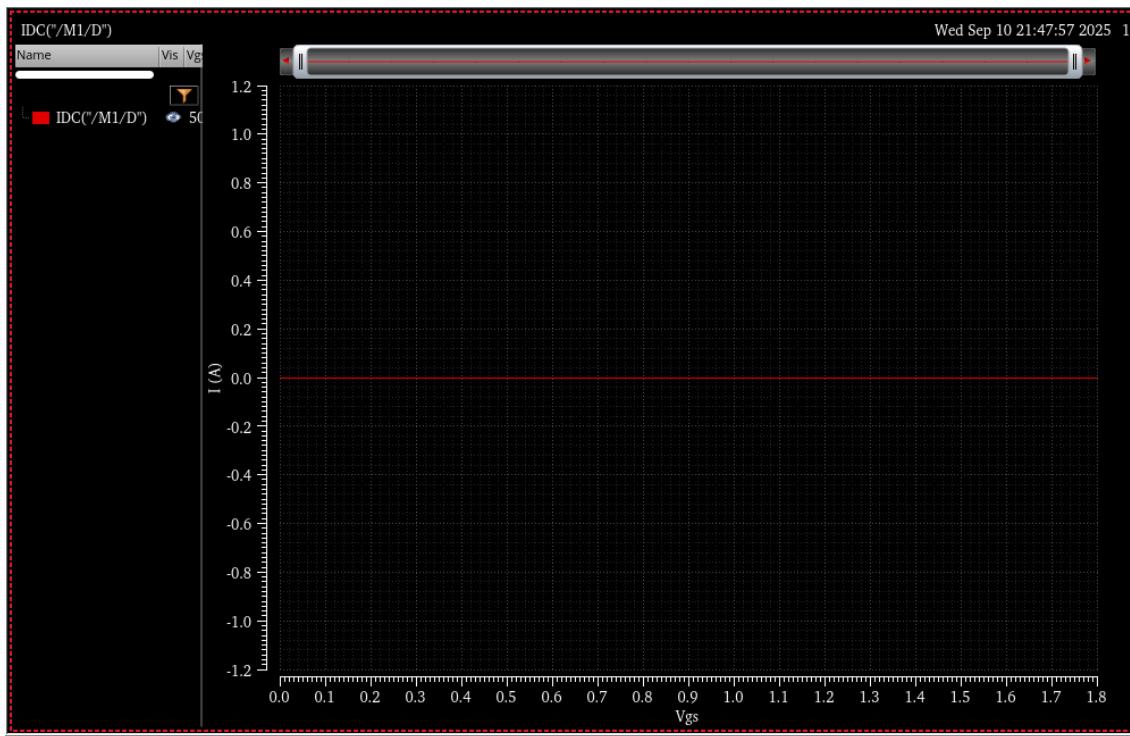


(ii)  $W/L = 1\mu/1\mu$

(a)  $V_d = 500$  mV



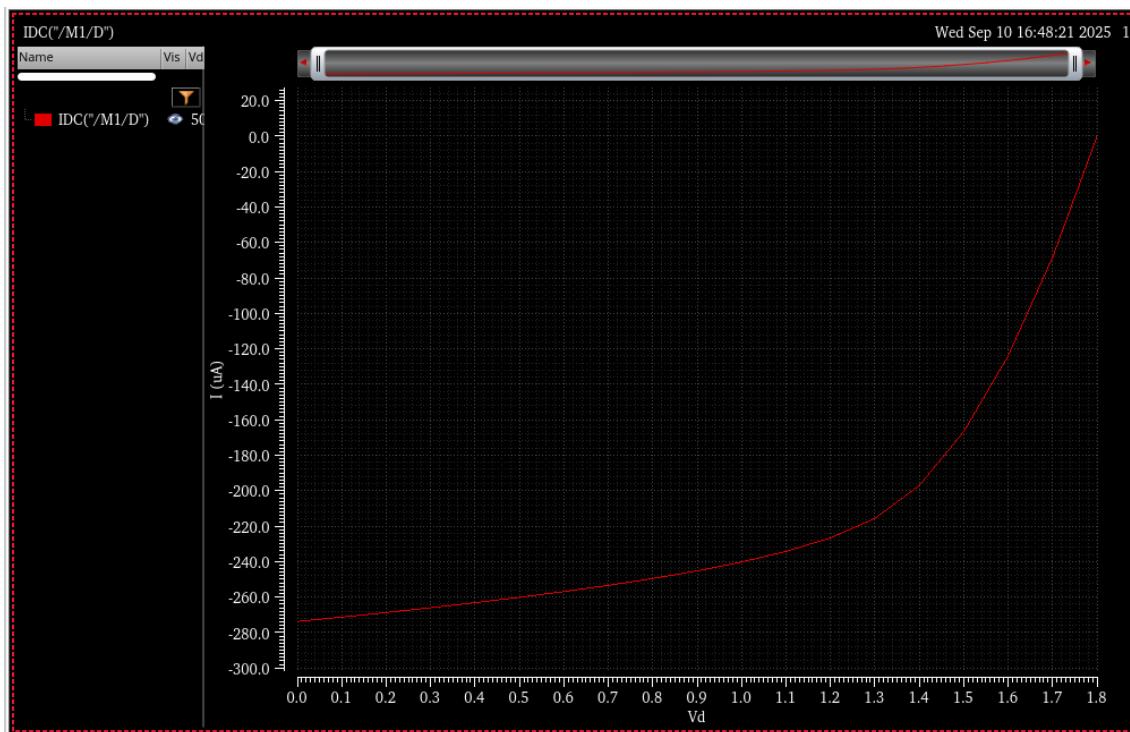
(b)  $V_d = 1.8$  V



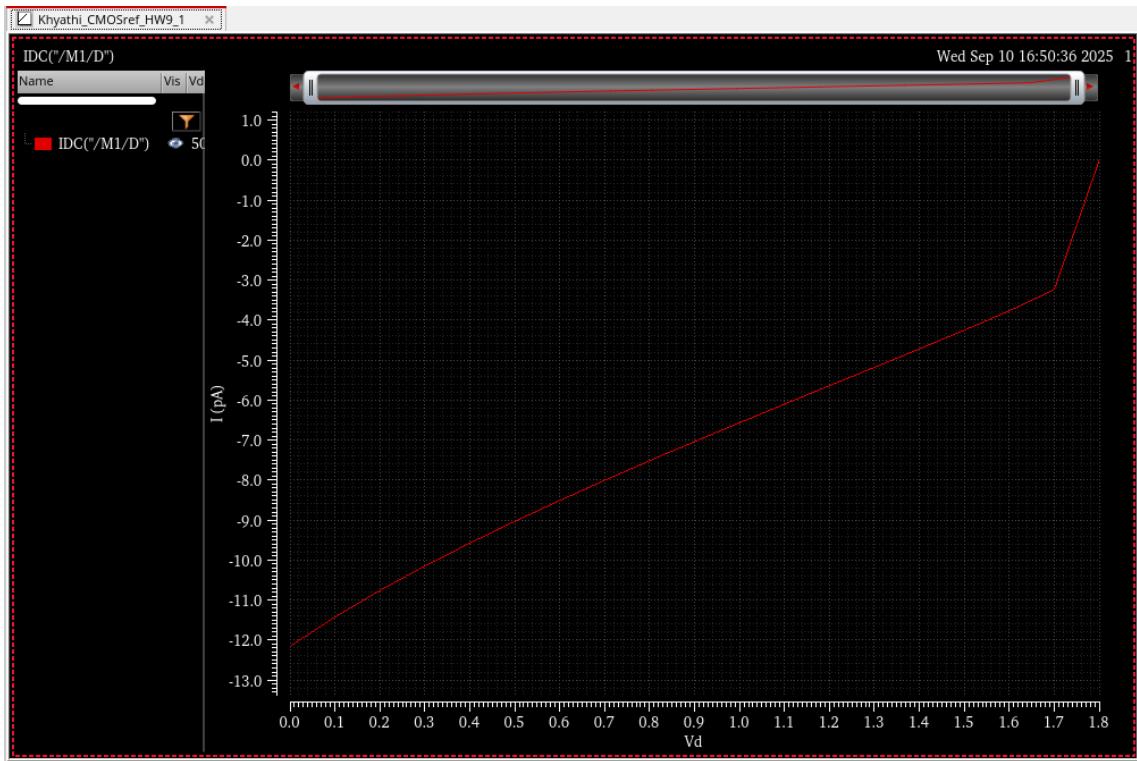
**Vd: 0 to 1.8V**

(i) **W/L = 220n/180n**

(a)  $V_{gs} = 500$  mV

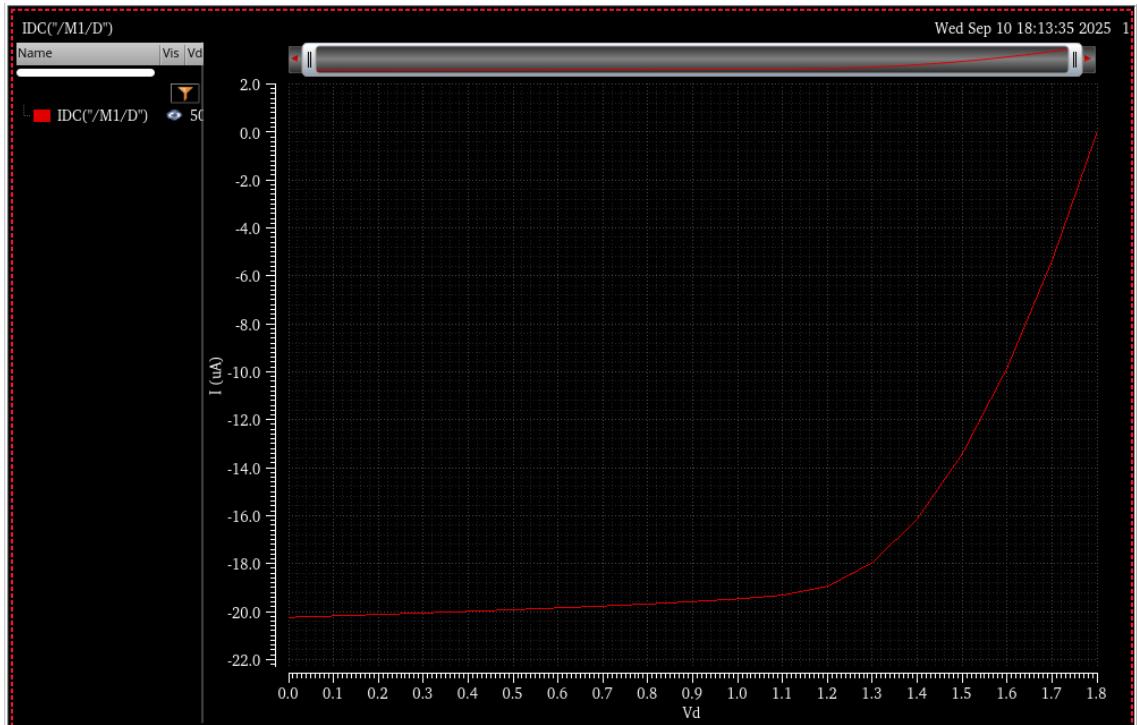


(b)  $V_{gs} = 1.8$  V

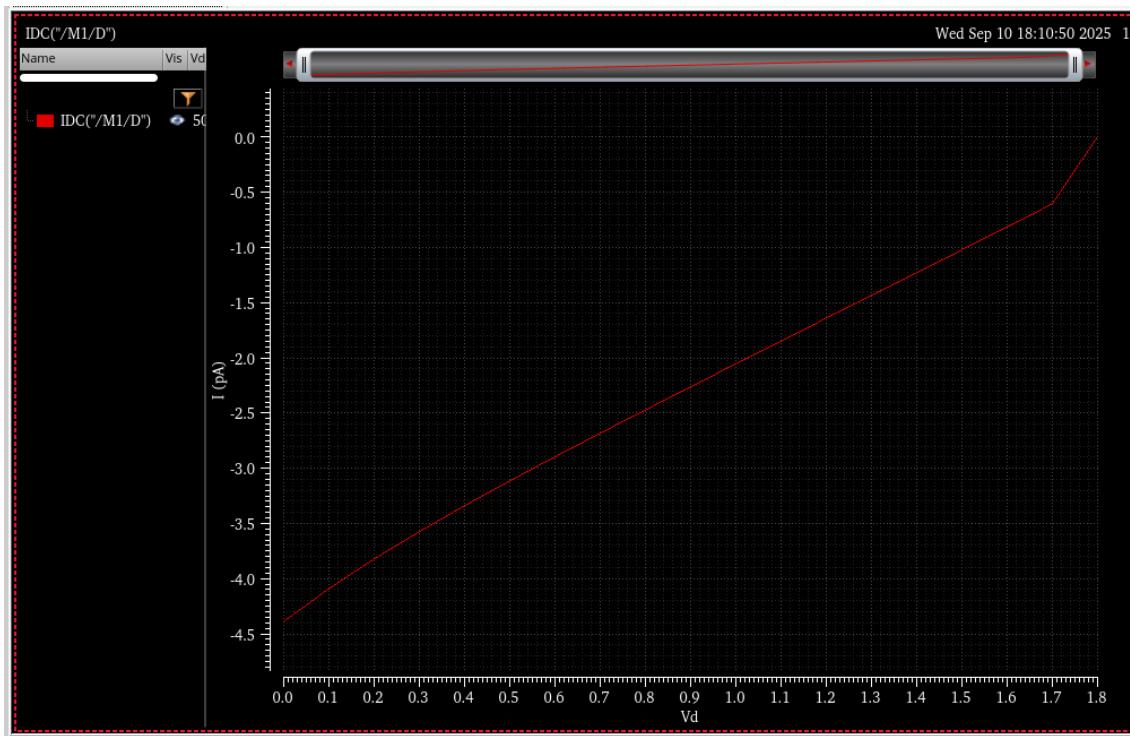


(ii)  $W/L = 1\mu/1\mu$

(a)  $V_{gs} = 500 \text{ mV}$



(b)  $V_{gs} = 1.8 \text{ V}$



## 10 Lecture 10 - Current Mirrors

### 10.1 Prove that Threshold voltage is linear and CTAT

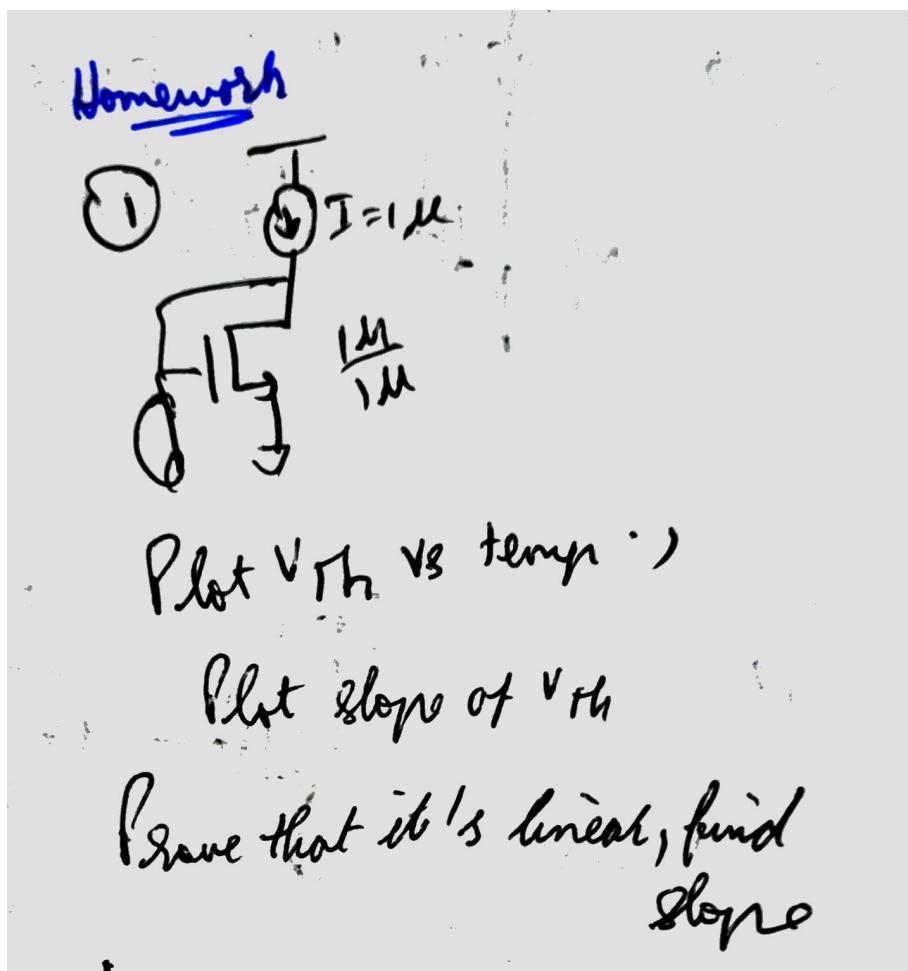


Figure 49: Lecture 10 - Question 1

**Answer:**

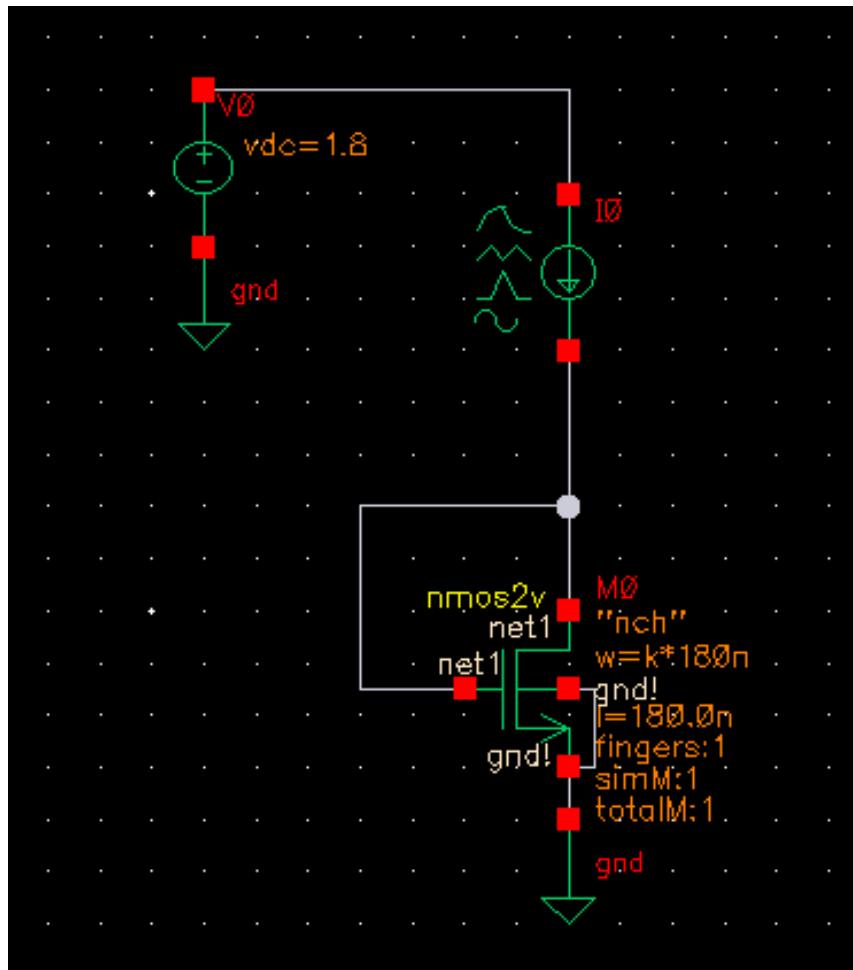


Figure 50: Schematic

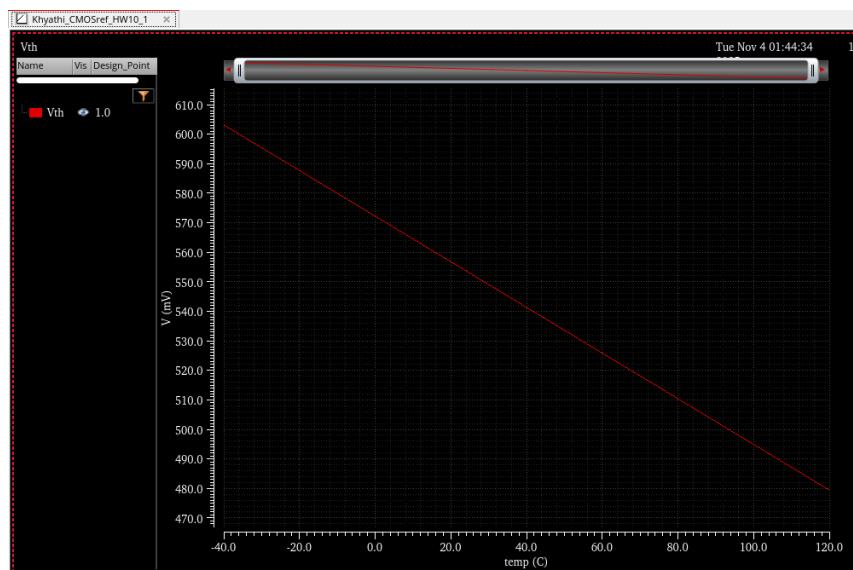


Figure 51: Plot of  $V_{th}$  vs Temperature

Clearly,  $V_{th}$  has a CTAT nature and is linear when varied with temperature.



Figure 53: Slope across slow, typical and fast corners



Figure 52: Slope of  $V_{th}$  vs Temperature

From the above plot, we can see that the slope of the  $V_{th}$  is almost constant.

## 10.2 Finding the current and sizing of the mosfet required to make $V_{GS}$ as Reference

Homework

② Plot  $V_{DS}$  w.r.t. Temp.  $\rightarrow$  find " $T$ " s.t.  $V_{DS}$  becomes a  $V_{ref}$

$V_{DS}$  w.r.t. Process  $\rightarrow$  find " $w/l$ " s.t.  $V_{DS}$  becomes a  $V_{ref}$

Figure 54: Lecture 10 - Question 2

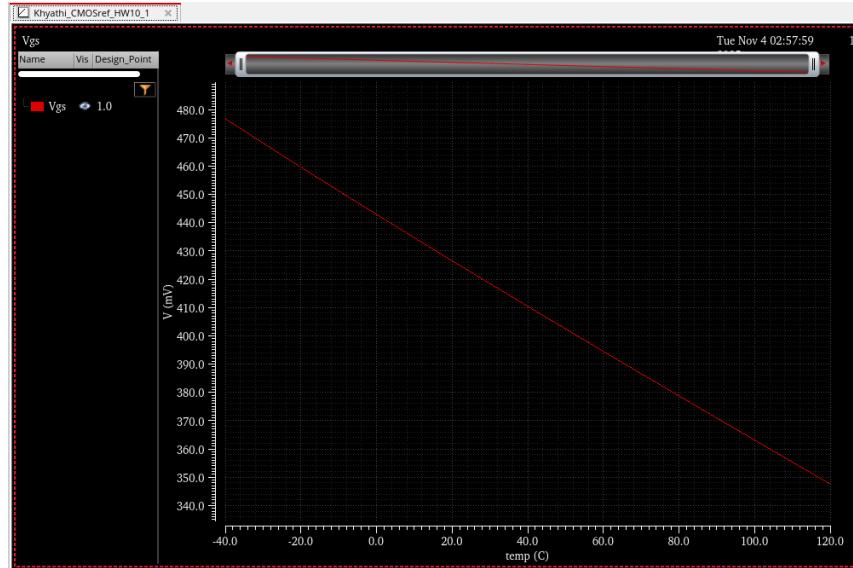


Figure 55:  $V_{gs}$  vs Temperature

- (i) Find  $I$  such that  $V_{gs}$  becomes  $V_{ref}$

Since  $V_{ref}$  isn't specifically given, let's aim for  $V_{ref} = 0.5V$ . And the  $W/L$  for this is  $2u/180n$ . Now, we sweep the current in the circuit to find the value of  $I$  for which we obtain  $V_{gs} = V_{ref}$ .

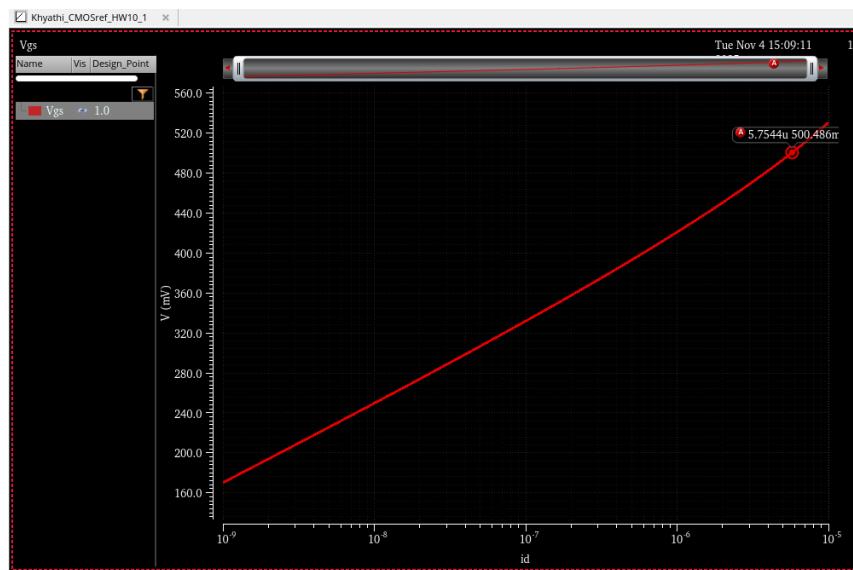


Figure 56:  $V_{gs}$  vs  $Id$

$$I = 5.75 \text{ uA} \text{ for } V_{gs} = V_{ref} = 0.5V$$

- (ii) Find  $W/L$  such that  $V_{gs}$  becomes  $V_{ref}$   
Let us consider  $V_{ref} = 0.5V$  and reference current as  $3uA$ .

$$\text{Let } L = 180n \text{ and } W = k * 180n$$

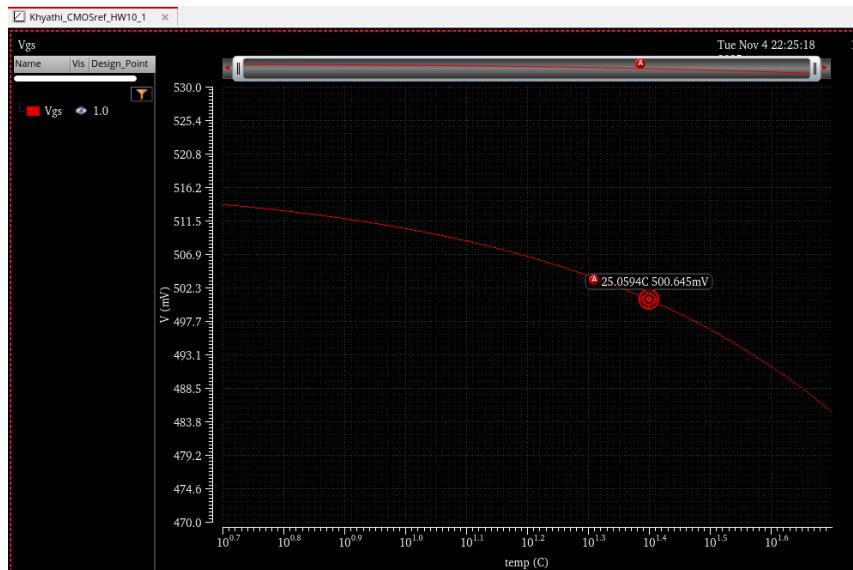


Figure 57: Vgs vs k

From the sweep of value of k, we obtain Vref at Vgs at k = 25.05.  
Thus, W/L = 25.05.

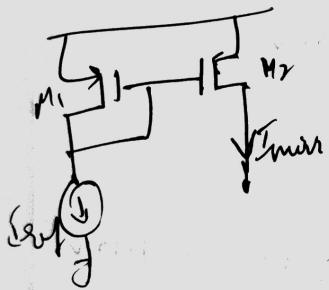
### 10.3 PMOS Current Mirror - Simple, Widlar, Low swing, High swing

(3) Draw PMOS simple, widlar, low sl, high V cascode current mirror.

Figure 58: Lecture 10 - Question 3

**Answer:**

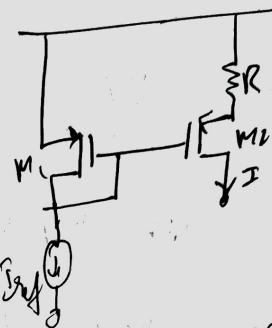
1) Simple current mirror



$$\text{Headroom: } V_{DD} - V_{SG1}$$

$$R_{out} = r_o$$

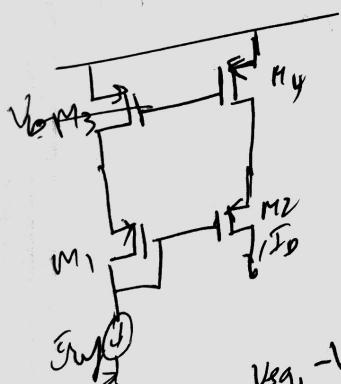
2) Widlar Current Mirror



$$\text{Headroom: } V_{DD} - V_{SG1}$$

$$R_{out} = r_o + R + g_m r_o \cdot R$$

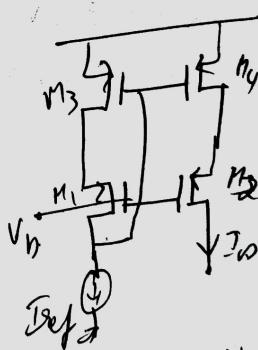
3) (High Voltage cascode mirror  
(low swing))



$$\text{Headroom: } V_{DD} - V_{SG1} - V_{SG3}$$

$$R_{out} = r_o + r_{out} + g_m r_o \cdot r_{out}$$

4) Low Voltage Cascode Mirror  
(high swing)

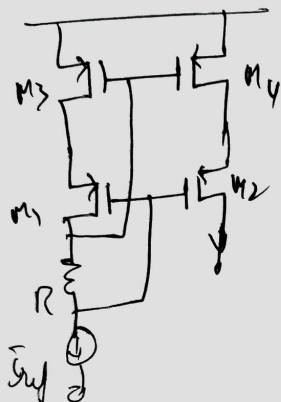


$$\text{Headroom: } V_{DD} - V_{SG3}$$

$$R_{out} = r_o + r_{out} + g_m r_o \cdot r_{out}$$

Figure 59: Lecture 10 - Question 3 - Solution

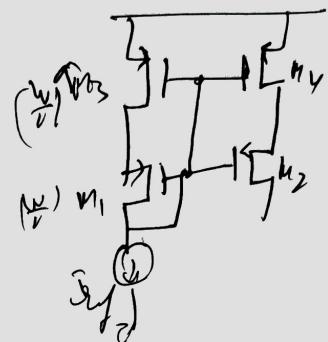
5) No external bias low voltage cascode



$$\text{Headroom} = V_{DD} - IR - V_{GS3}$$

$$R_{out} = \frac{1}{g_{DS1} + g_{DS2} + g_{DS4}}$$

6) Poor Man's Cascode



$$\text{Headroom} = V_{DD} - V_{GS3}$$

$$R_{out} = \frac{1}{g_{DS1} + g_{DS2} + g_{DS4}}$$

Figure 60: Lecture 10 - Question 3 - Plots

#### 10.4 Plot $V_{EB}$ w.r.t Process

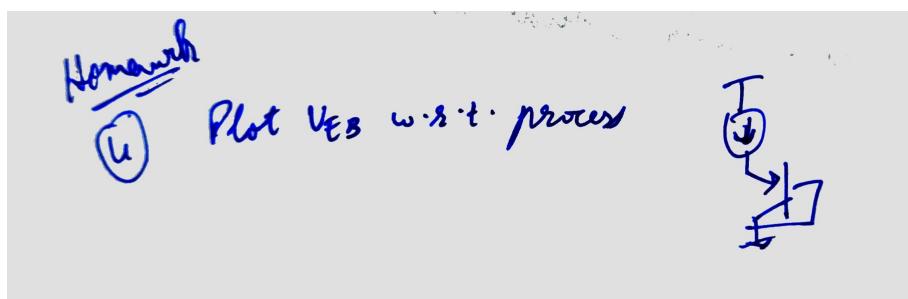


Figure 61: Lecture 10 - Question 4



Figure 62: Vbe in different corners

## 11 Lecture 11 - Startup Condition, Power Down Signal, Random Mismatch

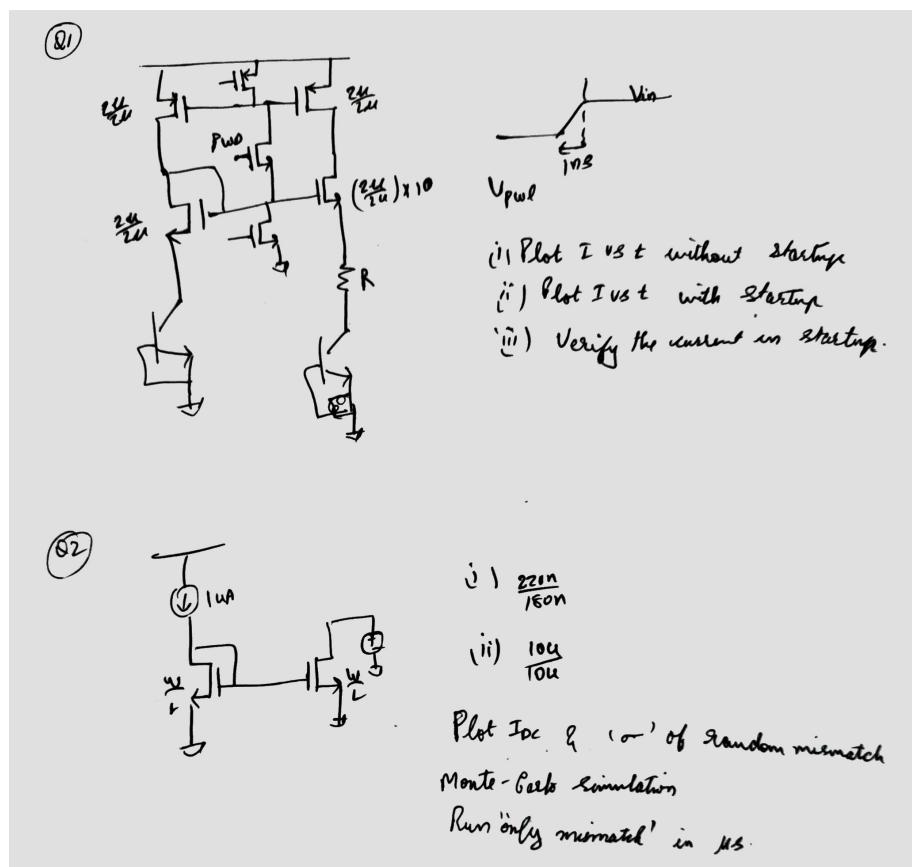
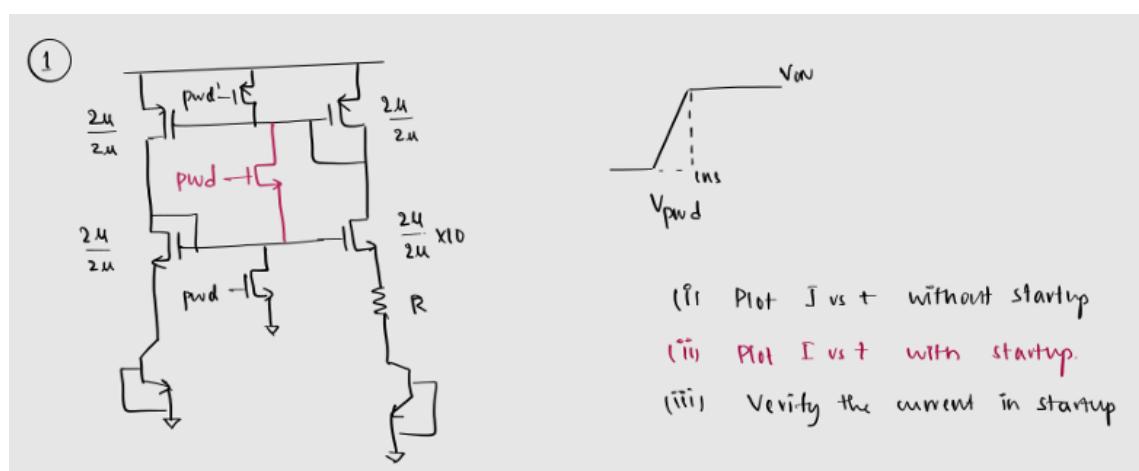
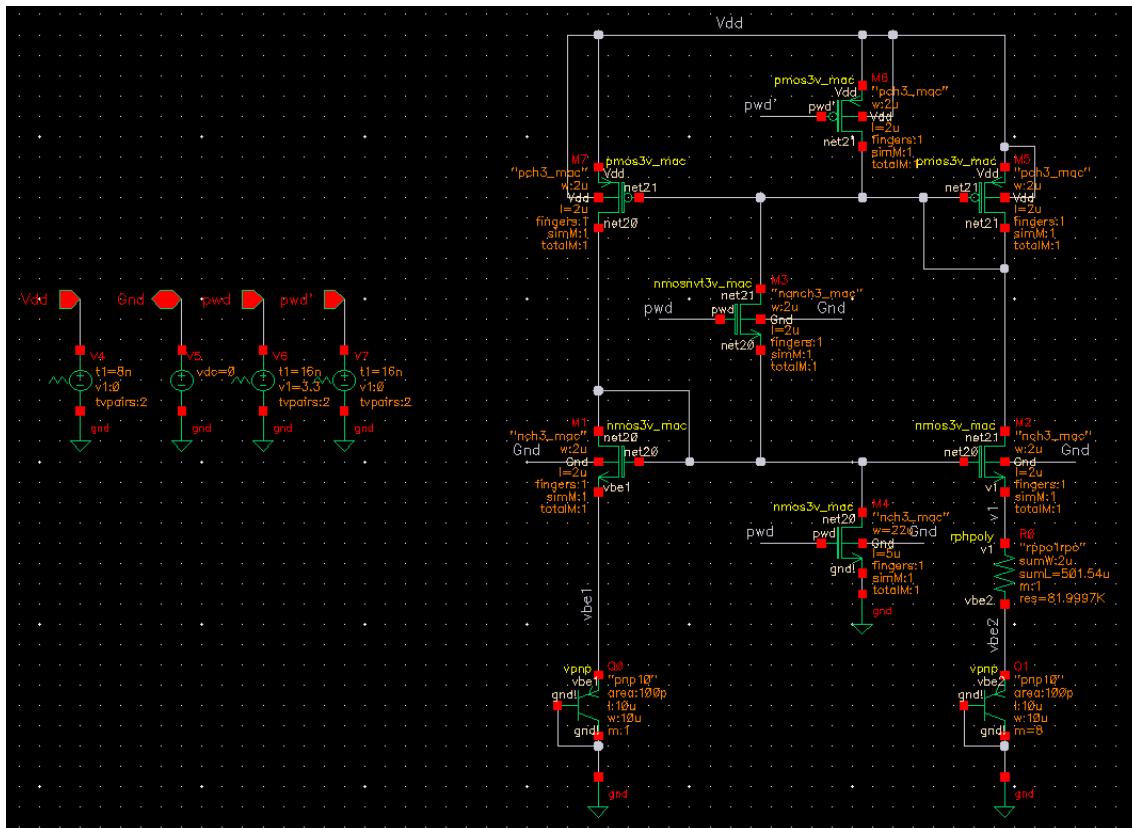


Figure 63: Lecture 11 - Question 1 and Question 2

### 11.1 Question 1





(i) Plot I vs t without Startup circuit

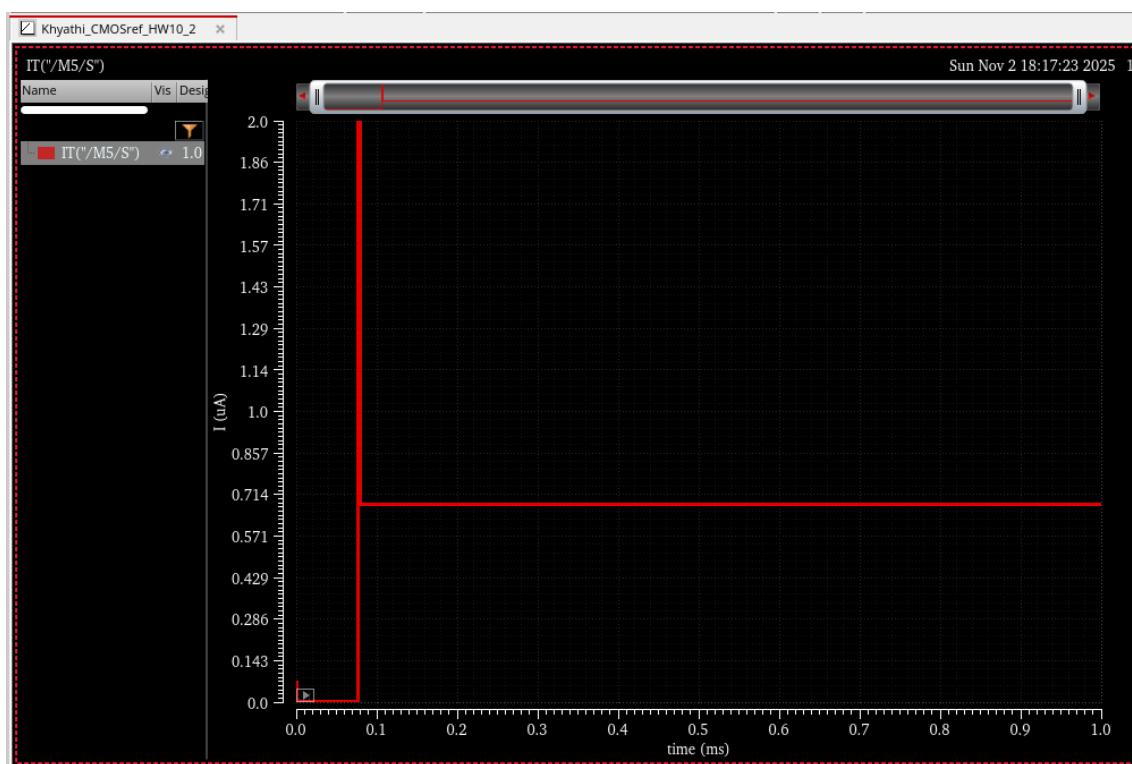
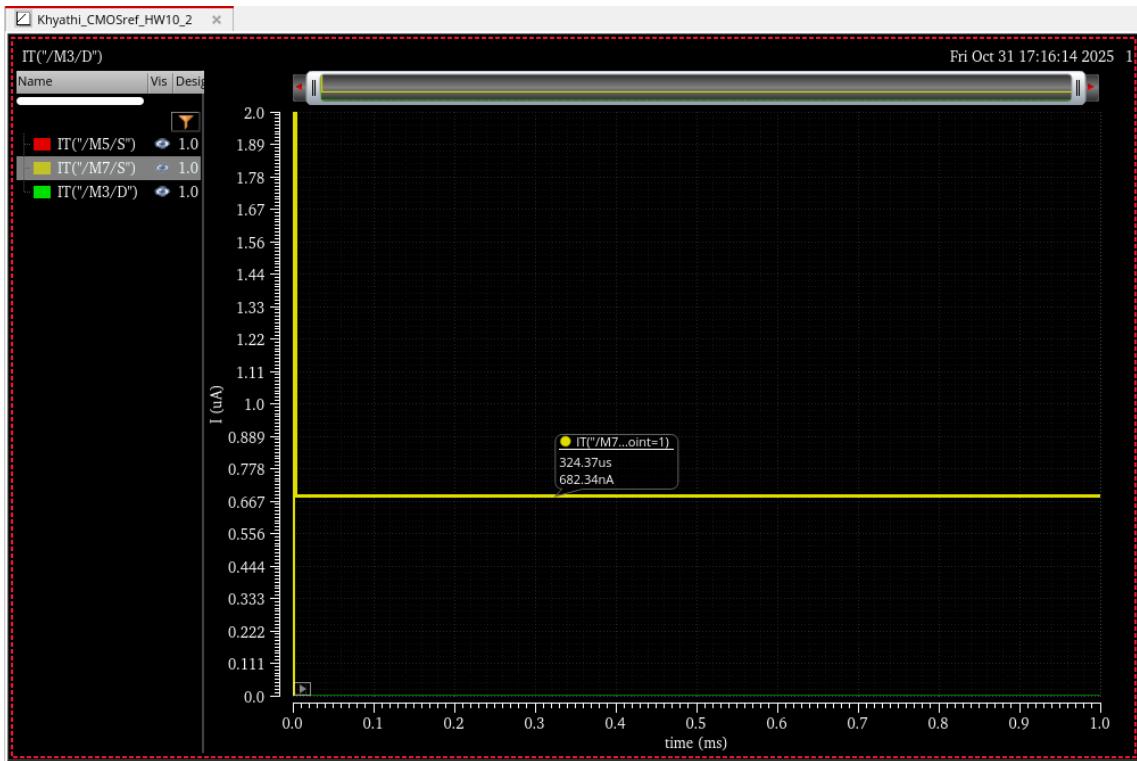


Figure 64: Current in the circuit without startup circuit

(ii) Plot I vs t with Startup circuit



We can see that without the startup circuit, the current in the branch has settled to the desired 0.67uA after significant time of 80us.

But, after introducing the startup circuit, we can see that the current has settled in afew nano seconds. This verifies that the startup circuit is working.

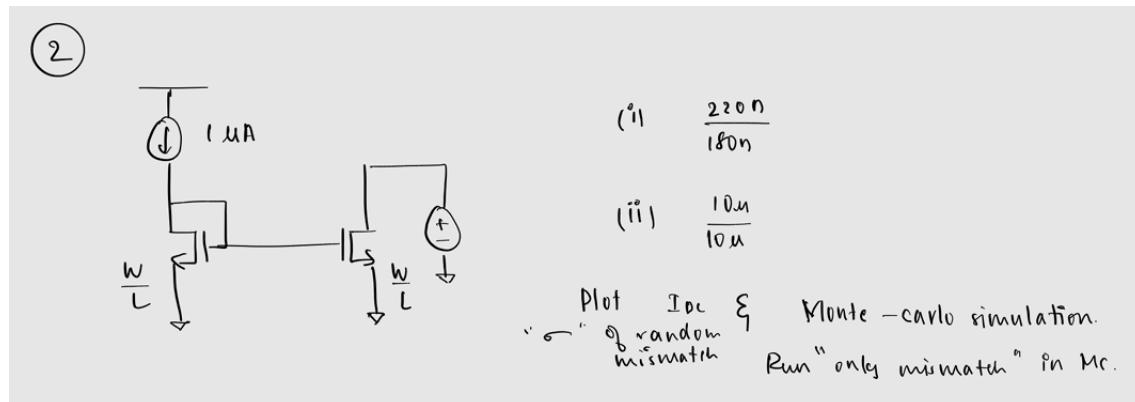
### (iii) Current in Startup Circuit



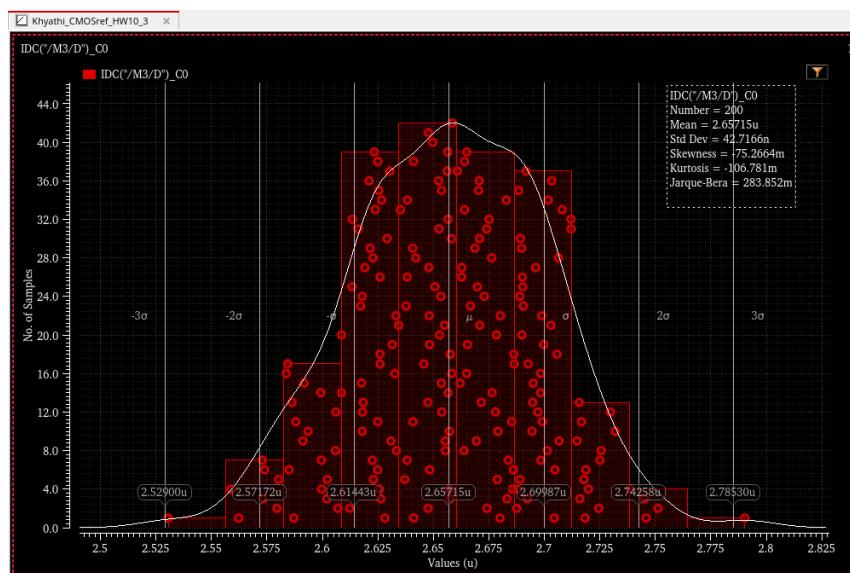
Figure 65: Current in startup circuit

The current in the startup circuit is almost 3pA after the current in the branches is settled at required 0.67uA, which is very small as needed, since it should interfere with the normal working of the circuit.

## 11.2 Question 2

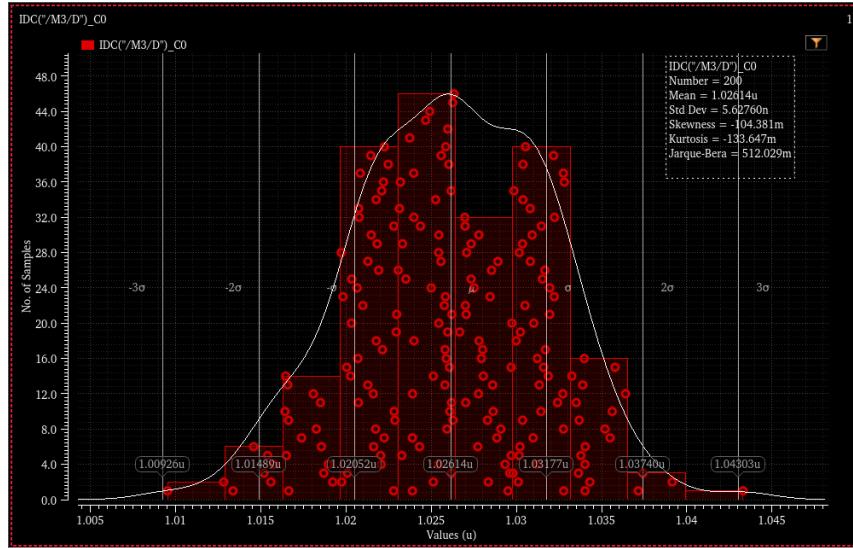


(i)  $220n/180n$



Mean = 2.657u  
Std Dev = 42.72n

(ii)  $10\mu/10\mu$



Mean = 1.026u  
Std Dev = 5.628n

We can clearly observe that smaller device dimensions result in significantly higher mismatch, whereas larger device dimensions exhibit much lower mismatch.

This behavior is explained by Pelgrom's mismatch model, which states that the standard deviation of mismatch is inversely proportional to the square root of the device area:

$$\sigma_{\text{mismatch}} \propto \frac{1}{\sqrt{WL}}$$

Thus, increasing the transistor width  $W$  and length  $L$  decreases the mismatch variation.

## 12 Lecture 12 - Small Signal Analysis of Current Mirrors

### 12.1 Derivation of small signal equivalent

Homework

$$① \quad v_1 = f(I_1, I_2)$$

$$v_2 = g(I_1, I_2)$$

Derive small signal circuit equivalent .

Figure 66: Lecture 12 - Question 1

Solution:

$$V_1 = f(I_1, I_2)$$

$$V_2 = g(I_1, I_2)$$

$$V_1 + \Delta V_1 = f(I_1 + \Delta I_1, I_2 + \Delta I_2)$$

$$= f(I_1, I_2) + \frac{\partial f}{\partial I_1} \cdot \Delta I_1 + \frac{\partial f}{\partial I_2} \cdot \Delta I_2 + \text{higher terms}$$

$$\Delta V_1 = \frac{\partial f}{\partial I_1} \cdot \Delta I_1 + \frac{\partial f}{\partial I_2} \cdot \Delta I_2$$

$$\Delta V_2 = \frac{\partial g}{\partial I_1} \cdot \Delta I_1 + \frac{\partial g}{\partial I_2} \cdot \Delta I_2$$

$$Z_{11} = \frac{\partial V_1}{\partial I_1} \text{ when } I_2 = 0$$

$$Z_{12} = \frac{\partial V_1}{\partial I_2} \text{ when } I_1 = 0$$

$$Z_{21} = \frac{\partial V_2}{\partial I_1} \text{ when } I_2 = 0$$

$$Z_{22} = \frac{\partial V_2}{\partial I_2} \text{ when } I_1 = 0$$

Figure 67: Lecture 12 - Question 1 - Solution

## 12.2 Finding the output resistance of the current mirror

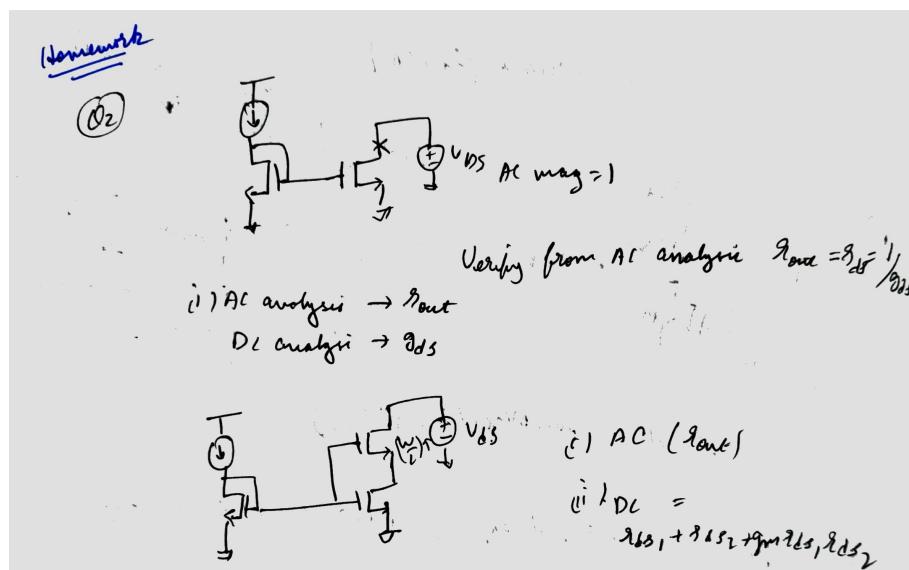


Figure 68: Lecture 12 - Question 2

## 13 Lecture 13 - Amplifiers

### 13.1 CS Amplifier with resistive load

Design a CS amplifier with resistive load to get a gain of 20dB,  $V_{DD} = 1.8V$ ,  $I_Q = 1\mu A$

Solution:

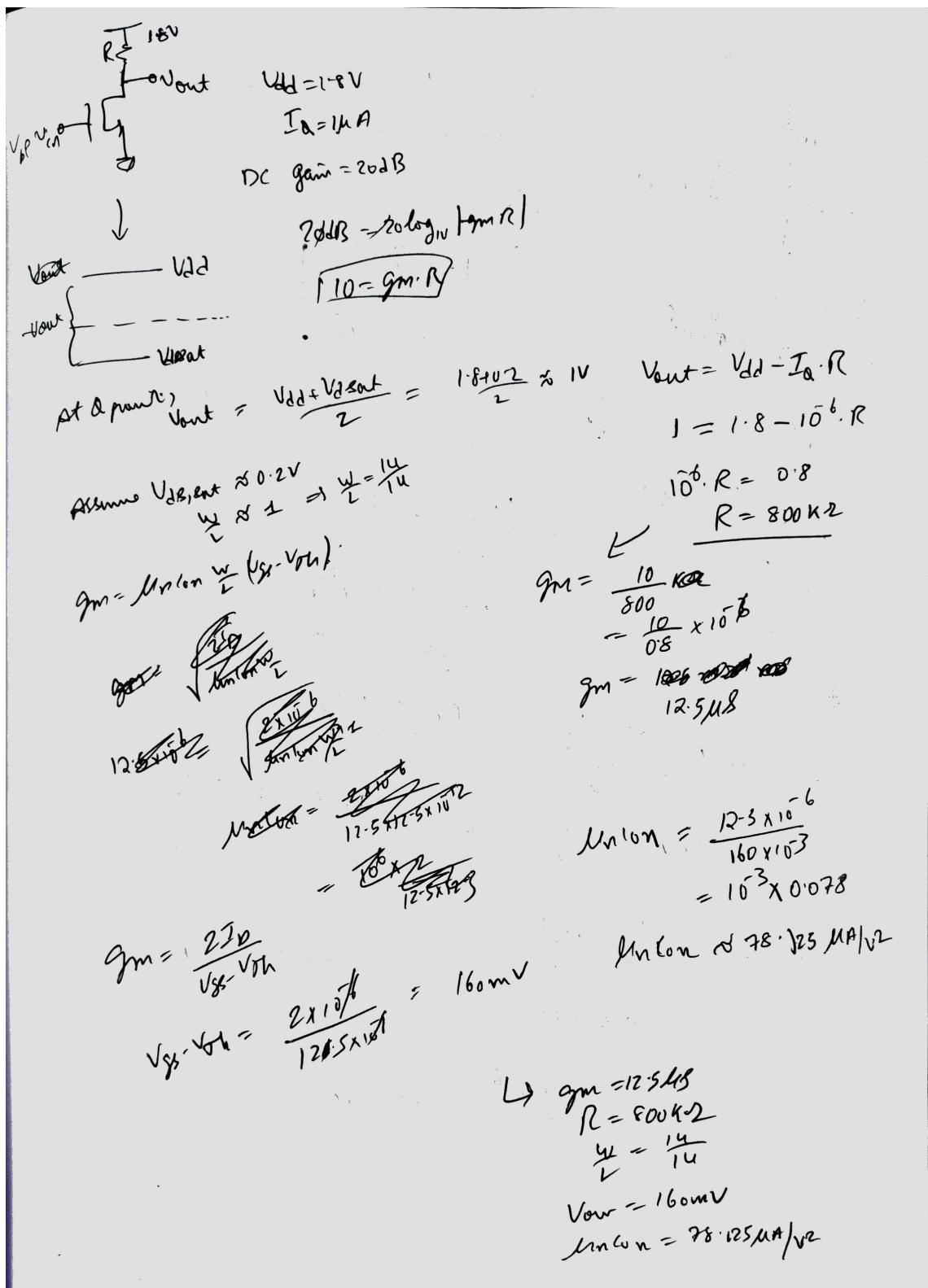


Figure 69: Lecture 13 - Question 1 - Solution - Theory

## 14 Lecture 14 - Single Stage Amplifiers

### 14.1 Drain feedback CS Amplifier

Find conditions for  $C_1, C_2$  to be short circuit in a drain feedback CS amplifier(NMOS based).

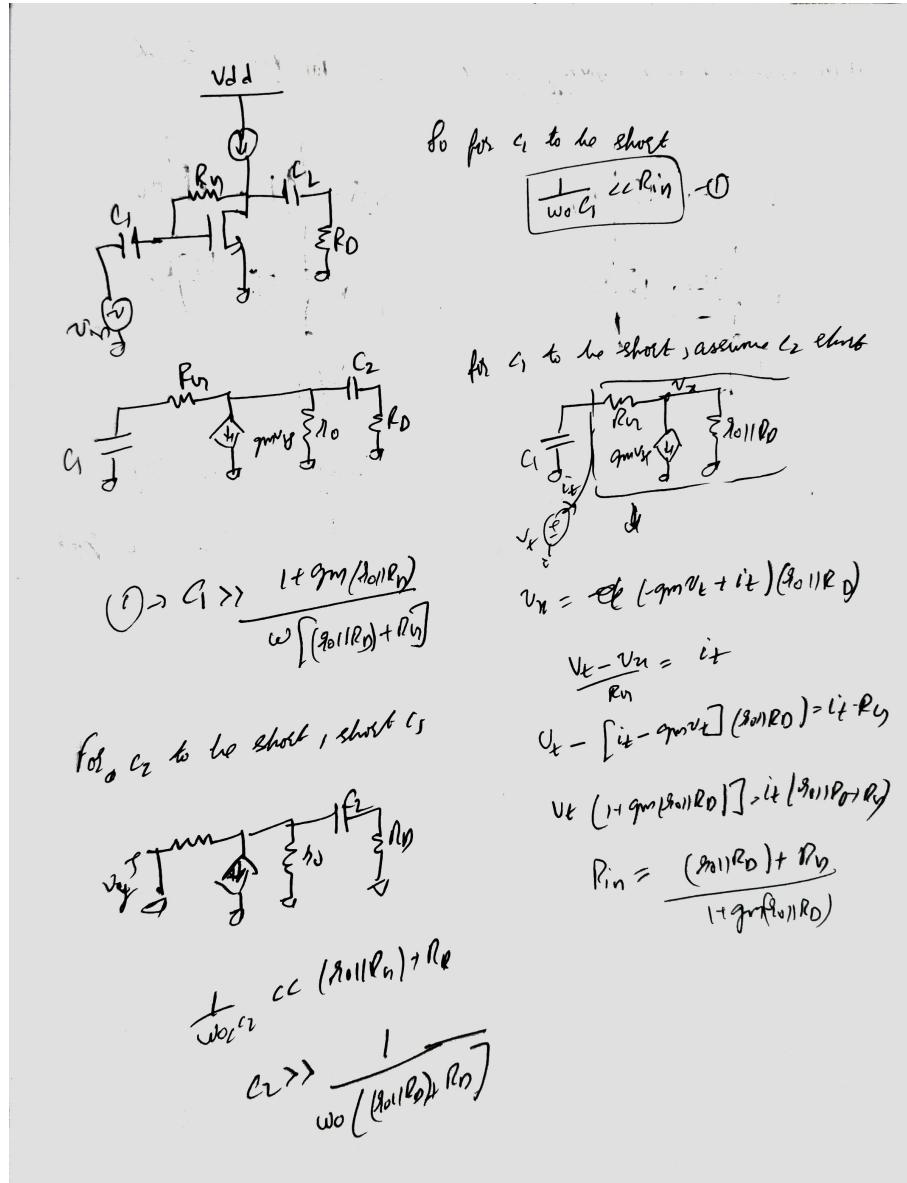


Figure 70: Lecture 14 - Question 1

### 14.2 Source feedback CS Amplifier

Find conditions on  $R_G, C_1, C_2$  in source feedback bias CS Amplifier(NMOS based).

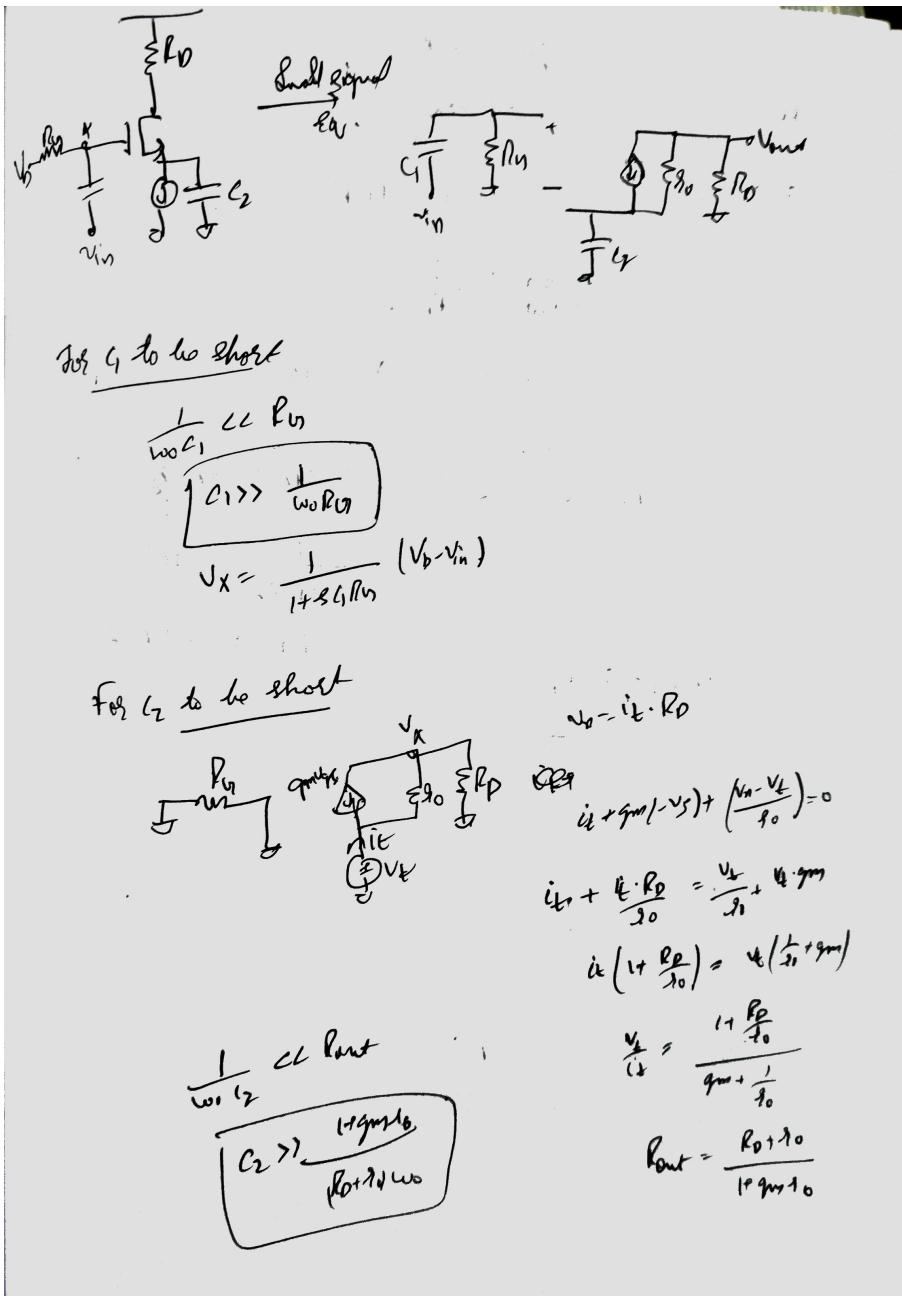


Figure 71: Lecture 14 - Question 2

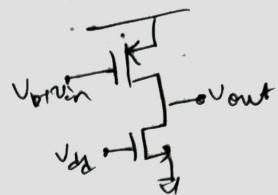
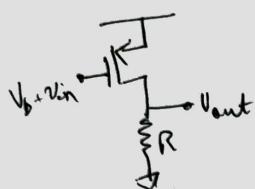
### 14.3 PMOS equivalent of CS Amplifiers

Draw PMOS equivalent of voltage mode CS Amplifier (6), Current Mode CS Amplifier(3), CD and CG amplifier.

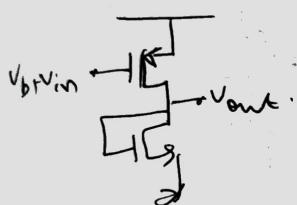
Solution:

PMOS CS Amplifier - Voltage Mode

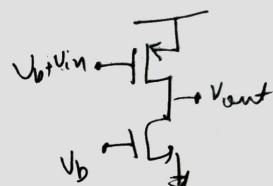
- 1) CS Amp with resistive load    2) CS Amp with triode load



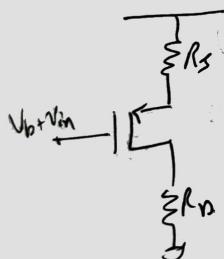
- 3) CS Amp with ~~current~~ connected load



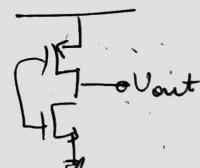
- 4) CS Amp with current sense load



- 5) CS Amp with source degeneration

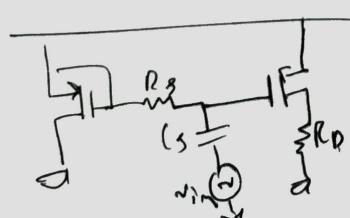


- 6) CS Amp with active load



PMOS CS Amp. - Current Mode

- 1) CS Amp. with current mirror bias



- 2) CS Amp. with ~~chain~~ feedback bias

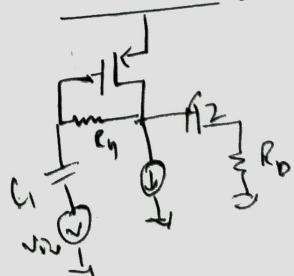
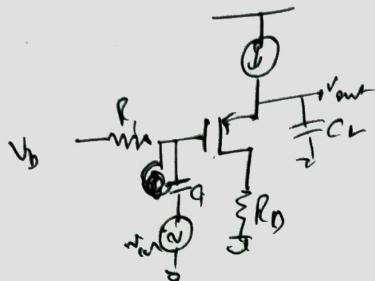
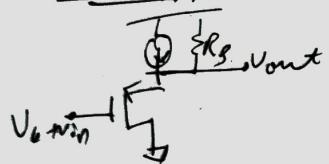


Figure 72: Lecture 14 - Question 3 - Solution - Part 1

3) C<sub>3</sub> Amplifier with Source feedback bias



PMOS C<sub>3</sub> Amplifier



PMOS C<sub>3</sub> Amplifier

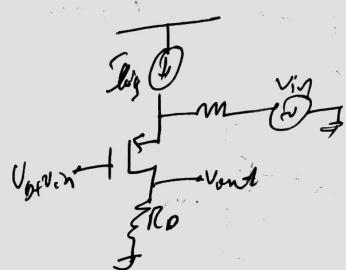


Figure 73: Lecture 14 - Question 3 - Solution - Part 2

## 15 Lecture 15 - Differential Amplifiers

### 15.1 ICMR and OCMR of PMOS differential pair

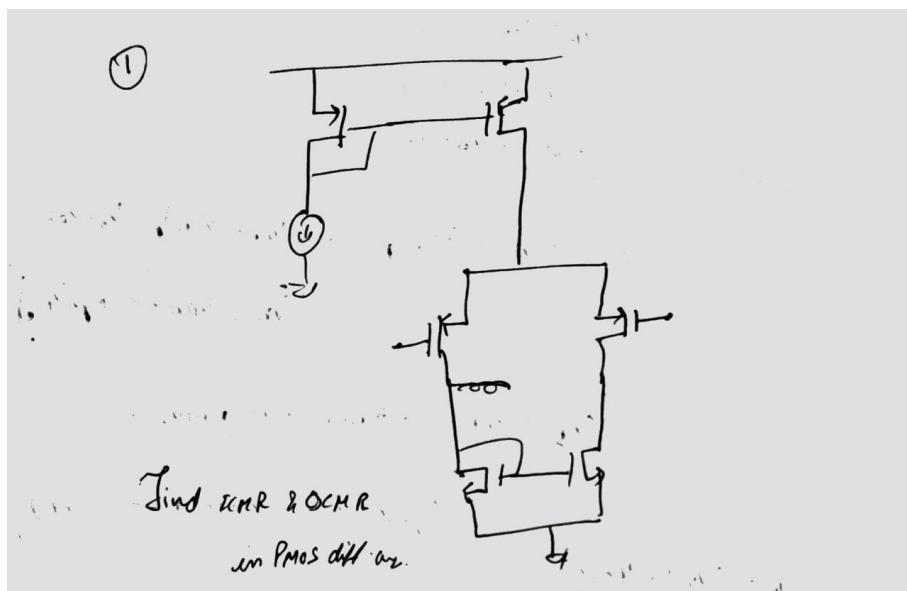


Figure 74: Lecture 15 - Question 1

Solution:

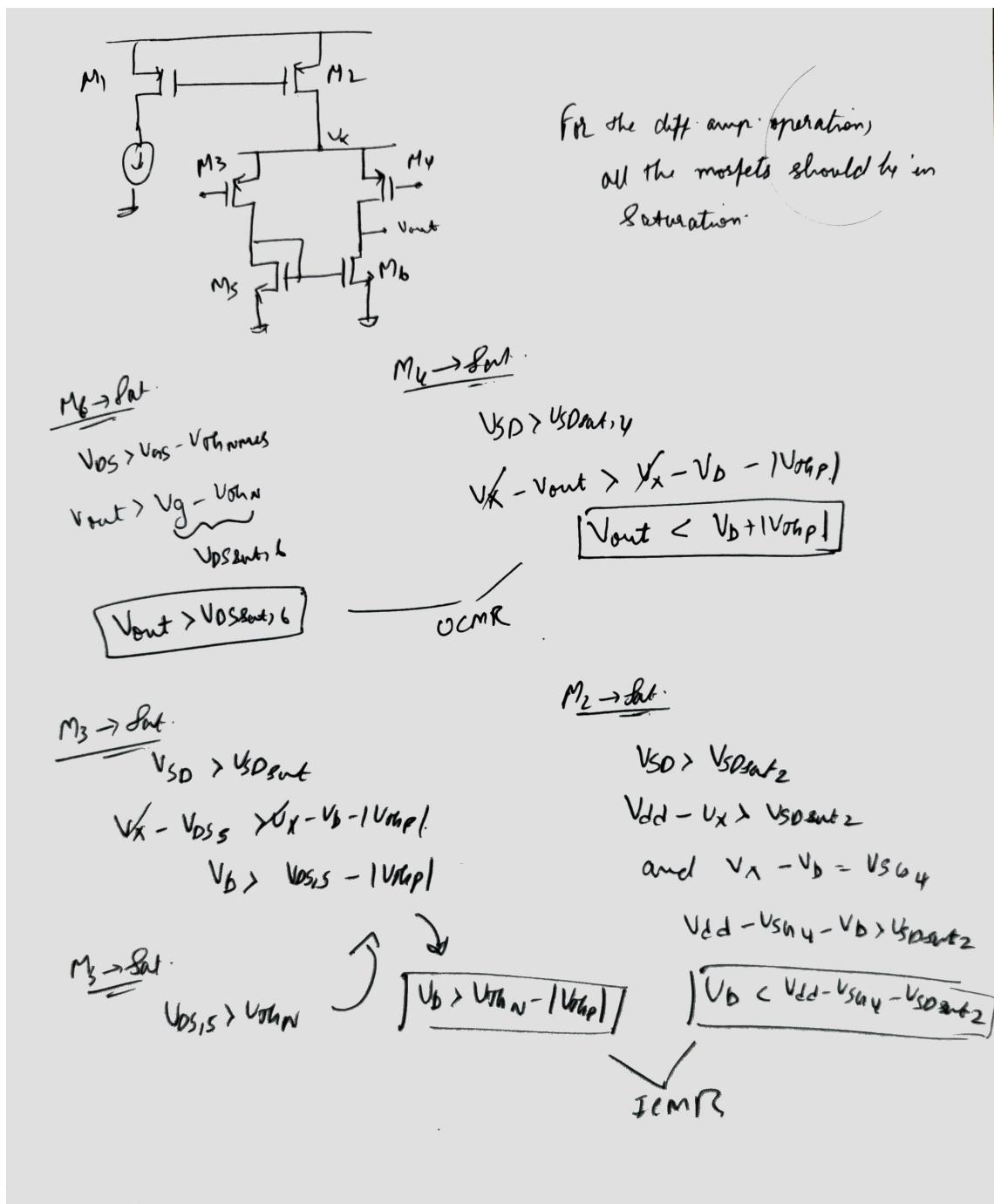


Figure 75: Lecture 15 - Question 1 - Solution

## 16 Lecture 16 - Parasitic Capacitances and Poles

### 16.1 Bode Plot of NMOS CS Amp with capacitive load

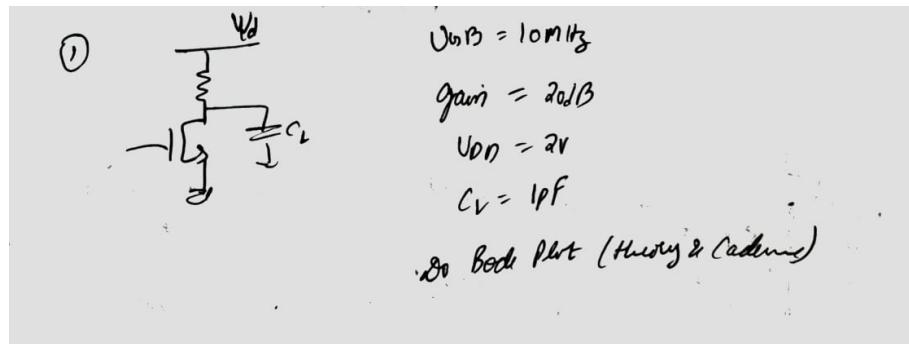


Figure 76: Lecture 16 - Question 1

Solution:

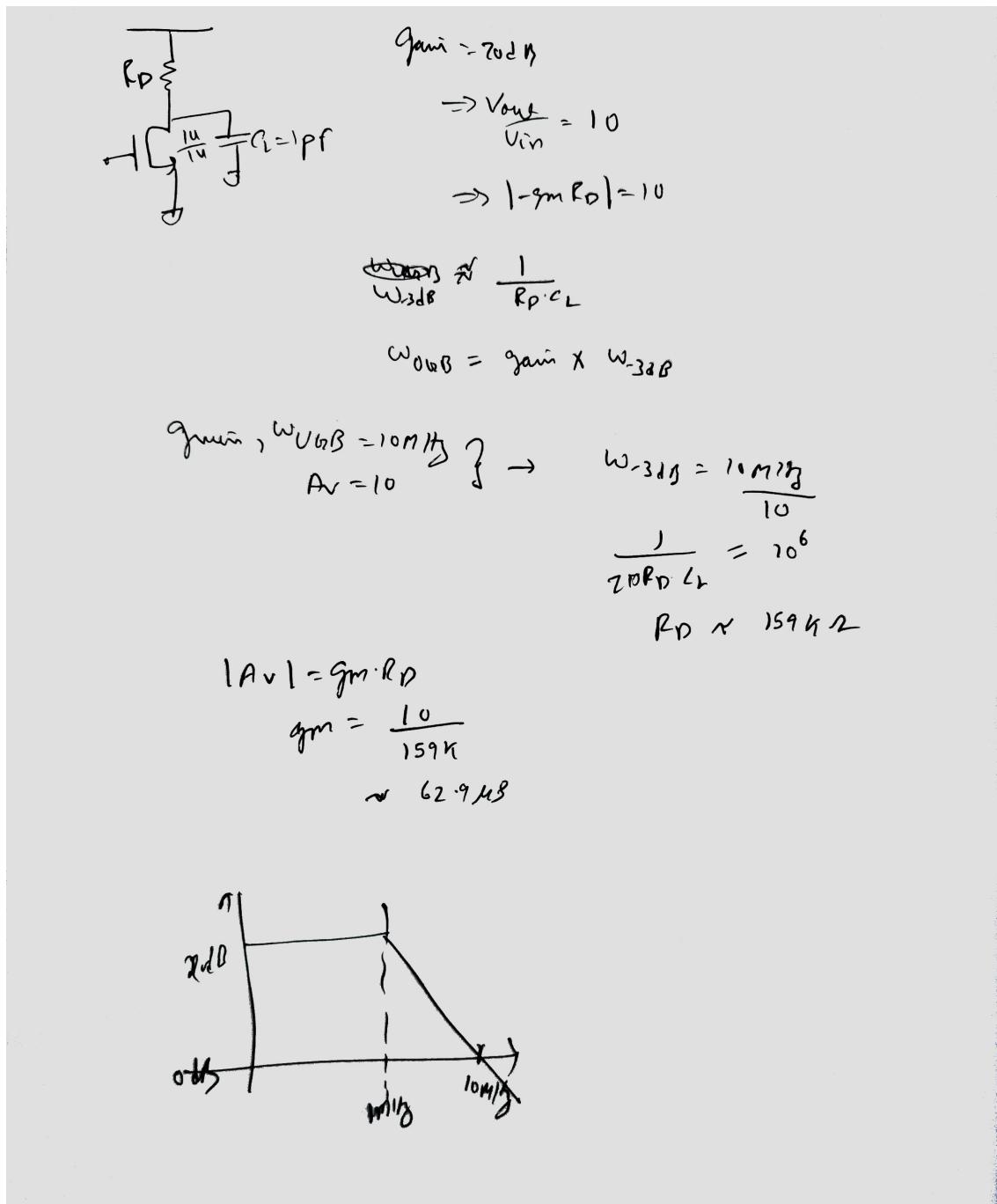


Figure 77: Lecture 16 - Question 1 - Solution

## 17 Lecture 17