

CMOS References and Regulators: Homework

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1 Lecture 1

1.1 Question 1

Do the 'DC Analysis' for the following circuits. Plot V vs I & write expression for the slope. Prove that its a resistance.

Answer:

Left graph shows the I - V characteristics of the device. Clearly, $I \propto V$. The right graph shows the expression for the slope.

Plot for (a) : Using a Voltage source

Plot for (b) : Using a Current source

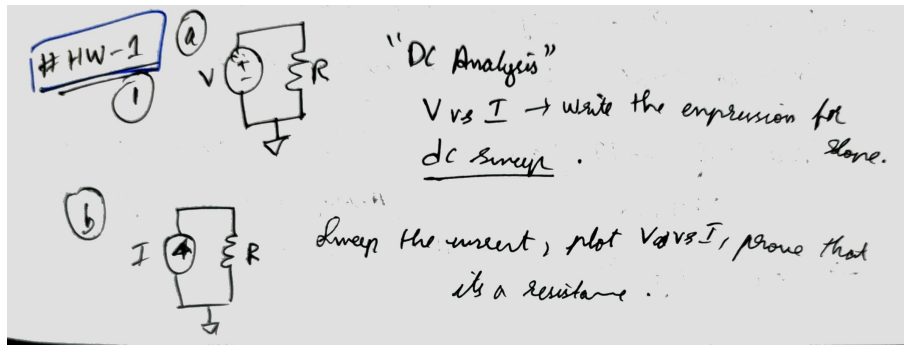


Figure 1: Lecture 1 - Question 1 - (a) and (b)

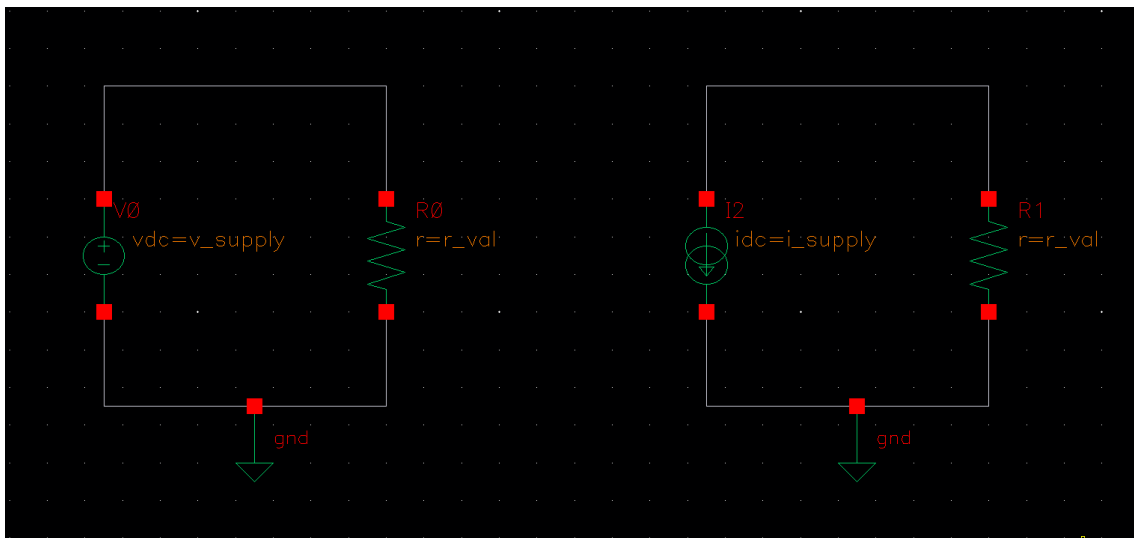


Figure 2: Testbench for (a) and (b)

1.2 Question 2

Design a capacitance amplifier using controlled sources.

Answer:

1.3 Question 3

Design a capacitance amplifier using controlled sources.

Answer:

1.4 Question 4

Sweep V vs I for (i) $k > 1$ (ii) $0 < k < 1$ (iii) $K < 0$ Prove R_{eff} in each case is $\frac{R}{1-k}$.

Answer:

2 Lecture 2

2.1 Question 1

find the effective output resistance at V_{out} i.e., $R_{out} = ?$

Answer:

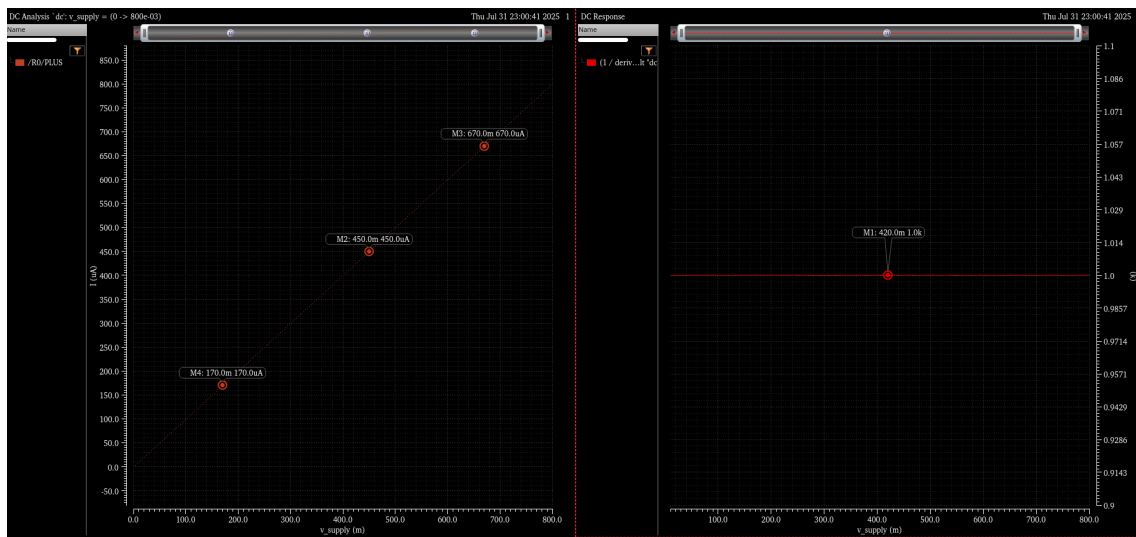


Figure 3: Plot for (a)

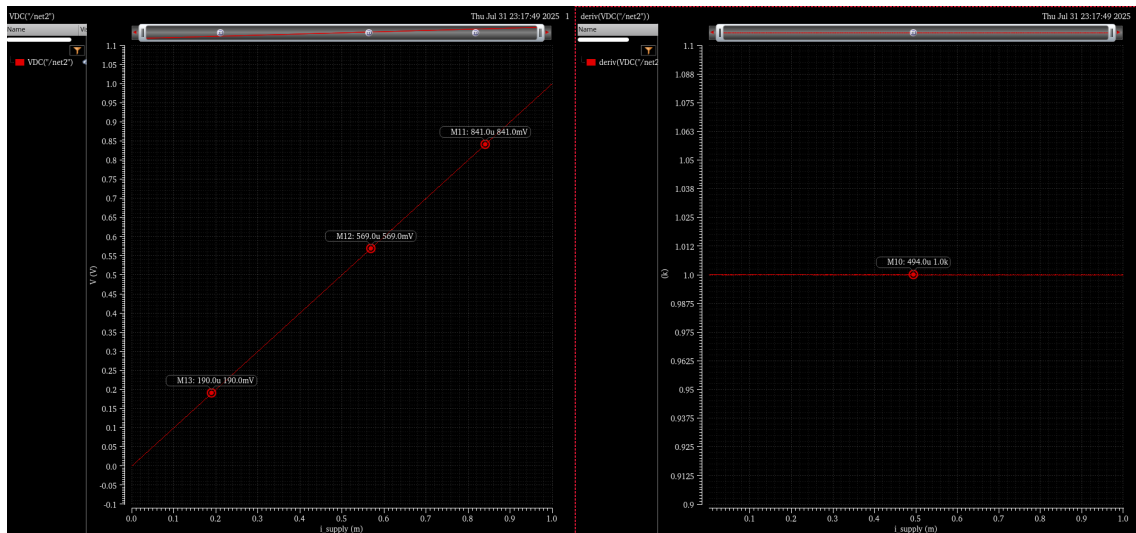
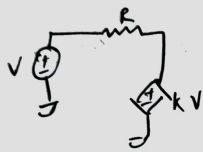


Figure 4: Plot for (b)

② design a capacitor amplifier using controlled sources (Theory)
 ③ design an inductor amplifier using " " (Theory)
 ④ 

Show V vs I for (i) $k > 1$
 (ii) $k < 1$
 (iii) $k < 0$
 Prove R_{eq} in each case.
 Assume "R" values.
 is $\frac{R}{1-k}$

Next class:- Misconceptions in RC circuits.

Figure 5: Lecture 1 - Question 2, 3, 4

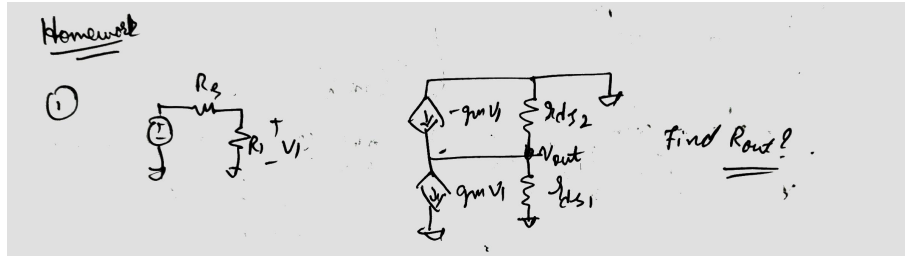


Figure 6: Lecture 2 - Question 1

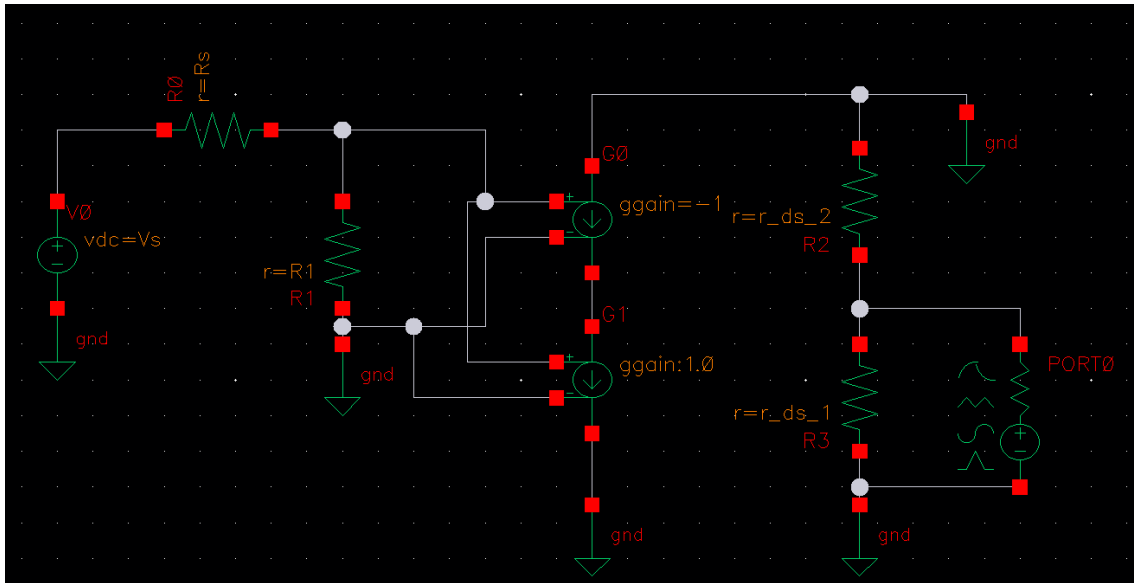


Figure 7: Testbench

When we nullify the $V1$, the vccs vanish and the effective output resistance at v_{out} node is $R_{out} = r_{ds1} || r_{ds2}$. Proved this using the plot with values.

2.2 Question 2

Plot V_{out} vs time in Cadence. Prove Theory.

Answer:

Copy this from the notes

Proved this using theory and from the simulations by finding the output voltage after 1 time constant.

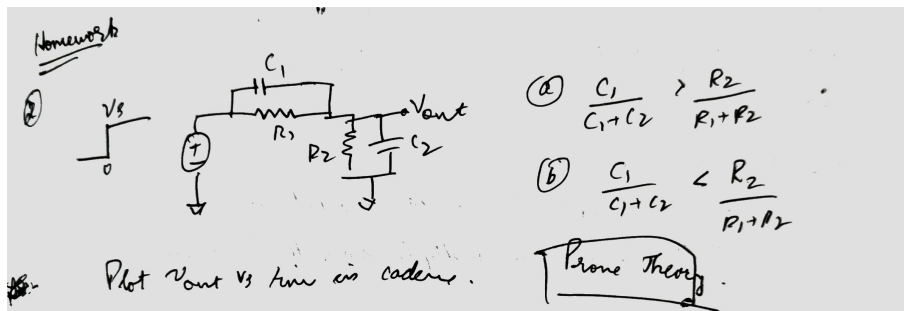


Figure 8: Lecture 2 - Question 2

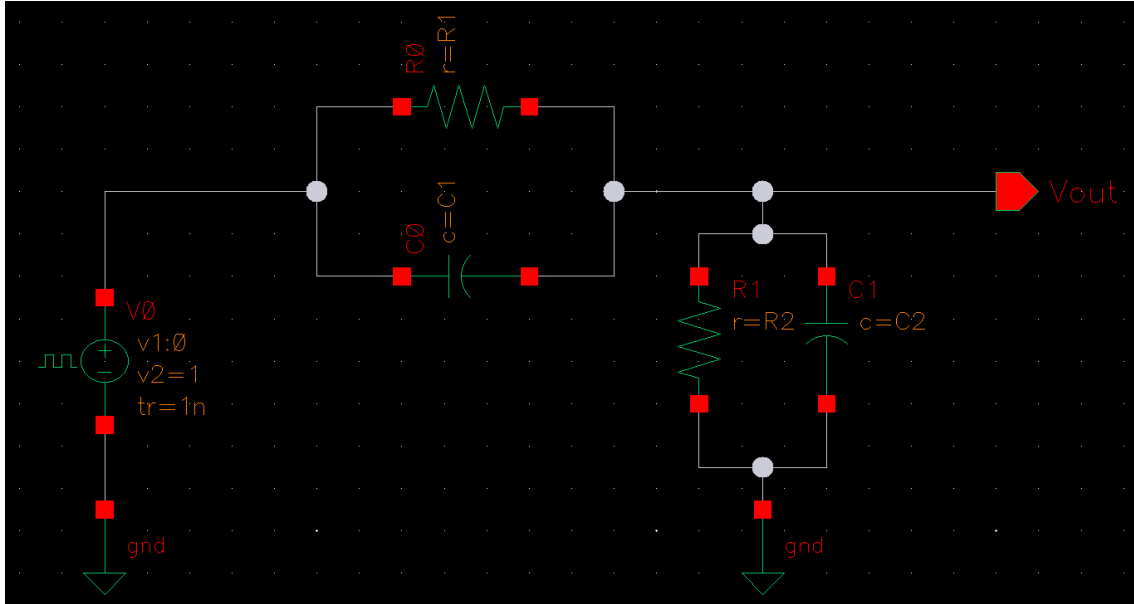


Figure 9: Question 2 Testbench

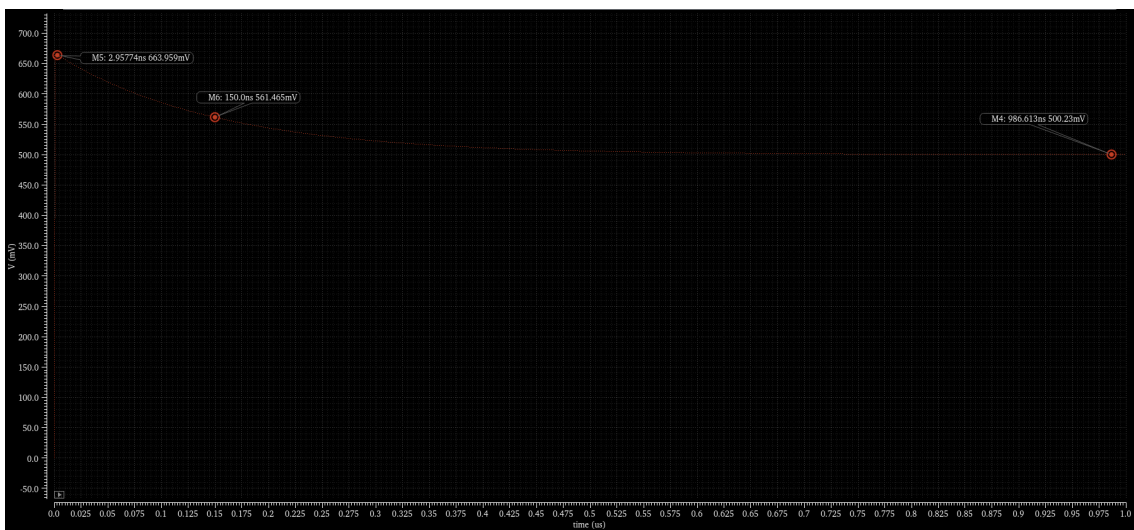


Figure 10: Part (a)

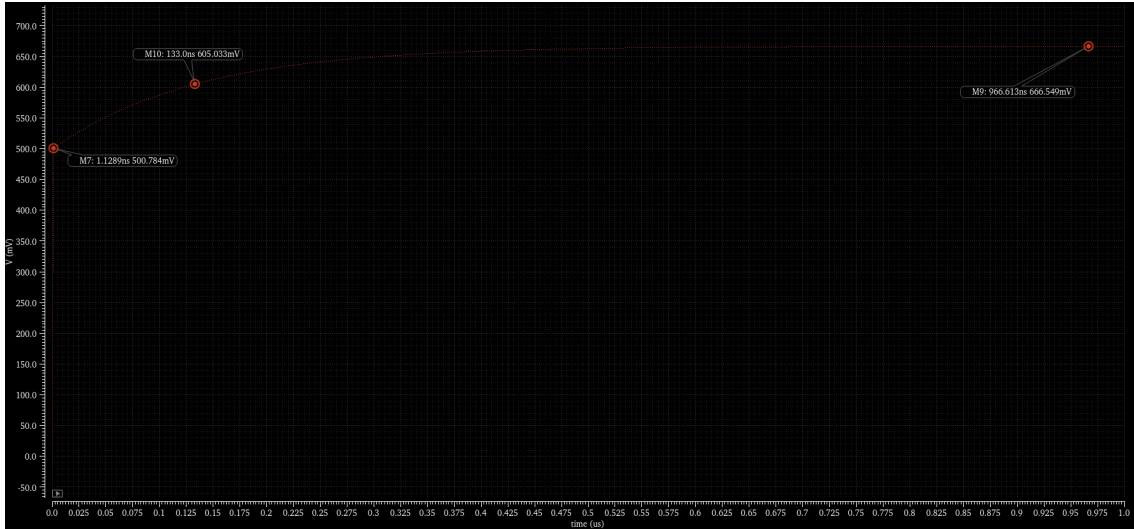


Figure 11: Part (b)

3 Lecture 3

3.1 Question 1

Plot V_{out} vs *time* and I_{out} vs *time*

-
-
-

3.2 Question 2

Plot V_{out} vs *time* (a) $D = 10\%$ (b) $D = 90\%$ (i) $T = 0.1RC$ (ii) $T = 10RC$ where $D = \frac{T_{ON}}{T}$

3.3 Question 3

Draw Bode plot for $H(s) = \frac{(s-z_1)(s+z_2)}{(s+p_1)(s+p_2)(s+p_3)}$ where (i) $z_2 \ll p_1 \ll p_2 \ll p_3 \ll z_1$ (ii) $p_3 \ll p_2 \ll p_1 \ll z_1 \ll z_2$

4 Lecture 4

4.1 Question 1

Design a non-inverting schmidt trigger using opamp based circuits.

4.2 Question 2

Find the expression for Closed loop Unity gain bandwidth.

4.3 Question 3

In cadence, Plot V_o vs V_{in} (Sweep V_{in} from $-V_{ss}$ to V_{DD}) for non-inverting amplifier using Opamp and VCVS for both positive and -ve feedback.

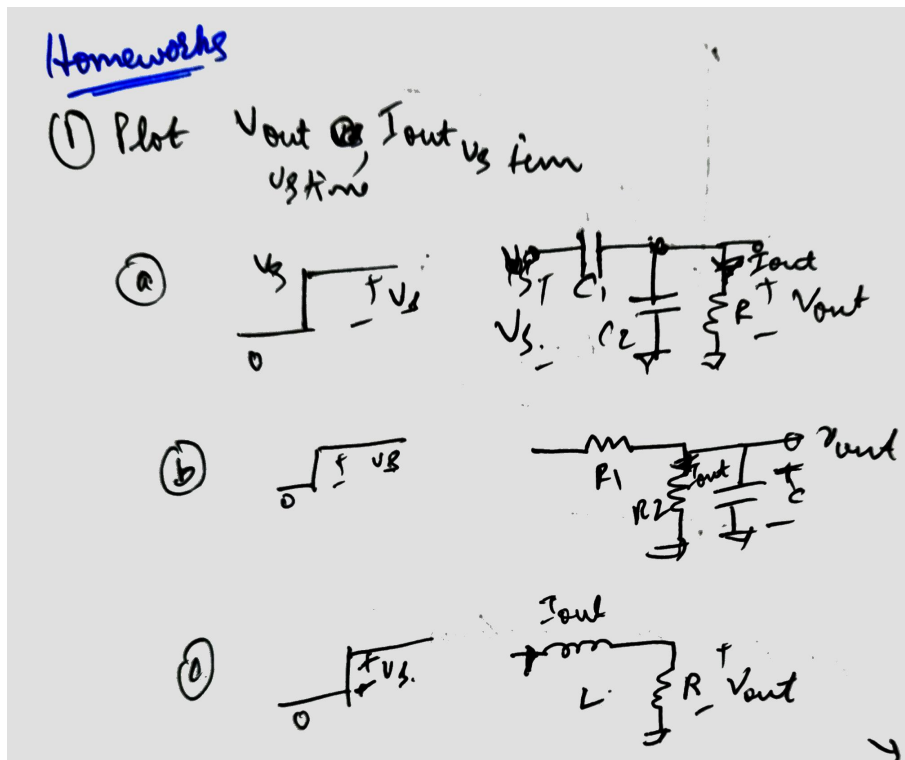


Figure 12: Lecture 3 - Question 1

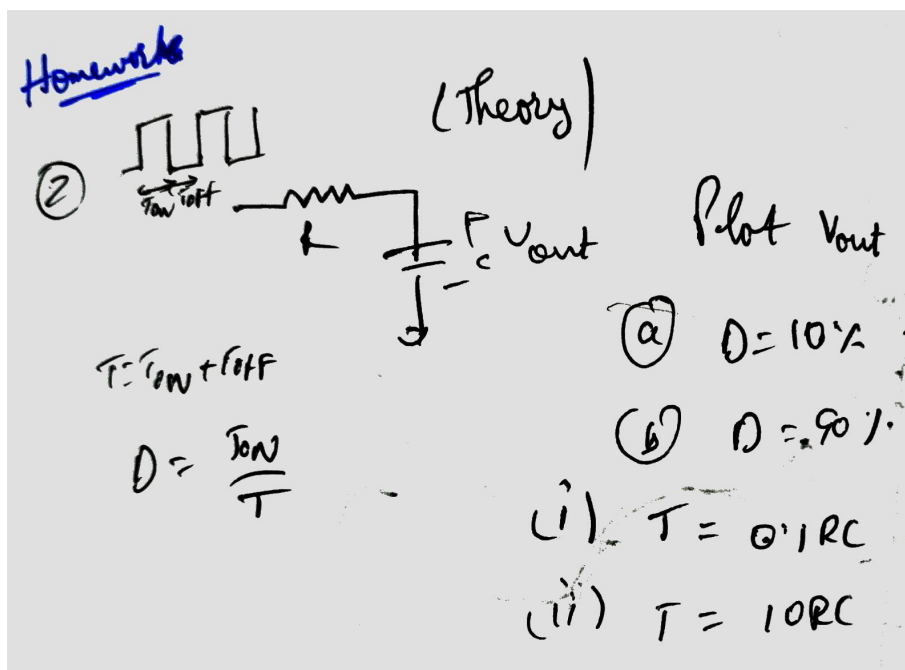


Figure 13: Lecture 3 - Question 2

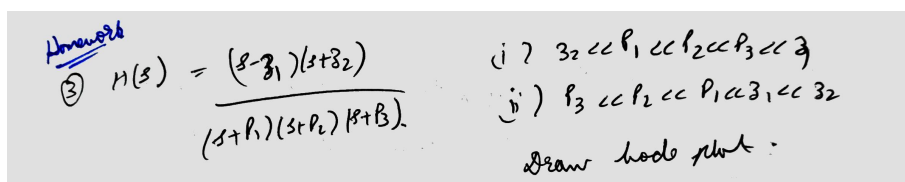


Figure 14: Lecture 3 - Question 3

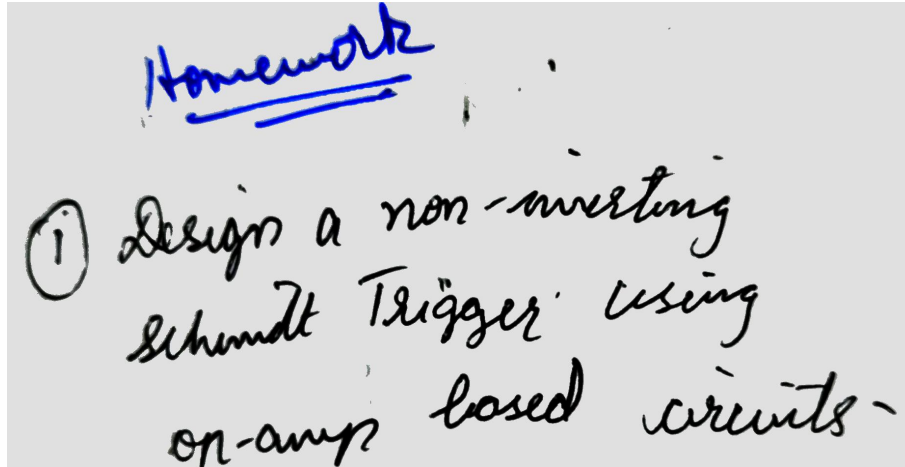


Figure 15: Lecture 4 - Question 1

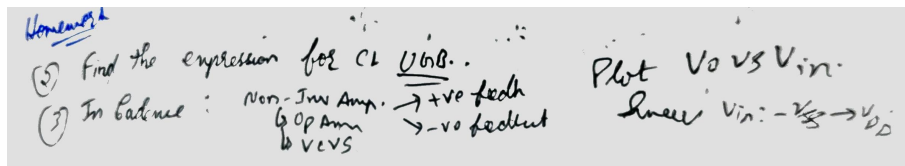


Figure 16: Lecture 4 - Question 2,3

5 Lecture 5

5.1 Question 1

In Cadence, Bode Plot for

1. $A = 100$, check V_x (offset) [DC]
2. $A = 1000$, check V_x (offset) [DC]
3. $UGB = 1\text{MHz}$, Gain = 1000, Design G_m , R_{out} , R_1 , R_2 , C , $V_{Ref} = 0.6V$, $V_{out} = 1.2V$

5.2 Question 2

In cadence, AC analysis. Bode Plot for $\frac{V_{out}}{V_{in}}$

1. $G_{m1} = G_{m2} = 10\mu F$, $R_1 = R_2 = 10M\Omega$, $C_1 = 10fF$, $C_2 = 2fF$
2. add $C_{effective}$ at C_1 and get phase margin = 45°

6 Lecture 6

6.1 Question 1

Draw Bode plot for miller compensated circuit.

$$G_{m1} = G_{m2} = 10\mu S, R_1 = R_2 = 10M\Omega, C_1 = 10fF, C_2 = 2fF$$

Find Phase Margin, Unity Gain Bandwidth and DC Gain. (Theory + Cadence) (AC analysis/STB)

6.2 Question 2

Simulate in cadence.

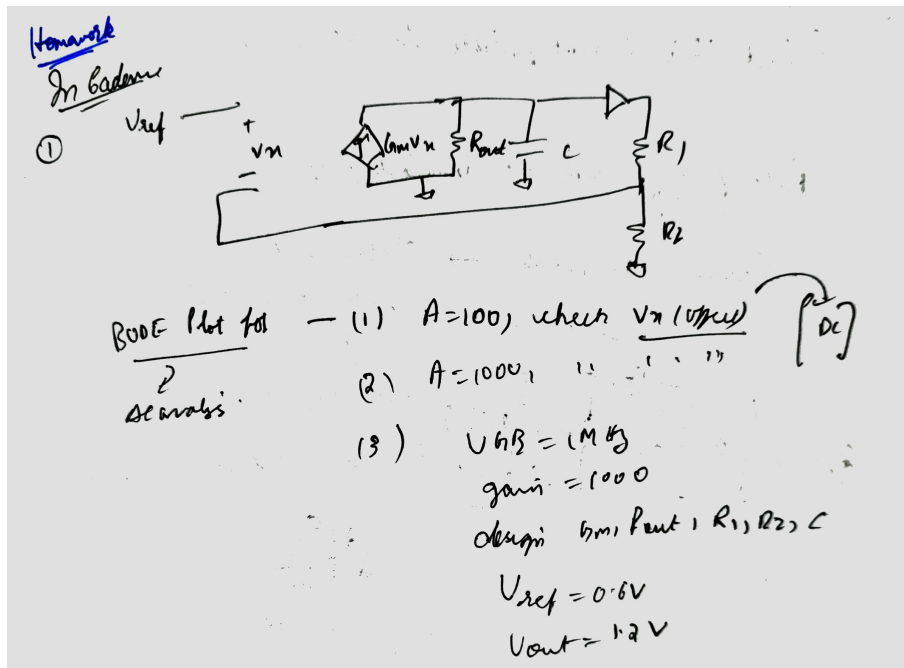


Figure 17: Lecture 5 - Question 1

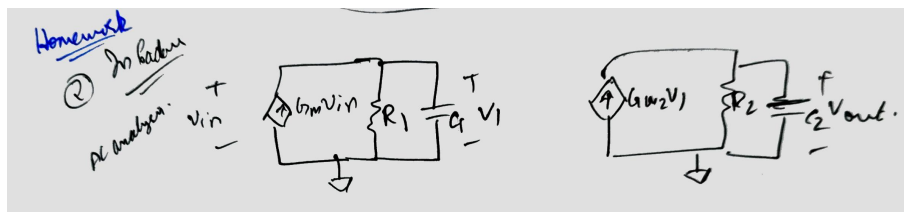


Figure 18: Lecture 5 - Question 2 - circuit

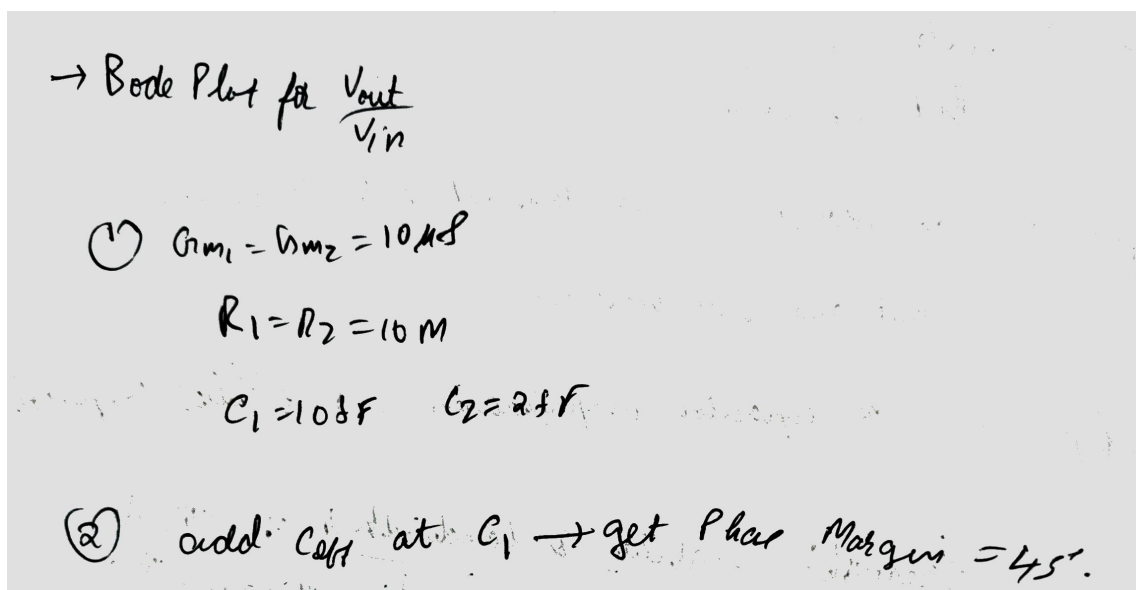


Figure 19: Lecture 5 - Question 2 - Question

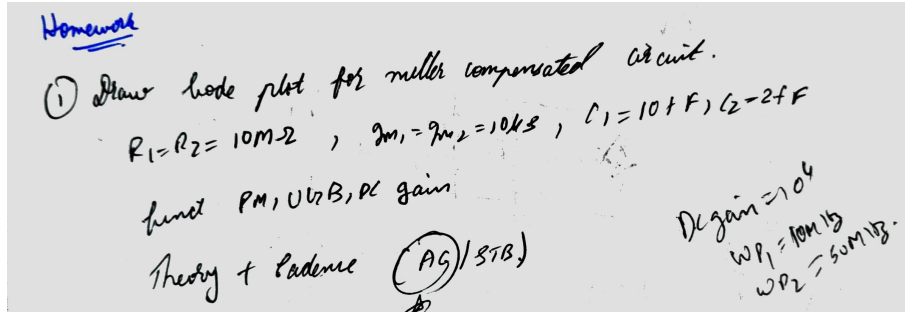


Figure 20: Lecture 6 - Question 1

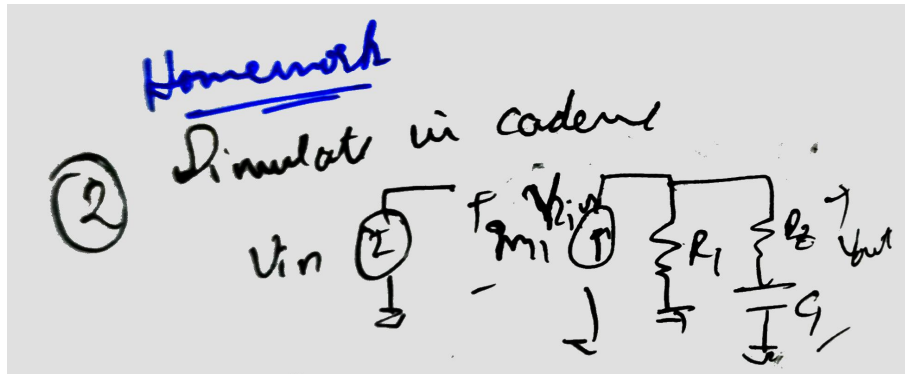


Figure 21: Lecture 6 - Question 2

7 Lecture 7

7.1 Question 1

TSMC 18 lib, Simulate all the resistors -40° to 125° (SS, TT, FF) TSMC 18 lib, Simulate all the resistors -40° to 125° (SS, TT, FF)

Resistor	Temperature Coefficient	Type	Process Spread	Linearity	Area
R1	Value	TypeA	Spread1	Linear1	Area1
R2	Value	TypeB	Spread2	Linear2	Area2
R3	Value	TypeC	Spread3	Linear3	Area3

Table 1: Resistor characteristics under different conditions

7.2 Question 2

Repeate Question 1 with a capacitor.

7.3 Question 3

$V_{PTAT}, V_{CTAT}, V_{Ref}$

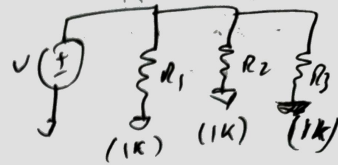
$I_{PTAT}, I_{CTAT}, I_{Ref}$

$R_{PTAT}, R_{CTAT}, R_{Ref}$

All P and C for 9 values.

Homework

Q.1 TSMC-18 lib
Simulate all the resistors
- 60°C → 125°C ($\frac{SS}{FF}$)



Resistor	TC	Type	Process spread	Linearity	Area

Which is better in terms of

- (i) Linearity
- (ii) Temp. Coeff. (least)
- (iii) Process spread (least)
- (iv) Area (least)

Q.2 Repeat Q.1 for capacitors.

$$I_{ref} = \frac{V_{PTAT}}{R_{PTAT}}, \frac{V_{CTAT}}{R_{CTAT}}, \frac{V_{ref}}{R_{ref}}$$

$$\frac{V_{PTAT}}{R_{PTAT}} \times R_{ref} = V_{ref}$$

Q.3

$V_{PTAT}, V_{CTAT}, V_{ref}$
 $I_{PTAT}, I_{CTAT}, I_{ref}$
 $R_{PTAT}, R_{CTAT}, R_{ref}$

All P.E.C for 9 values

Figure 22: Lecture 7 - Question 1,2,3

Capacitor	Temperature Coefficient	Type	Process Spread	Linearity	Area
C1	Value	TypeA	Spread1	Linear1	Area1
C2	Value	TypeB	Spread2	Linear2	Area2
C3	Value	TypeC	Spread3	Linear3	Area3

Table 2: Resistor characteristics under different conditions