

CMOS References and Regulators: Homework

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1 Lecture 1

1.1 Proving Resistance: Current is proportional to Voltage

Do the 'DC Analysis' for the following circuits. Plot V vs I & write expression for the slope. Prove that its a resistance.

Answer:

Left graph shows the I - V characteristics of the device. Clearly, $I \propto V$. The right graph shows the expression for the slope.

Plot for (a) : Using a Voltage source

Plot for (b) : Using a Current source

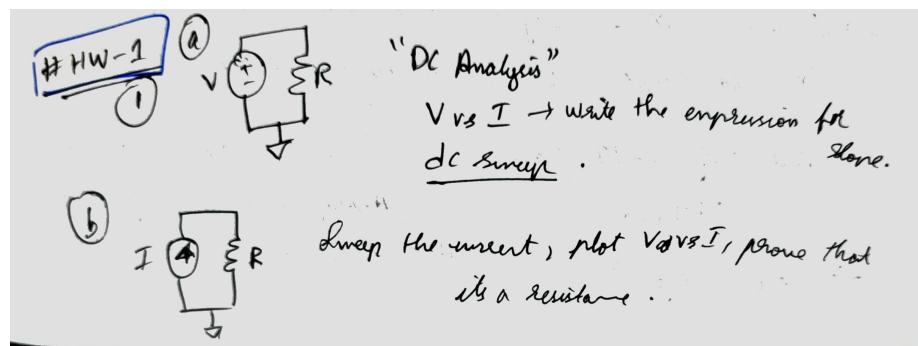


Figure 1: Lecture 1 - Question 1 - (a) and (b)

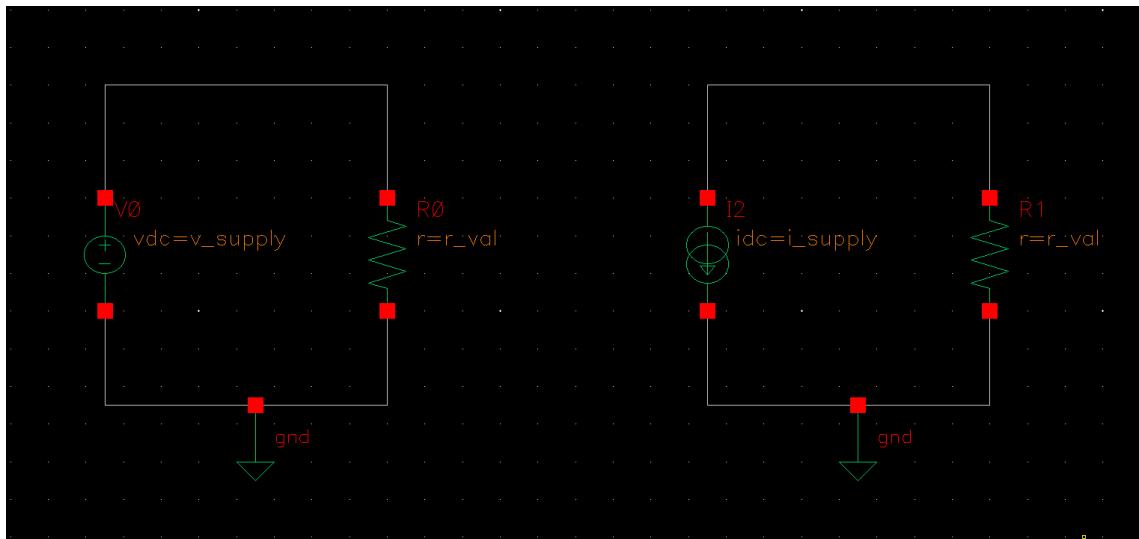


Figure 2: Testbench for (a) and (b)

1.2 Capacitance Amplifier using Controlled Sources

Design a capacitance amplifier using controlled sources.

Answer:

1.3 Inductance Amplifier using Controlled Sources

Design a inductance amplifier using controlled sources.

Answer:

1.4 Resistance Amplifier using Controlled Sources

Sweep V vs I for (i) $k > 1$ (ii) $0 < k < 1$ (iii) $K < 0$ Prove R_{eff} in each case is $\frac{R}{1-k}$.

Answer:

2 Lecture 2

2.1 Output Resistance

find the effective output resistance at V_{out} i.e., $R_{out} = ?$

Answer:

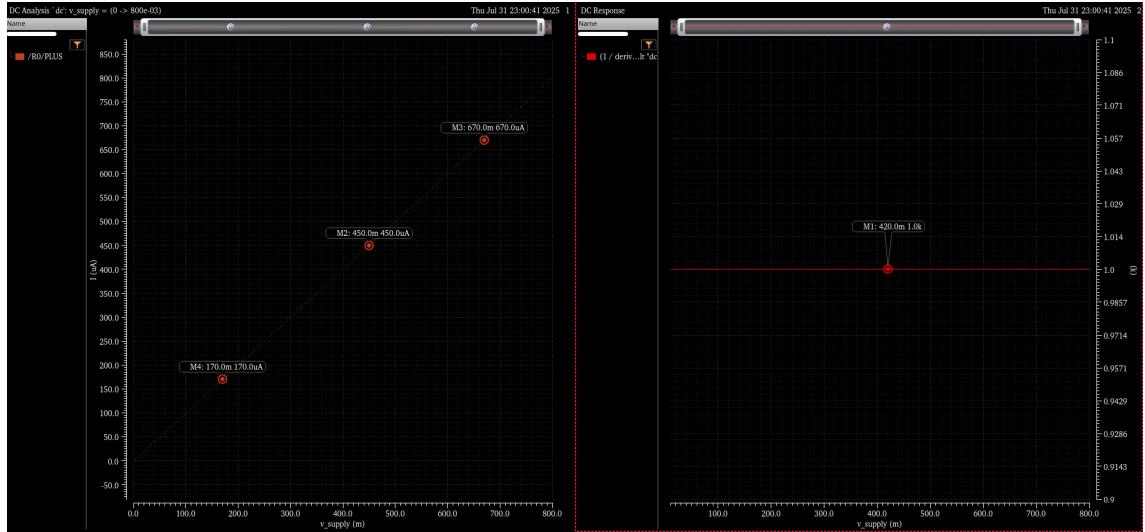


Figure 3: Plot for (a)

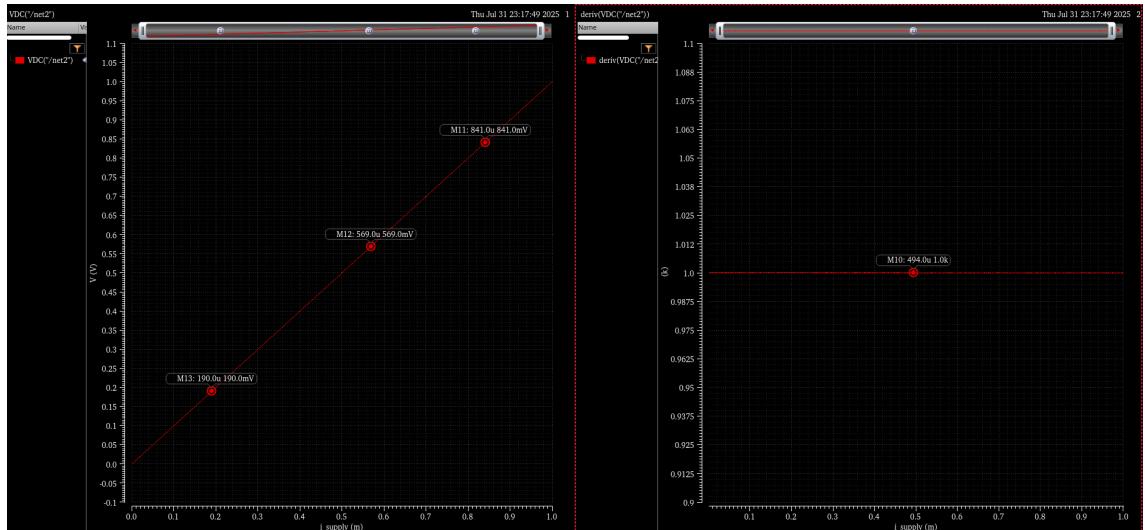


Figure 4: Plot for (b)

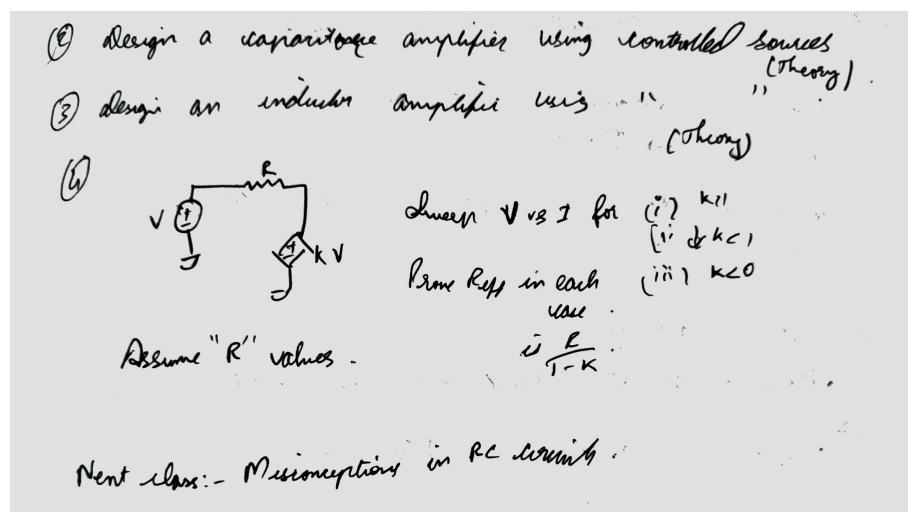
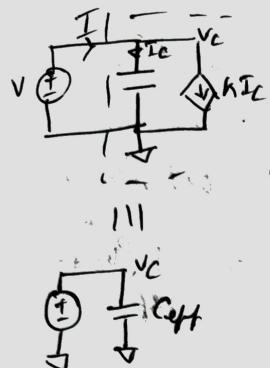


Figure 5: Lecture 1 - Question 2, 3, 4

Capacitance Amplifier using controlled sources

CCCS



$$I = I_{ct} + k \cdot I_c$$

$$= I_{ct}(1+k)$$

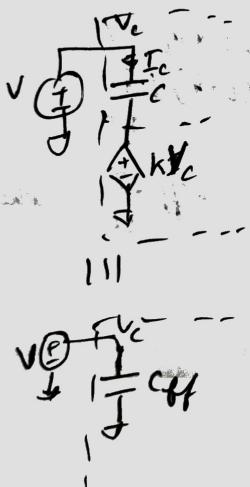
$$I = C \cdot \frac{dV_c}{dt} \cdot (1+k)$$

$$I = C(1+k) \cdot \frac{dV_c}{dt}$$

$$I \propto \frac{dV_c}{dt} \rightarrow \text{Capacitance.}$$

$$I = C_{eff} \cdot \frac{dV_c}{dt} \quad \text{where } \boxed{C_{eff} = C(1+k)}$$

V_{CVS}



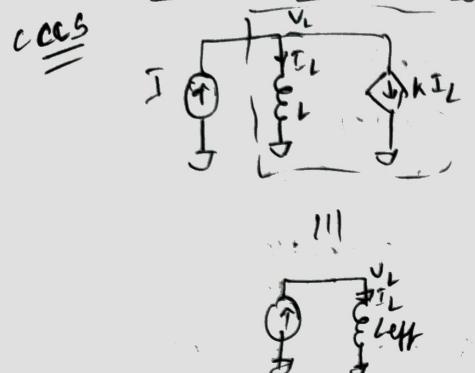
$$I_c = C \cdot \frac{d}{dt} (V_c - kV_c)$$

$$I_c = C \frac{dV_c}{dt} \cdot (1-k)$$

$$I_c \propto \frac{dV_c}{dt} \Rightarrow \boxed{C_{eff} = (1-k) \cdot C}$$

Figure 6: Question 2 - Solution

Inductance amplifier using controlled sources



$$I = I_L + k \cdot I_L \\ = I_L(1+k)$$

$$I = L \cdot \frac{dV_L}{dt} \cdot (1+k)$$

$$I = \frac{1}{L_{eff}} \int V_L \cdot dt \Rightarrow L_{eff} = \frac{L}{1+k}$$

JCVS

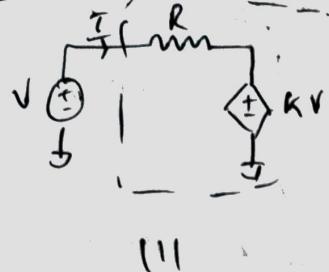


$$V = V_L + kV_L \\ = (1+k) L \frac{dI}{dt}$$

$$V = L_{eff} \frac{dI}{dt} \text{ where } L_{eff} = L(1+k)$$

Figure 7: Question 3 - Solution

Resistance Amplified using controlled sources



$$(V - kV) = I \cdot R$$

$$V(1-k) = I \cdot R$$

$$V = \frac{I \cdot R}{1-k}$$

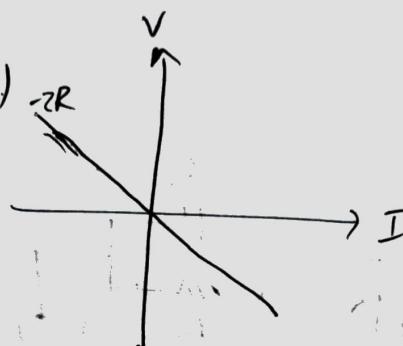
$$V = I \cdot R_{eff}$$



$$\text{where } R_{eff} = \frac{R}{1-k}$$

(i) $k > 1 \Rightarrow R_{eff} < 0$
(Neg. resistance)

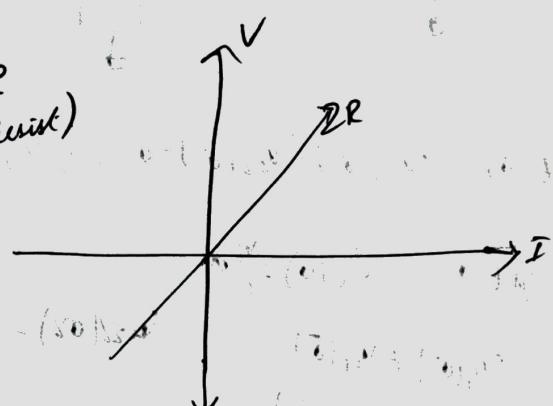
$$k=1.5 \Rightarrow R_{eff} = -2R$$



(ii) $0 < k < 1 \Rightarrow R_{eff} < \infty$

$$k=0.5 \rightarrow R_{eff} = 2R$$

(Amplified resist)



(iii) $k < 0 \Rightarrow R_{eff} < R$

$$k=-\frac{1}{2} \rightarrow R_{eff} = \frac{R}{1.5} = \frac{2R}{3}$$

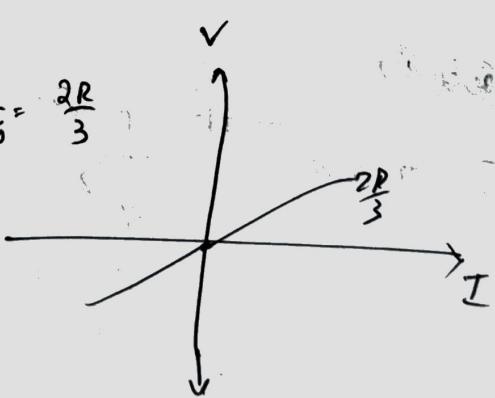


Figure 8: Question 4 - Solution

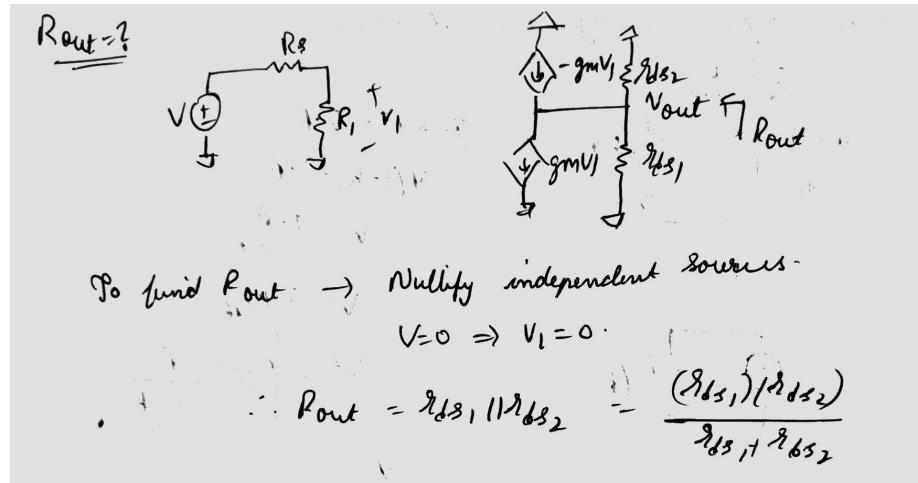


Figure 9: Lecture 2 - Question 1

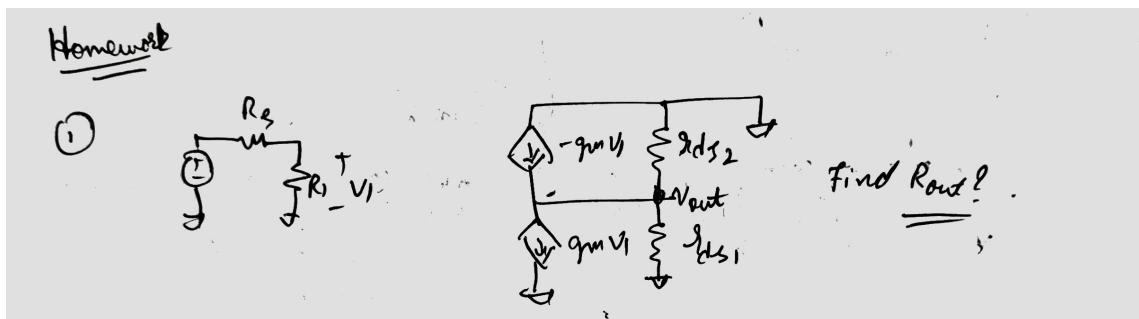


Figure 10: Solution for Question 1

When we nullify the V_1 , the vccs vanish and the effective output resistance at v_{out} node is $R_{out} = r_{ds1} || r_{ds2}$. Proved this using the plot with values.

2.2 Step Response for RC Circuit

Plot V_{out} vs time in Cadence. Prove Theory.

Answer:

Copy this from the notes

Proved this using theory and from the simulations by finding the output voltage after 1 time constant.

3 Lecture 3

3.1 Step Response for passive RLC circuit Combinations

Plot V_{out} vs time and I_{out} vs time

-
-
-

3.2 Pulse Response for RC Circuit with varying Duty Cycle and Time Period

Plot V_{out} vs time (a) $D = 10\%$ (b) $D = 90\%$ (i) $T = 0.1RC$ (ii) $T = 10RC$ where $D = \frac{T_{ON}}{T}$

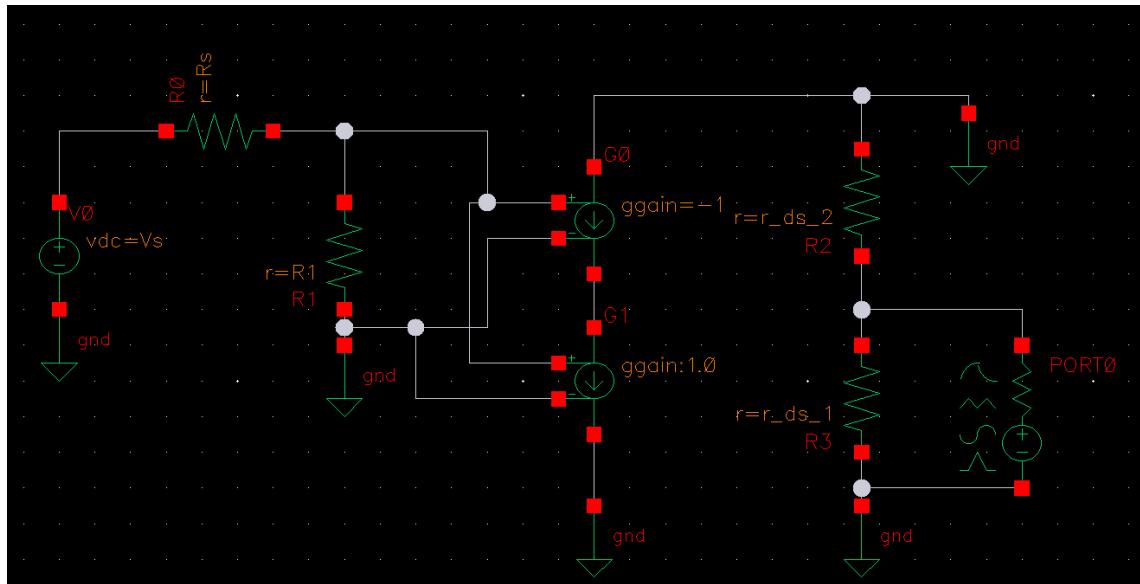


Figure 11: Testbench

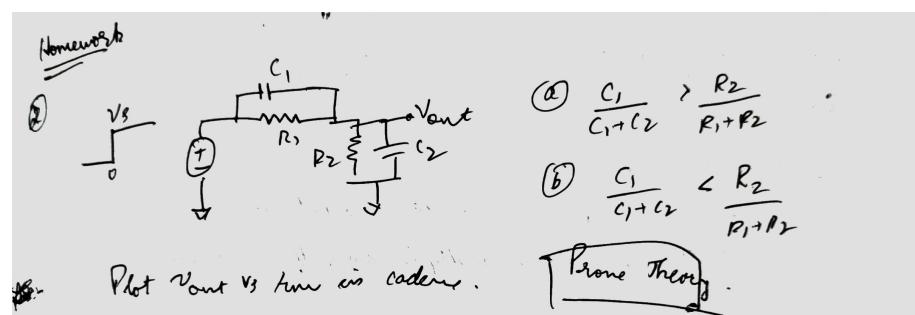


Figure 12: Lecture 2 - Question 2

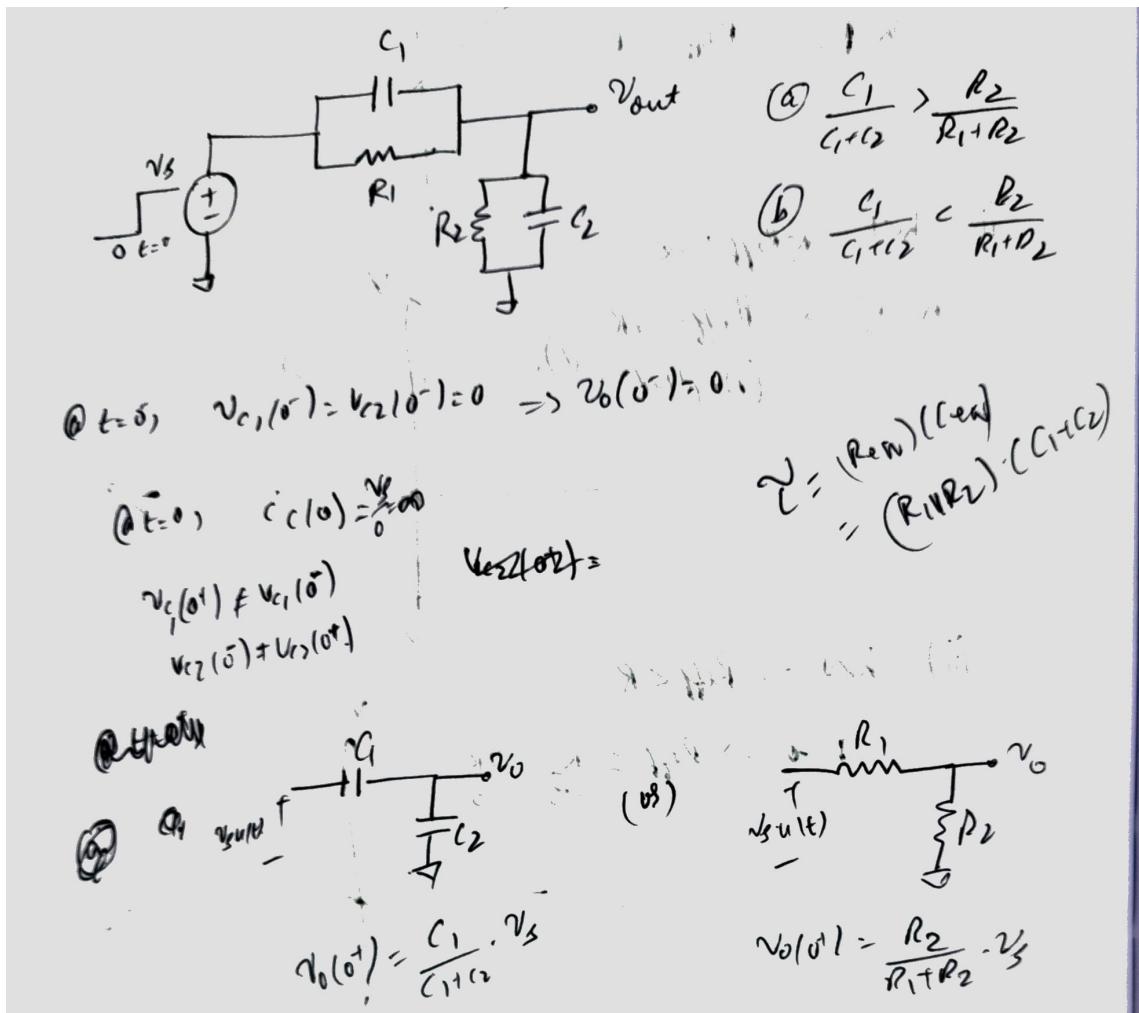


Figure 13: Solution for Question 2

(a) $V_o(0^+) = \frac{R_2}{R_1+R_2} \cdot V_s$

$$V_o(\infty) = \frac{C_1}{C_1+C_2} \cdot V_s$$

$$V_o(t) = \left\{ \frac{V_s C_1}{C_1+C_2} + \left(\frac{V_s R_2}{R_1+R_2} - \frac{V_s \cdot C_1}{C_1+C_2} \right) e^{-\frac{t}{\tau}} \right\} u(t)$$

Given:
 $C_1 = 2\text{n}$
 $C_2 = 1\text{n}$
 $R_1 = 100\Omega$
 $R_2 = 100\Omega$
 $\tau = 150\text{ms}$

$\frac{2}{3} > \frac{1}{2}$

$$V(t) = 0.5 + (0.66 - 0.5)e^{-\frac{t}{\tau}}$$

$$V(\infty) = 0.5 + 0.37 \times 10^{-16}$$
 $= 560\text{mV}$

(b) $V_o(0^+) = \frac{C_1}{C_1+C_2} \cdot V_s$ $V_o(\infty) = \frac{R_2}{R_1+R_2} \cdot V_s$

$$V_o(t) = \left\{ \frac{V_s R_2}{R_1+R_2} + \left(\frac{V_s \cdot C_1}{C_1+C_2} - \frac{V_s R_2}{R_1+R_2} \right) e^{-\frac{t}{\tau}} \right\} u(t)$$

Figure 14: Solution for Question 2

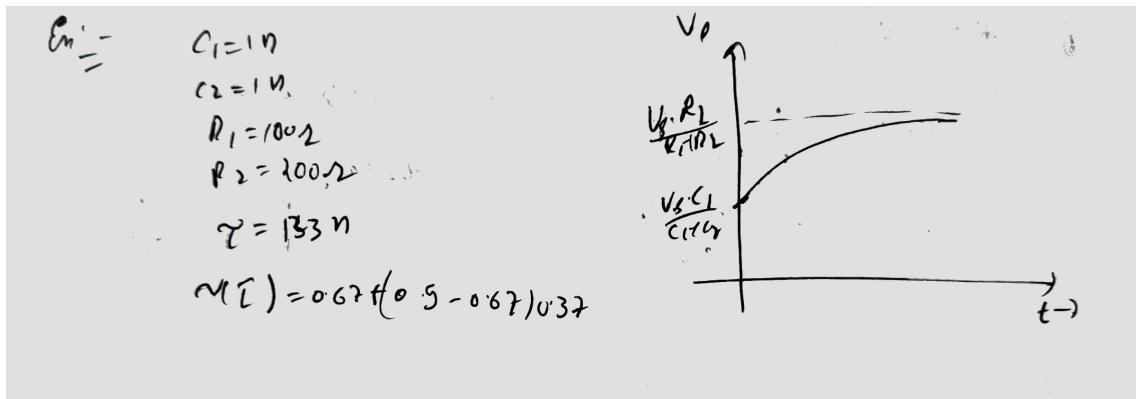


Figure 15: Solution for Question 2

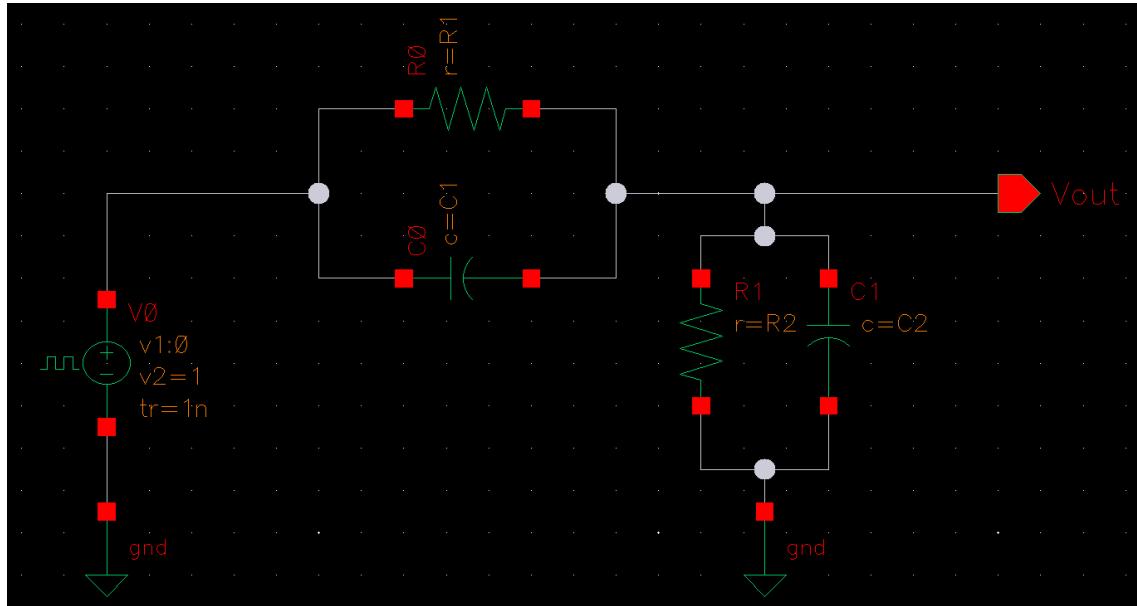


Figure 16: Question 2 Testbench

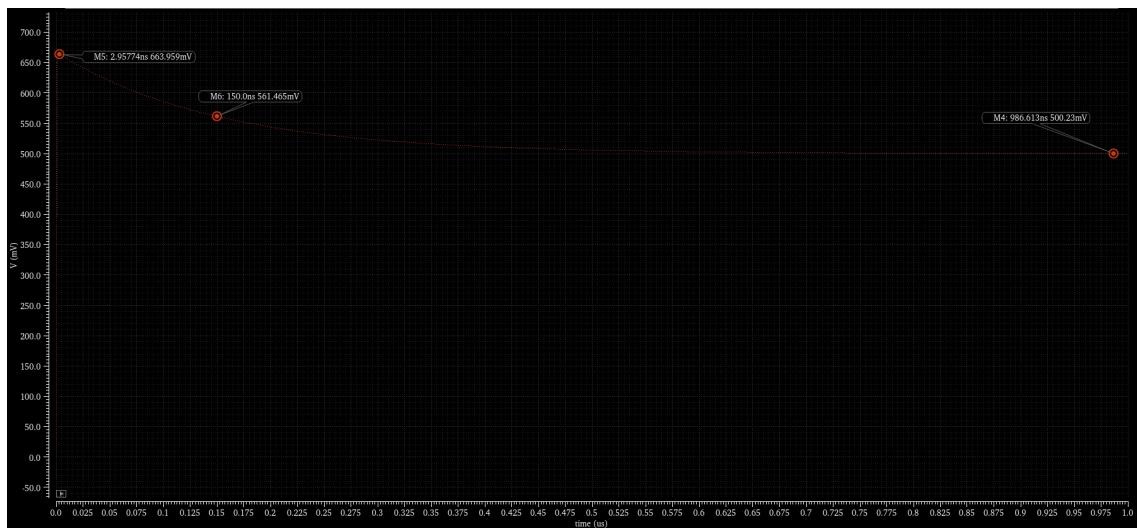


Figure 17: Part (a)

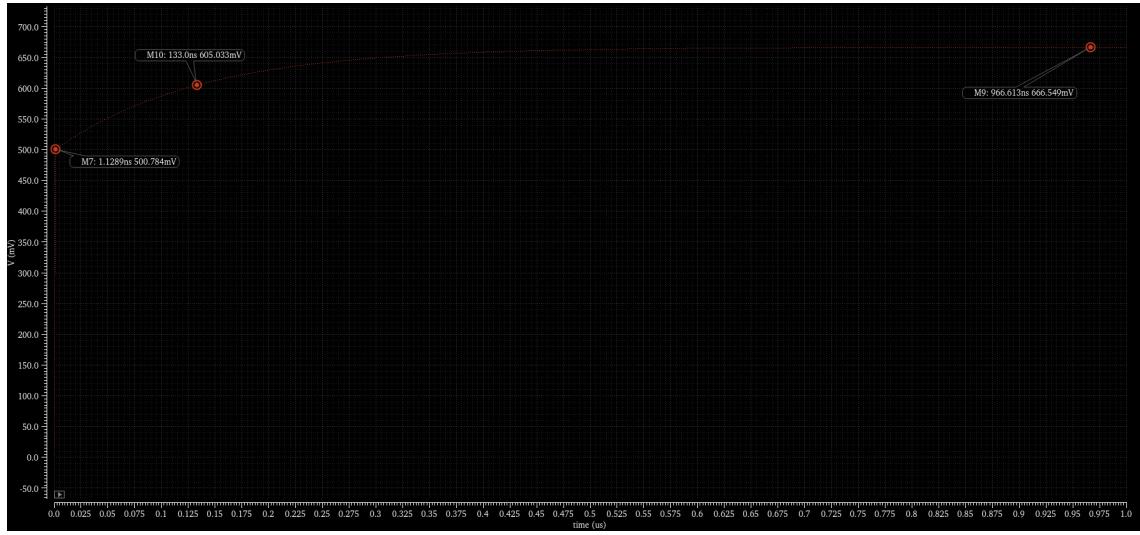


Figure 18: Part (b)

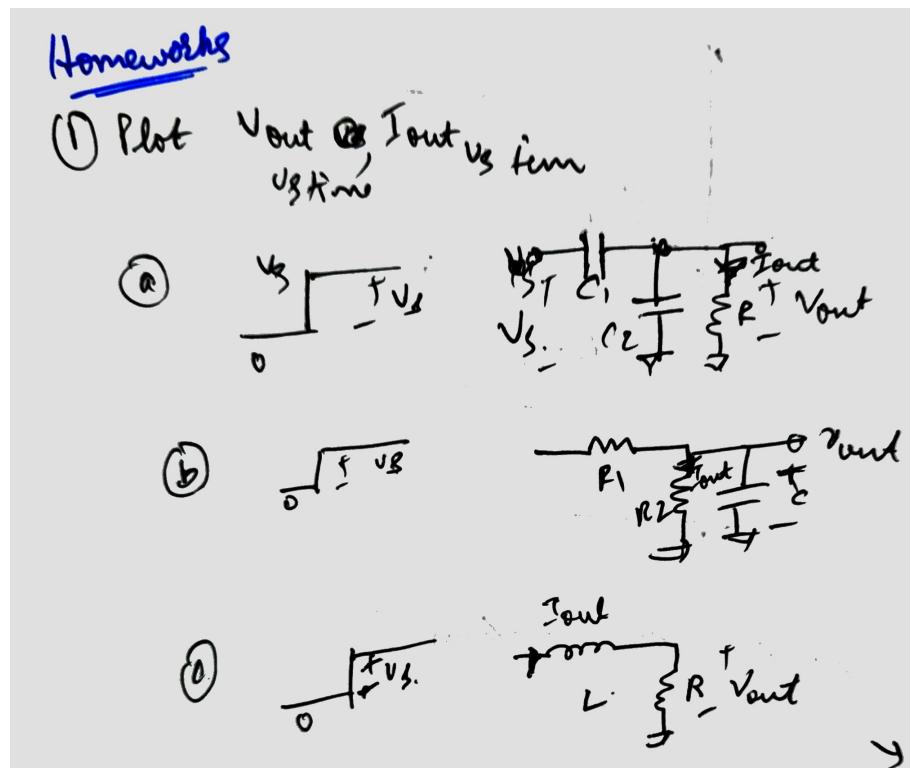


Figure 19: Lecture 3 - Question 1

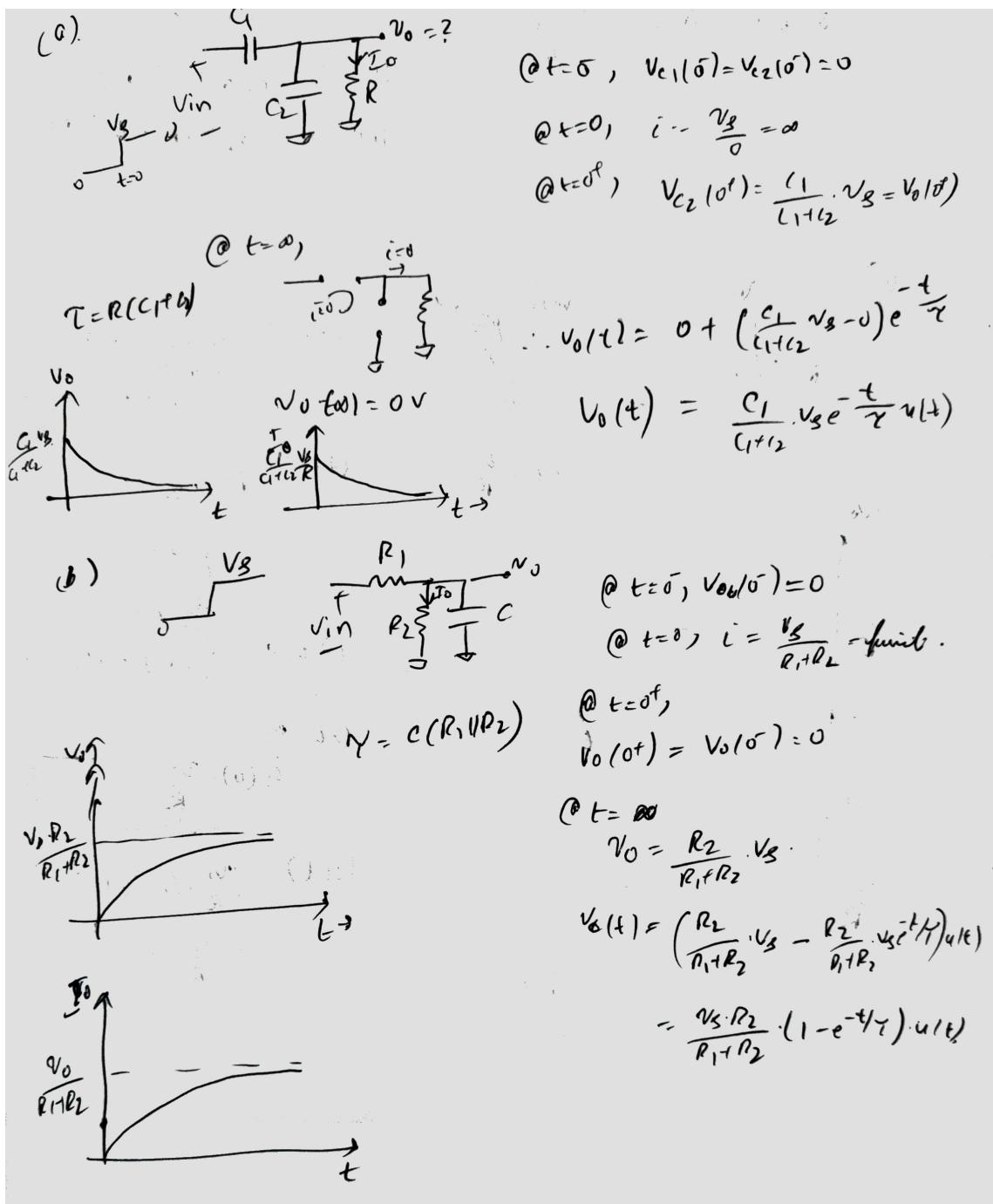


Figure 20: Solution for Question 1

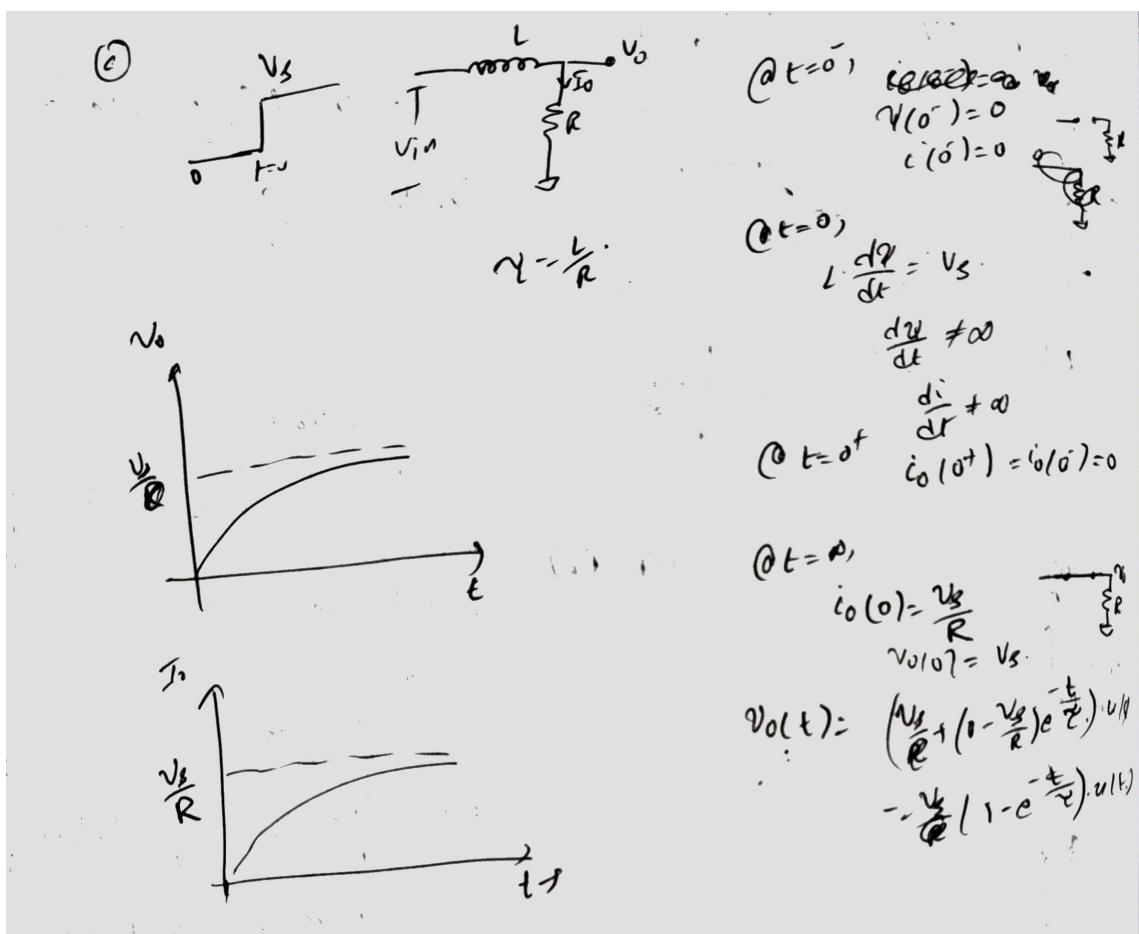


Figure 21: Solution for Question 1

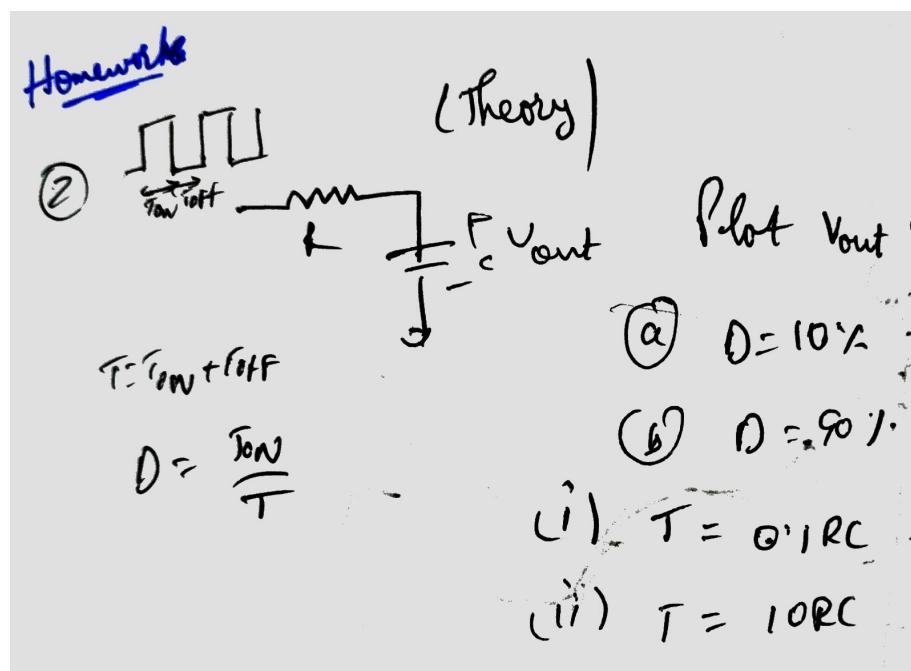
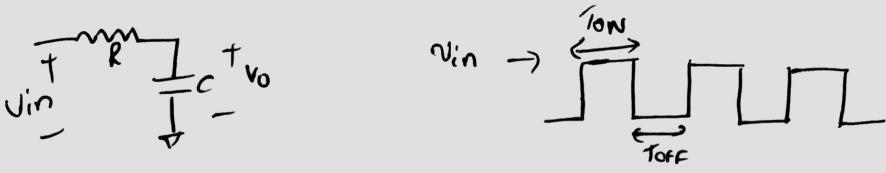


Figure 22: Lecture 3 - Question 2



$$\textcircled{a} \quad D = 10\%$$

$$\textcircled{i} \quad T = 0.1RC$$

$$\textcircled{b} \quad D = 90\%$$

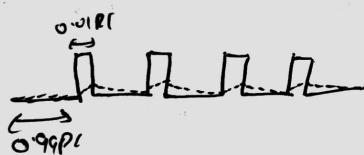
$$\textcircled{ii} \quad T = 10RC$$

$$\textcircled{i} \quad T = 0.1RC$$

$$\textcircled{a} \quad \frac{T_{ON}}{T} = 10\%$$

$$T_{ON} = 0.01RC$$

$$T_{OFF} = 0.99RC$$



\textcircled{b}

$$\textcircled{b} \quad \frac{T_{ON}}{T} = 90\%$$

$$T_{ON} = 0.9RC$$

$$T_{OFF} = 0.1RC$$



$$\textcircled{ii} \quad T = 10RC$$

$$\textcircled{a} \quad \frac{T_{ON}}{T} = 10\%$$

$$T_{ON} = RC$$

$$T_{OFF} = 9RC$$



$$\textcircled{b} \quad \frac{T_{ON}}{T} = 90\%$$

$$T_{ON} = 9RC$$

$$T_{OFF} = RC$$

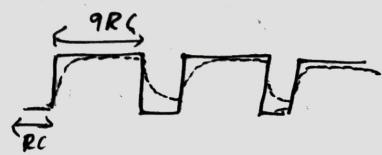


Figure 23: Solution for Question 2

Homework
 $\text{Q3} \quad H(s) = \frac{(s-z_1)(s+z_2)}{(s+p_1)(s+p_2)(s+p_3)}$

(i) $z_2 \ll p_1 \ll p_2 \ll p_3 \ll z_1$
 (ii) $p_3 \ll p_2 \ll p_1 \ll z_1 \ll z_2$
 Draw bode plot.

Figure 24: Lecture 3 - Question 3

3.3 Bode Plot for a given Transfer Function

Draw Bode plot for $H(s) = \frac{(s-z_1)(s+z_2)}{(s+P_1)(s+P_2)(s+P_3)}$ where (i) $z_2 \ll p_1 \ll p_2 \ll p_3 \ll z_1$ (ii) $p_3 \ll p_2 \ll p_1 \ll z_1 \ll z_2$

4 Lecture 4

4.1 Non-inverting Schmitt Trigger

Design a non-inverting schmitt trigger using opamp based circuits.

4.2 Expression for Closed loop Unity gain bandwidth

Find the expression for Closed loop Unity gain bandwidth.

4.3 Non-Inverting Amplifier using Opamp and VCVS

In cadence, Plot V_o vs V_{in} (Sweep V_{in} from $-V_{ss}$ to V_{DD}) for non-inverting amplifier using Opamp and VCVS for both positive and -ve feedback.

5 Lecture 5

5.1 Single Pole Opamp with Feedback - Bode Plot

In Cadence, Bode Plot for

1. $A = 100$, check V_x (offset) [DC]
2. $A = 1000$, check V_x (offset) [DC]
3. UGB = 1MHz, Gain = 1000, Design G_m , R_{out} , R_1 , R_2 , C , $V_{Ref} = 0.6V$, $V_{out} = 1.2V$

5.2 Bode Plot for a 2 Pole System

In cadence, AC analysis. Bode Plot for $\frac{V_{out}}{V_{in}}$

1. $G_{m1} = G_{m2} = 10\mu F$, $R_1 = R_2 = 10M\Omega$, $C_1 = 10fF$, $C_2 = 2fF$
2. add $C_{effective}$ at C_1 and get phase margin = 45°

6 Lecture 6

6.1 Miller compensation - Bode Plot

Draw Bode plot for miller compensated circuit.

$$G_{m1} = G_{m2} = 10\mu S, R_1 = R_2 = 10M\Omega, C_1 = 10fF, C_2 = 2fF$$

Find Phase Margin, Unity Gain Bandwidth and DC Gain. (Theory + Cadence) (AC analysis/STB)

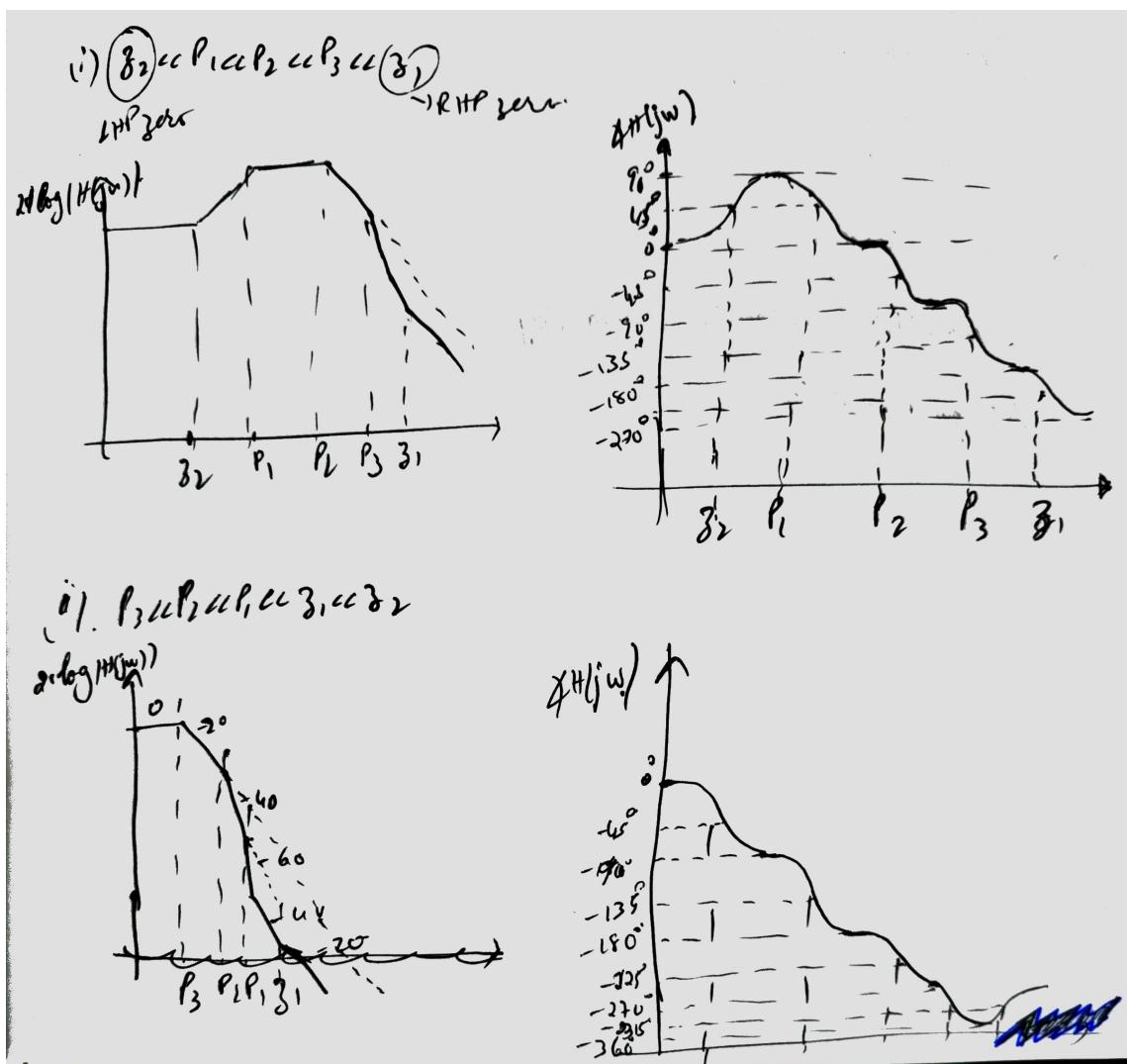


Figure 25: Solution for Question 3

Homework

① Design a non-inverting Schmitt Trigger using op-amps based circuits.

Figure 26: Lecture 4 - Question 1

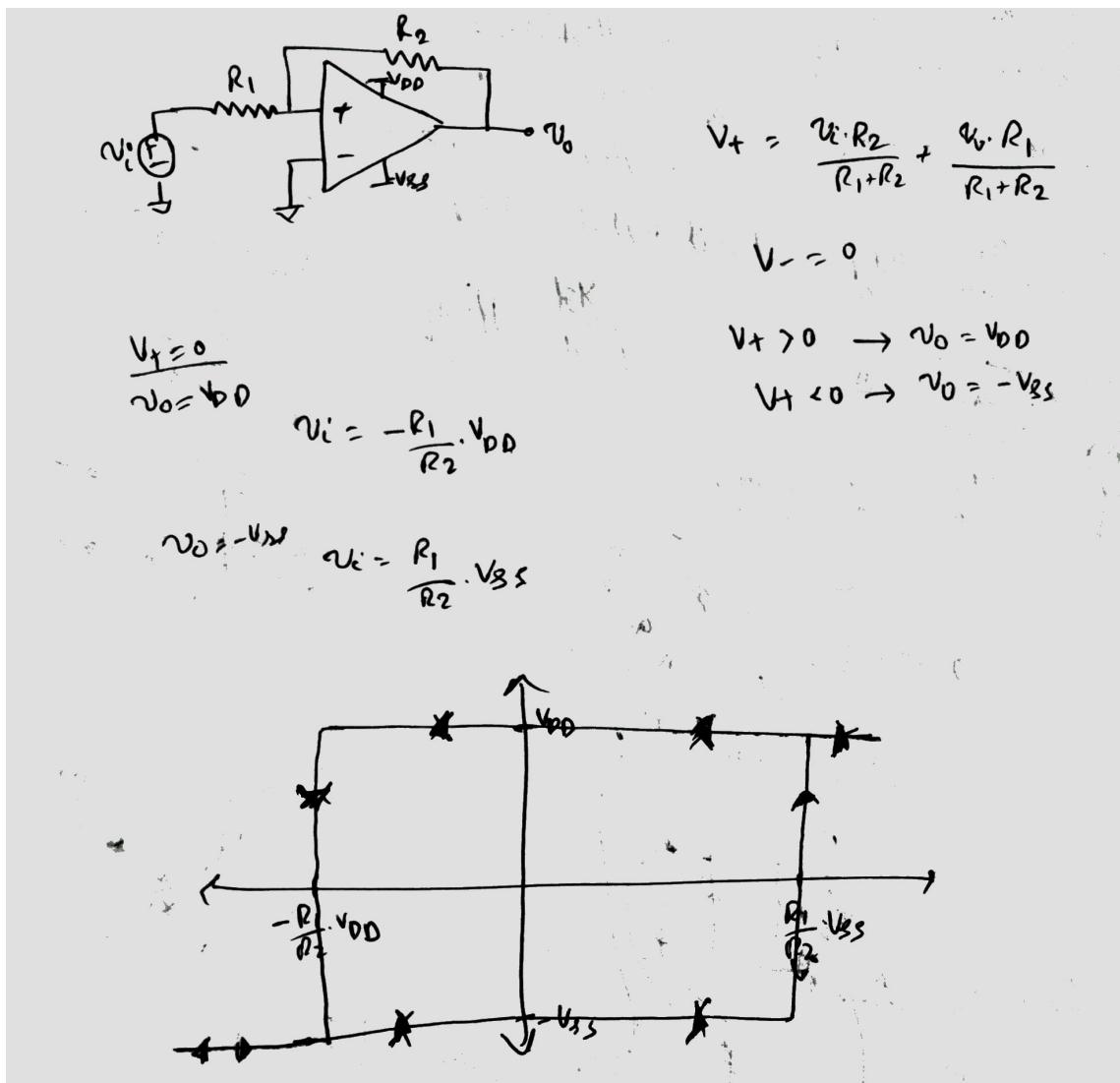


Figure 27: Solution for Question 1

Homework

(i) Find the expression for CL V_{oB} .

(ii) In balance : Non-Inv Amp. $\xrightarrow{\text{Op Amp}}$ +ve feedback
 $\xrightarrow{\text{Op Amp}}$ $\xrightarrow{\text{Op Amp}}$ -ve feedback
 $\xrightarrow{\text{Op Amp}}$ $\xrightarrow{\text{Op Amp}}$ $\xrightarrow{\text{Op Amp}}$

Plot V_o vs V_{in} .
 linear $V_{in} = -\frac{V_{SS}}{V_{DD}} \rightarrow V_o$

Figure 28: Lecture 4 - Question 2,3

$$V_{o(s)} = \frac{A}{1 + \frac{s}{(1+A\beta)W_P}} \cdot V_{in(s)}$$

$$W_P = \frac{1}{R_{out} \cdot C}$$

$$A = G_m R_{out}$$

$$(1+A\beta) \cdot W_P \approx \frac{G_m \beta}{C}$$

$$\Rightarrow \left| \frac{A}{1 + \frac{jw}{\frac{G_m \beta}{C}}} \right| = 1$$

$$\Rightarrow A^2 = 1 + \frac{w^2}{\frac{G_m^2 \beta^2}{C^2}}$$

$$\Rightarrow A \frac{G_m \beta}{C} = w_{VnB}$$

$$\Rightarrow A v_o(j) \cdot W_P = w_{VnB}$$

Figure 29: Solution for Question 2

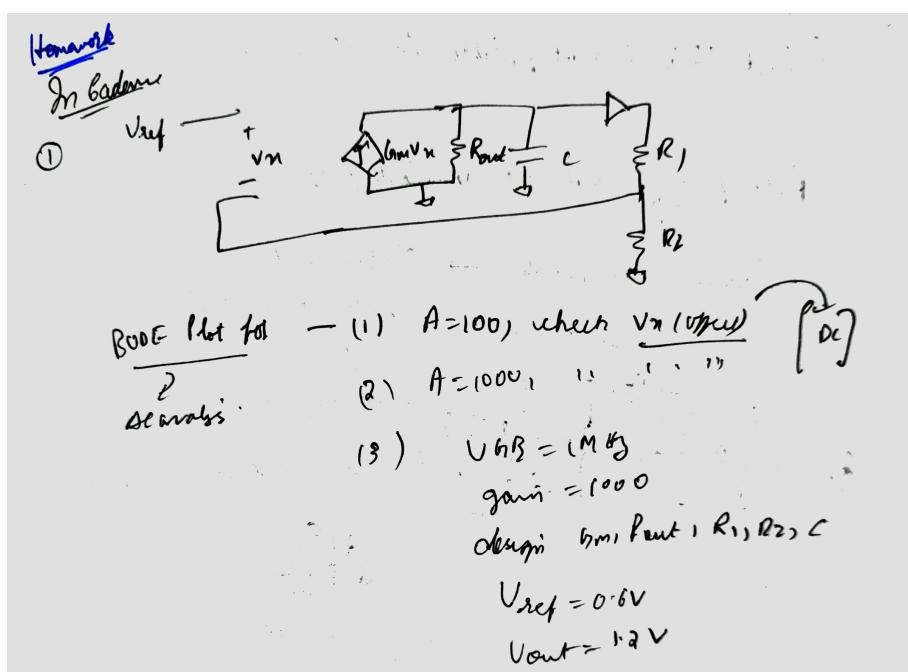


Figure 30: Lecture 5 - Question 1

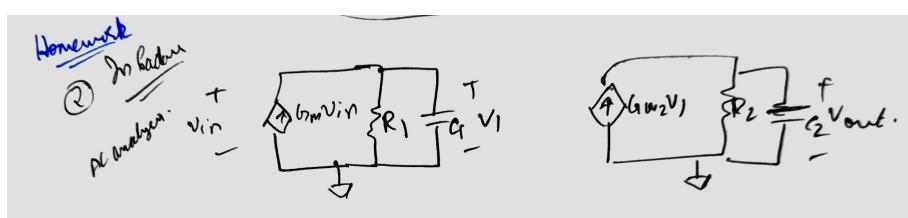


Figure 31: Lecture 5 - Question 2 - circuit

→ Bode Plot for $\frac{V_{out}}{V_{in}}$

$$\textcircled{1} \quad Gm_1 = Gm_2 = 10 \text{ MS}$$

$$R_1 = R_2 = 10 \text{ M}$$

$$C_1 = 10 \text{ fF} \quad C_2 = 2 \text{ fF}$$

$\textcircled{2}$ add cap at $C_1 \rightarrow$ get Phase Margin = 45°.

Figure 32: Lecture 5 - Question 2 - Question

Homework

$\textcircled{1}$ Draw node plot for Miller compensated circuit.

$$R_1 = R_2 = 10 \text{ M}, \quad g_{m1} = g_{m2} = 10 \text{ MS}, \quad C_1 = 10 \text{ fF}, \quad C_2 = 2 \text{ fF}$$

find PM, UTLB, DC gain

Theory + Cadence $(AG/3TB)$

$$\begin{aligned} \text{DC gain} &= 10^4 \\ W_P &= 10 \text{ M} \\ W_R &= 50 \text{ M} \end{aligned}$$

Figure 33: Lecture 6 - Question 1

Homework

$\textcircled{2}$ Simulate in cadence



Figure 34: Lecture 6 - Question 2

6.2 Adding a zero to a system

Simulate in cadence.

7 Lecture 7

7.1 Characterization of Resistors in TSMC 180nm

TSMC 18 lib, Simulate all the resistors -40° to 125° (SS, TT, FF) TSMC 18 lib, Simulate all the resistors -40° to 125° (SS, TT, FF)

Resistor	Temperature Coefficient	Type	Process Spread	Linearity	Area
R1	Value	TypeA	Spread1	Linear1	Area1
R2	Value	TypeB	Spread2	Linear2	Area2
R3	Value	TypeC	Spread3	Linear3	Area3

Table 1: Resistor characteristics under different conditions

7.2 Characterization of Capacitors in TSMC 180nm

Repeate Question 1 with a capacitor.

Capacitor	Temperature Coefficient	Type	Process Spread	Linearity	Area
C1	Value	TypeA	Spread1	Linear1	Area1
C2	Value	TypeB	Spread2	Linear2	Area2
C3	Value	TypeC	Spread3	Linear3	Area3

Table 2: Resistor characteristics under different conditions

7.3 PTAT, CTAT, Ref - Voltage, Current and Resistance Design Combinations

$$V_{PTAT}, V_{CTAT}, V_{Ref}$$

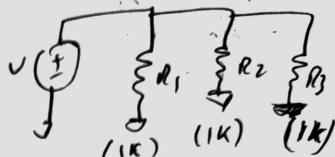
$$I_{PTAT}, I_{CTAT}, I_{Ref}$$

$$R_{PTAT}, R_{CTAT}, R_{Ref}$$

All P and C for 9 values.

Homework

Q.① TSMC-18 bit
Simulate all the resistors
 \rightarrow $100\Omega \rightarrow 125\Omega \left(\frac{33}{ff} \right)$



Resistor	TC	Type	Process spread	Linearity	Area

Which is better in terms of (i) linearity

(ii) Temp Coeff (least)

(iii) Process spread (least)

(iv) Area (least)

Q.② Repeat ① for capacitor.

$$I_{ref} = \frac{V_{PSTAT}}{R_{PSTAT}}, \frac{V_{CTAT}}{R_{CTAT}}, \frac{V_{RAT}}{R_{RAT}}$$

$$\frac{V_{PSTAT}}{R_{PSTAT}} \times R_{RAT} = V_{ref}$$

Q.③

$V_{PSTAT}, V_{CTAT}, V_{RAT}$
 $I_{PSTAT}, I_{CTAT}, I_{RAT}$
 $R_{PSTAT}, R_{CTAT}, R_{RAT}$

All P.C to 9 values

Figure 35: Lecture 7 - Question 1,2,3

Solution:

$$\begin{aligned}V_{PTAT} &= I_{PTAT} \cdot R_{Ref} \\V_{PTAT} &= I_{Ref} \cdot R_{PTAT} \\V_{PTAT} &= \frac{V_{CTAT}}{R_{CTAT}} \cdot R_{PTAT} \\V_{PTAT} &= \frac{V_{PTAT}}{R_{PTAT}} \cdot R_{PTAT} \\V_{PTAT} &= (I_{PTAT} + I_{CTAT}) \cdot R_{PTAT} \\V_{CTAT} &= I_{CTAT} \cdot R_{Ref} \\V_{Ref} &= I_{Ref} \cdot R_{Ref} \\I_{PTAT} &= \frac{V_{PTAT}}{R_{Ref}} \\I_{CTAT} &= \frac{V_{CTAT}}{R_{Ref}} \\I_{Ref} &= \frac{V_{Ref}}{R_{Ref}} \\R_{PTAT} &= \frac{V_{PTAT}}{I_{Ref}} \\R_{CTAT} &= \frac{V_{CTAT}}{I_{Ref}} \\R_{Ref} &= \frac{V_{Ref}}{I_{Ref}}\end{aligned}$$