

Sub-Regulator Design

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1 Introduction

This document presents the design and analysis of a sub-regulator circuit.

2 Design of Sub-Regulator

2.1 Design Methodology

2.2 Theoretical Design

2.3 Simulation results

3 Implementation of Sub-Regulator

Implemented a Sub-Regulator circuit as shown in Figure 1 using a PMOS pass transistor, 5 transistor Operational Transconductance Amplifier (5T OTA), a resistive feedback network and a simple beta-multiplier based bandgap reference.

Target specifications for the sub-regulator are as follows:

- **Input Voltage:** 3.3V (Range: $\pm 10\%$ i.e., 2.97V – 3.63V)
 - **Output Voltage:** 2.8V (Target)
 - **Load Current:** 0 to 1mA (Nominal Range)
 - **Quiescent Current:** < 500 μ A (No Load condition)
 - **PVT Variation:** < 5 mV (Across Process, Voltage, Temperature)
 - **Monte Carlo (MC):** < $\pm 1.5\%$ (Random Variation)
 - **Phase Margin:** > 45° (Full Load)
 - **UGB:** > 1 MHz (Full Load)
 - **PSRR (DC):** > 40 dB
 - **PSRR (High Freq):** > 0 dB (Must not drop below 0dB at any frequency)
 - **Impulse Response:** Capable of handling a sudden 6mA impulse (on top of 1mA static load) with a maximum undershoot of 25mV
 - **De-coupling Capacitor:** Optimized to meet the undershoot specification

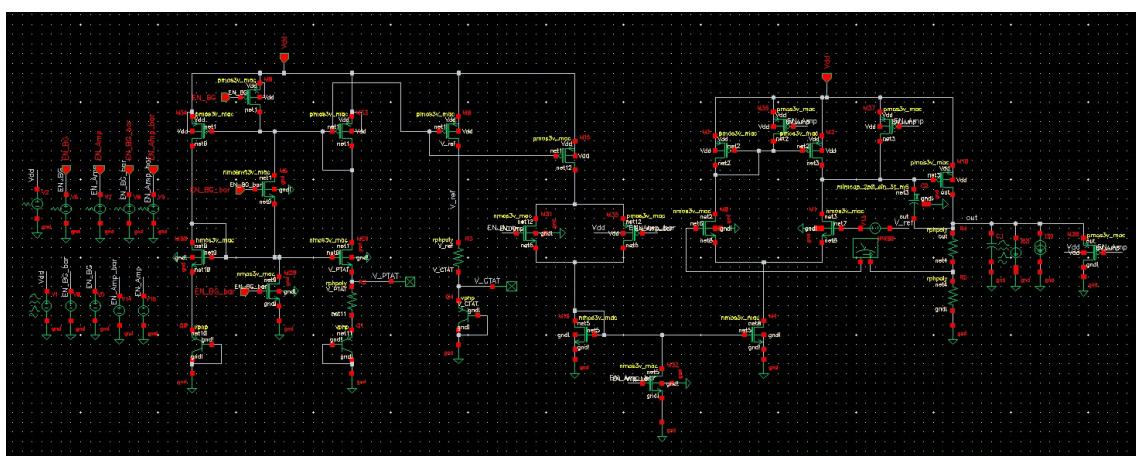


Figure 1: Sub-Regulator Circuit

4 Stability Analysis

The phase margin of the designed sub-regulator is found to be 57.753 degrees > 45 degrees, indicating a stable system.

Unity gain bandwidth is observed to be 1.7067 MHz > 1 MHz requirement.



Figure 2: Loop Gain Analysis (No Load Condition)

Used a 10pF miller compensation capacitor at the output node to achieve the desired phase margin.

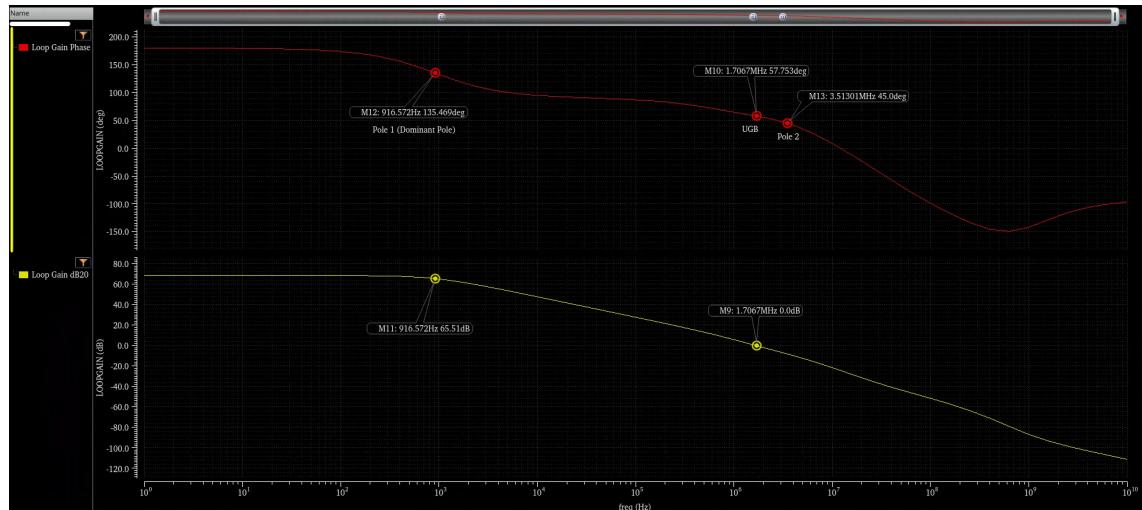


Figure 3: Phase Margin Analysis (No Load Condition)

5 LDO Operation

5.1 DC Operation

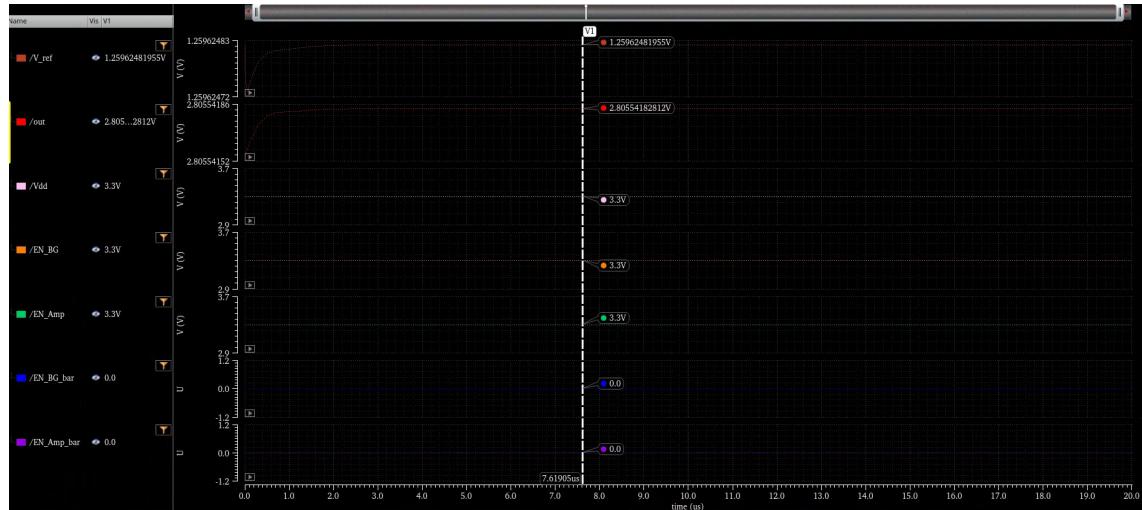


Figure 4: LDO DC Operation

5.2 Transient Operation



Figure 5: Node Voltages in Transient Operation

6 PSRR Analysis

PSRR is analysed in Typical corner at 27C, 3.3V supply voltage. The PSRR at 0Hz is found to be 32.3377dB < 40dB requirement.

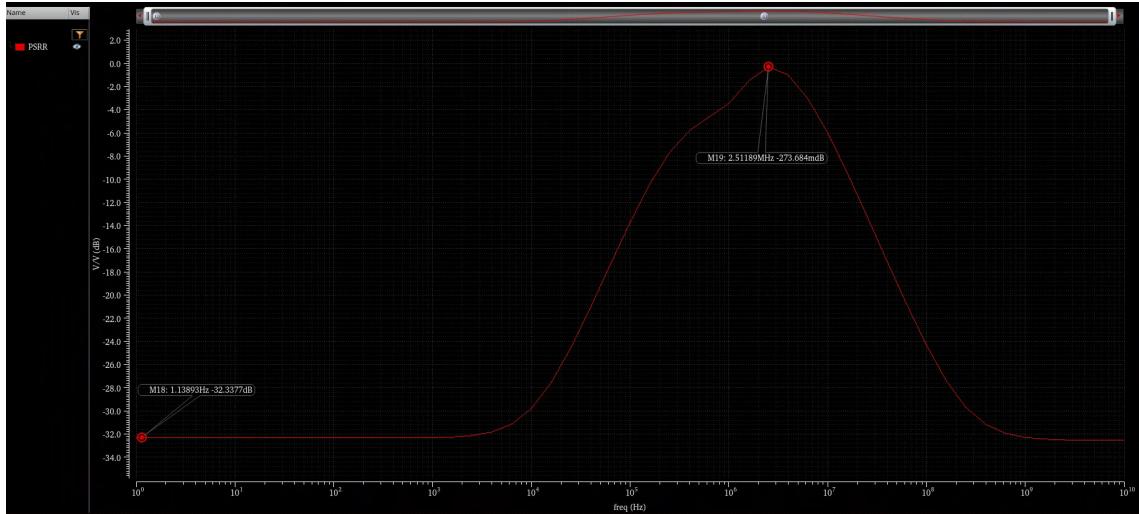


Figure 6: PSRR Analysis

7 Load Regulation Analysis

Load regulation is analyzed by varying the load current from 0mA to 1mA (static load). The output voltage variation is found to be 2.1mV. (In Typical corner at 27C, 3.3V supply voltage)

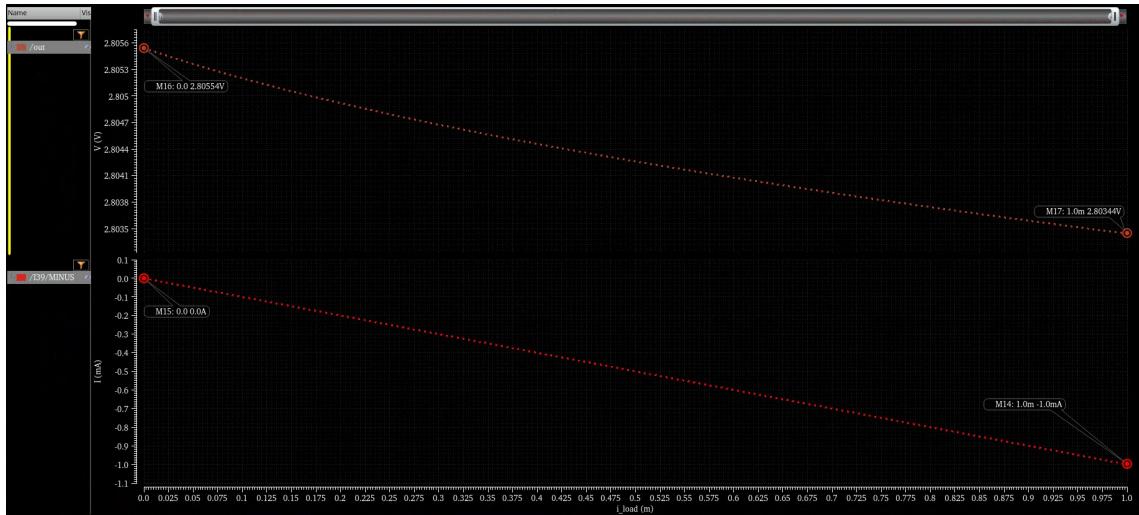


Figure 7: Load Regulation Analysis

8 Load Transient Analysis

110mV overshoot is observed in the output voltage when there is a load step change from 1mA to 7mA.



Figure 8: Overshoot Analysis

9 Testbench setup

Test	Name	Type	Details	EvalType	Plot	Save	Spec	Weight	Units	Digits	Notation	Suffix
Filter	v.ref	expr	VDC1/V.ref"	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	Filter	<input checked="" type="checkbox"/>			Filter	<input checked="" type="checkbox"/>
DC		expr	value(V.ref-40)	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	> 1.2					
DC		expr	value(V.ref-27)	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	> 1.2					
DC		expr	value(V.ref-125)	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	> 1.2					
DC	V.reg	expr	VDC1/out"	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>						
DC		expr	value(V.reg-40)	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	> 2.6					
DC		expr	value(V.reg-27)	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	> 2.6					
DC		expr	value(V.reg-125)	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	> 2.6					
DC	I_tot	expr	(IDC1/M18/5)+IDC1/M2/5+IDC1/M3/5...	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	< 500u					
Time_domain	v/V.ref; tran(V)	expr	vtmet(tran ?V.ref?)	point	<input type="checkbox"/>	<input type="checkbox"/>						
Time_domain	v/V.out; tran(V)	expr	vtmet(tran ?out?)	point	<input type="checkbox"/>	<input type="checkbox"/>						
Time_domain	i/V1/PLUS; tran(I)	expr	itmet(tran ?V1/PLUS?)	point	<input type="checkbox"/>	<input type="checkbox"/>						
Frequency_domain	Loop Gain Phase	expr	phaseDegUnwrappedgetData("loopGain"?r...	point	<input type="checkbox"/>	<input type="checkbox"/>						
Frequency_domain	Loop Gain dB20	expr	db(mag getData("loopGain"?result "stb"))	point	<input type="checkbox"/>	<input type="checkbox"/>						
Frequency_domain	v/out; ac dB20(V)	expr	db(vfreq("out"))	point	<input type="checkbox"/>	<input type="checkbox"/>						
Frequency_domain	v/out; ac deg(V)	expr	phaseDegUnwrapped(freq(ac ?out))	point	<input type="checkbox"/>	<input type="checkbox"/>						
Frequency_domain	V/V1; xf dB20(V/V)	expr	db(getData("V1"?result "xf"))	point	<input type="checkbox"/>	<input type="checkbox"/>						

Figure 9: Output setup in Maestro

10 PVT Variation

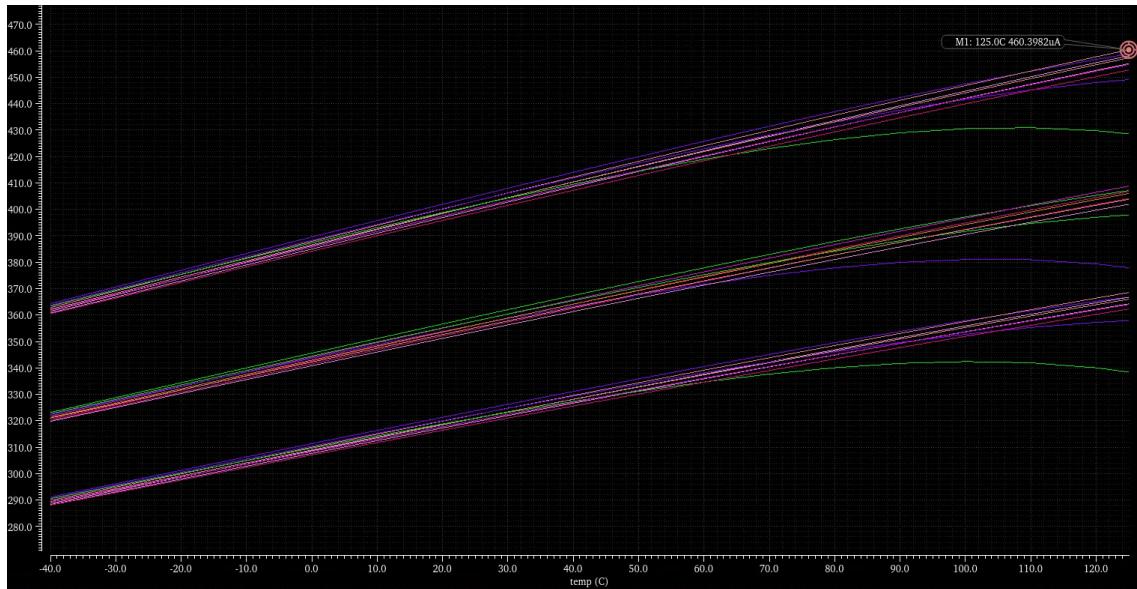


Figure 10: Total current consumption across PVT corners

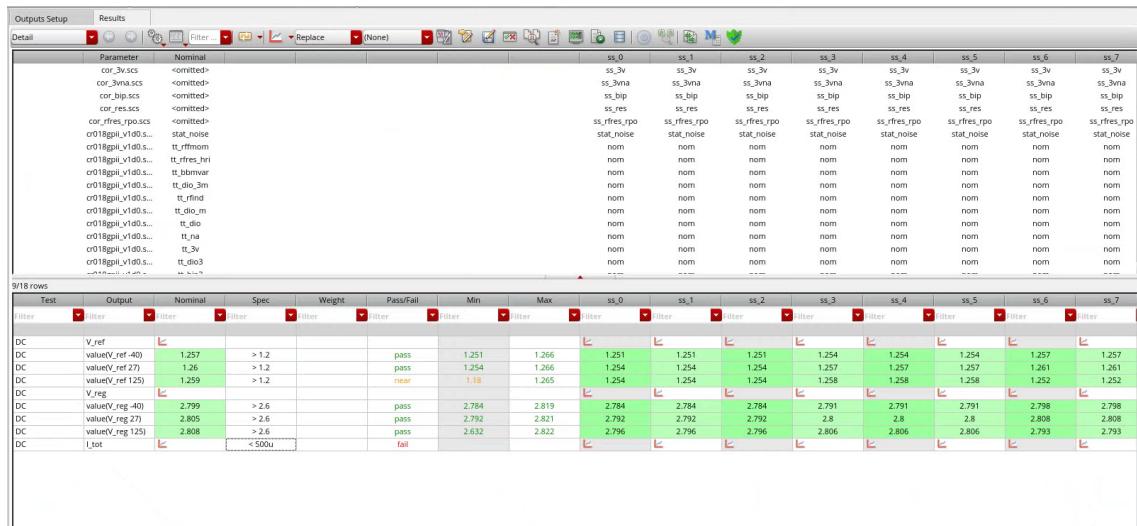


Figure 11: PVT Variation in Output Voltage

11 Monte Carlo Analysis

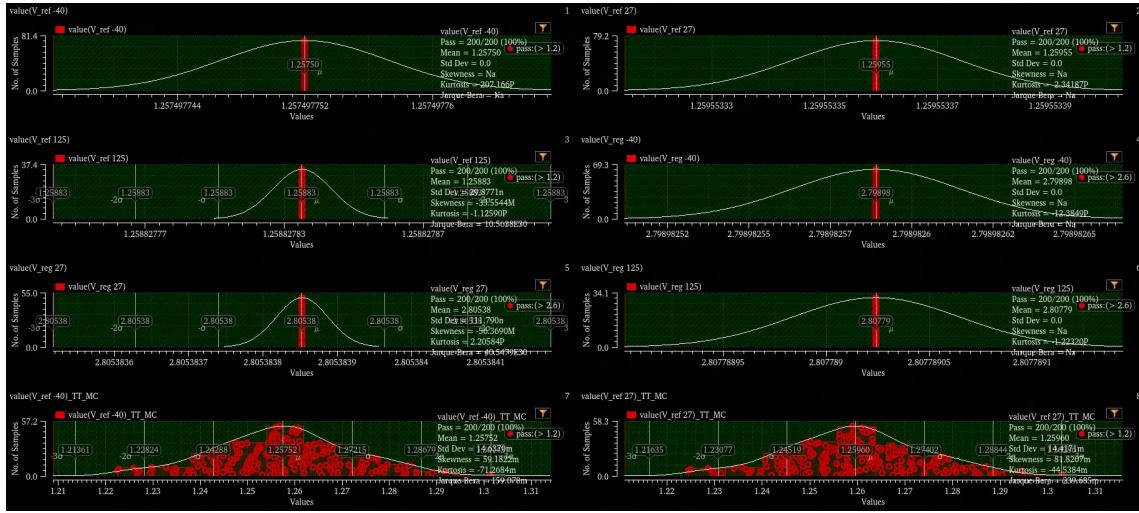


Figure 12: Monte Carlo Analysis Results

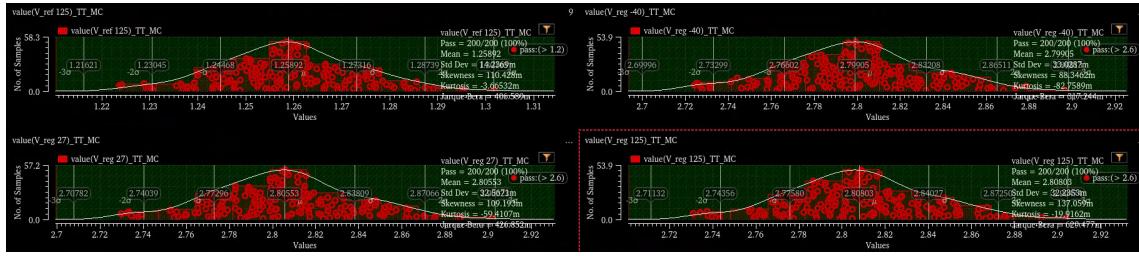


Figure 13: Total Current Consumption in Monte Carlo Analysis

12 Note:

- All the Sub-regulator parameters like PSRR, PM, UGB, load regulation, etc., are captured in a single corner (Typical, 27C, 3.3V). Similar analysis needs to be done in all corners to ensure the design meets the specifications across PVT variations.
- PSRR of the design is less than the required specification of 40dB at 0Hz. Further improvements like cascading the current mirrors, using a different BGR topology, etc., can be explored to improve the PSRR and match the specification across corners and across frequency.
- Used a Miller compensation technique to achieve the desired phase margin. Other compensation techniques can also be explored to optimize the design.
- The overshoot specification is not matched, further optimization via adding a decoupling capacitor at the output node of BGR can be explored to meet the specification.
- The resistive trimming can be done to improve the output voltage accuracy across PVT corners.
- Used an ideal miller capacitor for compensation, the effect of parasitic capacitances can be explored further.
- Need to calculate PVT variation and MC variation percentage properly based on the simulation results and make sure they meet the specifications.
- While designing need to design keeping mind the PVT and MC variations, so that the design meets the specifications across all corners.
- Redo the calculations done for BGR (the one included in this report + the other 3 designs like using different cascaded beta current multipliers) to ensure the design meets the specifications.
- The gain of the OTA can be increased further to improve the PSRR and phase margin.
- Fix the Maestro testbench. (Always use the value from the plot to verify the corner results)