

## VLSI Design : Quiz-2

Monsoon 2024, IIIT Hyderabad (Instructor: Prof. Abhishek Srivastava)

Date : 19<sup>th</sup> October, 2024, Duration : 1 Hour, Max. Marks : 10

### Instructions:

- Clearly write your assumptions (if any)
- Refrain from copying
- Use the previously given 180 nm technology file for the NGSPICE simulations
- You are allowed to use your laptop for simulations and upload to moodle
- You are allowed to use 2 A-4 sheets of own handwritten notes

1. Compute logic functions  $f_1$  and  $f_2$  from Fig. 1. Comment on the static power consumption of the circuit. [2]

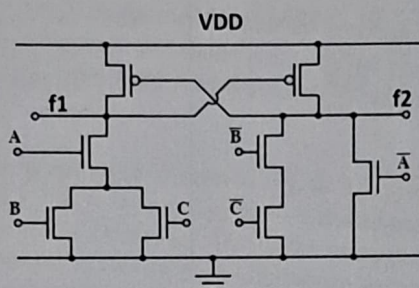


Figure 1

2. What is the logic function  $f$  implemented in Fig. 2(a) using the pass transistor logic (PTL). What is the problem with this implementation. Do you think that the circuit shown in Fig. 2(b) can solve that problem. Explain and also find the logic functions  $f_1$  and  $f_2$ . Implement a two input XNOR function using the logic style shown in Fig. 2(b). [2]

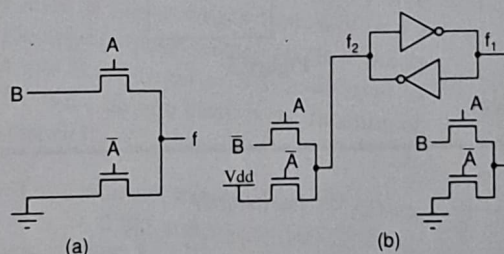


Figure 2

3. Consider the given SPICE netlist quiz\_2\_vlsid\_2024\_prb.cir.

- (a) Draw the full transistor based schematic of the circuit represented by the given netlist by clearly specifying the **nodes, device names and sizes (W/L)** mentioned in the given netlist. To get full credit, it is important to clearly mark the above asked circuit parameters. [1]
- (b) Which circuit is this? Write  $f_{out}$  as a function of signals  $a$ ,  $b$  and  $n$ . [1]
- (c) Calculate C\_LOAD parameter in fF unit and use that value in your simulation.  $C_{LOAD} = (100 + \text{sum of first 8 digits of your roll number} + \text{last 2-digit number of your roll number})$ .  
Example: Roll number: 2023102029,  $C_{LOAD} = 100 + (2+0+2+3+1+0+2+0) + (29) = 139$  fF.  
Roll number: 2024122005  $C_{LOAD} = 100 + (2+0+2+4+1+2+2+0) + (05) = 118$  fF. [0]

100 + 2 + 0 + 2 + 3 + 1 + 0 + 2 + 0 + 29 = 139  
111  
12  
128

- (d) Simulate the given netlist and plot waveforms (pen/paper) of  $n$ ,  $a$ ,  $b$  and  $f_{out}$ , which you observe in simulation results. Also attach plots of  $n$ ,  $a$ ,  $b$  and  $f_{out}$  from simulation **with your roll number and name** printed on the graph. Use set `curplottitle= Your-name-roll`. [1]
- (e) Report and clearly mark on the plot (pen/paper) the on-time and off-time of different  $f_{out}$  pulses observed from 45 ns to 80 ns. ON-TIME is the time for which signal remains high before making the next transition, OFF-TIME is the time for which signal remains low before making the next transition. You can ignore rise and fall time of the pulses. [1]
- (f) Uploads: 1) Netlist with **Name, roll-number, CLOAD value and required plot commands**, 2) all plots in single pdf. (Necessary to get any credit in the previous parts)
4. What do you understand by Blocking and Non-Blocking assignment in Verilog. Draw the diagrams for test-1 and test-2 circuits from the given Verilog descriptions. For both circuits, plot Q1 and Q2 for a given CLK and D signal shown in Fig. 3. [2]

```

module test-1(D, CLK, Q1, Q2);
    output      Q1, Q2;
    input       D, CLK;
    reg         Q1, Q2;

    always @ (posedge CLK)
        begin
            Q1 = D;
            Q2 = Q1;
        end
endmodule

```

```

module test-2(D, CLK, Q1, Q2);
    output      Q1, Q2;
    input       D, CLK;
    reg         Q1, Q2;

    always @ (posedge CLK)
        begin
            Q1 <= D;
            Q2 <= Q1;
        end
endmodule

```

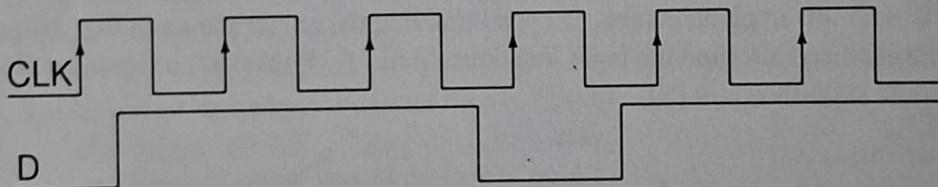


Figure 3

Good luck !!