

CMOS OSCILLATOR IN 5G COMMUNICATIONS.

A project report submitted in partial fulfilment

of the requirements for the degree of

Bachelor of Technology

in

Electronics & Communication Engineering

by

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April 2025



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I hereby declare that the report titled **CMOS OSCILLATOR IN 5G COMMUNICATIONS** submitted by B Madhan Kumar Reddy (21BEC1509) to the School of Electronics Engineering, Vellore Institute of Technology, Chennai in partial fulfillment of the requirements for the award of **Bachelor of Technology in Electronics and Communication Engineering** is a bona-fide record of the work carried out by me under the supervision of **Dr. S UMADEVI**.

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Abstract

This project focuses on the design and optimization of a CMOS ring oscillator intended for high-frequency, low-power applications in 5G communication systems. With the rising demand for efficient circuit designs in modern wireless technologies, the work compares two key architectures: an improved existing method (Method ROCSN) and a proposed SAPON-included method. The existing method incorporates current starvation and negative skewing techniques to enhance frequency performance. Building on this, the SAPON technique adds a carefully placed PMOS and NMOS pair to further reduce power consumption while maintaining reasonable frequency levels. Both designs were implemented and simulated using Cadence Virtuoso in 45nm CMOS technology. Method ROCSN achieved a frequency of 36.36 GHz and consumed 492 μ W of power. The SAPON included design achieved a lower power consumption of 277.77 μ W while maintaining a decent frequency of 28.44 GHz. This project highlights how circuit-level modifications can achieve significant gains in energy efficiency without a substantial sacrifice in performance. A detailed comparison of waveforms and schematic behavior is also presented to validate the effectiveness of the proposed changes. The results clearly show that the SAPON-included design is more power-efficient and better suited for 5G applications.

Acknowledgements

We wish to express our sincere thanks and deep sense of gratitude to our project guide, Dr. Umadevi S, Associate Professor, School of Electronics Engineering, for her consistent encouragement and valuable guidance offered to us in a pleasant manner throughout the course of the project work.

We are extremely grateful to Dr. Ravishankar A, Dean Dr. Reena Monica, Associate Dean (Academics) & Dr. John Sahaya Rani Alex, Associate Dean (Research) of the School of Electronics Engineering, VIT Chennai, for extending the facilities of the school towards our project and for his unstinting support.

We express our thanks to our Head of the Department Dr. Mohanaprasad K for his support throughout the course of this project.

We also take this opportunity to thank all the faculty of the school for their support and their wisdom imparted to us throughout the course.

We thank our parents, family, and friends for bearing with us throughout the course of our project and for the opportunity they provided us in undergoing this course in such a prestigious institution.

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Chapter 1

Introduction

1.1 Introduction to Voltage Controlled Oscillators (VCOs)

A Voltage-Controlled Oscillator (VCO) is a fundamental electronic circuit that produces an oscillating signal—typically a sine wave, square wave, or triangular wave—whose frequency can be controlled by an external input voltage. VCOs are crucial components in a wide range of electronic systems such as wireless communication devices, radar systems, signal modulators/demodulators, and phase-locked loops (PLLs). These circuits enable the dynamic generation of carrier signals for signal processing and modulation tasks.

In the context of modern wireless communications, especially 5G, VCOs play a pivotal role by supporting frequency synthesis and clock generation. The rapid switching and wide tuning range capabilities of VCOs make them suitable for supporting the multi-band operation required in 5G infrastructure. The primary requirements for VCOs in these applications include low phase noise, wide frequency range, compact size, and minimal power consumption. CMOS-based VCOs, especially ring oscillators, have become prominent due to their integrability with existing IC technologies and adaptability for low-power designs.

1.2 Types of Voltage Controlled Oscillators and Their Operation

VCOs can be broadly classified into the following types based on their circuit implementation and output characteristics:

- 1. LC VCOs (Inductor-Capacitor VCOs):** These use a resonant LC tank circuit to generate oscillations. The resonance frequency is determined by the inductance (L) and capacitance (C) values, which can be tuned using varactors (voltage-controlled capacitors). LC VCOs provide excellent phase noise characteristics and frequency stability due to their high Q-factor, making them suitable for RF and high-precision applications. However, they are not easily integrable due to the large area consumed by inductors.
- 2. Ring Oscillator VCOs:** These are composed of an odd number of inverters connected in a feedback loop. The oscillation is sustained by the delay through each inverter stage, and the frequency is determined by the total propagation delay. Ring oscillators are fully

CMOS-compatible, occupy less chip area, and are easier to implement compared to LC VCOs. They are ideal for digital and SoC applications where integration is key, although they suffer from poorer phase noise.

3. **Relaxation VCOs:** These operate by charging and discharging a capacitor using current sources or resistors, generating non-sinusoidal waveforms such as sawtooth or triangle waves. They offer a large tuning range and simplicity in design but are not suitable for applications requiring high-frequency stability.
4. **Colpitts and Hartley VCOs:** Variants of LC VCOs, these utilize different configurations of inductors and capacitors. They are more common in analog designs and radio frequency circuits.
5. **RC VCOs:** These utilize resistor-capacitor combinations instead of inductors. They offer ease of integration and moderate tuning range but typically have poor phase noise performance.

Each of these VCO types has unique advantages and is selected based on application requirements, such as tuning range, noise tolerance, power consumption, and integration capabilities.

1.3 Ring Oscillators and Their Advantages

Ring oscillators consist of an odd number of NOT gates or inverters connected in a feedback loop. The signal transitions through the inverter stages, and due to the total loop delay, the output oscillates between high and low voltage levels. The frequency of a ring oscillator is given by:

$$f = \frac{1}{2nT_d}$$

where n is the number of inverter stages and T_d is the propagation delay per inverter.

Advantages of ring oscillators include:

- **Full CMOS compatibility:** No need for external inductors or capacitors.
- **Compact size:** Suitable for integration in system-on-chip (SoC) and mobile platforms.
- **Low power consumption:** Especially when optimized with current-starved or skewed inverter techniques.
- **Wide tuning range:** Easily controlled by adjusting voltage or current sources.

Despite their higher phase noise compared to LC VCOs, ring oscillators are widely used in high-speed, low-power environments like 5G modems, where space and power budgets are limited.

1.4 VCOs in Phase-Locked Loops (PLLs) and Applications in 5G

Phase-Locked Loops (PLLs) are feedback control systems that synchronize the output frequency of a VCO to a reference input signal by continuously adjusting the VCO's control voltage. A basic PLL comprises a Phase Detector (PD), Low-Pass Filter (LPF), Voltage Controlled Oscillator (VCO), and a Feedback Divider.

PLLs serve crucial functions in clock recovery, frequency synthesis, modulation, and demodulation. In the context of 5G, PLLs are instrumental in generating stable carrier signals and supporting rapid switching between frequency bands, which is vital for high-speed data communication.

Below is a block diagram representation of a typical PLL:

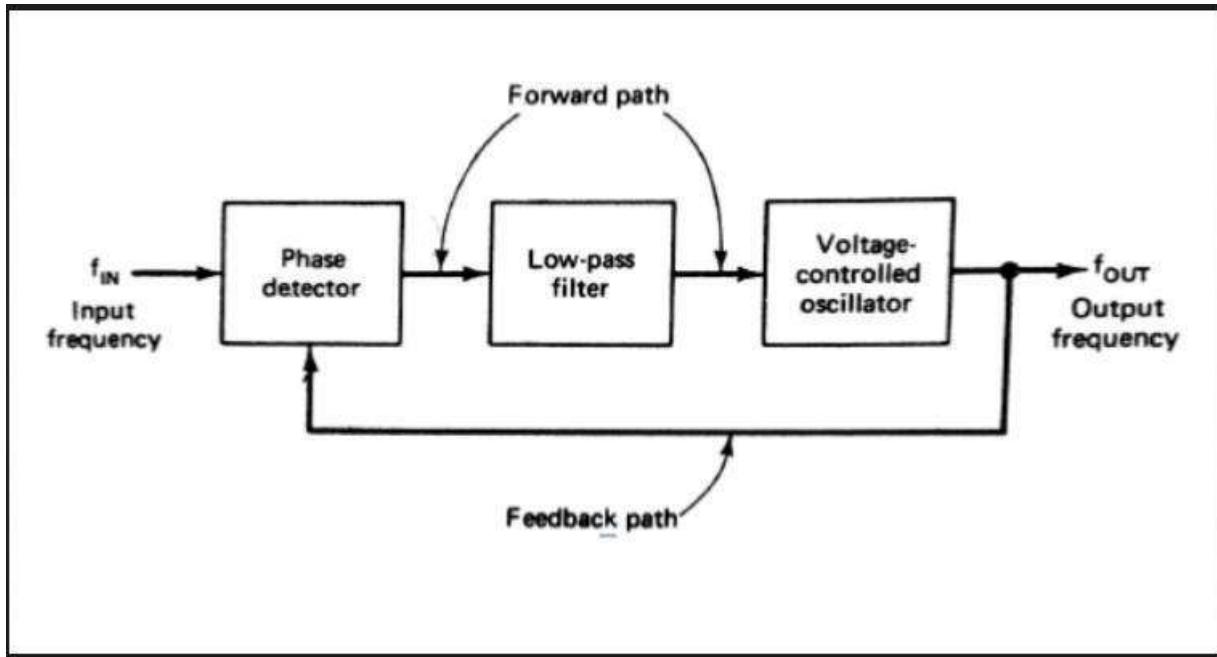


Fig.PLL

The VCO inside the PLL must exhibit low phase noise and fast tuning capabilities. The loop ensures frequency stability and quick adaptation to variations in the reference input. For 5G applications, such attributes are vital due to the stringent timing and frequency accuracy required by the standard.

The deployment of 5G technology introduces significant demands on oscillator performance. With spectrum allocations extending into the millimeter-wave (mmWave) bands (above 24 GHz), VCOs must deliver extremely high frequencies while consuming minimal power. Furthermore, carrier aggregation and MIMO technologies in 5G require multiple synchronized oscillators within transceivers.

VCOs used in 5G systems must be capable of fast tuning, stable operation, and reduced jitter. CMOS ring oscillators are increasingly favored due to their integrability and efficiency. By applying techniques like current starvation, negative skewing, and the SAPON method, designers can significantly enhance the power-frequency trade-off of ring oscillators. These advancements enable their application in high-speed 5G modems, small cells, and IoT devices.

1.5 Design Trade-offs in VCO Architectures

VCO design often involves balancing multiple performance metrics:

- **Phase noise:** Critical for signal clarity and reducing bit error rate.
- **Power consumption:** Especially important in battery-powered and mobile devices.
- **Tuning range:** Required for multi-band and agile systems.
- **Chip area and integration feasibility.**

LC VCOs are superior in noise and stability but require large chip area due to inductors. Ring oscillators, though inferior in noise, are better suited for integration. Techniques such as current starvation reduce power by limiting the drive current, while negative skewing enhances the signal slope for faster transitions. The SAPON method combines switching and power optimization, further improving ring oscillator suitability for 5G.

1.6 Project Motivation and Scope

This project aims to explore advanced CMOS ring oscillator architectures tailored for 5G communication systems. Traditional designs struggle to meet the combined requirements of low power and high frequency, especially in integrated environments. This work addresses these limitations by evaluating and optimizing ring oscillator topologies.

Starting with a baseline CMOS design, the project incorporates current starvation and negative skewing to improve delay characteristics and reduce power consumption. A novel SAPON technique is introduced to further minimize energy usage while retaining acceptable oscillation frequency. Comparative analysis of power and frequency across multiple methods provides insights into their practical viability in future communication hardware.

1.7 Objectives

The primary objective of this project is to design and optimize a CMOS ring oscillator that meets the stringent demands of 5G technology. This includes achieving a balance between high frequency and low power consumption, essential for next-generation wireless systems. Specific goals include:

- Design and analysis of conventional and modified CMOS ring oscillator circuits.
- Implementation of current starvation and negative skewing to improve performance.
- Introduction and validation of the SAPON method for further optimization.
- Comparative evaluation of frequency and power metrics across different methods.
- Verification through simulation and schematic/layout design in 45 nm technology.

These objectives help establish a robust framework for integrating efficient oscillators in high-speed communication devices.

Chapter 2

Literature Survey

The ring oscillator, particularly in CMOS technology, remains a topic of significant interest due to its critical role in frequency generation for high-speed applications, including 5G communication systems. With the ever-growing demands for smaller, faster, and more energy-efficient devices, numerous researchers have focused on innovating and optimizing oscillator architectures. This literature review presents a comprehensive overview of research efforts relevant to this project, particularly those targeting improvements in power consumption, area reduction, frequency control, and leakage minimization.

2.1 Optimization of Ring Oscillator Using PTL Logic

One of the more efficient approaches to oscillator design was proposed in the paper “*Optimization of Ring Oscillator Using PTL Logic*”. The study introduced a ring oscillator structure based on Pass Transistor Logic (PTL), which is known for significantly reducing transistor count. By using pass transistors instead of full CMOS inverters, the design minimizes switching elements, thereby conserving power and saving layout area.

The oscillator achieved its primary goal of area and power reduction, using only 37 MOS transistors, which is a substantial improvement over conventional designs that often use upwards of 60 transistors. Although this simplification brought gains in area and efficiency, the circuit suffered slightly from degraded signal integrity due to weaker drive strength of pass transistors. Despite this, the paper demonstrated that with careful design, PTL-based oscillators could serve well in applications where minimal silicon real estate and low power are prioritized.

2.2 Design of Low Power Ring Oscillator Using Current Starved Inverter

Another pivotal paper investigated the current-starved inverter configuration, a technique that restricts the current flowing into inverter stages to control delay and power usage. This design is particularly relevant for portable devices and IoT systems that operate on strict power budgets.

The architecture works by placing two transistors in series with the standard CMOS inverter to “starve” the current. As a result, the frequency of oscillation can be finely tuned by controlling the gate voltage of the current-limiting transistors. Although this architecture introduces a slight complexity in design and tuning, the benefits in terms of power saving are substantial. The paper illustrated how this approach maintains stable oscillation at moderate frequencies while significantly cutting down on static and dynamic power losses.

2.3 Design and Performance Analysis of a 5 GHz CMOS Ring Oscillator

In the context of 5G, which operates at frequencies above 3 GHz, the paper “Design and Performance Analysis of a 5 GHz CMOS Ring Oscillator” stood out as particularly relevant. The authors implemented a ring oscillator operating at 5.14 GHz using 0.9V supply in 45nm CMOS technology. Their simulation showed promising performance with a remarkably low power consumption of $1.2 \mu\text{W}$.

The study thoroughly analyzed the effects of transistor sizing and stage count on oscillator performance. It concluded that while increasing stages enhances frequency range and reduces jitter, it can also increase delay and power. Therefore, a careful balance was struck to optimize for 5G’s speed demands while maintaining energy efficiency. The design methodology from this paper informed this project’s approach to achieving high-speed oscillation within tight power constraints

2.4 Area and Power Optimized Ring Oscillator Using Modified Delay Cell

The paper “*Area and Power Optimized Ring Oscillator*” explored a custom delay cell architecture designed to reduce power consumption and silicon footprint. Instead of relying on traditional inverter chains, the modified delay cell incorporated current mirrors and differential structures to improve control over delay and reduce static power.

The resulting circuit achieved an oscillation frequency of 2.83 GHz, with a total power dissipation of $34.63 \mu\text{W}$ and a silicon area of just $191.88 \mu\text{m}^2$. These results demonstrate the efficiency of architectural changes in reducing resource consumption. The paper serves as a valuable reference in optimizing delay elements a key strategy used in this project for achieving frequency control and layout compactness.

2.5 Leakage Reduction Using SAPON in Ring Oscillator Designs

As technology nodes shrink, leakage power becomes a more serious issue. In the paper detailing the SAPON technique (*Stackly Arranged low Power ON transistor*), a novel method of stacking transistors was introduced to reduce leakage currents without impacting active performance.

The approach works by arranging ON transistors in a stacked configuration, thereby increasing the effective resistance in the OFF state and suppressing leakage flow. The SAPON structure was tested within a ring oscillator framework and demonstrated significant reductions in leakage power, especially during idle states.

This innovation aligns perfectly with energy-efficient circuit design, as it allows devices to operate for longer durations without sacrificing performance during active states. SAPON was directly implemented in this project to reduce both static and dynamic power.

2.6 5GHz Ring Oscillator Design in 45nm Technology

A separate study reinforced the importance of technology scaling in oscillator design. Using 45nm CMOS, the authors designed a compact ring oscillator capable of reaching 5 GHz. This research demonstrated how advanced process nodes improve frequency capability and reduce overall parasitics, leading to more efficient designs.

Through SPICE simulations, it was shown that by adjusting load capacitance and lowering the supply voltage, a high-frequency oscillator could be designed without the need for LC tanks. The circuit, operating on 0.9V supply, achieved both area savings and improved tuning capability. This work provided key insights into optimizing layout and load balancing to improve circuit performance concepts that were adopted during this project's layout phase..

2.7 Comparison of Oscillator Architectures for High-Frequency Systems

An analytical study compared the performance of Colpitts, Hartley, LC tank, and ring oscillators across different parameters such as phase noise, area, and power. The analysis concluded that while LC-based designs offer better spectral purity, they require bulky inductors and capacitors, making them unsuitable for dense VLSI systems.

In contrast, ring oscillators despite having higher phase noise excel in integration, simplicity, and scalability. This comparison validated the choice of ring oscillator for 5G applications where compactness and energy efficiency often outweigh minor performance losses in noise characteristics.

2.8 Modified Current Starved Ring Oscillator for VCOs

The final reference analyzed a Modified Current Starved Ring Oscillator tailored for use in voltage-controlled oscillator (VCO) applications. By introducing biasing transistors and adjustable current sources, the oscillator's frequency range was widened significantly, allowing it to meet variable signal generation requirements.

This configuration was tested in a PLL environment, showcasing excellent linearity in control voltage to frequency mapping. While slightly more complex than basic current-starved designs, the modified architecture showed clear advantages for applications requiring flexible tuning as is often the case in adaptive 5G communication systems.

2.9 Design and Implementation of Low Phase Noise CMOS Ring Oscillator for High-Speed Applications

The paper “Design and Implementation of Low Phase Noise CMOS Ring Oscillator for High-Speed Applications” presents an enhanced CMOS ring oscillator topology optimized for low phase noise operation, which is essential in high-speed digital and RF systems. The authors introduced an adaptive feedback loop and utilized symmetric delay cells to control jitter and maintain signal integrity. Through careful manipulation of transistor sizing and layout symmetry, the design achieved a phase noise of -90 dBc/Hz at 1 MHz offset while operating above 4.8 GHz in a 65nm CMOS process.

This research highlights the critical relationship between phase noise and circuit symmetry, an insight that directly applies to our project’s focus on stable frequency generation in 5G environments. The techniques discussed—such as differential buffering and controlled capacitance—guide the refinement of our oscillator architecture, particularly in minimizing timing inconsistencies and enhancing noise immunity in ring oscillator-based VCO systems.

2.10 CMOS Ring Oscillator Design Techniques for Low Supply Voltages

The study “CMOS Ring Oscillator Design Techniques for Low Supply Voltages” explored how voltage scaling influences the behavior of ring oscillators, particularly under 1V operation. The researchers implemented level shifters and modified inverter stages to ensure functionality at reduced voltages, targeting energy-constrained devices like IoT and edge computing systems.

Their design achieved reliable oscillation at 3.6 GHz while consuming less than 1.5 μ W of power, making it ideal for modern low-voltage platforms.

In addition to the hardware adjustments, the paper also analyzed the delay variations and gain degradation associated with low-voltage operation. These observations reinforce the importance of balancing supply voltage and transistor sizing, a principle incorporated in our project's SAPON-based optimization. The low-voltage strategies discussed informed our design constraints, ensuring efficient operation without compromising on frequency performance or stability.

2.11 Analysis of Low Phase Noise Ring Oscillators for RF Applications

The paper “Analysis of Low Phase Noise Ring Oscillators for RF Applications” explores how ring oscillator topology affects phase noise, a critical parameter in RF and communication circuits. By analyzing various design parameters such as number of stages, load capacitance, and biasing conditions, the authors presented a comparative evaluation of different ring oscillator configurations in the RF domain. The study emphasized the detrimental effects of phase noise on signal integrity and data transfer reliability, especially in high-frequency communication systems like 5G.

A notable contribution of this paper is the methodical optimization of stage delay and transistor sizing to minimize phase noise without significantly increasing power consumption. By incorporating differential signaling and symmetry in layout, the design successfully reduced jitter and spurious noise. These insights are relevant to our project, particularly in shaping strategies to reduce timing inconsistencies in ring oscillator outputs used in synchronization systems.

2.12 Compact VCO Design for Multi-Band 5G Systems

The paper titled “Compact VCO Design for Multi-Band 5G Systems” targets the demand for compact and power-efficient VCOs operating across multiple frequency bands. With 5G systems requiring seamless switching between sub-6GHz and mmWave bands, the authors proposed a dual-mode ring oscillator architecture that switches between two different delay paths. This enabled operation across a wide frequency range without significantly increasing layout complexity.

The design used dynamic biasing to enhance frequency control and incorporated digital calibration circuits to compensate for process and temperature variations. The paper highlighted that this dual-mode operation improved tuning linearity while maintaining energy efficiency an essential balance in 5G mobile applications. Its findings provide a conceptual foundation for the frequency tuning mechanisms considered in this project.

2.13 Frequency Tuning and Linearity Improvement Techniques in CMOS VCOs

In “Frequency Tuning and Linearity Improvement Techniques in CMOS VCOs”, the authors addressed two key challenges in VCO design: non-linear frequency control and limited tuning range. They introduced a tuning circuit composed of switched capacitor arrays and digitally controlled current sources. This structure significantly enhanced both the linearity and tuning span of the VCO, which is critical in agile frequency-hopping systems such as those employed in 5G networks.

The study also explored the impact of parasitic capacitances and process variations, offering compensation techniques using on-chip trimming elements. It contributed valuable guidelines for our work, especially for the SAPON-enhanced VCO where tuning efficiency and predictable control-to-frequency response are crucial design targets.

2.14 Power-Aware Design of High-Speed Ring Oscillators in 28nm CMOS

This research focuses on the “Power-Aware Design of High-Speed Ring Oscillators in 28nm CMOS”, providing insight into how shrinking technology nodes influence oscillator behavior. The authors demonstrated that careful gate sizing, combined with body biasing techniques, could lead to substantial power savings while maintaining oscillation stability at GHz frequencies. Using FinFET-based devices, they achieved performance metrics surpassing those of traditional CMOS VCOs.

A major takeaway from this study is the use of adaptive voltage scaling and leakage minimization during inactive states, helping reduce average power consumption. This aligns with our project's goals of achieving high-speed, low-power operation in a modern CMOS process, particularly under the SAPON method.

2.15 Digitally Tuned Ring Oscillators for PLL-Based Frequency Synthesizers

In this paper, the authors investigated “Digitally Tuned Ring Oscillators for PLL-Based Frequency Synthesizers”, presenting a hybrid analog-digital approach to frequency control. The proposed design integrated digital tuning words to vary bias currents, offering both fine and coarse control over output frequency. This method was shown to greatly improve loop acquisition time and frequency stability in PLL circuits.

The paper highlighted the role of digital calibration in overcoming non-idealities caused by process variation and thermal noise, key concerns in advanced VLSI circuits. Such strategies offer inspiration for further refining our SAPON ring oscillator in PLL configurations, improving both precision and reliability.

Chapter 3

Methodology

3.1 Impact of Negative Skewing on Ring Oscillators

In digital and analog VLSI design, clock skew plays a critical role in the performance and stability of circuits, especially those reliant on time-sensitive operations like ring oscillators. One of the most interesting phenomena observed in clock systems is negative skew, where the destination register receives the clock signal before the source register. While typically considered a timing anomaly, negative skew can be intentionally induced and leveraged to optimize oscillator behavior, particularly in high-frequency systems.

In the context of ring oscillators, the impact of negative skewing is significant due to the recursive nature of the feedback loop. A ring oscillator operates based on a chain of inverters or logic gates connected in a closed loop, where the propagation delay of each stage determines the oscillation frequency. By introducing negative skew in the signal transitions between stages, the total loop delay can be slightly decreased, resulting in faster oscillation frequencies.

Moreover, negative skewing can assist in timing margin balancing. For example, in circuits with unequal stage delays, selectively skewing the clock or signal transitions can help equalize propagation paths, improving symmetry in oscillation waveforms. This technique is particularly helpful when scaling down transistor sizes or operating under lower voltages, both of which inherently introduce signal degradation and variability.

However, negative skew must be carefully managed. If the skew is too large, it can create race conditions or premature transitions that corrupt signal integrity. Therefore, in advanced ring oscillator designs, controlled negative skewing often achieved by adjusting load capacitance or transistor sizing is a subtle but powerful tool for enhancing frequency performance without additional circuit overhead.

In the case of the present design, negative skewing was leveraged as a secondary tuning mechanism. While not the core method of optimization, introducing slight timing shifts at selected stages helped fine-tune the feedback loop's timing characteristics, ultimately contributing to a more stable and higher-frequency oscillator that aligns with 5G's performance benchmarks.

3.2 Current Starvation Technique

One of the most effective techniques for minimizing power consumption in CMOS ring oscillators is the current starvation technique. This method modifies the traditional inverter chain by restricting the current available to each inverter, thereby reducing dynamic and static power dissipation.

In a standard CMOS inverter, current flow is unregulated during transitions, leading to rapid charging and discharging of load capacitances. This results in high power consumption, especially when oscillators operate at GHz-level frequencies. Current starvation addresses this by introducing series-connected transistors one NMOS and one PMOS before the power supply and ground rails. These transistors act as current-limiting devices, controlling the amount of current that each inverter stage can draw.

The advantages of this technique are two-fold:

- Power Efficiency: Limiting current reduces unnecessary power draw, especially in idle or low-activity states.
- Frequency Control: The oscillation frequency becomes a function of the current available to each stage, enabling fine-tuned control by simply varying the gate voltages of the current-limiting transistors.

In the proposed architecture of this project, current-starved inverters form the basic delay cells of the oscillator. This approach ensures that the oscillator remains within low-power design constraints while offering programmable frequency outputs. Moreover, by sizing the limiting transistors appropriately, trade-offs between speed and energy efficiency can be precisely controlled.

One challenge with current-starved inverters is the risk of output signal degradation due to reduced drive strength. If the limiting transistors are too small, the inverter may fail to transition fully, causing output waveform distortion. This was addressed in the current design through transistor sizing optimization and by limiting the number of stages to maintain signal integrity.

Ultimately, current starvation is a key enabler in building energy-efficient, frequency-controllable ring oscillators, making it ideal for 5G applications where both high performance and low power are critical.

3.3 SAPON Technique

As CMOS technology continues to scale down into deep sub-micron regions, leakage power becomes a dominant concern—particularly in always-on circuits like oscillators. The SAPON (Stackly Arranged low Power ON Transistor) technique is an innovative strategy that significantly reduces leakage currents without requiring complex circuitry or active control mechanisms.

The core idea behind SAPON is the vertical stacking of transistors in the OFF state, increasing the resistance of the leakage path. In a typical CMOS transistor, sub-threshold leakage occurs even when the gate is low (OFF), particularly when operating at low threshold voltages. By stacking two or more such OFF transistors in series, the total leakage path resistance increases, and the intermediate node voltages cause the effective threshold voltages of individual transistors to rise. This phenomenon, known as the stack effect, leads to exponential reductions in leakage current.

The SAPON technique applies this concept elegantly by designing delay cells with multiple transistors in a stacked configuration. This allows the oscillator to retain its core function while consuming drastically less power in idle states. Importantly, SAPON achieves this without the need for external control signals, making it a passive yet highly effective leakage mitigation method.

In the proposed ring oscillator, SAPON-based delay cells are introduced as replacements for conventional inverter stages.

This modification not only preserves oscillation functionality but also enhances overall power efficiency, especially in sub-threshold or near-threshold operating regimes.

Another advantage of the SAPON technique is its layout compatibility. The stacked arrangement can be implemented within the same footprint as a traditional inverter cell, with only minor changes to the standard cell library. This makes SAPON particularly appealing for high-density SoC designs, where area constraints are critical.

In the context of this project, the SAPON methodology was utilized in conjunction with current-starved delay cells to produce a hybrid design that addresses both dynamic and leakage power concerns. The final architecture represents a balanced trade-off between frequency performance and ultra-low power operation, aligning perfectly with the stringent demands of 5G communication modules and IoT systems.

3.4 Conventional CMOS Ring Oscillator

The first method investigated as part of the project was the Conventional CMOS Ring Oscillator, which serves as the baseline for comparison. This architecture is built using a simple loop of odd-numbered inverter stages, typically three, five, or seven, connected end-to-end. The last inverter's output is fed back to the input of the first, creating a delay loop. The resulting feedback causes the output to oscillate between high and low voltages.

In this section, we present an in-depth explanation of the mentioned circuit a power-conscious CMOS ring oscillator structure enhanced through a current-starving technique and current mirror biasing. This architecture is a refined variant of the traditional current-starved ring oscillator (CSRO), integrating additional control elements to improve power efficiency and operational stability, which are vital for modern low-power VLSI systems such as those used in 5G communication.

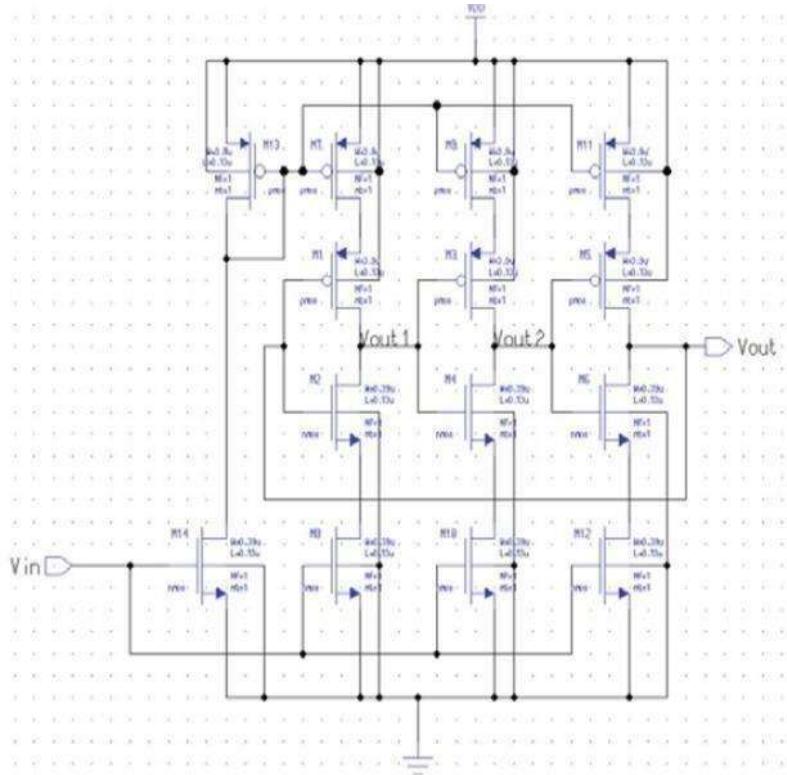


Fig. Conventional CMOS Ring Oscillator

3.4.1 Circuit Overview

The architecture of this method is built upon three fundamental CMOS inverter stages:

- **M1-M2,**
- **M3-M4, and**
- **M5-M6,**

Each of these inverter pairs forms the core switching elements of the oscillator. They are responsible for producing the oscillatory behavior by creating the necessary propagation delay across stages.

However, instead of connecting them directly to the supply rails (VDD and GND), each inverter is connected via current-limiting transistors, which serve as controlled resistive elements to modulate current flow.

Specifically:

- **M7 and M8** limit the current into the first CMOS inverter pair (M1-M2),
- **M9 and M10** perform the same function for M3-M4, and

- **M11 and M12** are associated with M5-M6.

These transistors are carefully biased such that they operate in the saturation region, thereby acting as current sources or sinks. By controlling the gate voltages of these transistors, the overall power consumption of the circuit can be adjusted dynamically.

To generate the required biasing voltages for these current limiters, a current mirror circuit is used, comprising **M13 (PMOS)** and **M14 (NMOS)**. These transistors replicate a reference current and distribute it symmetrically to the current-starving transistors, ensuring uniform behavior across all inverter stages.

3.4.2 Functional Behavior and Signal Flow

The operation begins when an input signal (**V_{in}**) is applied. This input is first passed through the current mirror formed by M13 and M14, which stabilizes the biasing environment for the rest of the circuit. From here, the signal propagates through each inverter stage (M1-M6), undergoing phase inversion and delay at each level.

The inclusion of current-starving transistors ensures that:

- The charging and discharging rate of the internal node capacitances is limited,
- The rise and fall times of the output signals are elongated, and
- Power dissipation is significantly reduced, particularly during high-frequency transitions.

By forcing the PMOS and NMOS transistors in each inverter to operate under controlled current conditions, the circuit avoids large surges of switching power, which is a known drawback in traditional CMOS ring oscillators.

At the output, after the third inverter stage, the signal is collected from V_{out}, completing the oscillatory loop.

The key internal nodes (V_{out1}, V_{out2}) between inverter stages further exhibit characteristic delays that cumulatively determine the oscillation frequency. Because this is a ring configuration with an odd number of inverter stages (three in this case), the feedback ensures a stable oscillation, provided the loop gain is sufficient and phase shift equals 180 degrees.

3.4.3 Analysis of Transistor Roles

- **Inverter Pairs (M1–M6):**

These six transistors form three classic CMOS inverters. Each inverter flips the logic state of the signal, contributing a delay that is essential for oscillation. The PMOS (M1, M3, M5) sources current when the input is LOW, and NMOS (M2, M4, M6) sinks current when the input is HIGH.

- **Current-Starving Transistors (M7–M12):**

These act as series resistors (or current gates) above and below the inverters. Their function is to limit the amount of current that can pass through the inverter stage. They are typically biased in such a way that they remain in saturation, offering near-constant current flow. This controlled current flow directly limits the charging speed of parasitic capacitances at the inverter output nodes, effectively managing dynamic power.

- **Current Mirror Pair (M13–M14):**

The purpose of these transistors is to replicate a reference current and maintain bias stability. M13 (PMOS) and M14 (NMOS) are configured in such a way that they mirror and regulate the current into each of the current-starving branches. This ensures a uniform power distribution and prevents overloading of any single stage, even under fluctuating input conditions.

3.4.4 Advantages and Disadvantages

This method strikes a solid balance between simplicity and control. Here are the primary benefits of this structure:

- **Power Efficiency:** By starving the inverters using controlled current paths, unnecessary dynamic power is reduced significantly. This helps in low-power applications such as on-chip timers and PLLs.
- **Design Simplicity:** The architecture remains compact and easy to simulate, with the use of only basic building blocks — CMOS inverters and current mirrors.
- **Voltage Controllability:** The current mirror network allows external voltage (V_{in}) to indirectly influence the delay and frequency of the oscillator. This makes the design adaptable and suitable for use in voltage-controlled oscillators (VCOs).

However, while this approach introduces power-saving mechanisms, it is not without its shortcomings:

- **Limited Frequency Range:** Since the inverters are deliberately starved of current, the oscillation frequency is constrained. This limits the circuit's application in high-frequency domains like mmWave or 5G-level speeds.

- **Reduced Drive Strength:** With current starved operation, the output drive becomes weaker, which can lead to degraded signal integrity, especially if the output needs to feed multiple stages.
- **Voltage and Temperature Sensitivity:** The performance of the current mirror circuit is heavily dependent on process-voltage-temperature (PVT) variations. This can lead to undesired frequency fluctuations under changing environmental or load conditions.
- **Increased Delay Variation:** The starved inverters exhibit higher delay variation, making it less reliable in timing-sensitive applications.

3.5 Ring Oscillator with Combined Current Starvation and Negative Skewing (ROCSN)

As a step forward from the traditional current-starved oscillator, the second method integrates two advanced techniques selective current starvation and negative skewing to improve both performance and efficiency. This design was developed to address the limitations observed in Existing Method 1, such as reduced speed, limited frequency control, and increased delay variation. The new architecture blends control and speed optimization by selectively starving certain stages of the oscillator, while allowing others to switch freely, thereby reducing cumulative delay and enhancing stability.

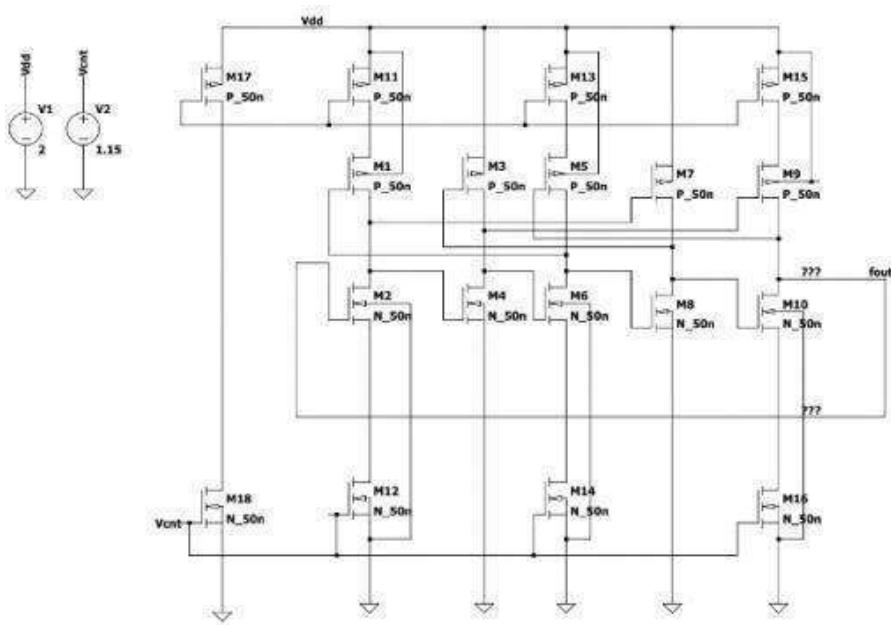


Fig. Ring Oscillator with Combined Current Starvation and Negative Skewing

3.5.1 Circuit Overview and Configuration

As illustrated in above figure the circuit comprises five CMOS inverter stages formed by transistor pairs M1–M10, where:

- M1 & M2, M3 & M4, M5 & M6, M7 & M8, and M9 & M10 act as CMOS inverter pairs.
- Only M1-M2, M5-M6, and M9-M10 are current-starved using upper PMOS and lower NMOS limiters:
 - M11 & M12 control current for M1-M2.
 - M13 & M14 for M5-M6.
 - M15 & M16 for M9-M10.
- M17 (PMOS) and M18 (NMOS) form a current mirror pair, creating a stable reference across the current-starved branches.
- The intermediate stages (M3-M4 and M7-M8) are directly powered, enabling faster propagation and providing a negative skew effect in the timing.

The design uses two supply voltages:

- VDD = 2V standard supply to the main circuit.
- Vcnt = 1.15V control voltage applied to the current mirrors (M17, M18), regulating the starving current flow.

3.5.2 Working Mechanism and Design Strategy

The oscillator relies on the classic ring principle: an odd number of inverter stages looped together to produce continuous oscillation. However, unlike uniformly structured designs, this method breaks the symmetry intentionally.

- The current-starved stages (1st, 3rd, and 5th) introduce deliberate delay by restricting current through PMOS and NMOS control transistors.
- The 2nd and 4th stages are fully powered, switching at maximum speed, introducing negative skew i.e., signals transition faster than expected between some nodes, effectively reducing total loop delay.
- The current mirror formed by M17 and M18 distributes a uniform bias current across all control branches, ensuring stability despite variations in load or temperature.

This combination allows high-frequency operation with energy efficiency and gives designers

flexibility in controlling oscillation range.

3.5.3 Role of Each Component

- **M1–M10 (CMOS Pairs):** These form the core inverter stages of the oscillator. By selectively starving some while powering others, the design achieves hybrid control over delay and power.
- **M11–M16 (Starving Transistors):** These limit the current through selected inverters. Controlled via mirrored voltages, they dynamically shape the frequency response.
- **M17 & M18 (Current Mirror):** This pair supplies a consistent control current to all starving PMOS/NMOS pairs. It minimizes the effect of PVT variations on oscillator stability.

The presence of high-speed, non-starved stages in the loop serves as timing accelerators, which help maintain a high oscillation frequency even when other stages operate under restricted conditions.

3.5.4 Advantages and Disadvantages

This hybrid structure was chosen to address the key weaknesses of Conventional Method while keeping complexity minimal. Here's what this method improves:

- **Higher Oscillation Frequency:** By avoiding starvation in alternate stages, signal propagation becomes faster, pushing the frequency upward.
- **Power Savings Where Needed:** Starving only three out of five stages still achieves significant power savings without degrading performance.
- **Improved Drive Strength:** Fully powered stages compensate for weakened outputs in current-starved stages, improving signal integrity.

While Method ROCSN significantly enhances performance over the previous architecture, it is not without trade-offs:

- **Partial Leakage Remains:** Although current starvation helps reduce power, leakage currents in idle transistors can still cause unwanted dissipation.
- **Biasing Complexity:** Introducing multiple supply levels and mirrored biasing adds a layer of design and layout overhead.
- **Layout Area:** Because the circuit still requires additional transistors (control + mirrors), the total silicon footprint increases compared to a basic ring oscillator.
- **Temperature Sensitivity:** Current mirror behavior can drift slightly with temperature, which might affect the control voltages and frequency stability.

3.6 Proposed SAPON Design

This design approach is a continuation and enhancement of above described method, where in both negative skewing and current starvation techniques were integrated. In the SAPON-included design, an additional PMOS and NMOS transistor pair is incorporated—connected at the top and bottom of the ring structure, respectively to realize the SAPON (Stacked Adaptive Power Optimization Network) technique.

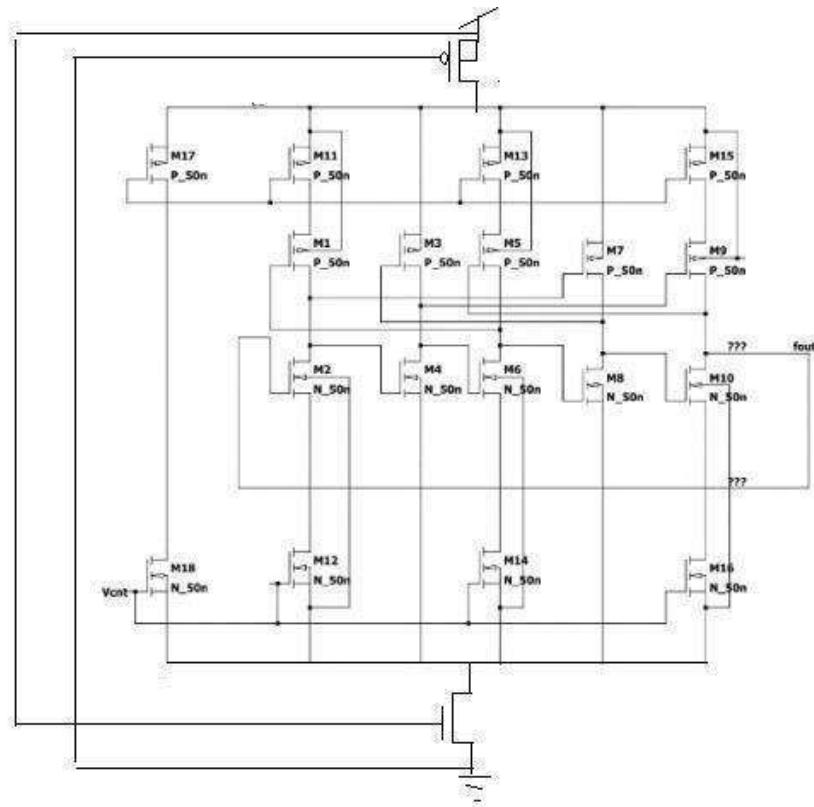


Fig. Proposed SAPON design

Circuit Description:

The base of this architecture is structurally similar to ROCSN. It comprises five CMOS inverter stages formed using transistors M1–M10, arranged in pairs: (M1, M2), (M3, M4), ..., (M9, M10). Each inverter has PMOS on top and NMOS on the bottom, forming the core logic of the oscillator.

- **Current Starvation** is employed by controlling three inverter stages (M1, M2), (M5, M6), and (M9, M10) with additional PMOS (M11, M13, M15) and NMOS (M12, M14, M16) transistors.
- **Current Mirror** technique is implemented using M17 and M18 for biasing and current regulation.
- **Negative Skewing** is achieved through the strategic interconnection of gate terminals among the CMOS stages.
- **SAPON Technique** is introduced by adding one PMOS transistor at the VDD side and one NMOS transistor at the GND side of the circuit. These transistors work as dynamic switches, regulating power flow in and out of the ring oscillator.

Working Principle:

The SAPON devices act as *power gates*:

- The PMOS at the top dynamically isolates or connects VDD to the ring structure based on the control signal.
- The NMOS at the bottom works similarly, controlling the connection to ground.

This mechanism limits unnecessary static power dissipation during transition states, especially when the oscillator is idle or in low-activity phases.

Advantages:

- **Reduced Power Consumption:** SAPON significantly cuts down static and leakage power by gating off power during non-switching intervals.
- **Enhanced Power Efficiency:** The adaptive power regulation ensures only the required amount of current flows into the oscillator, further conserving energy.
- **Better Temperature Stability:** The controlled power path helps mitigate temperature-related variations in delay and frequency.

Limitations:

- **Increased Design Complexity:** The addition of control logic and extra transistors increases design overhead and layout area.

- **Timing Overhead:** The delay introduced by the SAPON gating transistors must be carefully balanced to avoid degrading oscillator speed.

Summary:

The SAPON-included method offers a more **energy-efficient** alternative to conventional ring oscillator designs while preserving the advantages of current starvation and negative skewing. Its adaptability and power gating capability make it suitable for modern low-power, high-performance 5G CMOS applications.

3.7 Schematic Design in Cadence Virtuoso

The schematic design process is a fundamental step in analog and digital circuit development. In this project, Cadence Virtuoso was used to design two variations of a CMOS ring oscillator: the current-starved ROCSN design and the enhanced SAPON-included design. The goal was to create efficient, low-power oscillators suitable for 5G applications, using 45nm CMOS technology.

Step 1: Library and Cell Setup Before the circuit design, a new libraries named RO and sapon was created in the Library Manager. This library was linked to the 45nm technology file to ensure all design rules and device models were accessible. Within the library RO schematic cell named osc (for Method 2) and in library sapon cell sap are created

Step 2: Device Placement and Configuration Using the Schematic Editor, devices were inserted using the Add Instance tool (shortcut **i**). For the Method 2 design, 10 transistors (M1–M10) were used to construct five CMOS inverter stages. Three sets of current-starving transistors (M11–M12, M13–M14, and M15–M16) were added to limit current in selected stages, thereby improving power control. Biasing transistors M17 and M18 were added to act as current mirrors, helping stabilize the VIN signal.

Step 3: Power and Signal Connections All transistor terminals were carefully connected using the Wire tool (**w**). VDD and GND lines were routed to the appropriate supply terminals. Input and output signals were also connected and labeled, with particular attention to ensuring closed-loop feedback among the inverters to form a complete oscillator circuit.

Step 4: SAPON Enhancement For the SAPON design, two additional transistors were introduced: M19 (PMOS) and M20 (NMOS). These were placed above and below the main ring to serve as SAPON leakage control transistors. M19 was inserted between the main VDD and the ring's internal VDD, while M20 was placed between the ring's GND and actual ground. This configuration helped reduce standby leakage power.

Step 5: Node Labeling and Hierarchy Preparation All important nodes were labeled for clarity -VDC, OUT, VDD, and GND. This not only made the circuit easier to read but also helped in simulation. The schematic was checked for errors using the Check and Save tool. No floating nodes or unconnected pins were left unresolved.

Step 6: Simulation Readiness and Export The schematic was finalized, saved, and a symbol view was generated to allow hierarchical design and simulation. These symbols were then used to connect the schematic in a testbench for future simulation in ADE XL.

This schematic-level work ensures accurate, rule-compliant design logic for both ROCSN and SAPON-enhanced CMOS ring oscillators, forming a solid foundation for the layout phase.

The schematics generated are

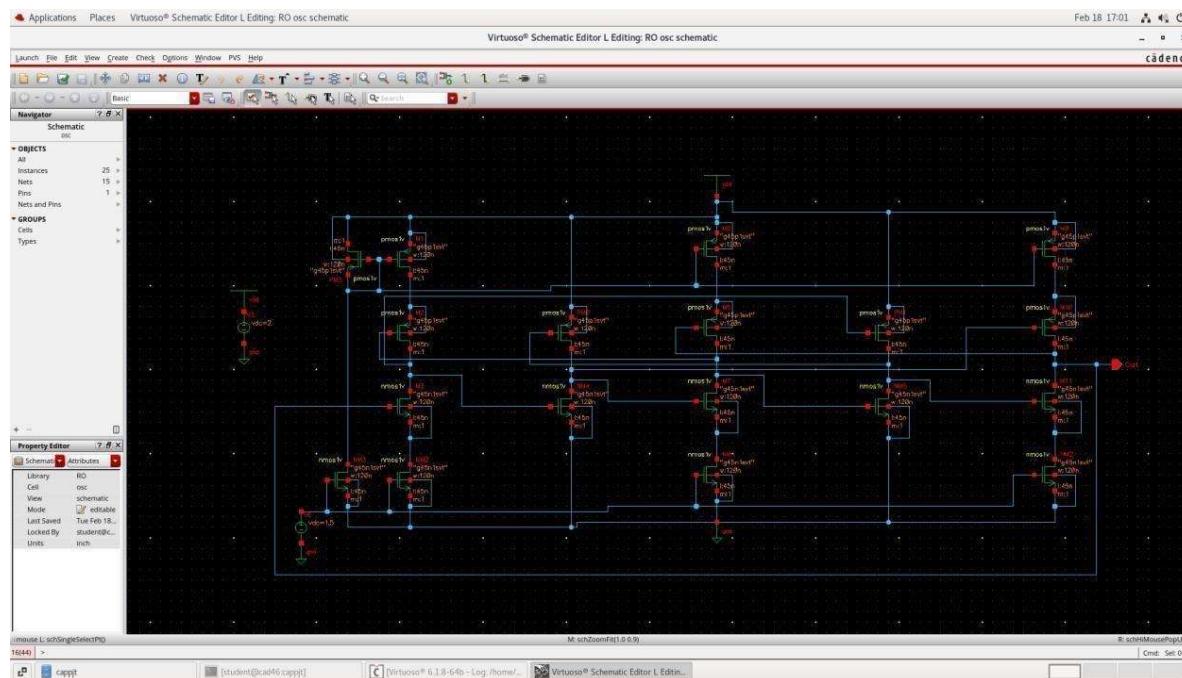


Fig. Circuit Schematic of ROCSN method

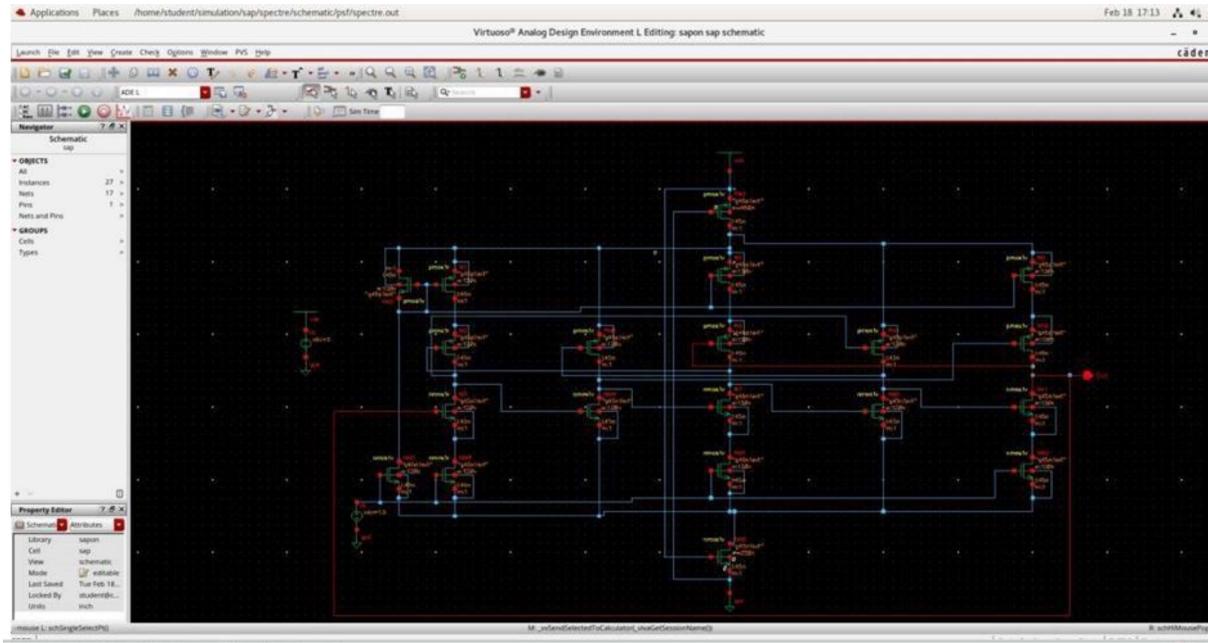


Fig. Proposed SAPON Design

3.8 Physical Layout Design in Cadence Virtuoso

The physical layout of the SAPON-enhanced CMOS ring oscillator was created using a schematic-to-layout (SDL) approach in Cadence Virtuoso Layout XL. This ensured alignment between the schematic netlist and the physical representation, which is crucial for LVS and fabrication readiness. The layout was performed using 45nm CMOS PDK.

Step 1: Layout Initialization and SDL Linking A layout cell named `sap` layout was created under the same library. Using Layout XL, the layout view was linked to the schematic with `Connectivity > Generate > All From Source`, importing all device instances directly from the schematic netlist. This allowed accurate mapping of pins and devices.

Step 2: Transistor Placement Strategy Transistors M1–M10 were placed in a row for balanced routing and minimal delay skew. Current-starved transistors (M11–M16) were positioned directly above or below their corresponding inverter stages for short routing paths. M17 and M18 were placed near the VIN node to form a biasing block. SAPON transistors (M19 and M20) were placed at the layout's top and bottom, aligning with the VDD and GND rails respectively.

Step 3: Routing Power, Signal, and Control Lines Power rails were defined using **Metal1** spanning horizontally across the top and bottom. **Metal1** and **Metal 2** was used for signal interconnects, and **Poly** was used for gate connections. Careful attention was paid to layer transitions, using vias where needed, especially in high-current regions.

Step 4: Substrate and Well Configuration Each PMOS transistor was placed within an **N-Well** region connected to VDD, and each NMOS was placed in a **P-Substrate** region tied to GND. Separate substrate contacts were added near each MOSFET to prevent latch-up and ensure proper isolation.

Step 5: Space Optimization and Error Correction The layout was compacted for efficiency while maintaining safe spacing between wells, metals, and active areas. Common errors such as overlap violations, spacing mismatches, and missing substrate contacts were identified and corrected manually. The SAPON devices were carefully integrated to preserve layout symmetry and ensure uniform current paths.

Step 6: Design Rule Check (DRC) Definition: DRC (Design Rule Check) verifies that the physical layout complies with the process design rules of the foundry.

- To run DRC, Assura or Calibre was used within Virtuoso.
- A rule file for the 45nm process was loaded.
- Errors such as minimum spacing violations, layer enclosures, and via misplacement were flagged.
- Each violation was cross-referenced and resolved.

Passing DRC ensured the layout was manufacturable and did not violate any physical constraints.

Step 7: Layout Versus Schematic (LVS) Definition: LVS (Layout Versus Schematic) checks the electrical equivalence of the schematic and layout netlists.

- LVS was run using Assura or Calibre.
- The schematic and layout netlists were generated and compared.
- Errors like missing devices, extra components, or mismatched connectivity were highlighted.
- These were resolved by renaming pins or adjusting layout nets.

Successful LVS ensured that the physical layout accurately represented the schematic design, both structurally and functionally. This step completed the verification process and prepared the design for parasitic extraction and simulation. The generated layout is given by

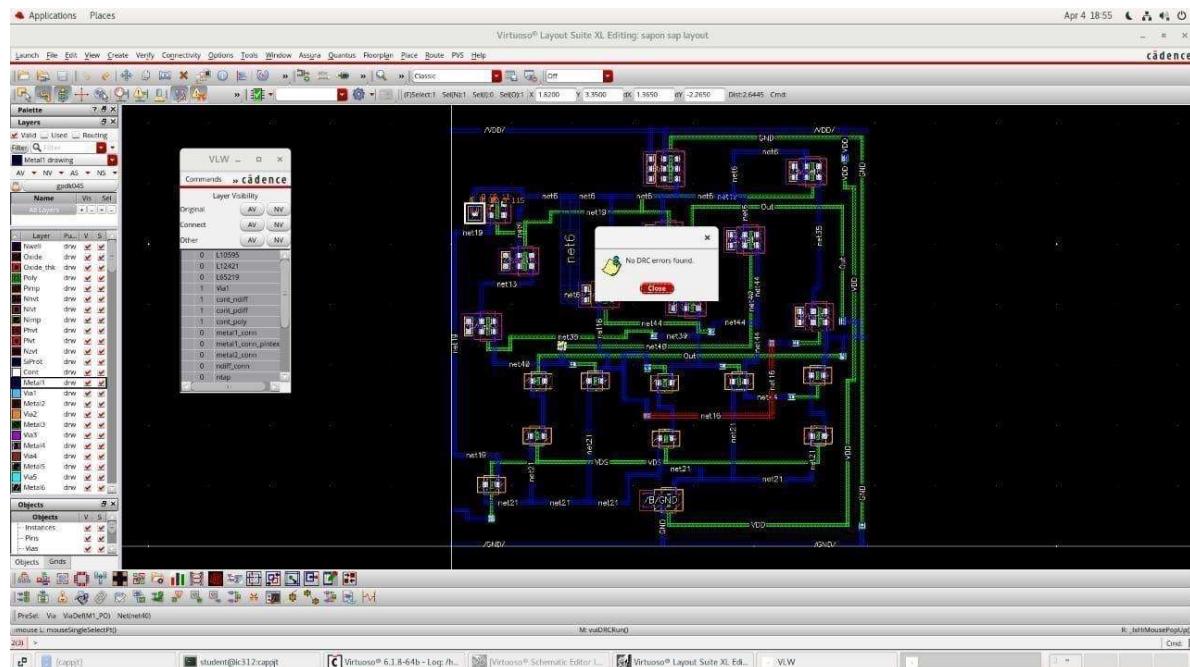


Fig. Layout of Proposed SAPON Design

Chapter 4

Results and Discussions

This section presents a comprehensive analysis of the simulation results obtained from the different CMOS ring oscillator designs Method ROCSN and the proposed SAPON- included method. All circuits were implemented using 45nm technology in the Cadence Virtuoso environment and tested under the same conditions to ensure a fair comparison.

The goal of this project was to reduce power consumption and maintaining the frequency range of the traditional ring oscillator for use in modern 5G applications.

The first method employed a basic current-starved approach, offering decent power control but falling short in speed. The second method enhanced performance through negative skewing and selective current starving, leading to improved frequency and noise behavior. The final design the SAPON-included method introduced an adaptive power optimization network using dynamic PMOS and NMOS switches, resulting in reduction of power usage while still be able to use on 5G networks.

4.1 Results and Comparison

In this section, we present a comparative analysis of the frequency and power consumption waveforms for both the Method ROCSN and the SAPON-included method. By examining the simulation outputs, we aim to highlight the performance improvements brought by the SAPON technique in terms of ability to operate in 5G (mm wave) and optimized power usage. The waveform comparisons provide visual confirmation of the enhancements achieved through the proposed modifications in the oscillator design.

4.1.1 Circuit Schematic ,Frequency and power waveforms – ROCSN

The schematic shown is for **Method ROCSN** of the CMOS Ring Oscillator, implemented in Cadence Virtuoso. It consists of **five stages of inverters**, each formed using PMOS and NMOS pairs. Additional transistors are placed in series with the inverters, acting as **current-starved elements** to control power consumption and oscillation frequency. A biasing circuit is used on the left side to manage current mirrors. The structure ensures stable oscillations with controlled delay across the loop.

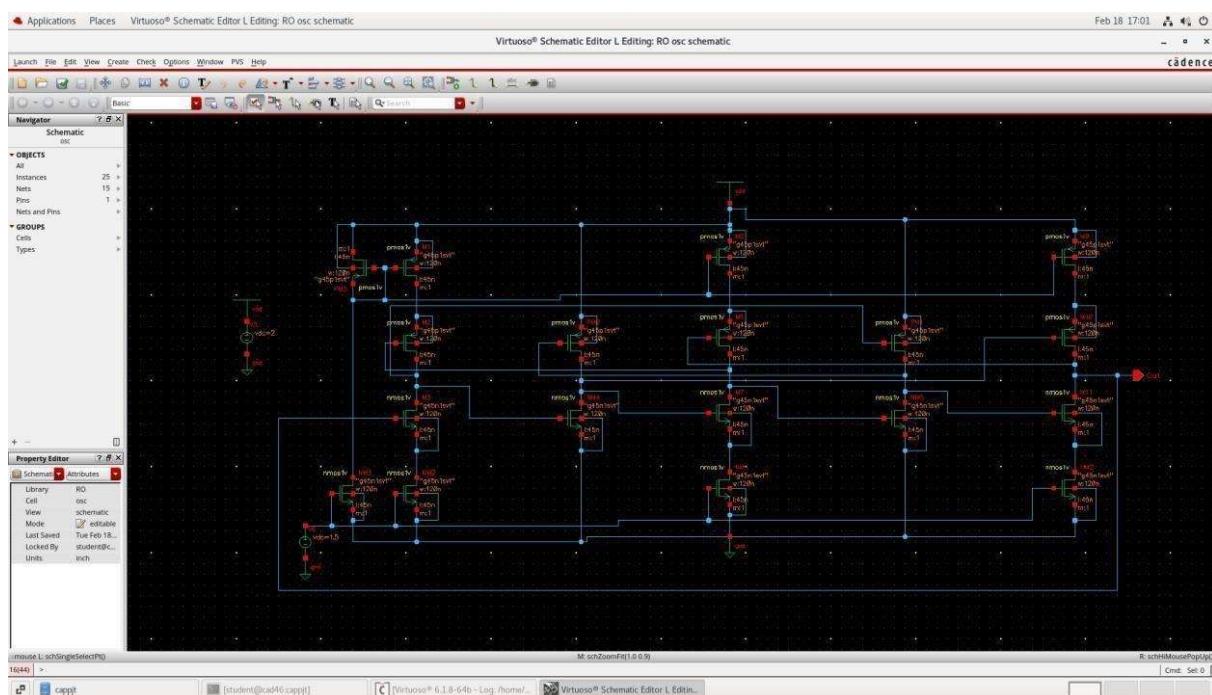


Fig. Circuit Schematic of ROCSN Design

The following waveforms represent the transient analysis performed on the Method ROCSN CMOS ring oscillator schematic in Cadence Virtuoso. The output frequency of oscillation was measured by analyzing the periodic nature of the output signal, while the average power consumption was calculated using the simulation waveform data and the built-in calculator tool in the waveform viewer. These results help in evaluating the efficiency and stability of the design. The frequency waveform confirms consistent oscillations across stages, and the power waveform illustrates the dynamic switching behavior under typical operating conditions.

Chapter 4. Proof of Implementation and Result comparison

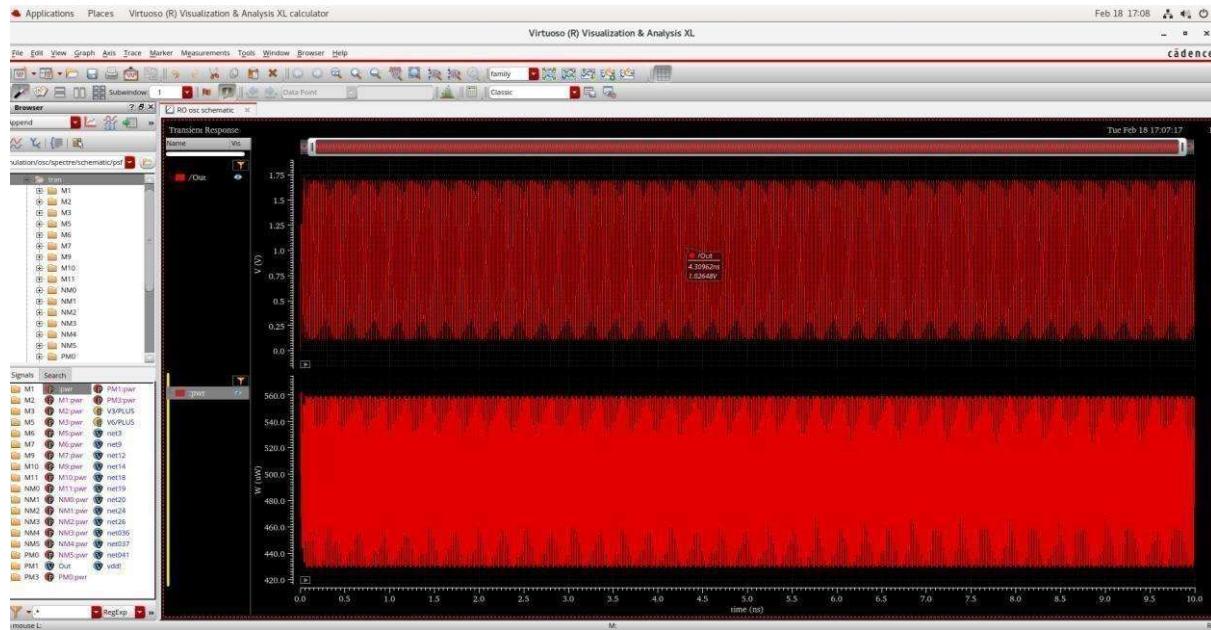


Fig. Simulated Waveforms of ROCSN design

frequency

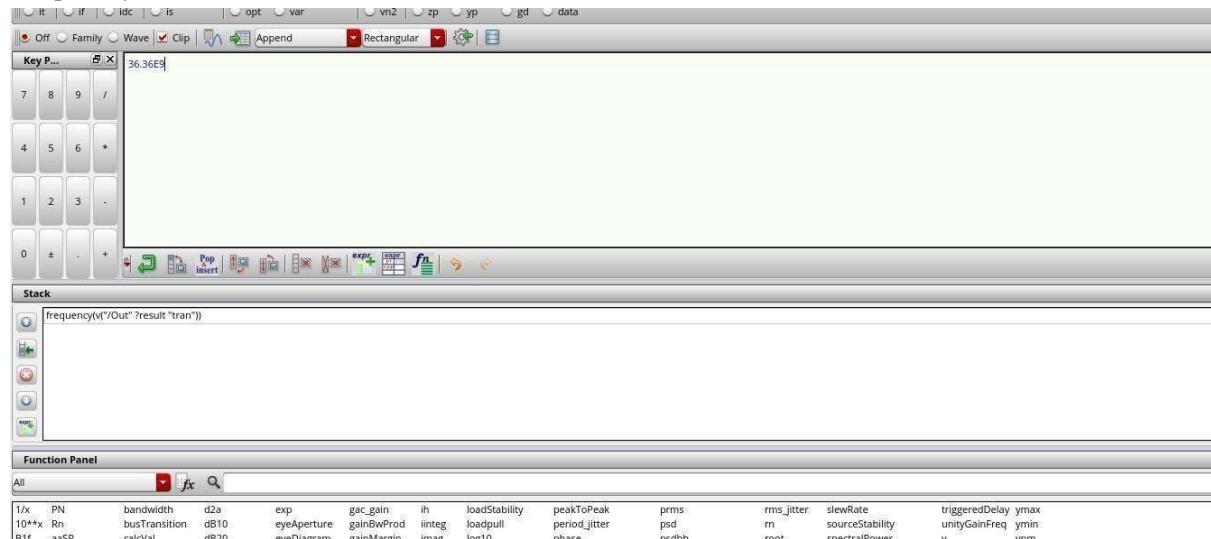


Fig. Frequency calculation of ROCSN design

Power

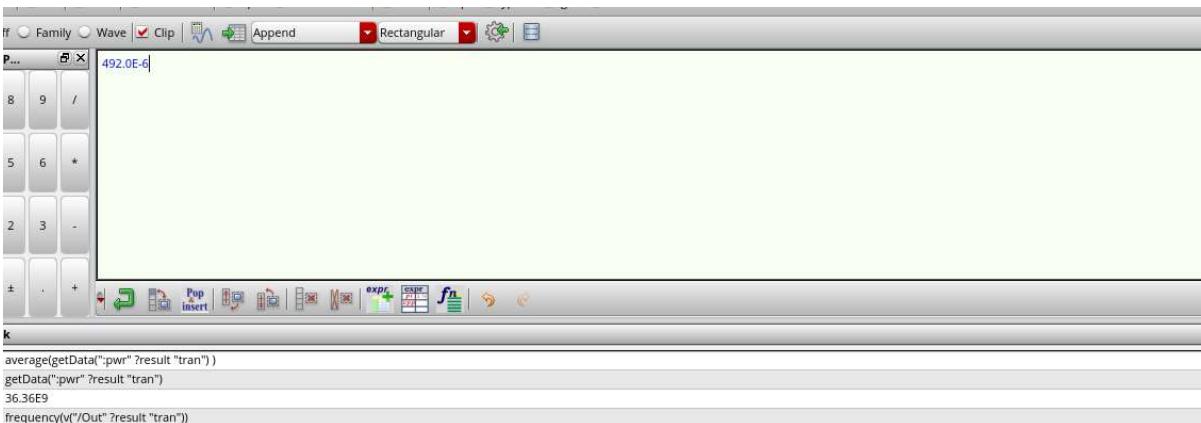


Fig. Power calculation of ROCSN design

4.1.2 Circuit Schematic ,Frequency and power waveforms – Proposed SAPON method

The schematic of the SAPON-based CMOS ring oscillator is an enhancement of Method ROCSN, incorporating two additional transistors—one PMOS and one NMOS placed between the VDD and GND rails. These transistors act as selective leakage controllers, dynamically regulating the supply rails and reducing power loss during idle states. The waveform captured during transient simulation demonstrates a stable and periodic output signal, verifying the effectiveness of the SAPON in maintaining oscillatory behavior while integrating leakage reduction techniques.

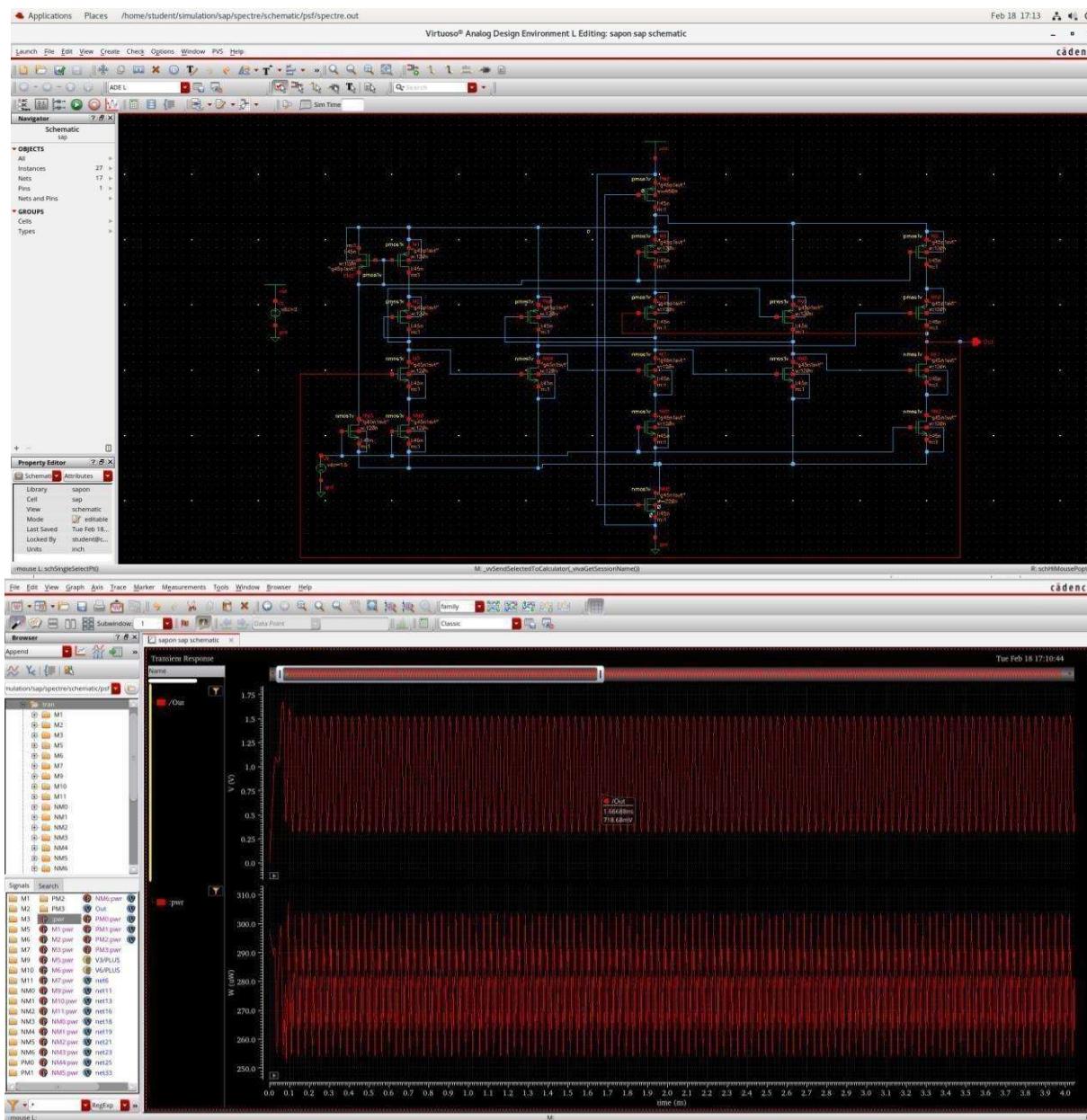
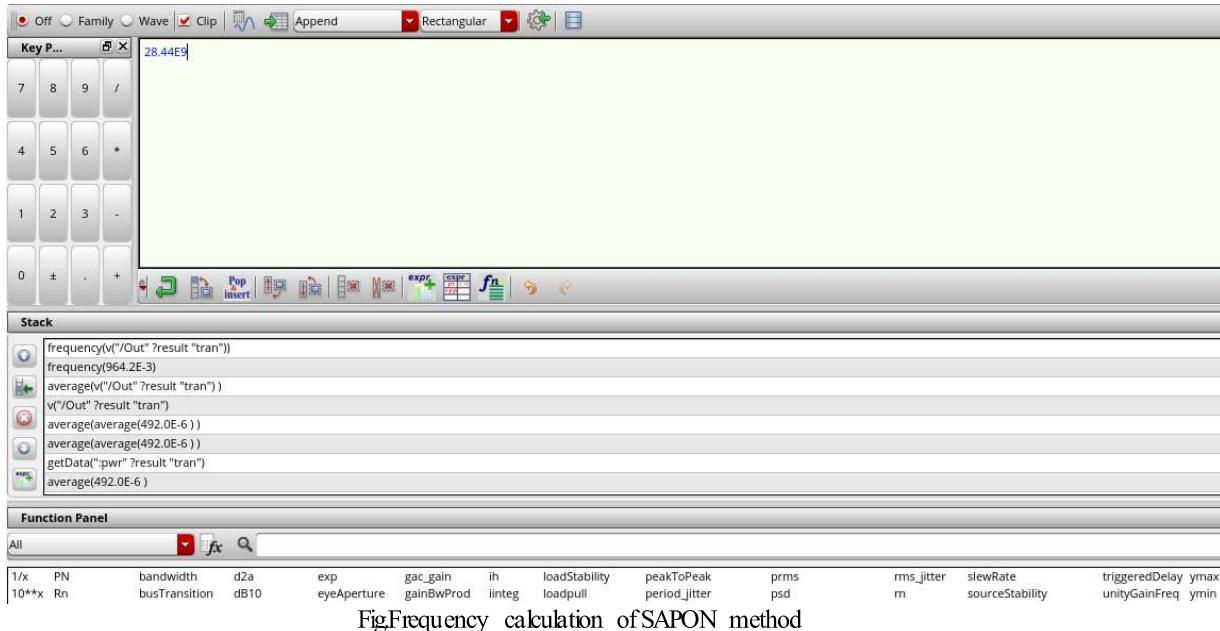


Fig. schematic and simulated waveform of proposed SAPON method

Chapter 4. Proof of Implementation and Result comparison

The following waveforms illustrate the power and frequency performance of the SAPON-based design, as extracted using Cadence's waveform viewer and calculator tool. The average power consumption is observed to be significantly reduced compared to Method 2, indicating the energy-efficient nature of the SAPON technique. Frequency measurements were taken based on the output signal's periodicity, showing that oscillation frequency is maintained while achieving better power control. These results affirm that the SAPON method effectively optimizes the trade-off between speed and power in CMOS ring oscillator circuits.

Frequency



Power

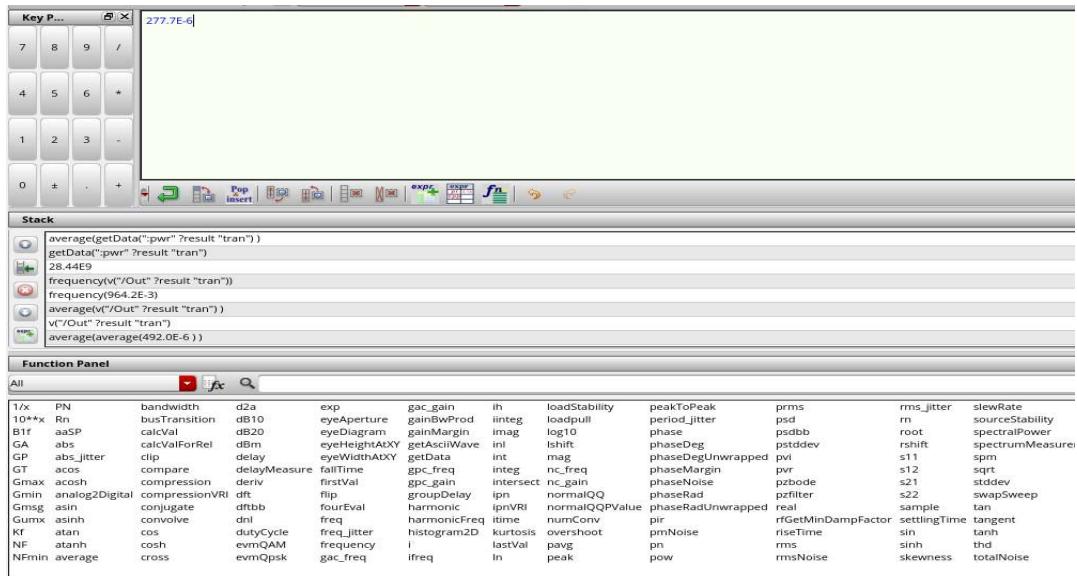


Fig. Power calculation of SAPON method

4.1.3 Physical layout design of proposed method and DRC and LVS validation

The physical layout of the SAPON-included CMOS ring oscillator was created in Cadence Virtuoso using a schematic-to-layout methodology. All PMOS and NMOS transistors were placed with appropriate N-well and P-substrate regions, ensuring electrical isolation and proper biasing. VDD and GND rails were routed using Metal2, while internal connections were established using Metall1 and poly for gate terminals. The SAPON transistors, added at the VDD and GND paths, were placed strategically to provide effective leakage control. After completing the layout, Design Rule Check (DRC) was performed using Assura to validate compliance with the 45nm CMOS process rules, and all checks were successfully passed. Layout Versus Schematic (LVS) verification was then carried out to confirm the electrical equivalence between the layout and schematic. A clean LVS match indicated accurate device placement, connectivity, and signal integrity, ensuring the SAPON layout was both functionally correct and physically manufacturable.

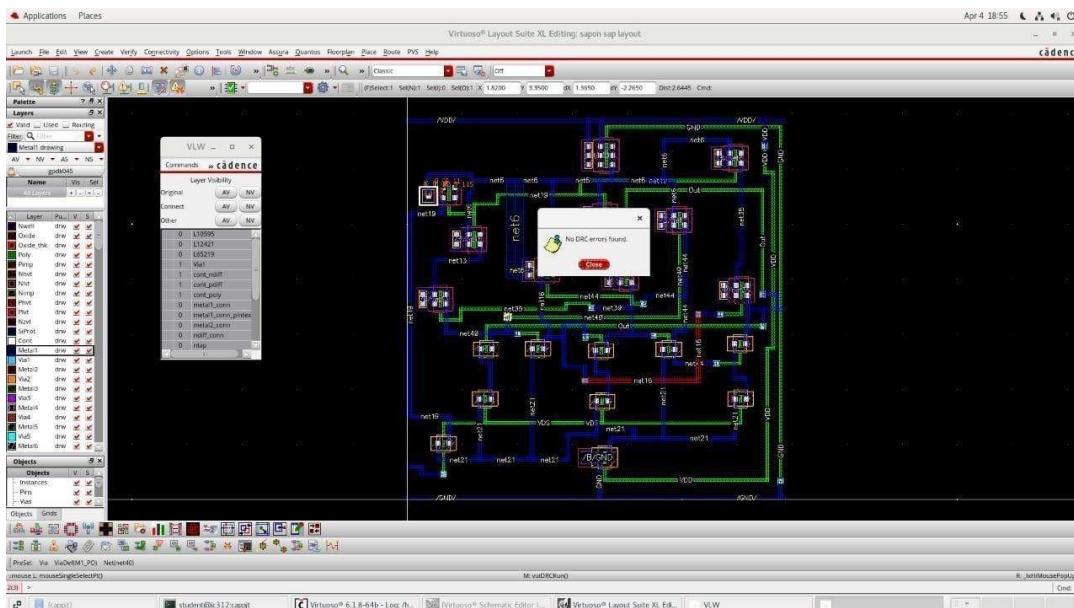


Fig. DRC and LVS verified layout of SAPON method

4.1.4 Comparison table

	Mos count	Power consumption(uw)	Frequency (GHz)
ROCSN method	18	492.0	36.36
Proposed SAPON method	20	277.7	28.44

Chapter 5

Conclusion and Future Scope

Conclusion

This project explored the enhancement of CMOS ring oscillators with a focus on achieving high-speed performance and low power consumption, aligned with the needs of 5G communication systems. By evolving from a basic current-starved architecture to a negatively skewed version and finally integrating the SAPON technique, each design demonstrated specific strengths in either frequency optimization or power efficiency. The simulations validated that these architectural modifications can significantly improve oscillator performance, while the successful layout implementation in advanced CMOS technology confirmed the practical viability and scalability of the designs. Together, these results highlight the effectiveness of combining timing control and adaptive power techniques in creating efficient, next-generation analog oscillators.

Future Scope

The next phase of this work involves fabricating the proposed designs and conducting real-time testing to validate their behavior under physical conditions, including temperature, noise, and process variations. Integrating these oscillators into complex RF systems such as PLLs or frequency synthesizers can further assess their application readiness. The SAPON mechanism offers room for improvement through the addition of dynamic feedback control, allowing real-time adaptation to power demands. Additionally, future studies could incorporate AI-based tuning algorithms to enhance performance adaptability, making these designs smarter and more efficient for diverse operational environments in modern wireless technologies.

Chapter 6

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