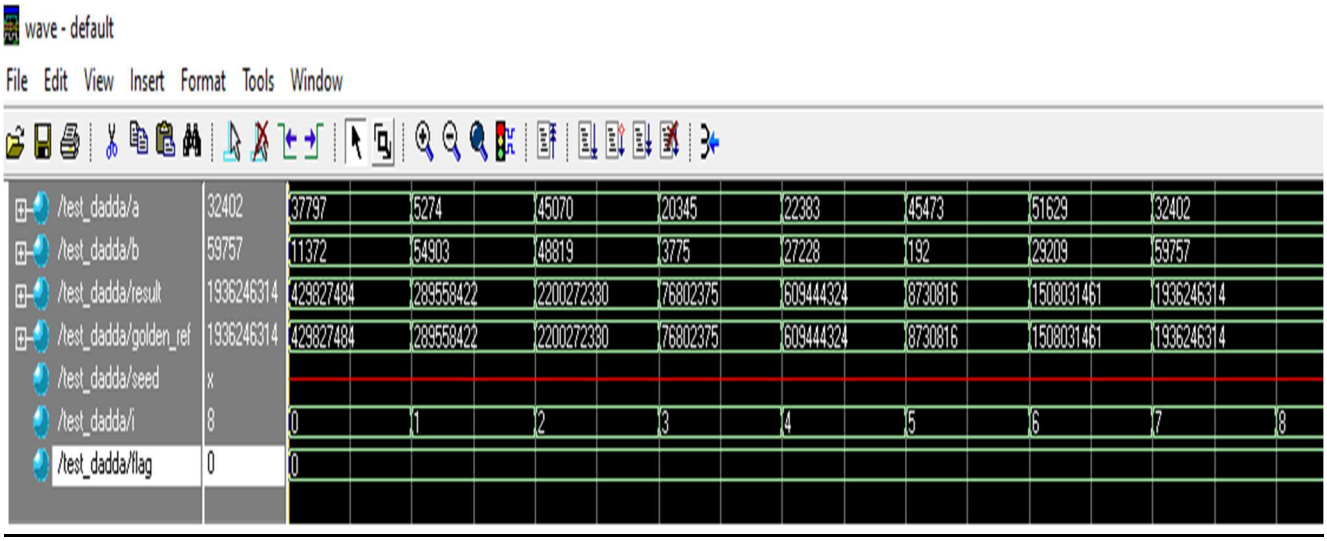
Design of 16-Bit Dadda Multiplier

Procedure:

- A 16 bit multiplier using Dadda architecture was designed using Verilog in ModelSim for unsigned multiplication
- Stages for addition of partial products were created to reduce total number partial products in any column to 2 or less
- Finally, using 32 bit brent Kung adder the final stage fast addition was carried out.

Output:

Waveform :



Terminal output which was printed(same as that in waveform):

```
run
# At time          0 , a is 37797 , b is 11372, result is  429827484
# At time         10 , a is  5274 , b is 54903, result is  289558422
# At time         20 , a is 45070 , b is 48819, result is 2200272330
# At time         30 , a is 20345 , b is  3775, result is   76802375
# At time         40 , a is 22383 , b is 27228, result is  609444324
# At time         50 , a is 45473 , b is   192, result is    8730816
# At time         60 , a is 51629 , b is 29209, result is 1508031461
# At time         70 , a is 32402 , b is 59757, result is 1936246314
# Success
```