Dr. Cherif Salama
Faculty of Media Engineering and Technology

CSEN 402 Computer Organization and System Programming
Practice Assignment 5
Spring 2014

NOT to be submitted
To be discussed during tutorial sessions

Exercise 1:

An instruction at address 021 in the basic computer has I=0, an operation code of the AND instruction and an address part equals to 083. The memory word at address 083 contains the operand B8F2 and the content of AC is A937. Go over the instruction cycle and determine the content of the following registers at the end of the execute phase: PC, AR, DR, AC and IR. Repeat the problem six more times staring with an operation code of another memory-reference instruction. (All numbers are in hexadecimal).

Solution:

Instruction	PC	AR	DR	AC	IR
Initial	021	-	-	A937	-
AND	022	083	B8F2	A832	0083
ADD	022	083	B8F2	6229	1083
LDA	022	083	B8F2	B8F2	2083
STA	022	083	-	A937	3083
BUN	083	083	-	A937	4083
BSA	084	084	-	A937	5083
ISZ	022	083	B8F3	A937	6083

Exercise 2:

Show the content in hexadecimal of registers PC, AR, DR, IR, and SC of the basic computer when an ISZ indirect instruction is fetched from memory and executed. The initial content of PC is 7FF. the content of memory at address 7FF is EA9f. The content of memory at address A9F is 0C35. The content of memory C35 is FFFF. Give the answer in a table with five columns, one for each register and a row for each timing signal. Show the contents of the registers after the positive transition of each clock pulse.

Solution:

Timing signals	PC	AR	DR	IR	SC
Initial	7FF	-	-	-	0
T_0	7FF	7FF	-	-	1
T_1	800	7FF	-	EA9F	2
T_2	800	A9F	-	EA9F	3
T_3	800	C35	-	EA9F	4
T_4	800	C35	FFFF	EA9F	5
T_5	800	C35	0000	EA9F	6
T_6	801	C35	0000	EA9F	0

Exercise 3:

Consider the *basic computer* with the following *hexadecimal* content of a few memory words with the given *hexadecimal* addresses:

Address	020	021	022	023	024	025
Content	7400	7100	7020	7004	4021	xxxx

If initially PC holds the hexadecimal value $(020)_H$, and AC holds the hexadecimal value $(FFFD)_H$, then by the time the instruction at memory address $(025)_H$ is fetched, what will be the value that is stored in E?

Solution:

The sequence of instructions is as follows:

address	Instruction	1st iteration	2nd iteration	3rd iteration
020	CLE	E=0		
021	CME	E=1	E=0	E=1
022	INC AC	AC=FFFE	AC=FFFF	AC=0000
023	SZA	PC=024	PC=024	PC=025
024	BUN, 021	PC=021	PC=021	
025	xxxx			Fetched

Then E will be equal to 1 by the time the instruction at address $(025)_H$ is fetched.

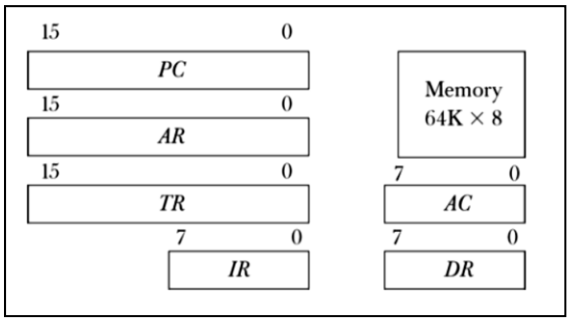
Exercise 4:

A computer uses a memory of 65,536 words with eight bits in each word. It has the following registers: PC, AR, TR (16 bits each), and AC, DR, IR (eight bits each). A memory-reference instruction consists of three words: an 8-bit operation code (one word) and a 16-bit address (in the next two words). All operands are eight bits. There is no indirect bit.

a. Draw a block diagram of the compter showing the memory and registers as in Fig. 5-3. (Do not draw the common bus).
b. Draw a diagram showing the placement in memory of a typical three-word instruction and the corresponding 8-bit operand.
c. List the sequence of microoperations for fetching a memory reference instruction and then placing the operand in DR. Start from timing signal T_0.

Solution:

a.



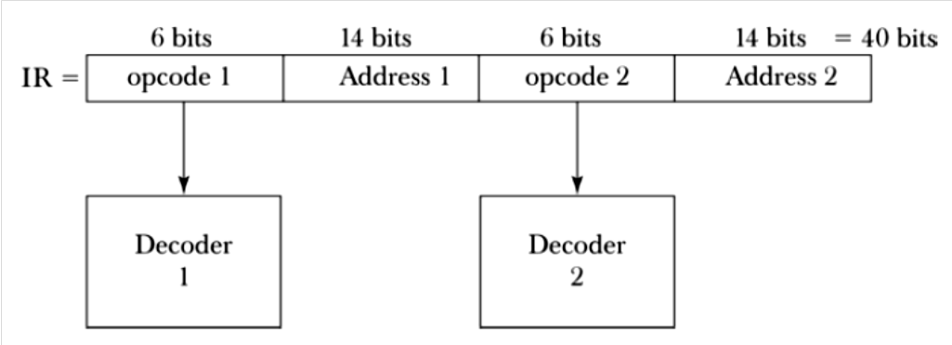
b.

c. T_0: AR ← PC
T_1: IR ← M[AR], PC ← PC+1
T_2: AR ← PC
T_3: TR(0-7) ← M[AR] , PC ← PC+1
T_4: AR ← PC
T_5: TR(8-15) ← M[AR] , PC ← PC+1
T_6: AR ← TR
T_7: DR ← M[AR]

Exercise 5:

A digital computer has a memory unit with a capacity of 16,384 words, 40 bits per word. The instruction code format consists of six bits for the operation part and 14 bits for the address part (no indirect mode bit). Two instructions are packed in one memory word, and a 40-bit instruction register `IR` is available in the control unit. Formulate a procedure for fetching and executing instructions for this computer.

Solution:



1. Read 40-bit double instruction from memory to IR and then increment PC
2. Decode opcode1
3. Execute instruction1 using address1
4. Decode opcode2
5. Execute instruction2 using address2
6. Go back to step1