

Digital Integrated Circuit Lab Report

Experiment 3

Submitted by
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1 Design of Static CMOS Inverter

A static CMOS inverter with a minimum width and length was designed in Cadence, as shown in Figure 1. The technology node used is 90nm (GDK90). The length of PMOS and NMOS was 100nm.

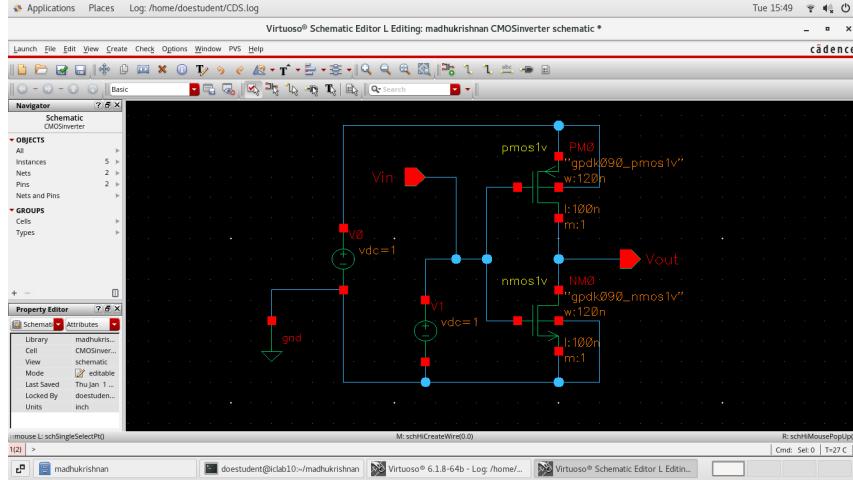


Figure 1: Static CMOS Inverter Schematic

1.1 DC Analysis

A V_{dc} of 1V was given as V_{dd} of the circuit, and the DC analysis was carried out in the circuit with V_{dc} of 1V as the input voltage, V_{in} . The Voltage Transfer Chara is described in Figure 2

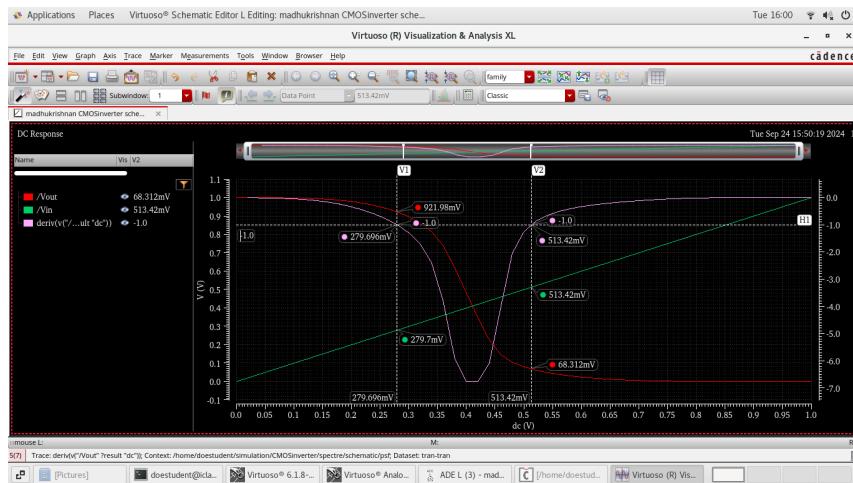


Figure 2: Static CMOS inverter voltage transfer chara

The voltage transfer chara contains an input vs. output voltage graph. The derivative of voltage transfer chara output was found using the calculator tool, and the same was used to find the low voltage output V_{OL} , the high voltage output V_{OH} , the low voltage input V_{IL} , and the high voltage input V_{IH} . These points correspond to the points in the input vs. output graph with a slope of -1 . The noise margins

of the circuit were mathematically found by substituting the values obtained from the graph in the Equations 1, 2, and 3. The results are tabulated in Table 1.

$$\text{Noise margin high, } NM_H = V_{OH} - V_{IH} \quad (1)$$

$$\text{Noise margin low, } NM_L = V_{IL} - V_{OL} \quad (2)$$

$$\text{Noise margin, } NM = NM_H - NM_L \quad (3)$$

Noise margin	Result
Voltage output high V_{OH}	921.980 mV
Voltage output low V_{OL}	68.312 mV
Voltage input high V_{IH}	513.420 mV
Voltage input low V_{IL}	279.696 mV
Noise margin high NM_H	408.560 mV
Noise margin low NM_L	211.384 mV
Noise margin NM	197.176 mV

Table 1: Noise margin

The switching threshold V_m is the voltage at which the input voltage, V_{in} , equals the output voltage V_{out} . The same is found in the DC analysis graph, as described in Figure 3.



Figure 3: Static CMOS inverter switching threshold

$$V_m = 410.684 \text{ mV}.$$

2 Transient analysis

An input pulse voltage of 1V with a period of $2nS$ and rise time and fall time of 1 percent was applied, and transient analysis was performed in the minimum size CMOS inverter designed. The transient response is described in Figure 4.

Various timing parameters such as high to low propagation delay, T_{PLH} and low to high propagation delay, T_{PHL} were calculated using the calculator tool in cadence virtuoso.

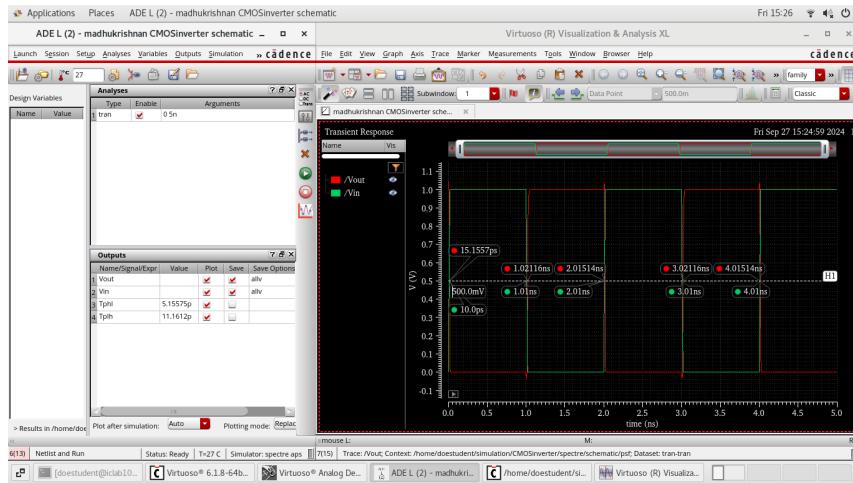


Figure 4: CMOS inverter transient analysis

$$T_{PLH} = 11.1612 \text{ ps.}$$

$$T_{PHL} = 5.15575 \text{ ps.}$$

3 Variation in transient response with change in width

3.1 Transient analysis results

The width of the PMOS doubled the previous width, as shown in Figure 5, and the transient response was carried out in the circuit. The result is shown in Figure 6. Then, the width of the PMOS was set to the minimum width, and the width of the NMOS was doubled, as shown in Figure 7. The transient analysis was performed, and the timing parameters were extracted using the calculator tool, as shown in Figure 8. The results are tabulated in Table 2. We assume that the resistance is inversely proportional to the width and the capacitance is directly proportional to the width of the MOSFET.

PMOS width	NMOS width	T_{PLH}	T_{PHL}
120 nm	120 nm	11.1612 ps	5.15575 ps
120 nm	240 nm	13.0794 ps	3.21396 ps
240 nm	120 nm	8.18305 ps	6.7509 ps

Table 2: Variation in transient response with change in width

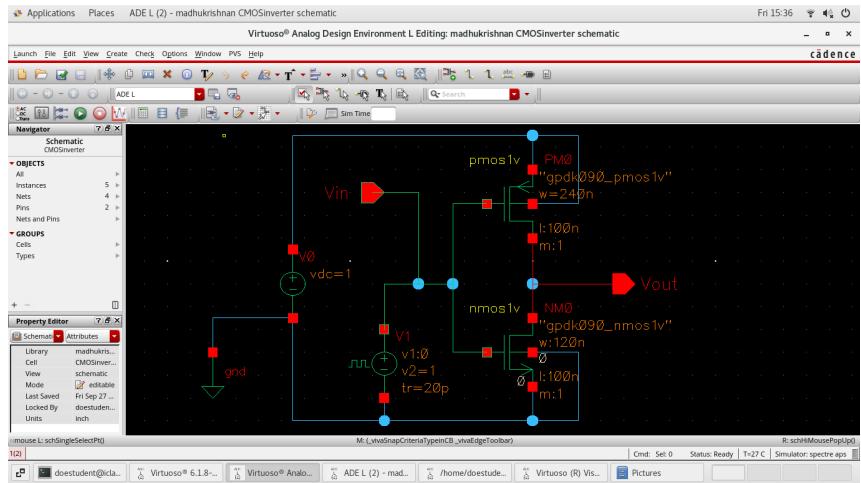


Figure 5: CMOS inverter width PMOS width doubled

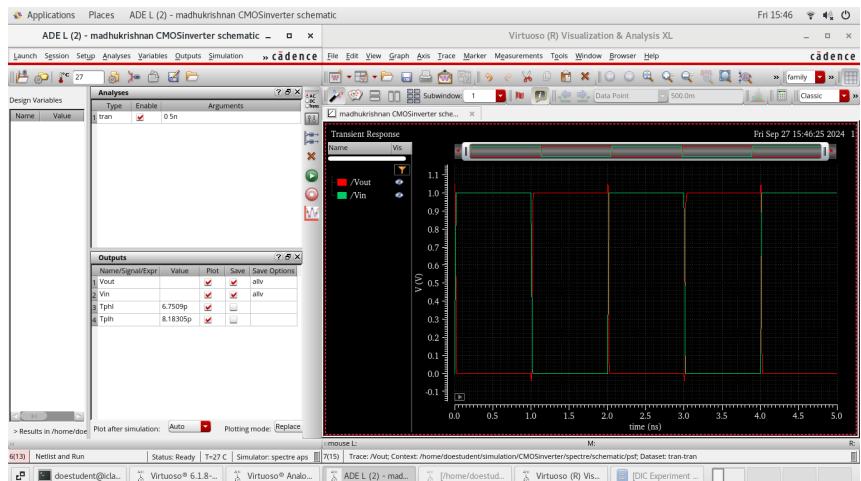


Figure 6: CMOS inverter width PMOS width doubled: Transient analysis

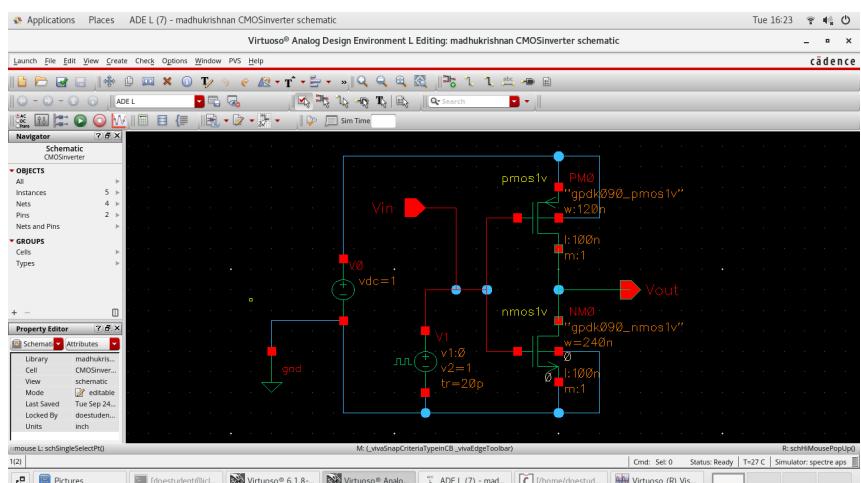


Figure 7: CMOS inverter width NMOS width doubled

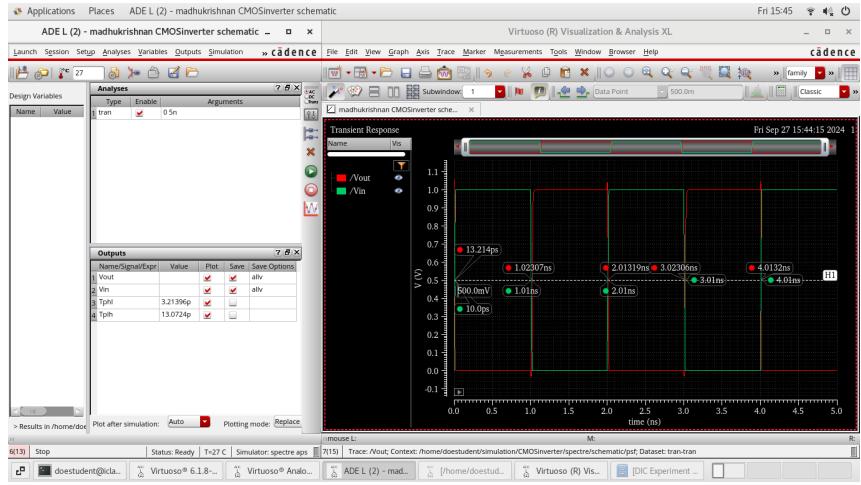


Figure 8: CMOS inverter width NMOS width doubled: Transient analysis

3.2 Propagation delay equations

The formulas for calculating various propagation delays are as follows.

Minimum size PMOS and NMOS

$$\text{High to low propagation delay, } T_{PHL} = 0.69 R_n (C_{dp} + C_{dn})$$

$$\text{Low to high propagation delay, } T_{PLH} = 0.69 R_p (C_{dp} + C_{dn}).$$

Minimum size PMOS and doubled-width NMOS

$$\text{High to low propagation delay, } T_{PHL} = 0.69 \frac{R_n}{2} (C_{dp} + 2 C_{dn})$$

$$\text{Low to high propagation delay, } T_{PLH} = 0.69 R_p (C_{dp} + 2 C_{dn}).$$

Minimum size NMOS and doubled-width PMOS

$$\text{High to low propagation delay, } T_{PHL} = 0.69 R_n (2 C_{dp} + C_{dn})$$

$$\text{Low to high propagation delay, } T_{PLH} = 0.69 \frac{R_p}{2} (2 C_{dp} + C_{dn}).$$

R_p = Resistance of PMOS.

R_n = Resistance of NMOS.

C_{dp} = Drain capacitance of PMOS.

C_{dn} = Drain capacitance of NMOS.

4 Inverter with 10 f F load capacitance

The minimum-sized inverter was loaded with a 10 f F capacitor, as described in Figure 9. The delay parameters were extracted using the calculator tool from the result shown in Figure 10

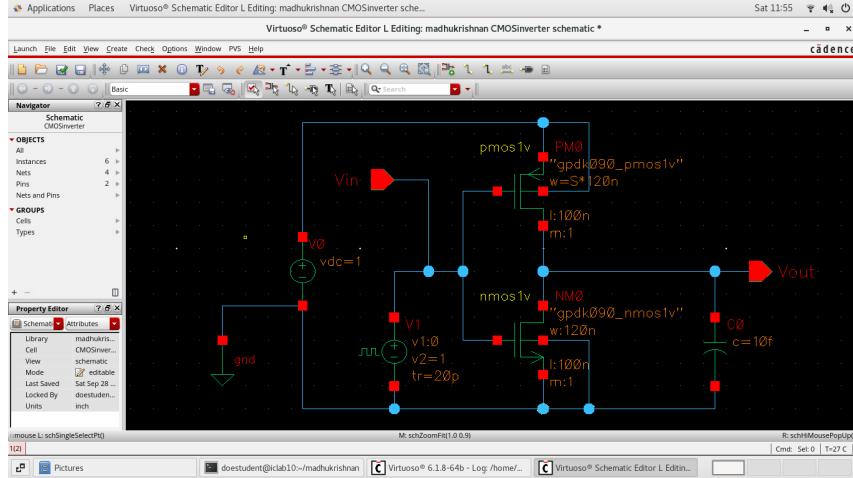


Figure 9: Inverter with 10 f F load capacitor

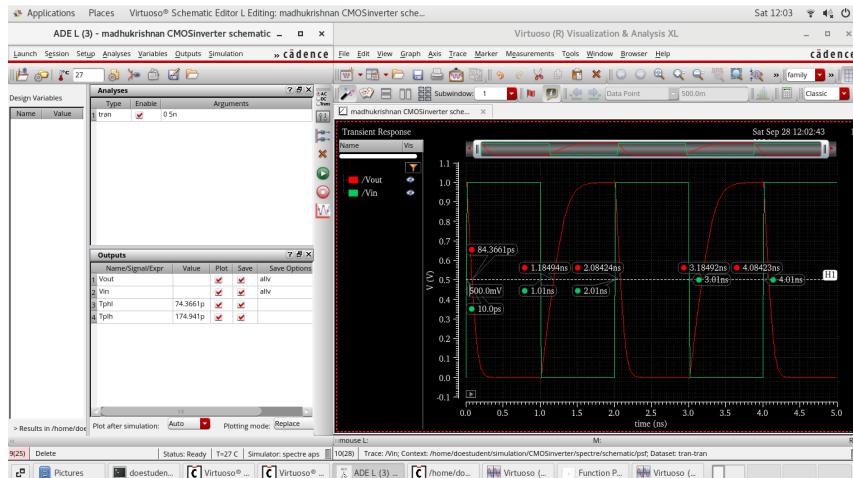


Figure 10: Transient response of inverter with 10 f F load capacitor

4.1 Transient response results

High to low propagation delay, $T_{PHL} = 74.3661 \text{ ps}$

Low to high propagation delay, $T_{PLH} = 174.941 \text{ ps}$.

4.2 MOS Parameters

The transient response results of loaded and unloaded inverters were used to find the drain capacitance and resistances of minimum-sized PMOS and NMOS transistors.

$$PMOS\ Resistance, R_p = 21714.05806 \Omega.$$

$$NMOS\ Resistance, R_n = 10030.48551 \Omega.$$

$$Drain\ capacitance, C_d = 7.4494 \times 10^{-16} F$$

5 Inverter with 20 f F load capacitance

The load capacitor was changed to 20 f F, as shown in Figure 11, and the delay parameters were analysed mathematically and through the simulation described in Figure 12. The same was compared.

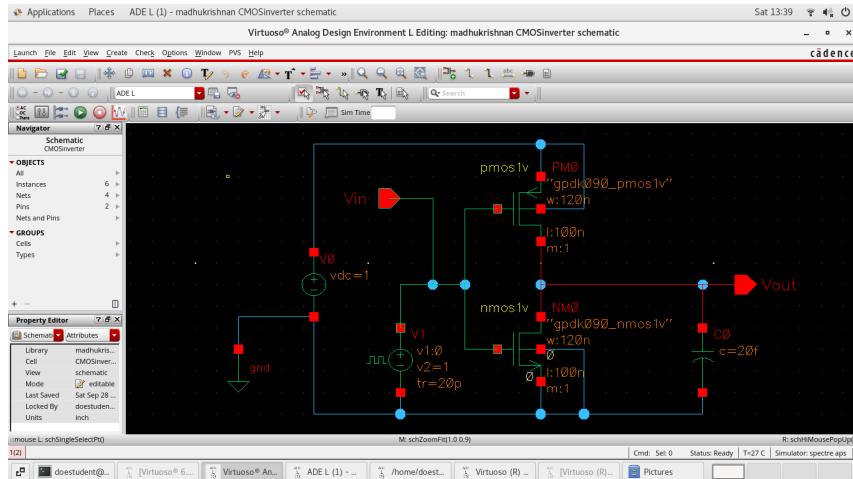


Figure 11: Inverter with 20 f F load capacitor

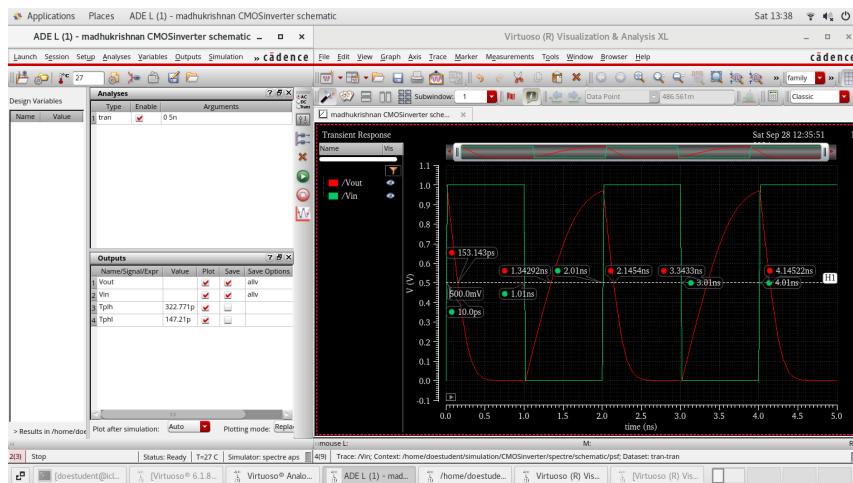


Figure 12: Transient response of inverter with 20 f F load capacitor

Theoretical result

High to low propagation delay, $T_{PHL} = 143.576 \text{ ps}$

Low to high propagation delay, $T_{PLH} = 310.821 \text{ ps.}$

Simulation result

High to low propagation delay, $T_{PHL} = 147.21 \text{ ps}$

Low to high propagation delay, $T_{PLH} = 322.771 \text{ ps.}$

The simulation and theoretical results were compared and found to be approximately equal. The differences are due to our approximations in delay and wire capacitance calculations.

6 PMOS width parameterised

The width of PMOS is parameterised as a multiple of minimum size, as shown in Figure 13. The input and output are short to find the variation of the switching threshold with a change in the width of PMOS. The transient response is shown in Figure 14

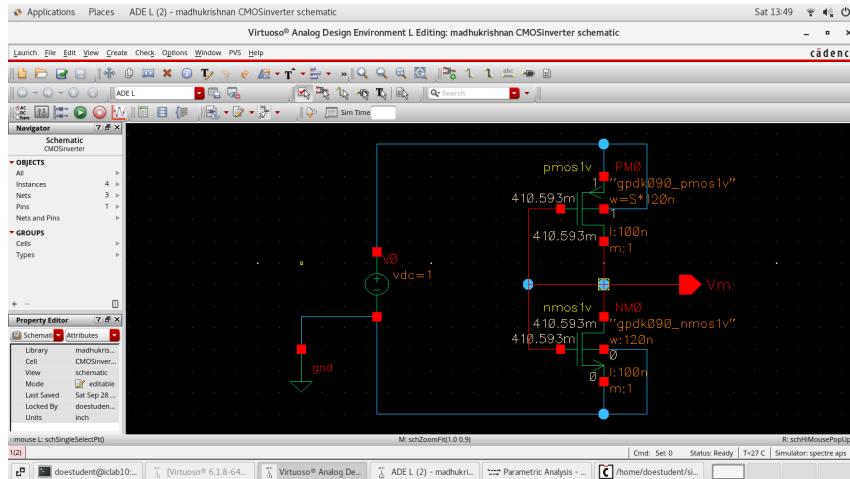


Figure 13: PMOS width parameterised circuit

Sizing factor from simulation, $S = 3.46534$

Sizing factor from calculation, $S = 2.16480$

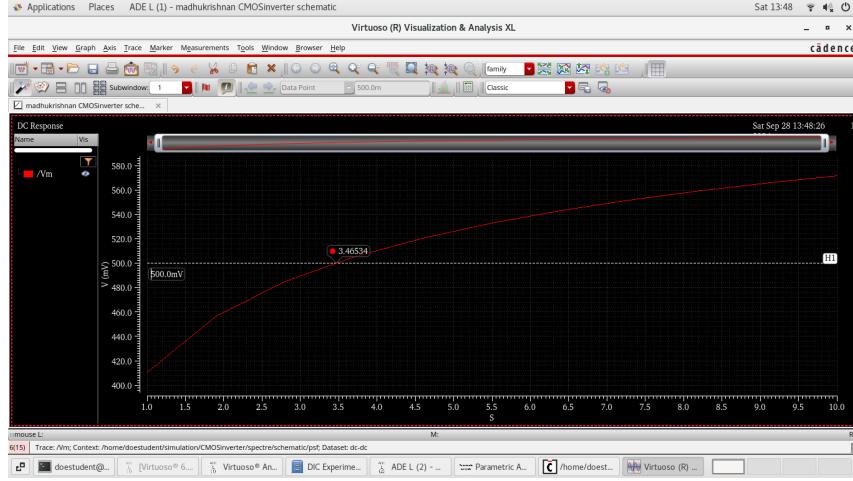


Figure 14: V_m vs. PMOS Width analysis

7 Estimation of transient response of unit-sized inverter

The PMOS width was changed using the resistance ratio we got from subsection 4.2. The new PMOS width is 260 nm . The inverter is connected to a load capacitance of $25fF$, as shown in Figure 15. Transient analysis was performed in the circuit, and the results shown in Figure 16 and Figure 17 were obtained. The results are compared with the theoretical results calculated using the resistance and capacitance values calculated from section 4.

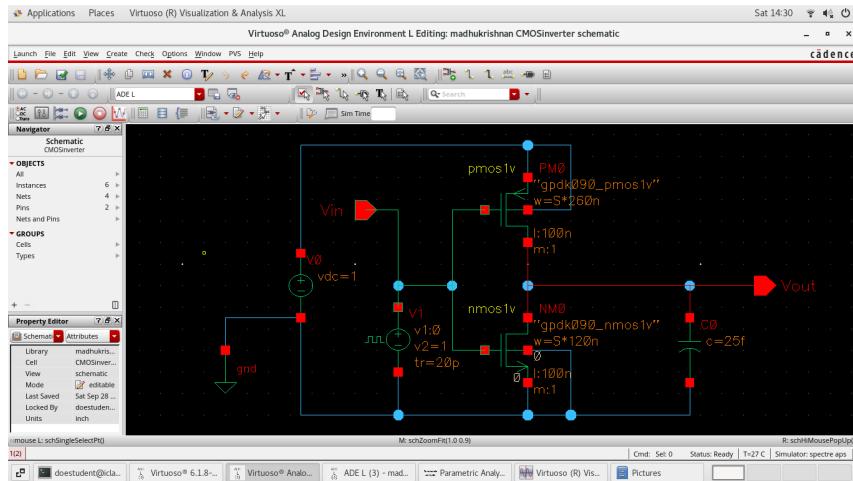


Figure 15: Unit-sized inverter with width parameterised

The delay parameters were used to calculate the drain capacitance of PMOS and NMOS of the unit-sized inverter.

$$\text{Drain capacitance of PMOS, } C_{dp} = 7.5413 \times 10^{-16} \text{ F}$$

$$\text{Drain capacitance of NMOS, } C_{dn} = 3.96877 \times 10^{-16} \text{ F}$$

$$\text{Total drain capacitance of unit-sized inverter, } C_g = 1.1510 \times 10^{-15} \text{ F}$$

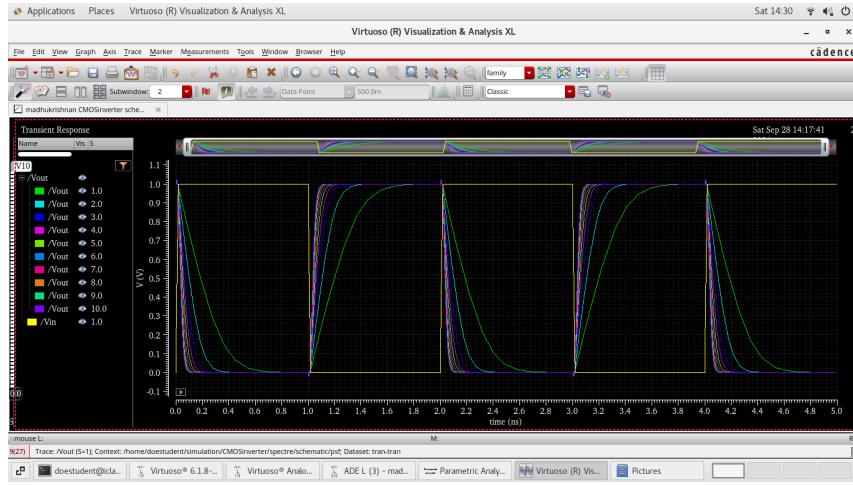


Figure 16: Unit-sized inverter with width parameterised: Transient analysis

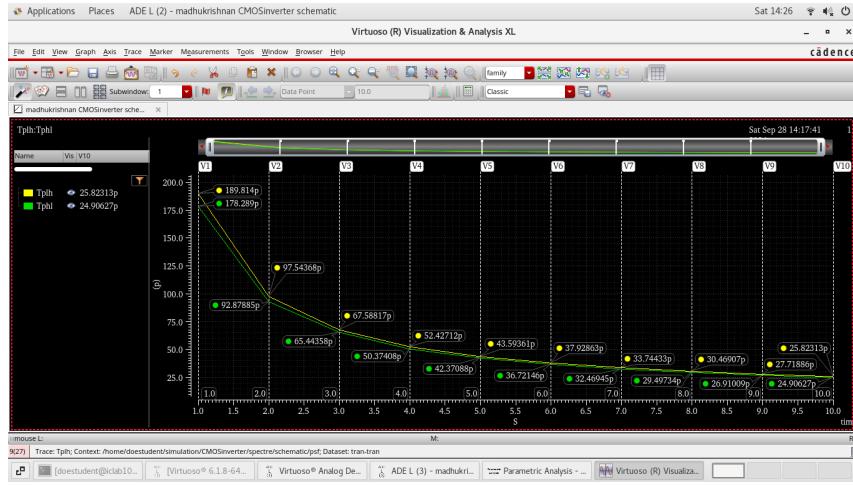


Figure 17: Unit-sized inverter with width parameterised: Delay vs. S graph

Sizing factor S	Simulation results		Theoretical results	
	T_{PHL}	T_{PLH}	T_{PHL}	T_{PLH}
1	178.289 ps	189.814 ps	180.992 ps	180.8366 ps
2	92.87885 ps	97.54368 ps	94.4791 ps	94.9800 ps
3	65.44358 ps	67.58817 ps	65.4147 ps	65.5851 ps
4	50.37408 ps	52.42712 ps	51.2226 ps	51.7867 ps
5	42.37088 ps	43.59361 ps	42.5714 ps	42.5348 ps
6	36.72146 ps	37.92863 ps	36.8038 ps	36.7722 ps
7	32.46945 ps	33.74433 ps	32.6842 ps	32.6561 ps
8	29.49734 ps	30.46907 ps	29.5944 ps	29.5690 ps
9	26.91009 ps	27.71886 ps	27.1913 ps	27.1679 ps
10	24.90627 ps	25.82313 ps	25.2688 ps	25.2471 ps

Table 3: Variation of delay with sizing factor

8 Unit-sized inverter cascaded with an identical inverter

A unit-sized inverter is cascaded with another identical inverter, as shown in Figure 18. The width of PMOS and NMOS of the second inverter was increased by a factor of 1 to 5, separately and together using parametric analysis, and the results shown in Figure 19, Figure 20, and Figure 21 were obtained.

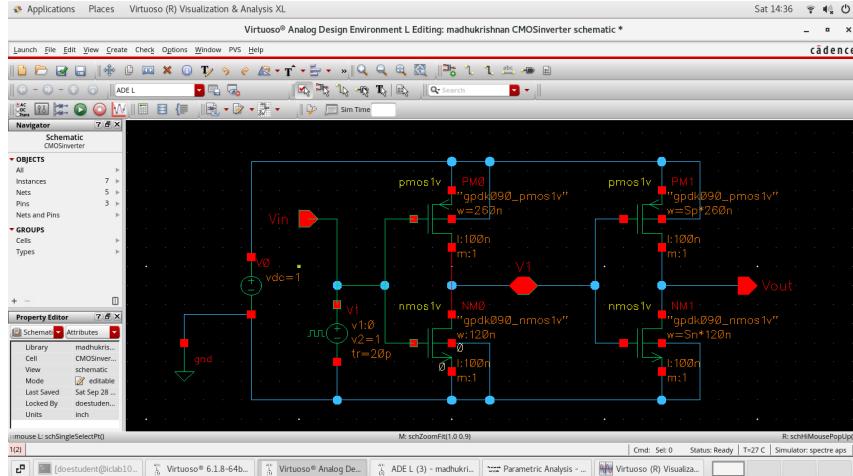


Figure 18: Unit-sized inverter cascaded with identical inverter



Figure 19: PMOS and NMOS of the second inverter sized

The transient analysis results were used to calculate the gate capacitance of the unit-sized inverter's PMOS and NMOS.

$$\text{Gate capacitance of PMOS, } C_{gp} = 4.62532 \times 10^{-16} \text{ F}$$

$$\text{Gate capacitance of NMOS, } C_{gn} = 2.399352 \times 10^{-16} \text{ F}$$

$$\text{Total gate capacitance of unit-sized inverter, } C_g = 7.024672 \times 10^{-16} \text{ F}$$

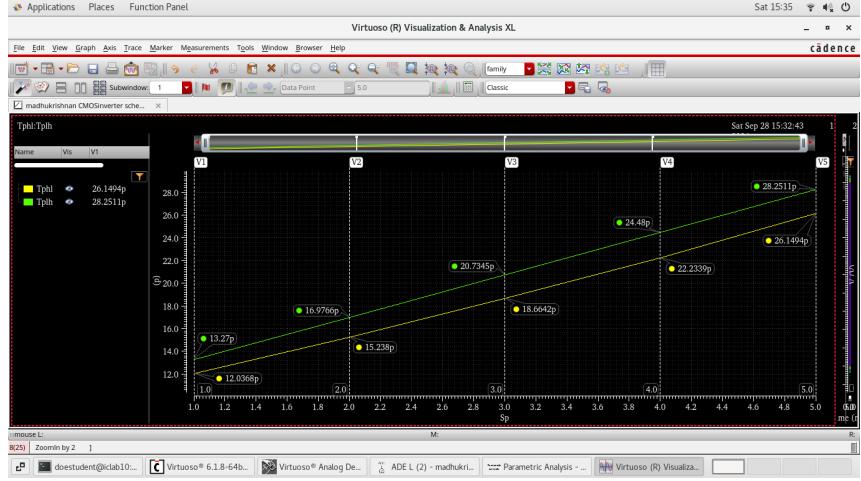


Figure 20: PMOS of the second inverter sized

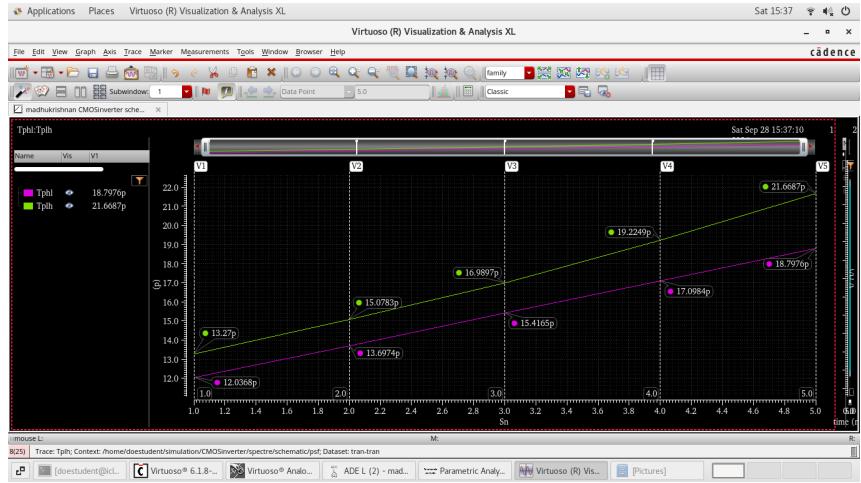


Figure 21: NMOS of the second inverter sized

9 Design of inverter chain

An inverter chain was designed to drive a load capacitance of 150 fF . The calculation results are as follows.

$$\text{Fan out, } F = \frac{C_L}{C_{g1}} = 213.5331$$

$$\text{Ideal number of inverters, } N = \frac{\log F}{\log f} = 4.083$$

Since branch effort (B) and logical effort (G) are unity, Path effort (H) = F.

$$\text{Fan out of gate, } f = F^{\frac{1}{N}}$$

We then use the same equations to design inverter chains with inverters one more and less than the ideal number of inverters. The sizes thus calculated are tabulated in Table 4

Inverter -	$N = 3$		$N = 4$		$N = 5$	
	PMOS	NMOS	PMOS	NMOS	PMOS	NMOS
Inverter 1	260	120	260	120	260	120
Inverter 2	1555	720	995	460	760	350
Inverter 3	9290	4290	3800	1755	2220	1025
Inverter 4			14525	6495	2300	120
Inverter 5					18990	6765

Table 4: Inverter chain size (in nm)

9.1 Inverter chain of 4 inverters

An inverter chain of 4 inverters was designed and simulated in Cadence, as shown in Figure 22. The delay was estimated using the calculator tool. The results are shown in Figure 23

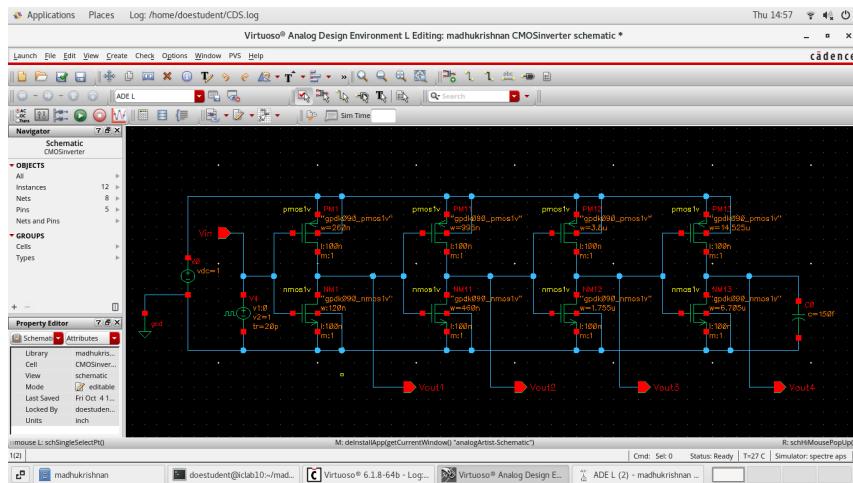


Figure 22: Inverter chain of 4 inverters

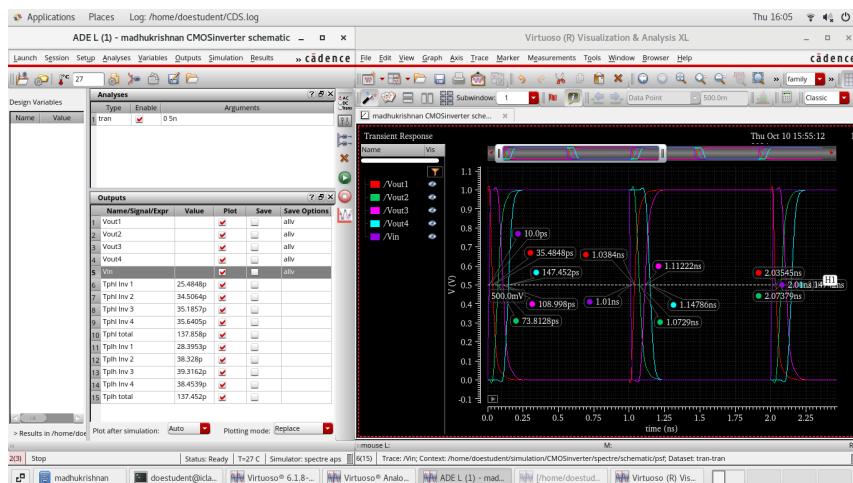


Figure 23: Inverter chain of 4 inverters: results

9.2 Inverter chain of 5 inverters

The number of inverters increased by one from the ideal number. The size parameters shown in Table 4 were used to construct the inverter chain in Figure 24. The simulation results are shown in Figure 25.

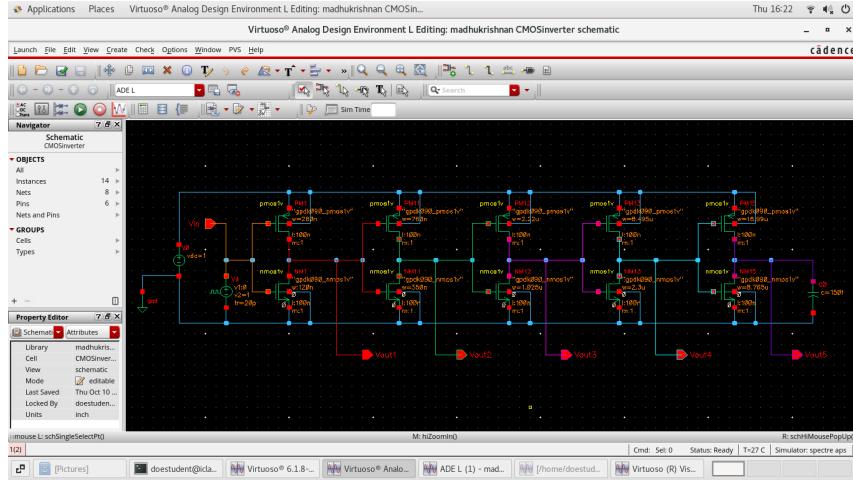


Figure 24: Inverter chain of 5 inverters

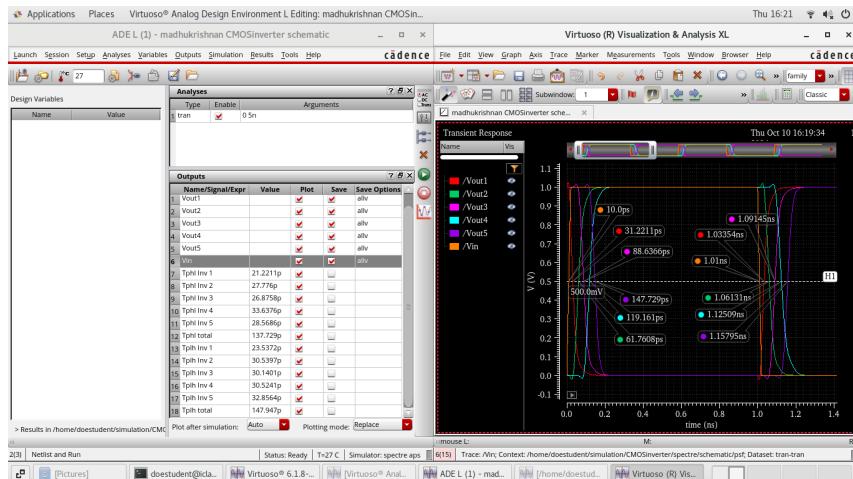


Figure 25: Inverter chain of 5 inverters: results

9.3 Inverter chain of 3 inverters

The number of inverters was reduced by one from the ideal number. The size parameters shown in Table 4 were used to construct the inverter chain in Figure 26. The simulation results are shown in Figure 27.

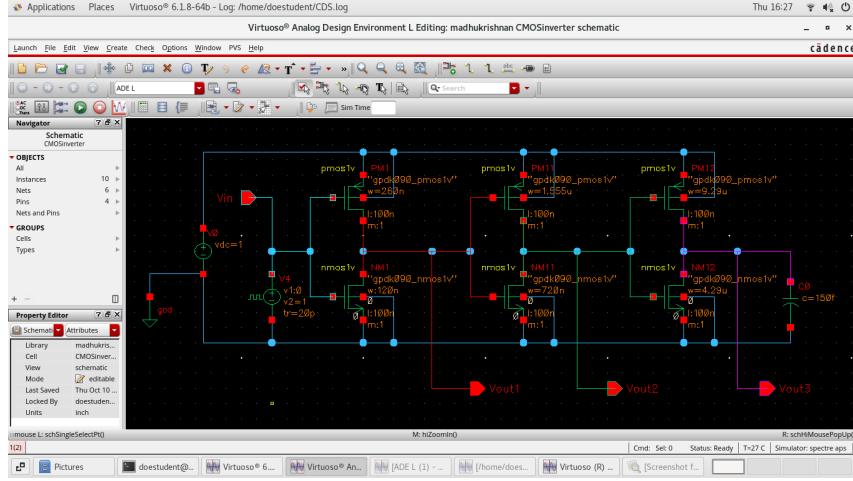


Figure 26: Inverter chain of 3 inverters

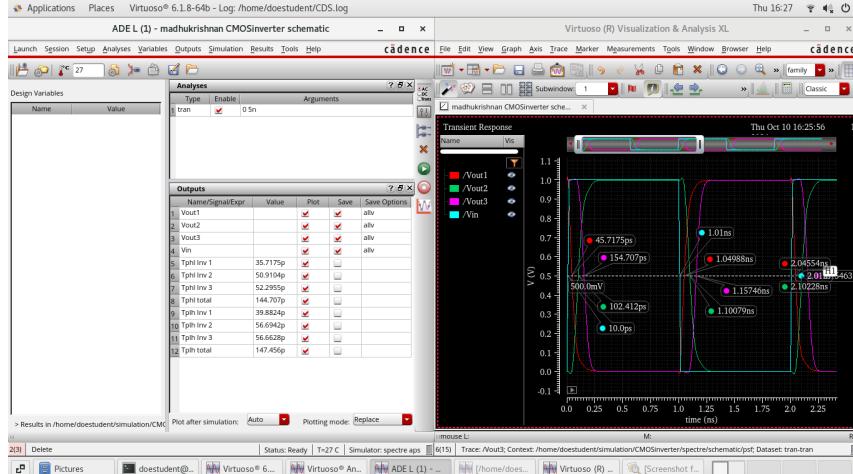


Figure 27: Inverter chain of 3 inverters: results

9.4 Comparison of transient analysis results

Inverter	$N = 3$		$N = 4$		$N = 5$	
	T_{PLH}	T_{PHL}	T_{PLH}	T_{PHL}	T_{PLH}	T_{PHL}
Inverter 1	39.8824	35.7175	28.3957	25.4848	23.5372	21.2211
Inverter 2	59.6942	50.9104	38.3280	34.5064	30.5397	27.7760
Inverter 3	56.6628	52.2955	39.3162	35.1857	30.1401	26.8758
Inverter 4			38.4539	35.6405	30.5241	33.6376
Inverter 5					32.8564	28.5686
Total	147.456	144.707	137.452	137.858	147.947	137.729

Table 5: Variation in delay with inverter chain size

The table 5 compares the propagation delays of each inverter chain design. The delay increases as the number of inverters varies from the ideal number estimated.

The size of the inverters at the same position is reduced as the number of inverters in the inverter chain increases. This means that we can drive the same load either by using a small chain of large inverters or a larger chain with smaller inverters, but at the cost of propagation delay when diverged from the ideal number of inverters.

10 Estimation of power

The dynamic and leakage power dissipation of the unit inverter designed was found using Cadence Virtuoso. The variation of power dissipation with size, drain voltage, and load capacitance variance were estimated.

10.1 Variance of power dissipation with size

The inverter size was parameterised as shown in Figure 28. The results of the dynamic and leakage power dissipation analysis are shown in Figure 29 and Figure 30 and are tabulated in Table 6

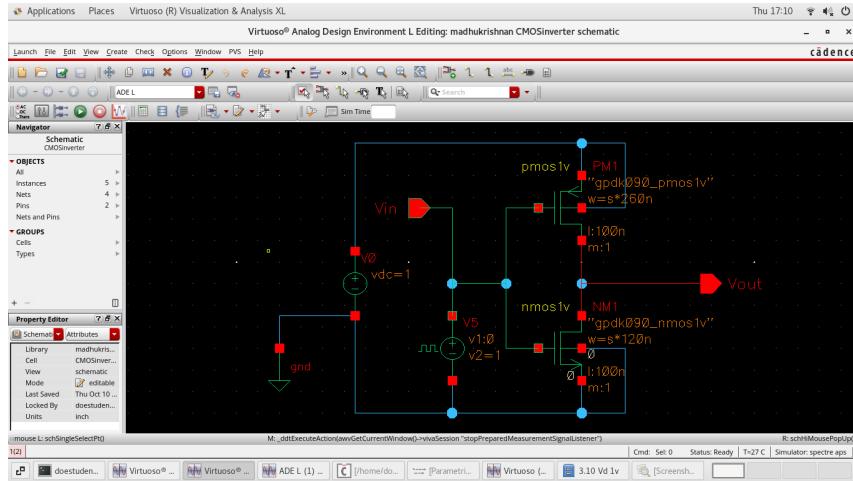


Figure 28: Inverter with size parameterised



Figure 29: Inverter with size parameterised: dynamic power

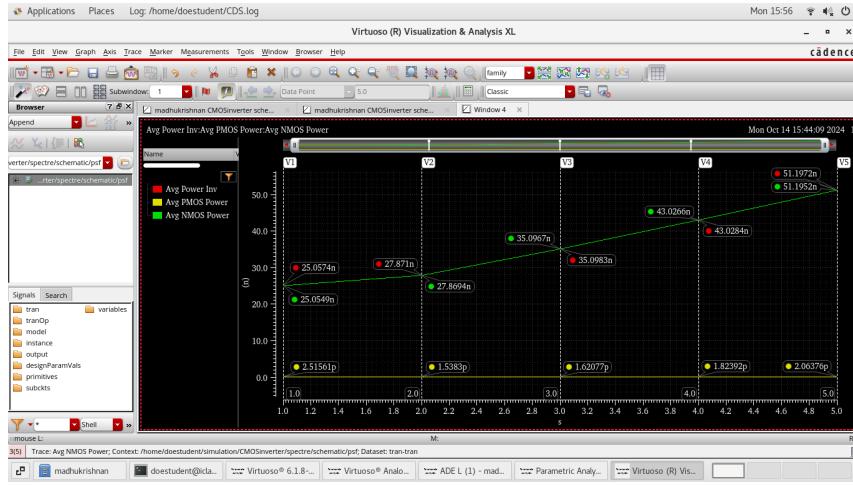


Figure 30: Inverter with size parameterised: leakage power

Inverter size	Dynamic power (μW)			Leakage power(nW)		
	PMOS	NMOS	Inverter	PMOS	NMOS	Inverter
1	0.3515	0.4168	0.7683	0.002515	25.0549	25.0574
2	0.6532	0.7728	1.4260	0.001538	27.8694	27.871
3	0.9802	1.1548	2.1350	0.001621	35.0967	35.0983
4	1.3069	1.5382	2.8451	0.001824	43.0266	43.0284
5	1.6334	1.9210	3.5544	0.002064	51.1952	51.1972

Table 6: Variation of average dynamic and leakage power with inverter size

10.2 Variance of power dissipation with drain voltage

The drain voltage of the inverter was parameterised, as shown in Figure 31, and parametric analysis was performed. The dynamic and leakage power dissipation graphs are shown in Figure 32 and Figure 33 and are tabulated in Table 7. The total power dissipated increases quadratic with the increase in drain voltage.

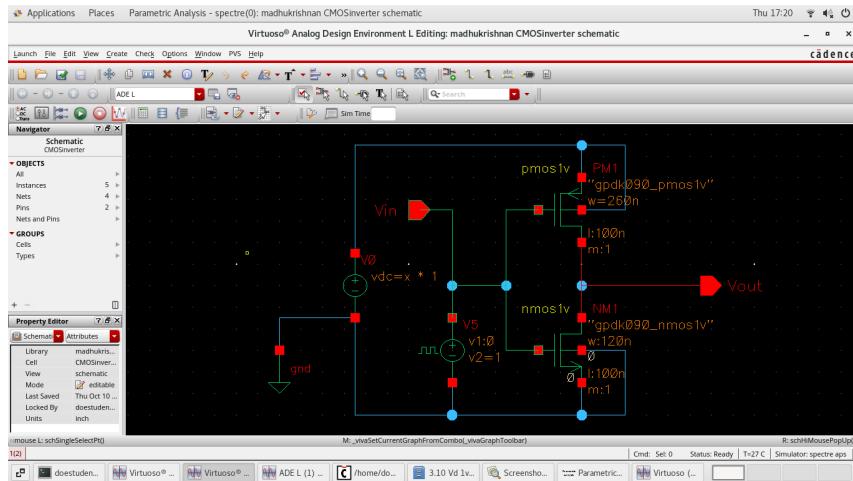


Figure 31: Inverter with drain voltage parameterised



Figure 32: Inverter with drain voltage parameterised: Dynamic power

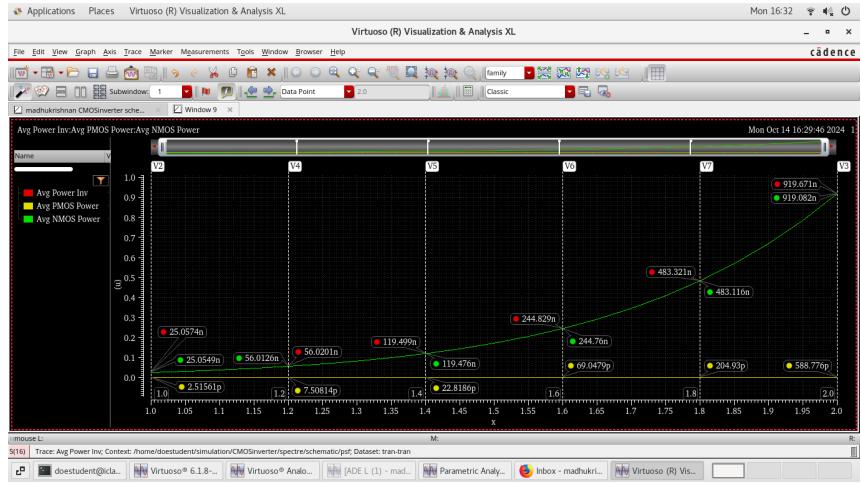


Figure 33: Inverter with drain voltage parameterised: Leakage power

Drain voltage	Dynamic power (uW)			Leakage power(nW)		
	PMOS	NMOS	Inverter	PMOS	NMOS	Inverter
1.0	0.3515	0.4168	0.7683	0.002516	25.0549	25.0574
1.2	0.7148	0.5676	1.2824	0.007508	56.0126	56.0201
1.4	7.6189	1.0297	8.6486	0.022819	119.476	119.4990
1.6	24.0115	3.6966	27.708	0.069048	244.760	244.8290
1.8	41.336	12.5236	53.8596	0.204930	483.116	483.3210
2.0	42.2206	37.1933	79.4139	0.588776	919.082	919.6710

Table 7: Variation of average dynamic and leakage power with drain voltage

10.3 Variance of power dissipation with load capacitance

A load capacitor was attached to the output, as shown in Figure 34. The power dissipation results are shown in Figure 35 and Figure 36 and are tabulated in Table 8.

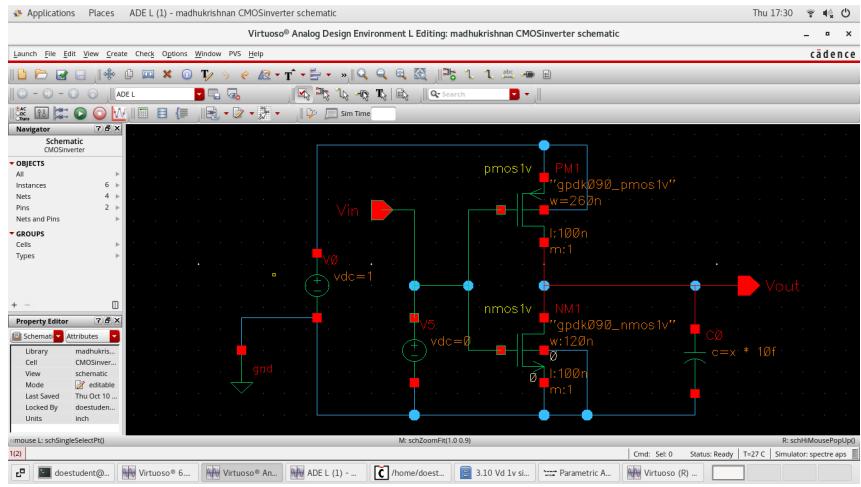


Figure 34: Inverter with load capacitance parameterised

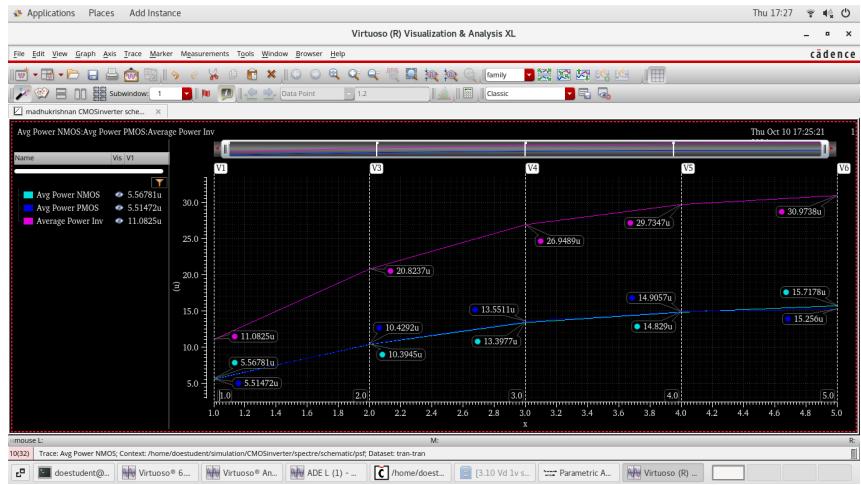


Figure 35: Inverter with load capacitance parameterised: dynamic power



Figure 36: Inverter with load capacitance parameterised: leakage power

Load capacitor	Dynamic power (μW)			Leakage power(nW)		
	PMOS	NMOS	Inverter	PMOS	NMOS	Inverter
10 fF	5.5147	5.5678	11.0825	25.0549	0.002516	25.0574
20 fF	10.4292	10.3945	20.8237	25.0549	0.002516	25.0574
30 fF	13.5511	13.3977	26.9489	25.0549	0.002516	25.0574
40 fF	14.9057	14.8290	29.7347	25.0549	0.002516	25.0574
50 fF	15.2560	15.2560	30.9738	25.0549	0.002516	25.0574

Table 8: Variation of average dynamic and leakage power with load capacitance

10.4 Comparison of power dissipation analysis

Variations in dynamic and leakage power dissipation were observed in various cases and were found to increase with size, drain voltage, and load capacitance. The dynamic power dissipation of PMOS occurs when the inverter output switches from low to high, and the dynamic power dissipation of NMOS occurs when the inverter output goes from high to low. The leakage power was found to be consistent throughout the transient analysis. This can be seen in Figure 37. In addition, the leakage power is relatively small (less than 3.5 percent) compared to dynamic power dissipation.

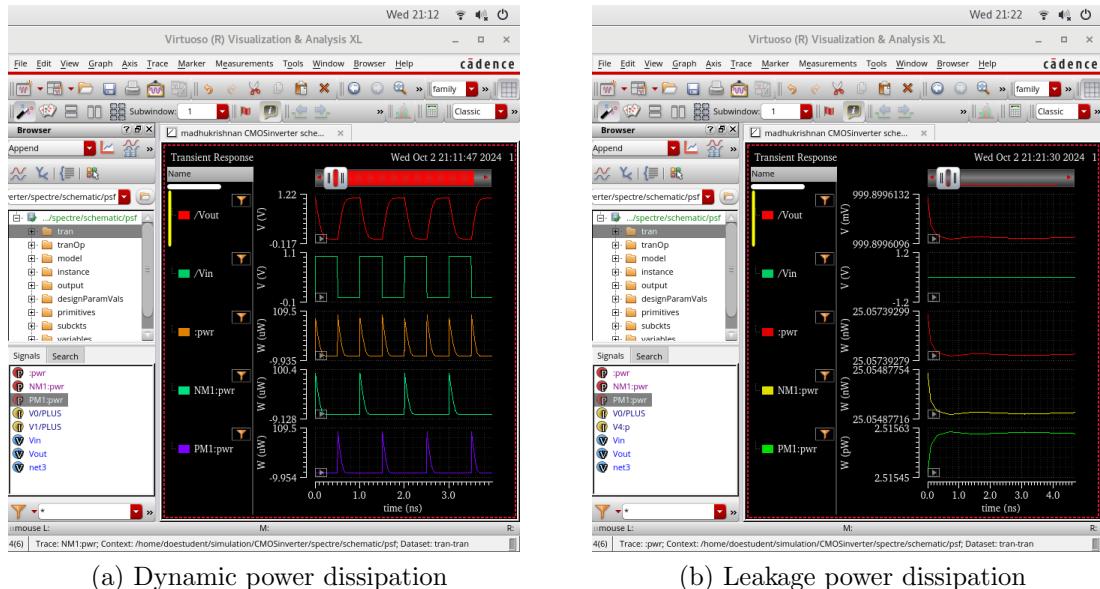


Figure 37: Comparison of dynamic and leakage power dissipation