Digital Integrated Circuit Lab Report

Experiment 4

Combinational Logic gates

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Contents

1 2-Input NAND gate

A 2-input NAND gate was designed using CMOS logic, as depicted in Figure 1. It consists of 2 PMOS for the pull-up circuit and 2 NMOS transistors for the pull-down circuit. Minimum-sized MOSFETs were used to create the circuit.

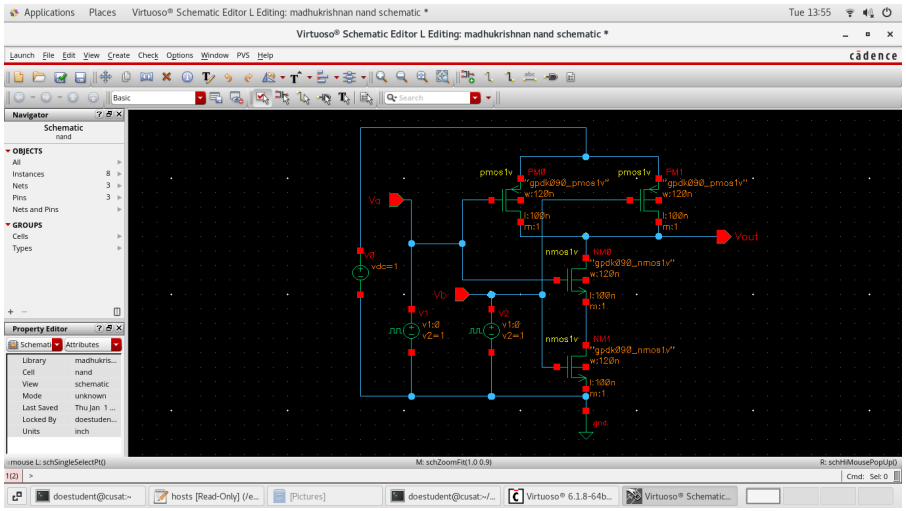


Figure 1: 2-input NAND gate schematic

1.1 Noise margin

Voltage transient characteristic graphs for three conditions were plotted as shown in Figure 2, Figure 3, and Figure 4.

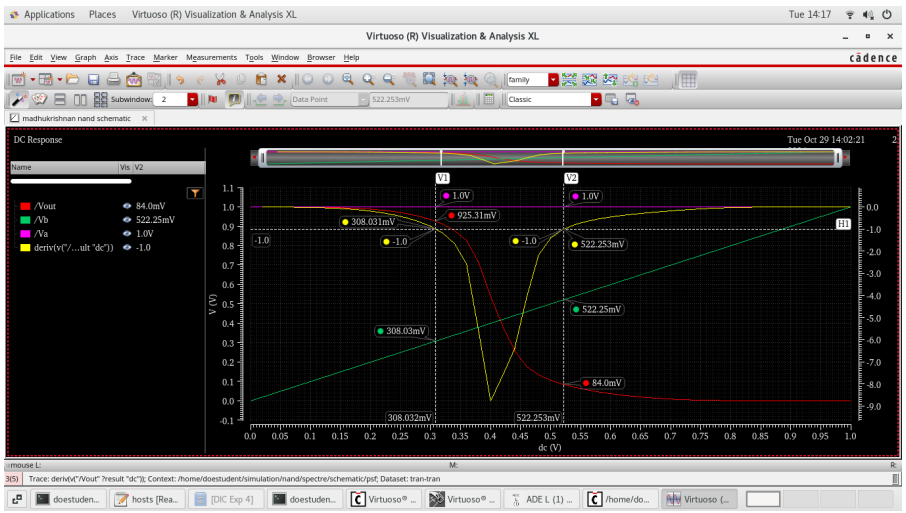


Figure 2: DC Analysis $V_A = 1V, V_B = 0 -> 1V$

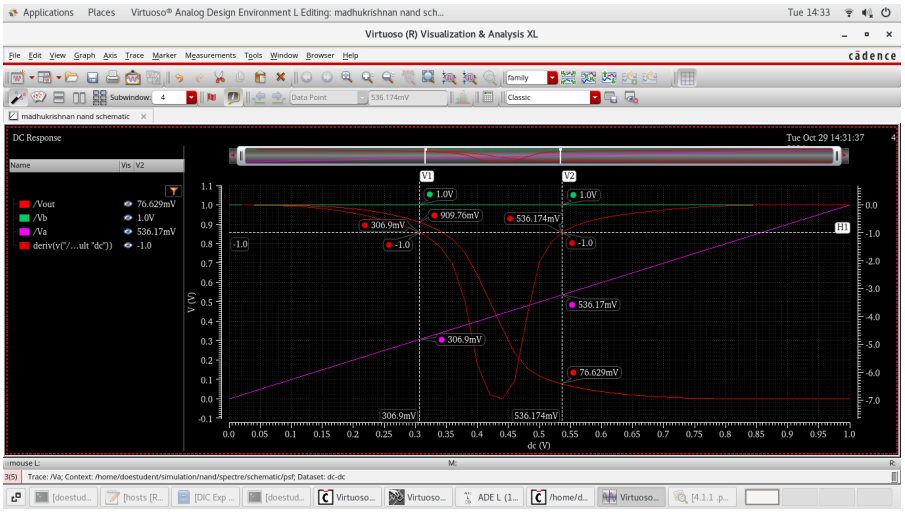


Figure 3: DC Analysis $V_A = 0- > 1V, V_B = 1V$

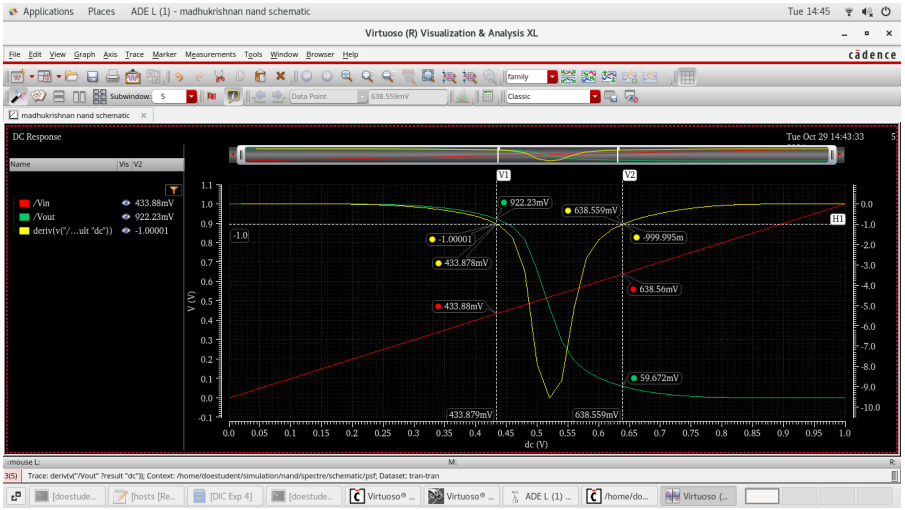


Figure 4: DC Analysis $V_A, V_B = 0- > 1V$

1.2 Comparison of noise margin

Noise margin are given by Equation 1, Equation 2, and Equation 3.

$$Noise\ margin\ high,\ NM_H = V_{OH} - V_{IH} \tag{1}$$

$$Noise\ margin\ low,\ NM_L = V_{IL} - V_{OL} \tag{2}$$

$$Noise\ margin,\ NM = NM_H - NM_L \tag{3}$$

Table 1 shows the noise margins of the CMOS 2-input NAND gate and inverter. The inverter has a better noise margin when compared to the CMOS 2-input NAND gate.

Specification	***NAND gate***			***Inverter***
	$V_A = 1$ $V_B = 0 \rightarrow 1V$	$V_A = 0 \rightarrow 1$ $V_B = 1V$	$V_A = 0 \rightarrow 1$ $V_B = 0 \rightarrow 1$	
Voltage output high V_{OH}	925.31 mV	909.76 mV	922.23 mV	921.980 mV
Voltage output low V_OL	84.0 mV	76.629 mV	59.672 mV	68.312 mV
Voltage input high V_IH	522.253 mV	536.174 mV	638.559 mV	513.420 mV
Voltage input low V_IL	308.03 mV	306.9 mV	433.879 mV	279.696 mV
Noise margin high NM_H	403.057 mV	373.586 mV	283.671 mV	408.560 mV
Noise margin low NM_L	224.03 mV	230.271 mV	374.207 mV	211.384 mV
Noise margin NM	179.027 mV	143.315 mV	-90.536 mV	197.176 mV

Table 1: Comparison of noise margin

2 Transient analysis

Transient analysis for $10nS$ was performed for all three cases. The results are shown in Figure 5, Figure 6, and Figure 5. Input to output delay was found for each case using the calculator tool. Input pulses with magnitude 1V were given a period of $2nS$. The comparison of the delays is tabulated in Table 2.

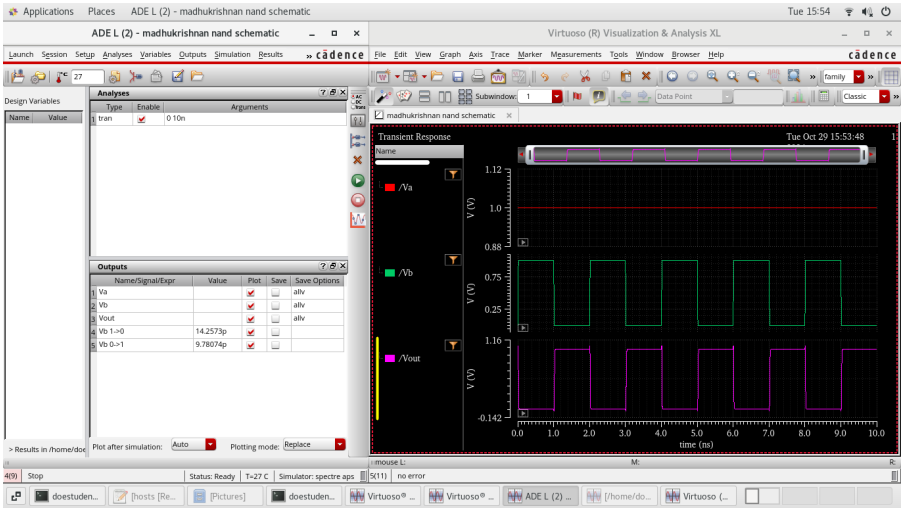


Figure 5: Transient analysis $V_A = 1V, V_B = 0 \rightarrow 1V$

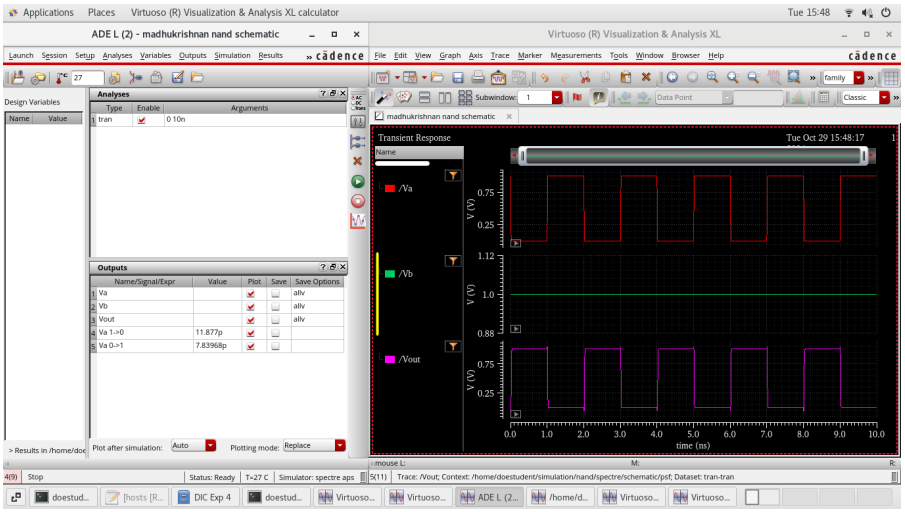


Figure 6: Transient analysis $V_B = 1V, V_A = 0 \rightarrow 1V$

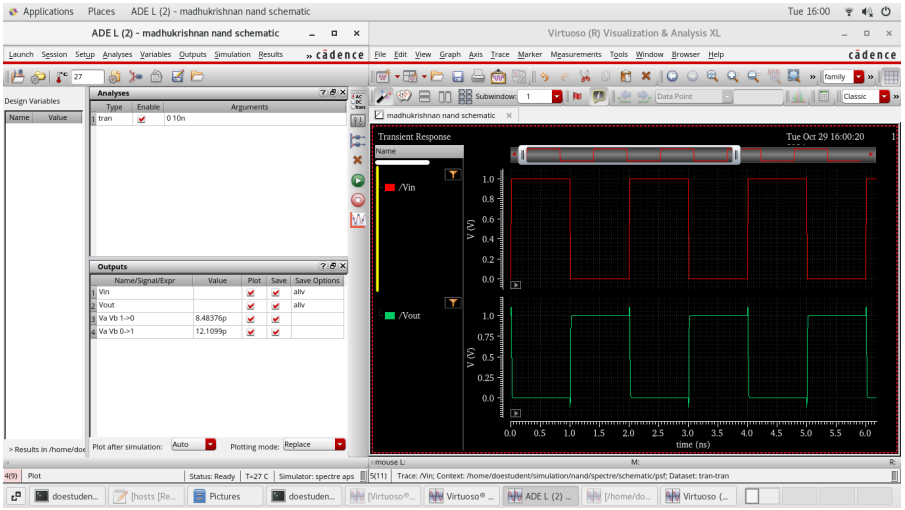


Figure 7: Transient analysis $V_A, V_B = 0 \rightarrow 1V$

Case	T_{plh}	T_{phl}
$V_A = 1V,\ V_B = 0 \rightarrow 1V$	14.2573 ps	9.78074 ps
$V_A = 0 \rightarrow 1V,\ V_B = 1V$	11.877 ps	7.83968 ps
$V_A, V_B = 0 \rightarrow 1V$	8.48376 ps	12.1099 ps

Table 2: Propagation delay of 2-input CMOS NAND gate

3 Calculation of delay using analytical method

The analytical method was used to estimate the delay of the 2-input CMOS NAND gate. Capacitance and resistance values of the MOSFETs were obtained from Experiment 3.

Drain capacitance of PMOS, $C_{dp} = 3.4806$ x 10^{-16} F

Drain capacitance of NMOS, $C_{dn} = 3.96877$ x 10^{-16} F

Resistance of PMOS, $R_p = 21714.05806\ \Omega$

Resistance of NMOS, $R_n = 10030.48551\ \Omega$

Case	***Simulation results***		***Theoretical results***	
	T_{plh}	T_{phl}	T_{plh}	T_{phl}
$V_A = 1V,\ V_B = 0 \rightarrow 1V$	14.2573 ps	9.78074 ps	16.3760 ps	15.12934 ps
$V_A = 0 \rightarrow 1V,\ V_B = 1V$	11.8770 ps	7.83968 ps	16.3760 ps	15.12934 ps
$V_A, V_B = 0 \rightarrow 1V$	8.48376 ps	12.1099 ps	8.1880 ps	15.12934 ps

Table 3: Comparison of delay results

4 Estimation of delay of unit-sized 2-input CMOS NAND gate

The MOSFETs were sized using the sizing ratios obtained from experiment 3, as shown in Figure 8. Resistance and capacitance obtained from the calculations of experiment 3 were used to calculate the delay of the unit-sized 2-input CMOS NAND gate. The same was compared with the simulation results.

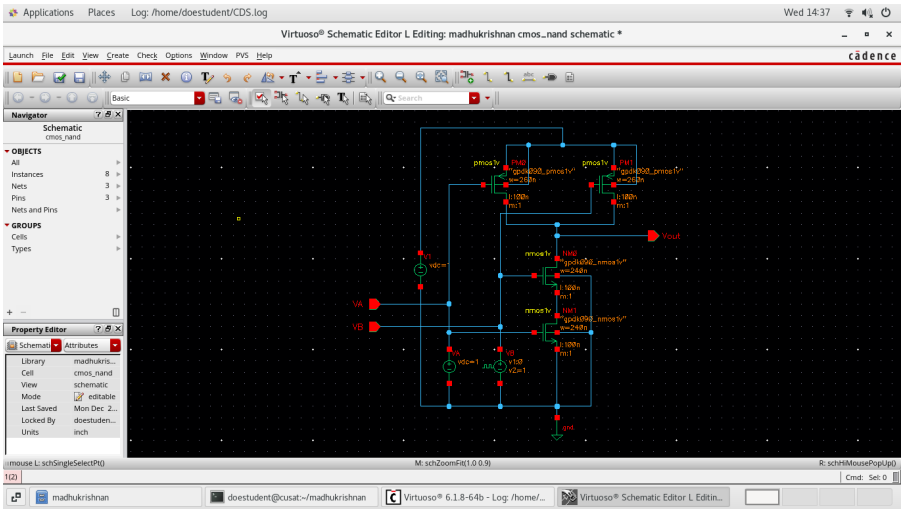


Figure 8: Unit sized CMOS NAND gate: Schematic

Width of PMOS = 260 nm

Width of NMOS = 240 nm

Drain capacitance of PMOS, $C_{dp} = 7.5413$ x 10^{-16} F

Drain capacitance of NMOS, $C_{dn} = 7.93754 \text{ x } 10^{-16}\ F$

Resistance of PMOS, $R_p = 10021.87295\ \Omega$

Resistance of NMOS, $R_n = 5015.242755\ \Omega$

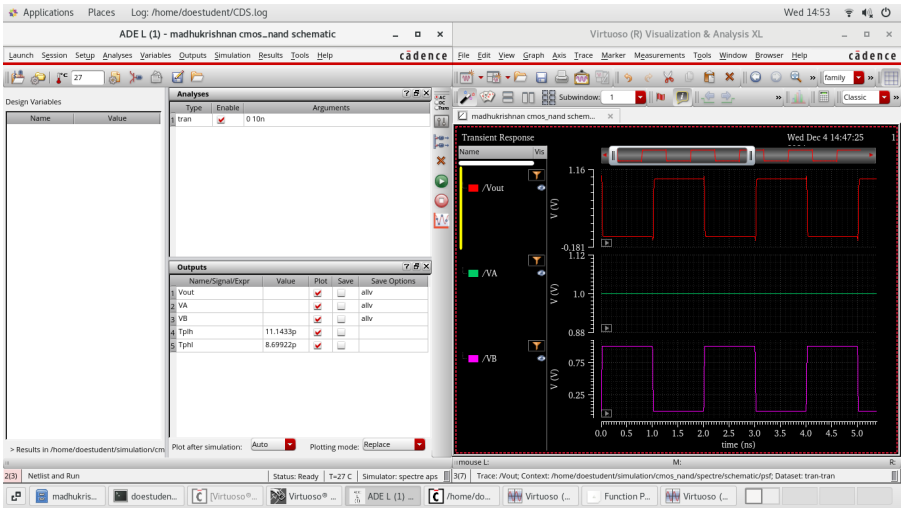


Figure 9: Transient analysis $V_A = 1V, V_B = 0 \rightarrow 1V$

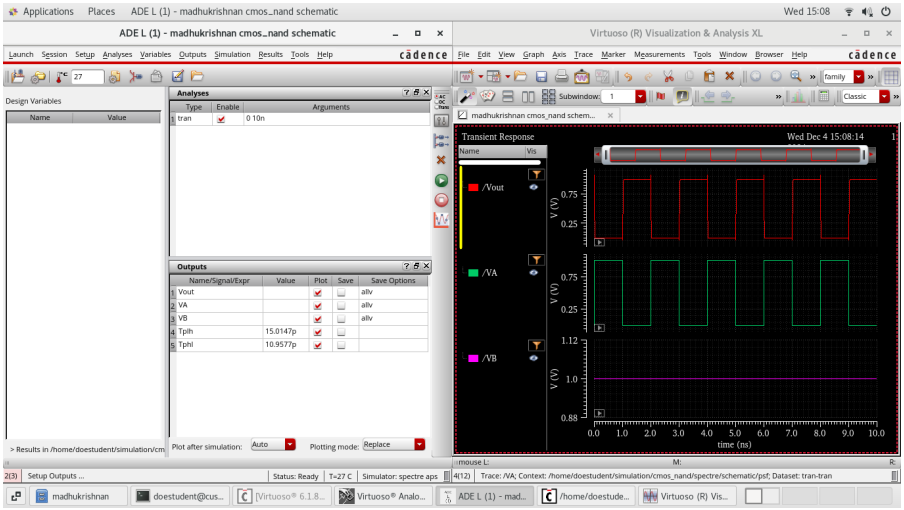


Figure 10: Transient analysis $V_B = 1V, V_A = 0 \rightarrow 1V$

Case	***Simulation results***		***Theoretical results***	
	T_{plh}	T_{phl}	T_{plh}	T_{phl}
$V_A = 1V,\ V_B = 0 \rightarrow 1V$	11.1433 ps	8.69922 ps	15.91864 ps	15.93232 ps
$V_A = 0 \rightarrow 1V,\ V_B = 1V$	15.0147 ps	10.9577 ps	15.91864 ps	15.93232 ps
$V_A, V_B = 0 \rightarrow 1V$	8.28752 ps	12.74 ps	7.95932 ps	15.93232 ps

Table 4: Comparison of delay results

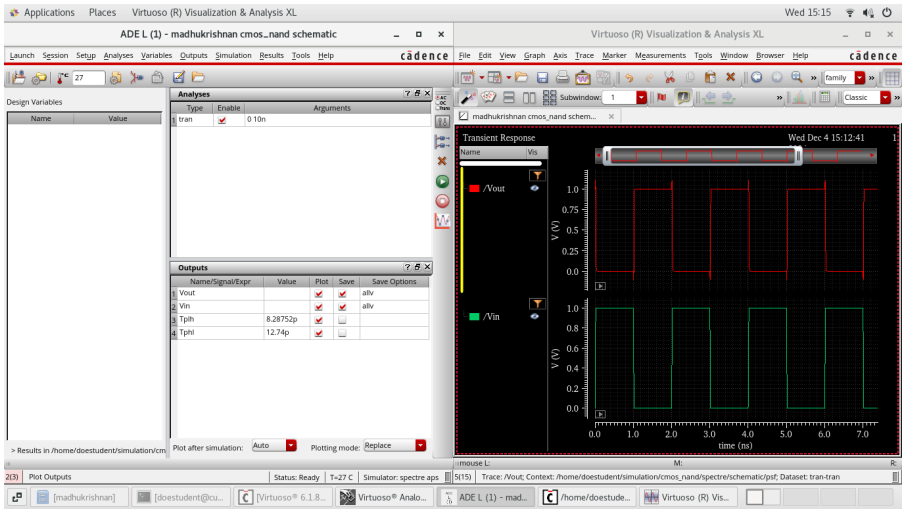


Figure 11: Transient analysis $V_A, V_B = 0 \rightarrow 1V$

5 Pseudo NMOS 2-input NAND gate

A Pseudo NMOS 2-input NAND gate has a PMOS connected to the ground, replacing the pull-up network. Therefore having N+1 number of MOSFETs. The schematic circuit is shown in Figure 12.

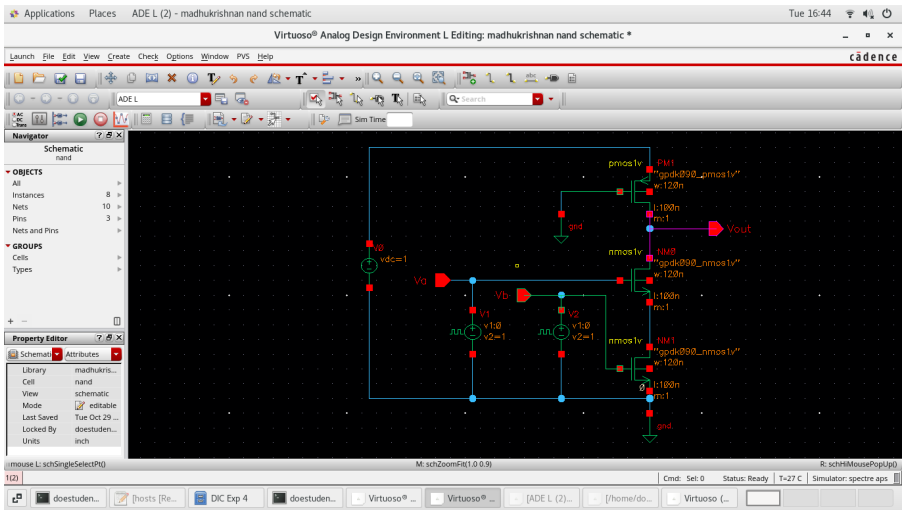


Figure 12: Pseudo NMOS 2-input NAND gate

5.1 DC Analysis

DC Analysis was performed for input V_A, V_B, and V_A & V_B together, as shown in Figure 13 and Figure 14.

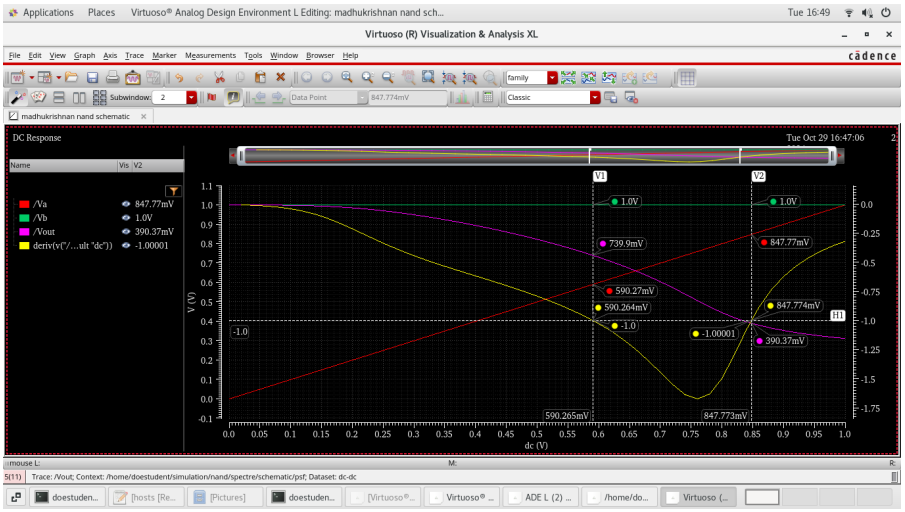


Figure 13: DC Analysis for input V_A

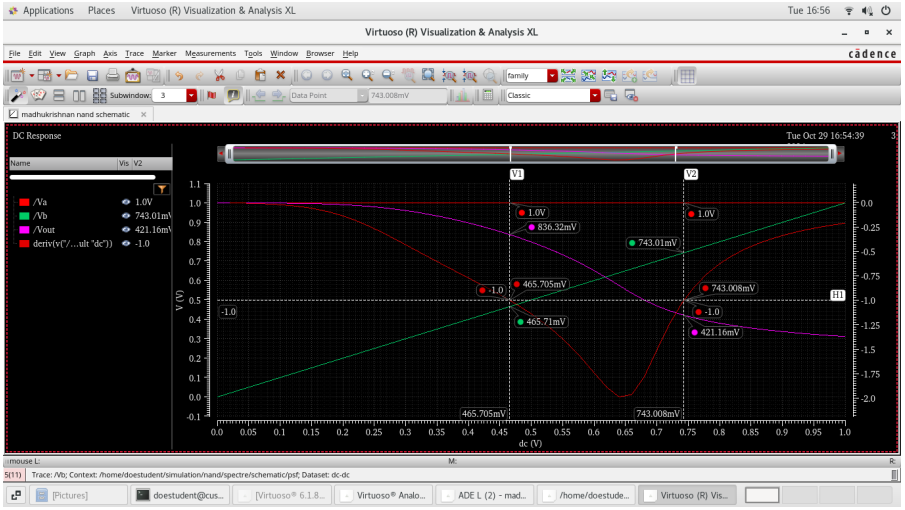


Figure 14: DC Analysis for input V_B

5.2 Transient analysis

Transient analysis for a duration of $10nS$ was performed for each input. The delay was calculated using the calculator tool and tabulated in Table 5.

Case	T_{plh}	T_{phl}
$V_A = 1V,\ V_B = 0 \rightarrow 1V$	2.68557 ps	11.4738 ps
$V_A = 0 \rightarrow 1V,\ V_B = 1V$	0.31027 ps	10.9208 ps
$V_A, V_B = 0 \rightarrow 1V$	0.078285 ps	12.6706 ps

Table 5: Propagation delay of Pseudo NMOS 2-input NAND gate

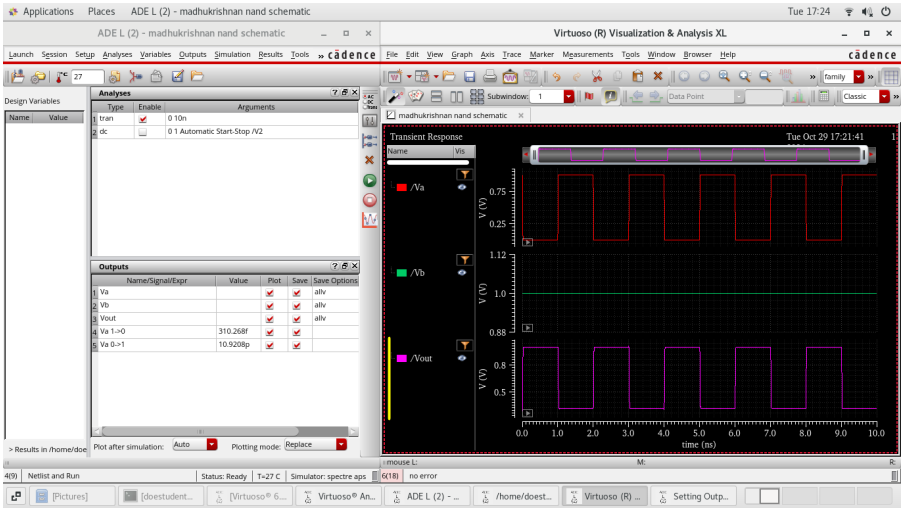


Figure 15: Transient Analysis for input V_A

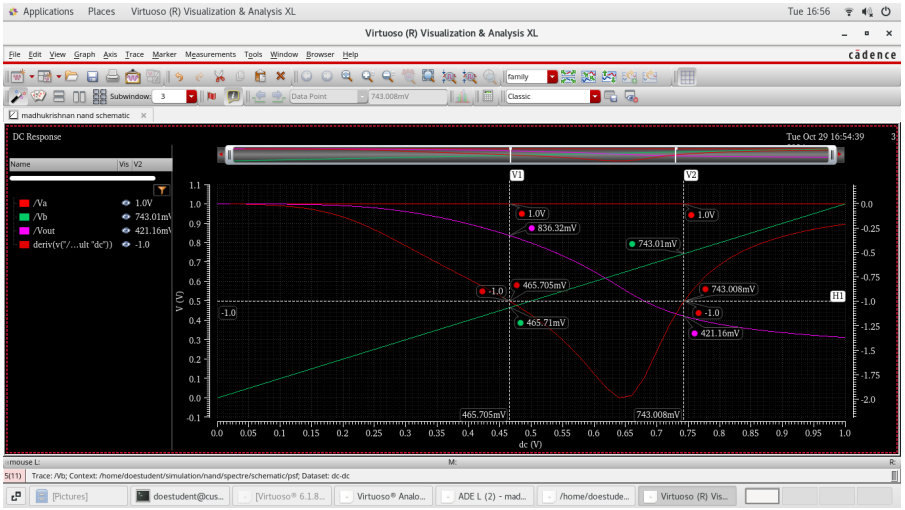


Figure 16: Transient Analysis for input V_B

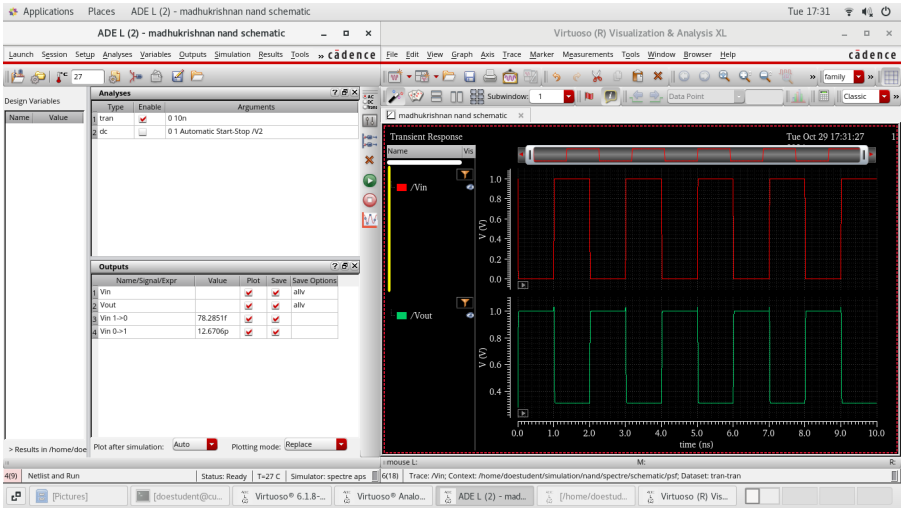


Figure 17: Transient Analysis for input V_A & V_B

6 Dynamic 2-input NAND gate

Dynamic 2-input NAND gate consists of a pull-down network connected to the V_{DD} and ground through a PMOS and NMOS switched using a clock signal, respectively. The schematic circuit is shown in Figure 18. Minimum-size PMOS and NMOS were used to construct the circuit.

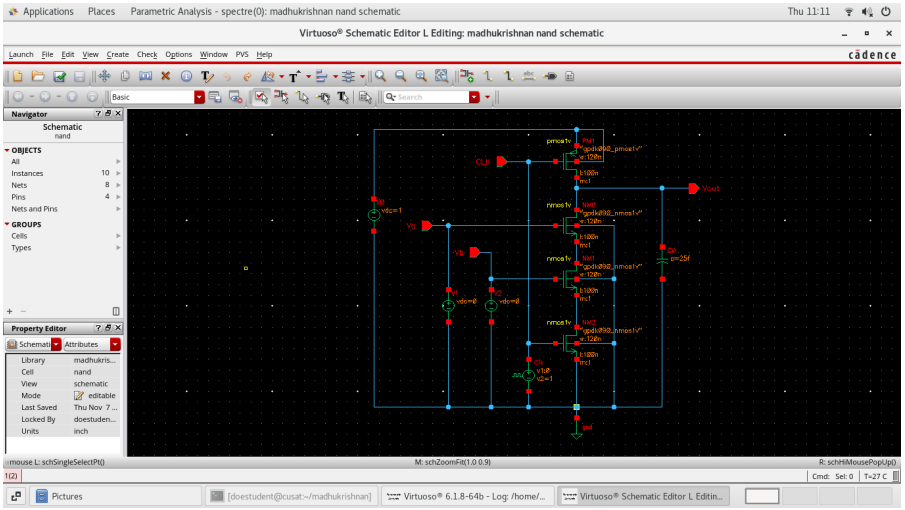


Figure 18: Dynamic 2-input NAND gate: Schematic diagram

6.1 Charge leakage

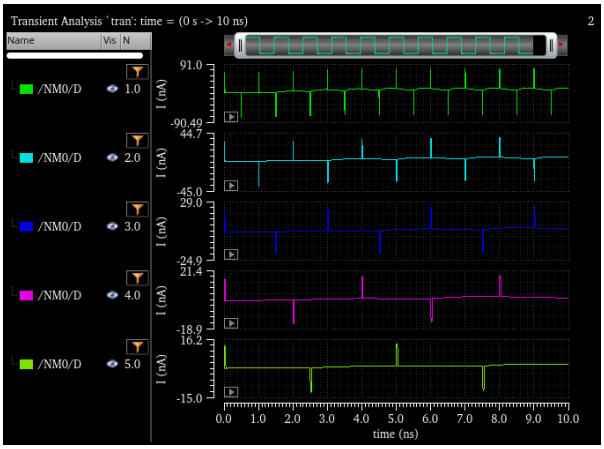
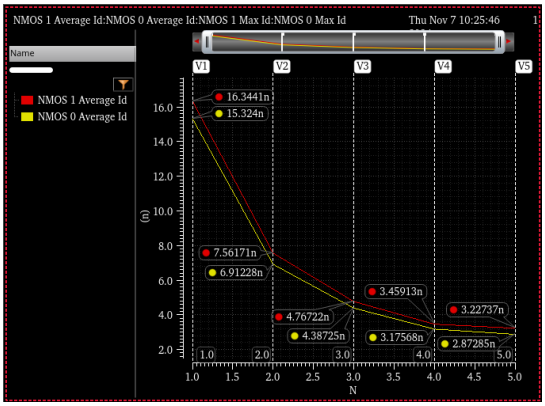
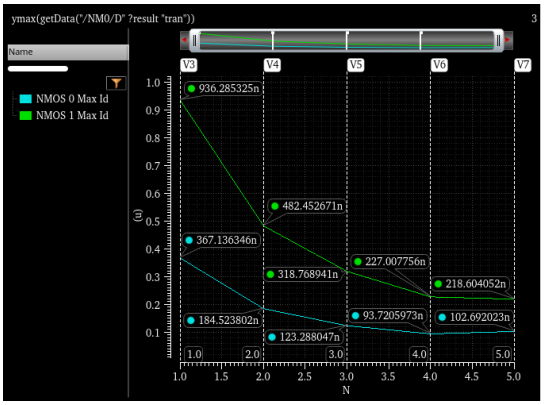


Figure 19: Dynamic 2-input NAND gate: Charge leakage

The charge leakage through the MOSFETs was observed using transient analysis. The maximum and average drain current for each NMOS was plotted, as shown in Figure 19. The clock frequency was parameterised, and variation in leakage current and maximum current was observed. It was seen that the leakage current reduces as the clock period increases. The graph is shown in Figure 20.



(a) Average leakage current



(b) Maximum leakage current

Figure 20: Leakage current

7 Pass transistor 2 to 1 multiplexer

A 2 to 1 multiplexer using PMOS logic was made, as shown in Figure 21. Transient analysis was performed on the circuit as shown in Figure 22. It can be seen that the output voltage doesn't reach V_{DD}.

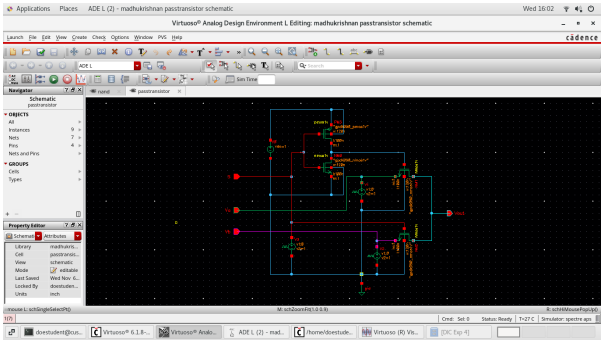


Figure 21: Pass transistor 2 to 1 multiplexer: Schematic diagram

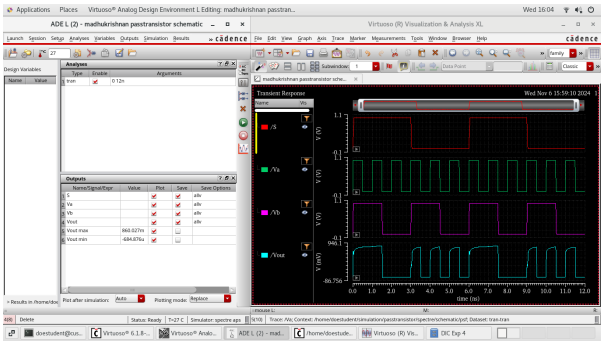


Figure 22: Pass transistor 2 to 1 multiplexer: Transient analysis

8 Transmission gate 2 to 1 multiplexer

A transmission gate 2 to 1 multiplexer was constructed, as shown in Figure 23. Transient analysis was performed on the circuit as shown in Figure 24. It can be seen that the output voltage reaches V_{DD}.

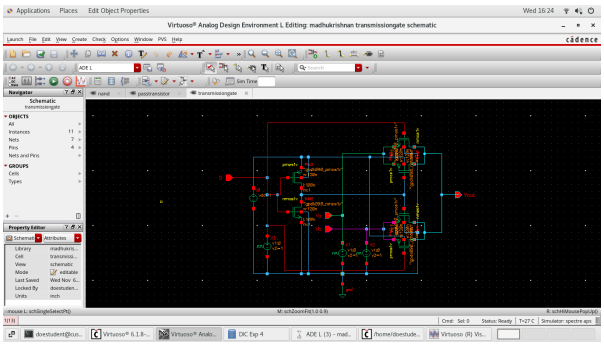


Figure 23: Transmission gate 2 to 1 multiplexer: Schematic diagram

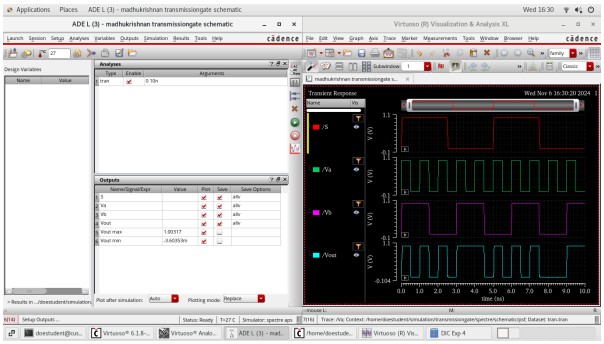


Figure 24: Transmission gate 2 to 1 multiplexer: Transient analysis