Subject Name & Code	CMOS VLSI CIRCUITS– EC630
No. of Teaching Hours: 40; Practical: 12 sessions.	Credits : 3:0:1 L-T-P
CIE Marks: 50	SEE Marks: 50

Course outcome: At the end of the course, the student should be able

1. Explain the CMOS Logic, VLSI Design flow and the CMOS Process technology.
2. Analyze the characteristics and compute the performance parameters of CMOS circuits, and interpret results.
3. Develop and illustrate the combinational and sequential circuits for circuit characterization and power estimation.
4. Design, Demonstrate and validate the analog and digital CMOS circuits using Cadence tool, document and give an effective presentation.

UNIT 1:

Introduction: A Brief History, MOS Transistors, CMOS Logic, CMOS fabrication and Layout, VLSI Design Flow, Fabrication, Packaging, and testing **08 Hours**

UNIT 2:

MOS Transistor Theory: Introduction, Ideal I-V Characteristics, C-V Characteristics, Non ideal I-V Effects, DC Transfer Characteristics, Switch - level RC Delay Models **08 Hours**

UNIT 3:

Circuit Characterization and Performance Estimation**:** Introduction, Delay Estimation, Logical effort and transistor sizing, Power Dissipation, Interconnect, Design Margin, and Reliability. **08 Hours**

UNIT 4:

Combinational and Sequential circuit design: SR Latch Circuit, Clocked Latch and Flip-Flop Circuits, D-Latch and Edge-Triggered Flip-Flop **08 Hours**

UNIT 5:

Dynamic Logic Circuits - Voltage Bootstrapping Synchronous Dynamic Circuit Techniques High-Performance Dynamic CMOS Circuits and Semiconductor Memories: ROM, SRAM, DRAM circuits. **08 Hours**

Self-Learning Component:

1. Analyze the characteristics and compute the read / write operation of SRAM cell.
2. Design and Develop the PLL for high frequency (5-GHz) applications.

Text Books:

1. **Neil H.E. Weste, David Harris, Ayan Bannerjee:"** CMOS *VLSI DESIGN: A Circuits and Systems Perspective,"* 3rd Edition, Published by Pearson Education, 2005.
2. **Douglas. A. Pucknell, Kamran Eshragian:** *"Basic VLSI Design,"* 3rd Edition, Eastern Economy Edition, 1994.
3. **R. Jacob, W. Li, David .E. Boyce:** *"CMOS Circuit Design, Layout, and Simulation,"* Prentice Hall India, 1998.
4. **Sung-Mo Kang, Yusuf Leblebici:** "*CMOS DIGITAL INTEGRATED CIRCUITS Analysis and Design,"* 2nd Edition, McGraw Hill, 2003.

E-Resource

1. https://youtu.be/Gv5fESGW2Ms?list=PLNhFkFk6qEgLxC8XgE38cYNgI1wldYxXZ
2. https://youtu.be/lRpt1fCHd8Y?list=PLCmoXVuSEVHlEJi3SwdyJ4EICffuyqpjk
3. https://youtu.be/o9vEnzLL-lY?list=PLojsqdbIzJGQtub91c4fF-TcCdzVYAInM

CMOS VLSI Circuits Lab

List of Experiments (The experiments are conducted using Cadence tool).

PART – A (Digital Experiments)

1. Draw the CMOS schematic and Layout of the inverter circuit, simulate both schematic and layout to determine propagation delay, rise time fall time and Q-point and comment on the results.
2. Draw the CMOS schematic of the 2 input NAND and NOR gate, also draw the layout of the same, and simulate for transient result.
3. Draw the CMOS schematic of the Half Adder circuit and verify it with truth table, and also draw the layout of the same, and simulate for transient result.
4. Draw the CMOS circuit of the 2:1 Multiplexer circuit and verify it with truth table, and also draw the layout of the same, and simulate for transient result.

PART – B (Analog Experiments)

1. Design the Common source amplifier schematic for a gain of 30dB and also draw the layout of the same, simulate the layout for ac analysis and comment on results.
2. Design the Common Drain amplifier schematic and also draw the layout of the same, simulate the layout for ac analysis and comment on results.
3. Design the Common Gate amplifier schematic (Current Gain of 30dB) and also draw the layout of the same, simulate the layout for ac analysis and comment on results.
4. Design the Differential amplifier schematic for a gain of 50dB.

E-Resource for Cadence tutorial:

1. https://www.youtube.com/watch?v=u0WgSMa1hrc&list=PLK2eyR1C9gjr7j-YoL_-JwJmjU6lNZGTO