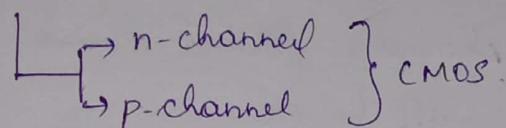


| <u>BJT</u>                  | <u>FET</u>                                   |
|-----------------------------|--|
| ① Bipolar                   | ① Unipolar.                                  |
| ② Current controlled device | ② Voltage controlled device.                 |
| ③ B cannot be scaled        | ③ Scaled.                                    |
| ④ Bulky                     | ④ Non-Bulky                                  |
| ⑤ More Vtg.                 | ⑤ Less vtg. is required to drive the device. |

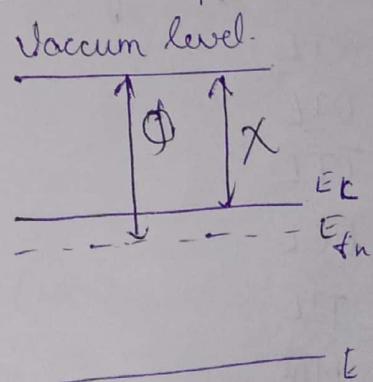
MOSFET: [Metal Oxide Semiconductor field effect transistor]



n-MOS:

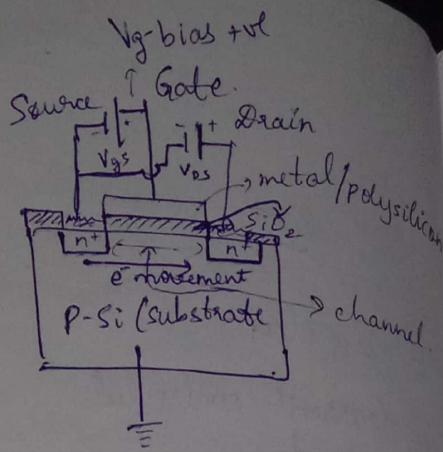
$E_f$  = fermi level gives the probability of  $e^-$

- \* work function ( $\phi$ )
- \*  $e^-$  affinity ( $X$ )
- \* Work function gives the energy required to pull  $e^-$  from  $E_f$
- \*  $e^-$  affinity ( $X$ ) is



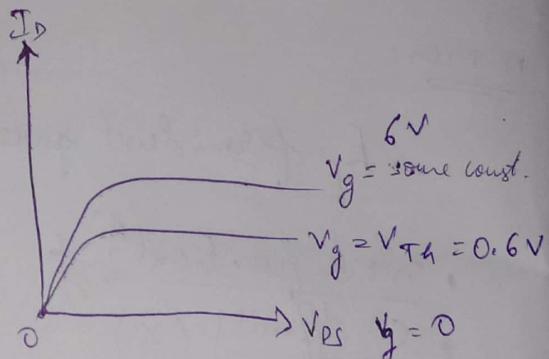
## n-mos (n-channel MOSFET)

Enhancement mode  
(normally off Transistor)  
Depletion mode  
(normally ON Transistor)



- \* channel is formed in enhancement when  $T_{ox}$  ON  
 $I_d \propto \{V_{ds}, V_{gs}\}$
- \* When  $V_{gs}$  applied,  $T_{ox}$  is ON
- \* When  $V_{ds}$  applied,  $e^-$  move through channel from Source to drain
- \* Depletion mode n MOSFET, channel is formed during fabrication.  
So even when  $V_{gs} = 0$ ,  $T_{ox}$  will be ON.

Transistor characteristic graph:



Logical family:

RTL

DTL

TTL

ECL

I<sup>2</sup>L

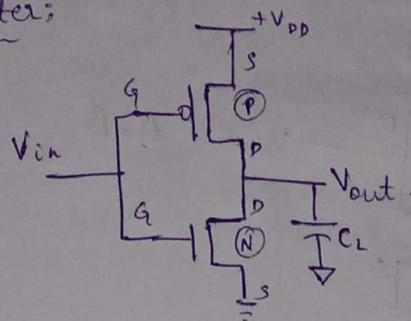
MOS

CMOS

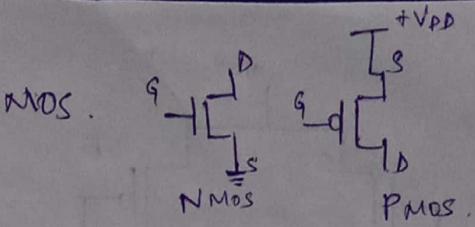
CMOS:

no. of PMOS = no. of NMOS.

a) Inverter:



ON



$$V_{in} \rightarrow D \quad V_{out} = \overline{V_{in}}$$

$V_g = 0$ , n-MOS  $\rightarrow T_x$  is off.

$V_g = \text{High}$ , P-MOS  $\rightarrow T_x$  is off  
(5V)

$V_g \geq V_{th}$ , n-MOS  $\rightarrow T_x$  is ON

$V_g \leq V_{th}$ , P-MOS  $\rightarrow T_x$  is ON  
i.e.  $V_g < 0 \rightarrow \text{" "}$

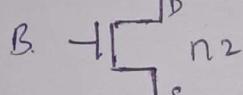
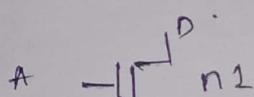
Pull-up-device = P-MOS, it ensures  $V_{out} = +V_{DD}$ .

Pull-down-device = n-MOS.

b) AND-Gate:

$$A \rightarrow D \quad B \rightarrow D \quad Y = A \cdot B$$

To realise AND logic, n-MOS in series. f P-MOS in ||.

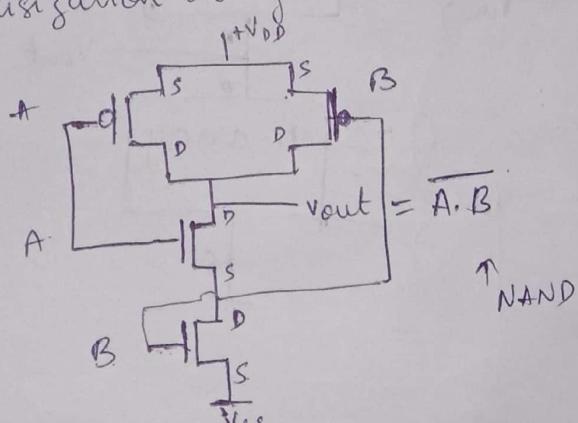


| A | B | n1  | n2  | $A \cdot B$ |
|---|---|-----|-----|-------------|
| 0 | 0 | off | off | 0           |
| 0 | 1 | off | on  | 0           |
| 1 | 0 | on  | off | 0           |
| 1 | 1 | on  | on  | 1           |

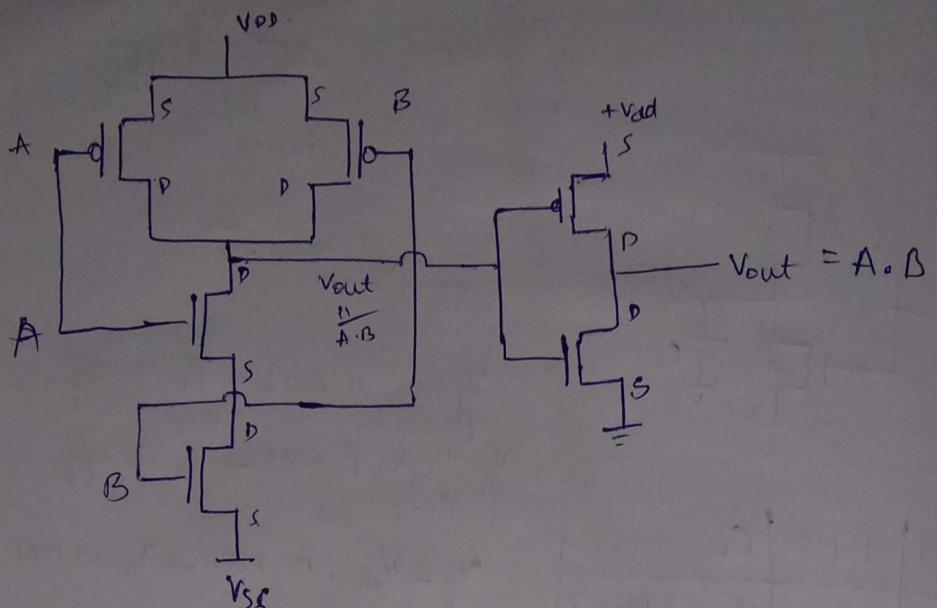
∴ n-MOS is in series to get AND logic

path  $\rightarrow n_1 \rightarrow D$  f  $n_2 \rightarrow S$   
from

∴ AND realization using n-MOS & P-Mos.

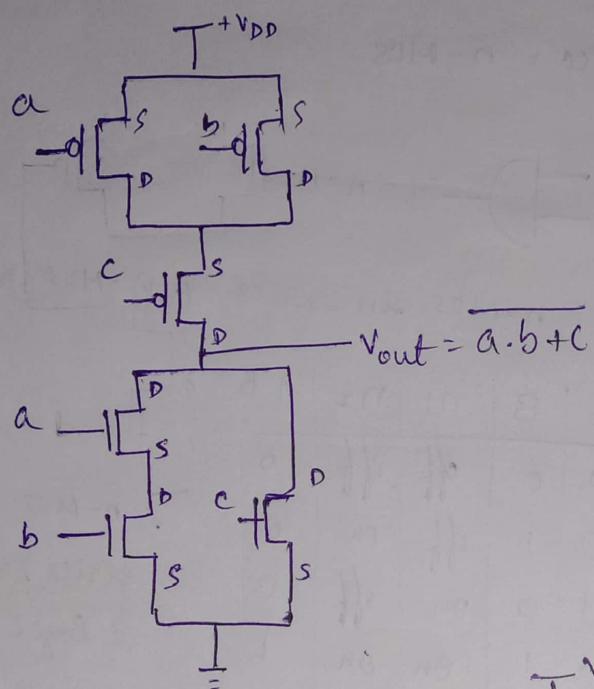


[Combination of P f n okt gives the compliment o/p].

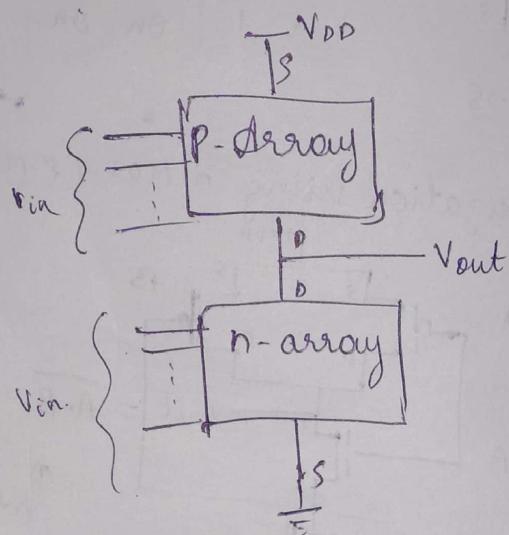


AND

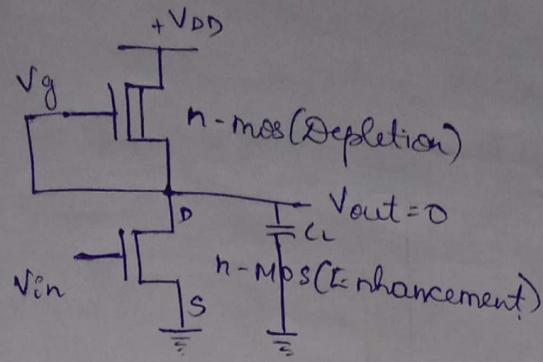
$$\textcircled{1} \quad f(a, b, c) = \overline{ab + c}$$



General C-MOS



## n-MOS inverter:



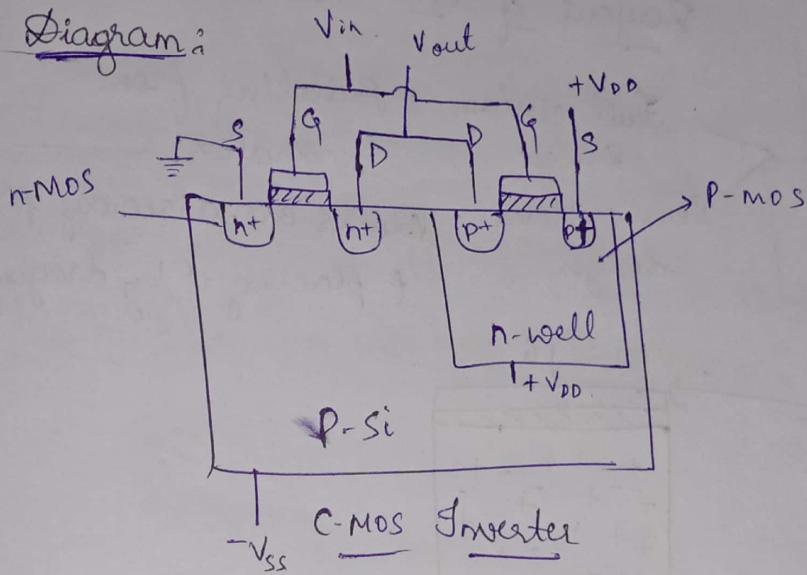
\* Depletion type n-Mos is always on for  $V_g \geq 0$

Initially  $V_{out} = 0 \therefore V_g$ .

i)  $V_{in}=0$ , n-mos(En) = OFF, n-mos(Dep) = ON,  $C_L$  charges,  $V_{out} = V_{DD}$ .

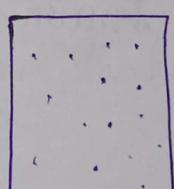
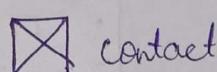
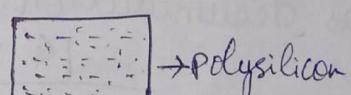
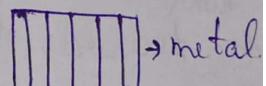
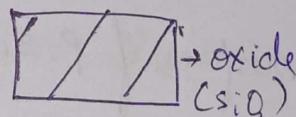
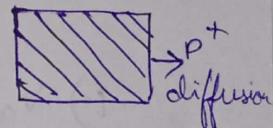
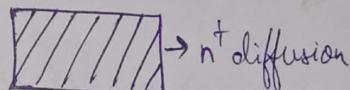
ii)  $V_{in}=1$ ,  $V_g = V_{DD}$ , n-mos(En) = ON,  $V_{out}=0$ ,  $C_L$  discharges through n-mos(enh)

## Layout Diagram:

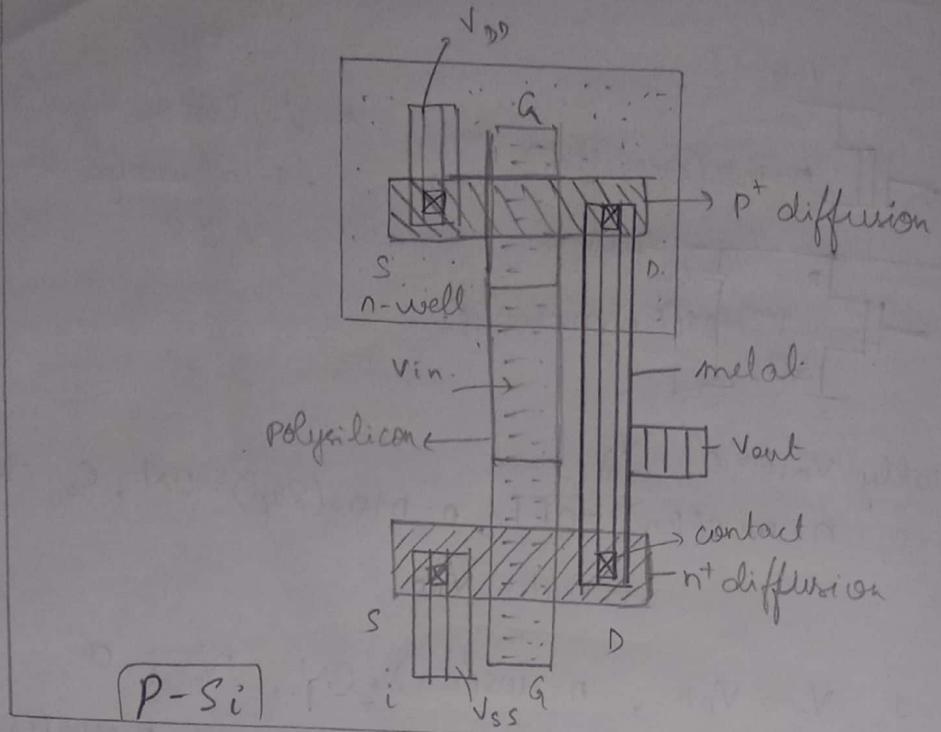


## C-MOS Inverter Layout:

$\lambda$ -based rules.



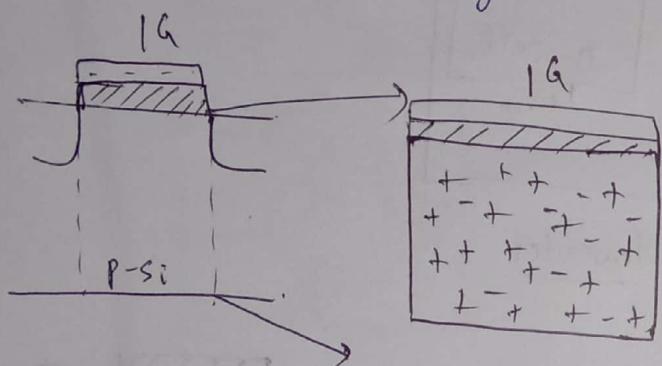
n well.



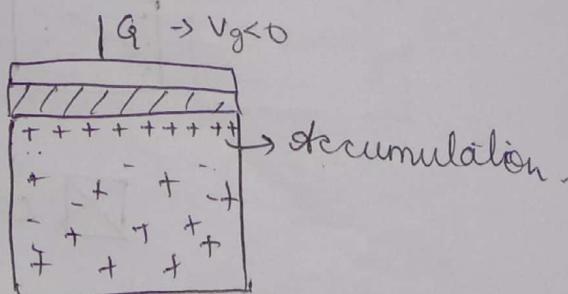
Layout of CMOS inverter (Full custom)

Layout      Full custom : Building from scratch

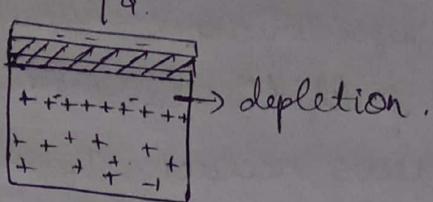
Design  
Semi custom design : Blocks are already present & placing it by dragging.



i.)  $V_g < 0$  (-ve) applied at gate, holes get attracted & move towards top surface of P-Si below oxide layer. This is known as accumulation.

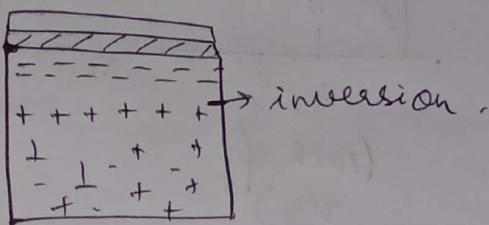


ii)  $0 < V_g < V_{th}$ . When certain +ve volg applied less to G,  $e^-$  get attracted & move at the top of p-si.



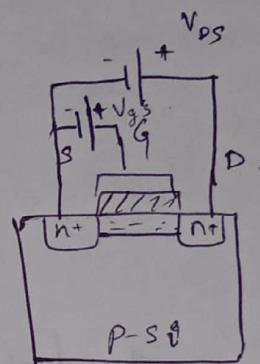
This leads to the region of no charges, known as depletion.

iii)  $V_g \geq V_{th}$ . When  $V_g$  is more positive,  $e^-$  are attracted & forms the channel. This is known as inversion.



### n-mos transistor:

i)  $V_{gs} = 0$ , n-mos = off,  $I_{ds} = 0$



ii)  $V_{gs} \geq V_{th}$ , n-mos = ON,  $\cancel{I_{ds}}$ .

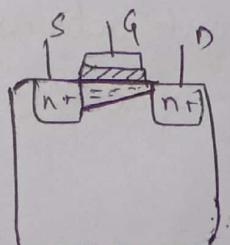
a)  $V_{ds} < V_{gs} - V_{th}$ ,  $I_{ds} \propto V_{ds}$

$V_{th} \rightarrow$  threshold  
voltage of n-channel  
-el.

b)  $V_{ds} \geq V_{gs} - V_{th}$

(Note: Source is given with -ve potential, since it should provide the charge carrier ( $e^-$ )).

\* The moment when  $V_{ds} = V_{gs} - V_{th}$ , the channel near drain seizes, since gate potential has no control at that time. Hence the channel thickness decreases &  $I_{ds}$  becomes constant.



- \* Though channel thickness almost becomes 0, current still exist because potential of  $V_D$  at drain is so high that even channel thickness is less it has power to pull the  $e^-$  & hence there exist  $I_D$ .
- \* Since carriers reduce,  $I_D$  will not increase but remain constant.

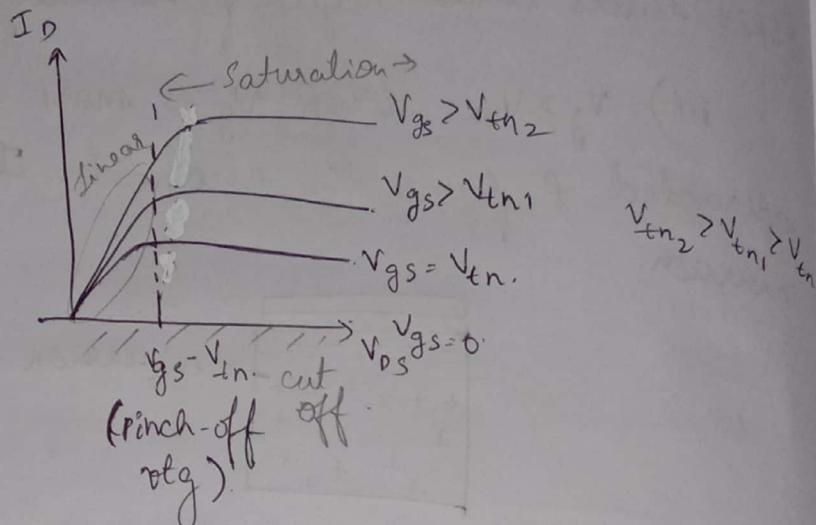
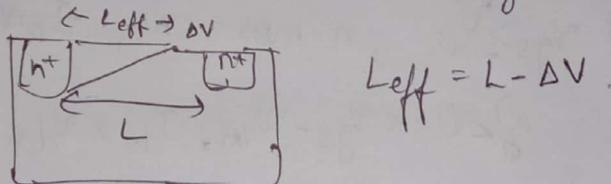


Fig:  $V_I$  characteristics.

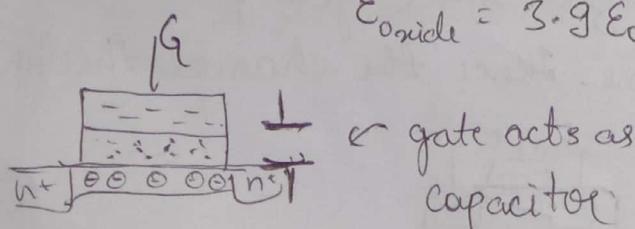
- \*  $L_{eff}$  is the channel length when  $V_{DS}$  is more.



- i) Cut-off or subthreshold region.
- ii) Linear or non-saturated region  $[I_D \propto V_{DS}]$
- iii) Saturated region  $[I_D \text{ is independent of } V_{DS}]$

$SiO_2$  = insulator = dielectric material

$$\epsilon_{oxide} = 3.9 \epsilon_0$$



- a) Channel is formed based on gate voltage.
- b)  $e^-$  drift from source to drain at the rate proportional to  $V_{DS}$ , i.e. electric field  $\frac{V_{DS}}{L} = S + D$ .
- c)  $I_D$  can be computed if we know the amount of charge in the channel & at what rate it moves
- d.) charge on each plate,  $Q = CV$ .
- $$Q_{\text{channel}} = C_g (V_{gc} - V_t)$$
- $$C_g = \frac{\epsilon_{ox} \text{Area}}{t_{ox}}$$
- where,  $t_{ox}$  = thickness of oxide area =  $L \times W$
- $$\epsilon_{ox} = 3.9 \epsilon_0$$
- $$\therefore C_g = \frac{\epsilon_{ox} \text{Area}}{t_{ox}} = \epsilon_{ox} \frac{W \cdot L}{t_{ox}}$$
- $$= C_{ox} W \cdot L$$
- $$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$
- $\Rightarrow$  capacitance per unit area.
- $$V_{gc} = \frac{V_{gs} + V_{gd}}{2} = \frac{V_g - V_s + V_g - V_d}{2} = \frac{2V_g - (V_d + V_s)}{2}$$
- $$\therefore V_{gc} = V_g - \frac{V_d + V_s}{2}$$

Drain & Gate voltage is wrt source, hence  $V_g \rightarrow V_{gs}$

$$\therefore V_{gc} = V_{gs} - \frac{V_{ds}}{2}$$

- e.) velocity,  $v \propto E$ ,  $v = \mu E$        $\mu_n$  =  $e^-$  mobility  
 $\mu_p$  = hole mobility.
- electric field,  $E = \frac{V_{ds}}{L}$        $L$  = channel length.
- Time required for carrier to cross channel is
- $$t = \frac{L}{v}$$
- $v$  = velocity.  
 $L$  = channel length.

$$\therefore I_{ds} = \frac{Q_{\text{channel}}}{t} = \frac{C_g (V_{gc} - V_t)}{L/v}$$

$$I_{ds} = \frac{C_{ox} \omega K (V_{gs} - V_t - \frac{V_{ds}}{2})}{K/2}$$

$$= C_{ox} \omega (V_{gs} - V_t - \frac{V_{ds}}{2}) / \mu E$$

$$= C_{ox} \omega (V_{gs} - V_t - \frac{V_{ds}}{2}) \mu \frac{V_{ds}}{L}$$

$$\boxed{I_{ds} = \mu_n C_{ox} \frac{\omega}{L} (V_{gs} - V_t - \frac{V_{ds}}{2}) V_{ds}}$$

$$\text{Let } \mu_n C_{ox} \frac{\omega}{L} = \beta$$

$$\therefore \boxed{I_{ds} = \beta (V_{gs} - V_t - \frac{V_{ds}}{2}) V_{ds}} \rightarrow I_{ds} \text{ for linear region}$$

$V_{ds} < V_{gs} - V_t$

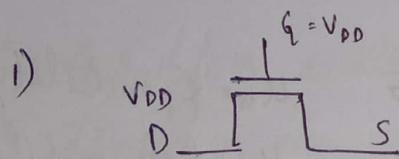
for saturation region,

$$V_{ds} = V_{gs} - V_t$$

$$\boxed{I_{ds} = \frac{\beta (V_{gs} - V_t)^2}{2}}$$

for cut off region,  $\boxed{I_{ds} = 0}$

Pass transistor logic:



i) Let S be at  $+V_{DD}$ .

$$V_{gs} = V_g - V_s = V_{DD} - V_{DD} = 0$$

ii) Let  $V_s = V_{DD} - V_{th}$ .

$$V_{gs} = V_g - V_s = V_{DD} - V_{DD} + V_{th}$$

$$V_{gs} = V_{th}$$

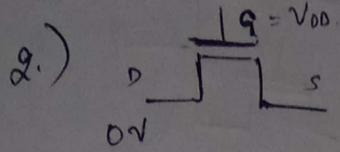
n MOS is ON.

But when  $V_g = V_{DD}$ , n mos should be on which is not in this case. Hence  $V_s \neq V_{DD}$  given

$$V_g = V_{DD}$$

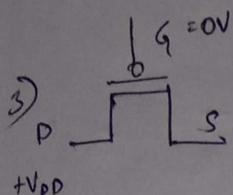
∴ If  $V_g = V_D = V_{DD}$ ,  $V_s$  is to be at  $V_{DD} - V_{th}$ .

\* n MOS conducts bad '1' since when  $V_D = V_{DD}$  given  $V_g = V_{DD}$ ,  $V_S$  cannot be  $V_{DD}$



Let  $V_D$  be at or given  $V_g$  at  $V_{DD}$ .

i) If  $V_S > 0V$ ,  $V_{GS} = V_g - V_S = V_{DD} - 0 = V_{DD}$ , n MOS is 'ON'.  
 $\therefore$  n-MOS conducts good '0'.

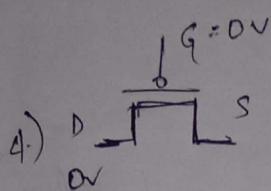


When  $V_D = V_{DD}$ ,  $V_g = 0$ . If  $V_S > V_{DD}$

$$V_{GS} = V_g - V_S = 0 - V_{DD} = -V_{DD}$$

p MOS is ON.

$\therefore$  PMOS conducts good '1'.



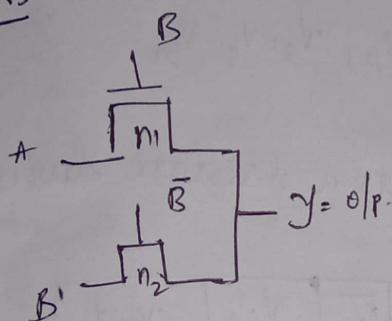
When  $V_D = 0V$ ,  $V_g = 0V$ . If  $V_S = |V_{tp}|$

$$V_{GS} = V_g - V_S = 0 - |V_{tp}|$$

$$= -|V_{tp}|$$

$\therefore$  PMOS conducts bad '1'

AND



| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

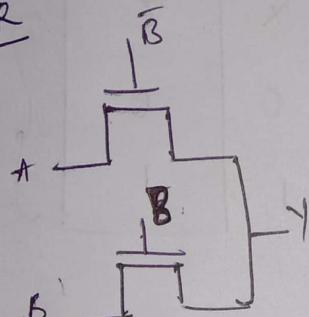
Eg: A=0, B=1.

n<sub>1</sub>=ON

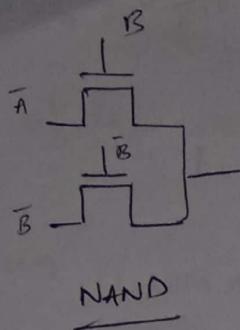
n<sub>2</sub>=OFF

A appears at o/p.

OR

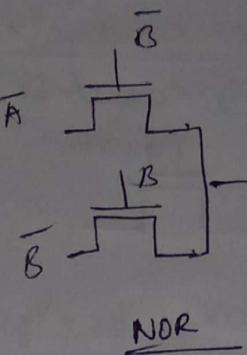


| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |



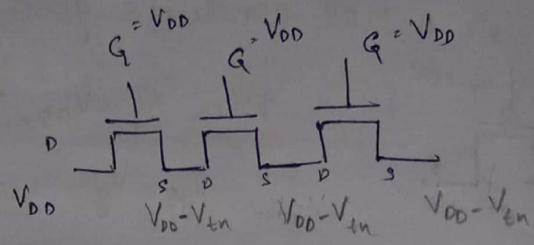
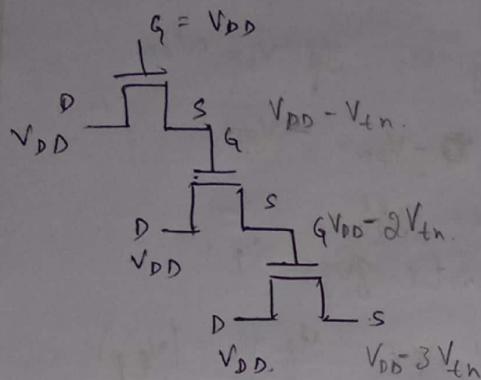
| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

NAND



| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

NOR

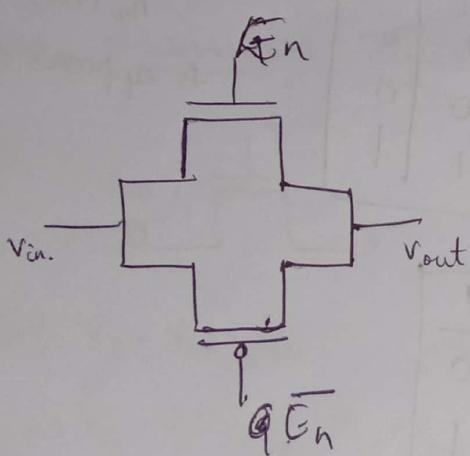


$V_{DD} - 3V_{tn}$

\* Provided gate & drain vlg same, then ~~itself~~ <sup>only</sup>  $V_S$  will be  $V_{DD} - V_{tn}$ .

\*  $V_D < V_g$ ,  $V_S = V_D$ . \*  $V_g < V_D$ ,  $V_S = V_g - V_{tn}$ .

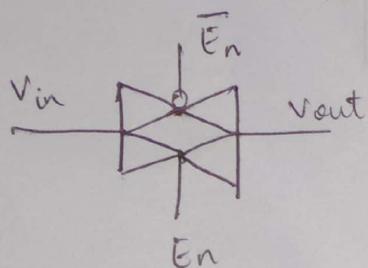
\* TG is a tristate device.



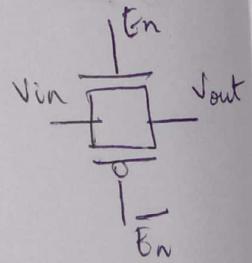
| En  | $\bar{En}$ | Vin | Vout |
|-----|------------|-----|------|
| 0/1 | X          | Z   | Z    |
| 1/0 | 0          | 0   | 0    |
| 1/0 | 1          | 1   | 1    |

} 3 states

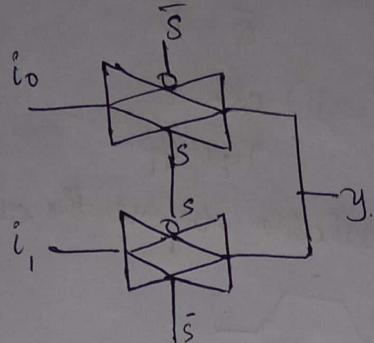
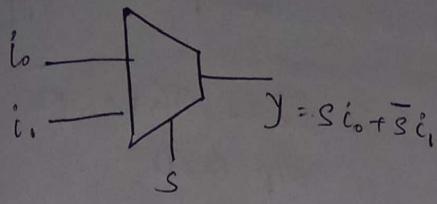
Transmission gate (TG)



Symbol of TG (6)



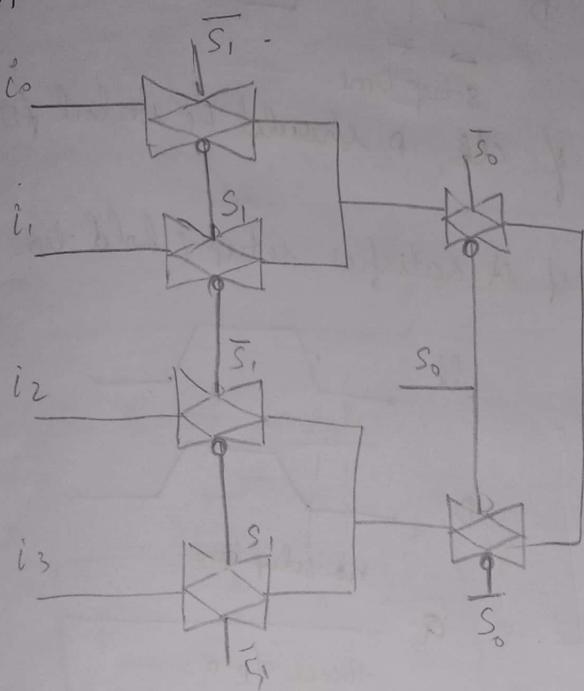
## Multiplexer using TG:



$$S=0, y=i_0$$

$$S=1, y=i_1$$

4<sup>th</sup>



| $S_0$ | $S_1$ | $y$   |
|-------|-------|-------|
| 0     | 0     | $i_0$ |
| 0     | 1     | $i_1$ |
| 1     | 0     | $i_2$ |
| 1     | 1     | $i_3$ |

$$y = S_0 S_1 i_0 + S_0 \bar{S}_1 i_1 + \bar{S}_0 S_1 i_2 + \bar{S}_0 \bar{S}_1 i_3$$

$S_1=0 \quad \bar{S}_1=1 \quad i_1, i_3 \text{ ON}$

$S_0=0 \quad \bar{S}_0=1 \quad i_3 \text{ ON}$

$S_1=1 \quad \bar{S}_1=0 \quad i_0, i_2 \text{ ON}$

$S_0=0 \quad \bar{S}_0=1 \quad i_2 \text{ selects}$

$S_1=0 \quad \bar{S}_1=1 \quad i_1, i_3 \text{ ON}$

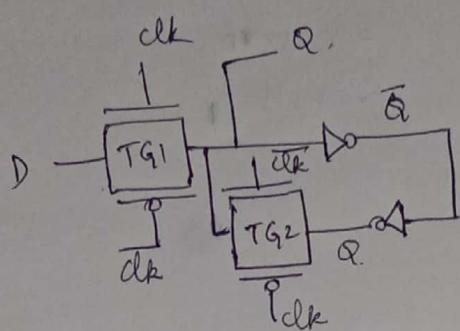
$S_0=1 \quad \bar{S}_0=0 \quad i_1 \text{ selects}$

$S_1=1 \quad \bar{S}_1=0 \quad i_0, i_2 \text{ ON}$

$S_0=1 \quad \bar{S}_0=0 \quad i_0 \text{ selects}$

D-latch using TG:

clock  $\rightarrow$  0/p changes. w.r.t 0/p  
 level sensitive flip-flops are latch.  
 Master Slave " " are pulse triggered



i)  $Clk = 1, TG1 = ON$

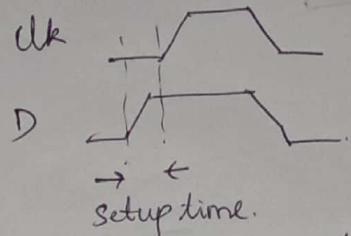
$$0/p = Q = D$$

$$\bar{Q} = \bar{D}$$

ii)  $Clk = 0$

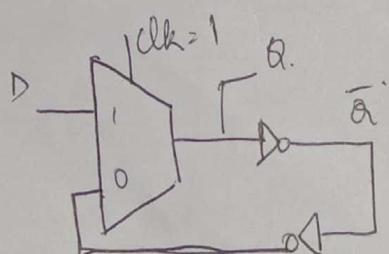
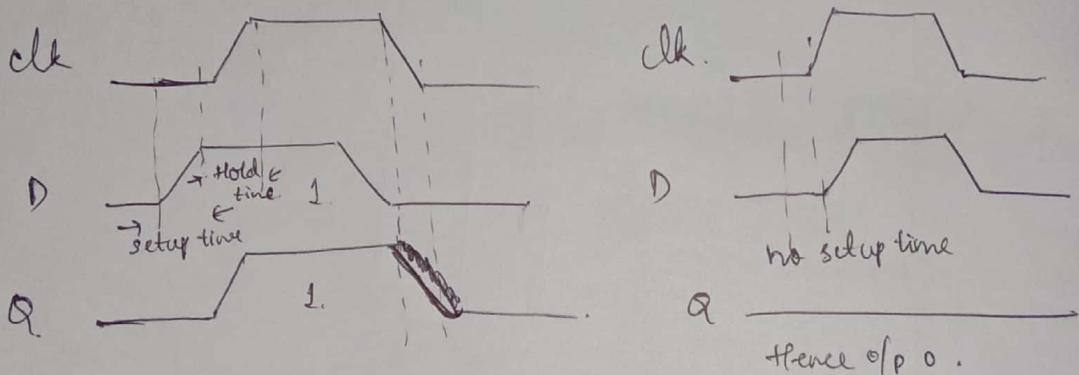
$TG1 = OFF$

Setup time  $\rightarrow$  min. D that is available before the clock comes.

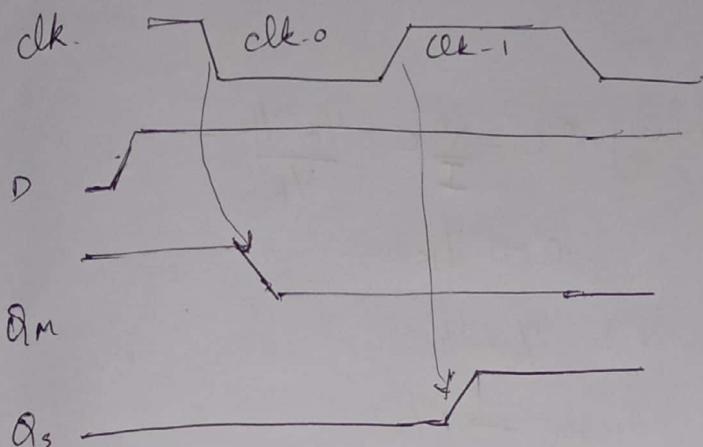
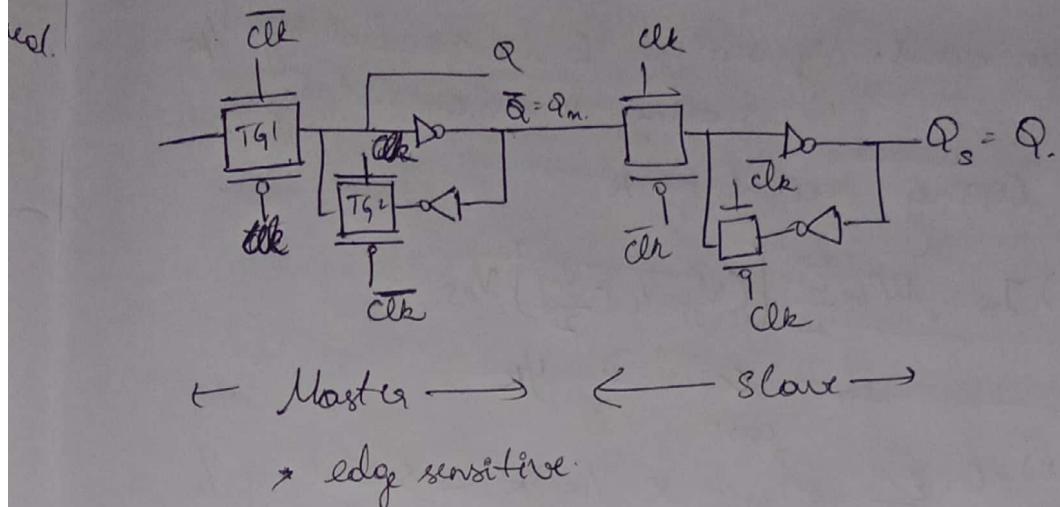


Hold-time: after appln of clk, Q should be valid for some time.

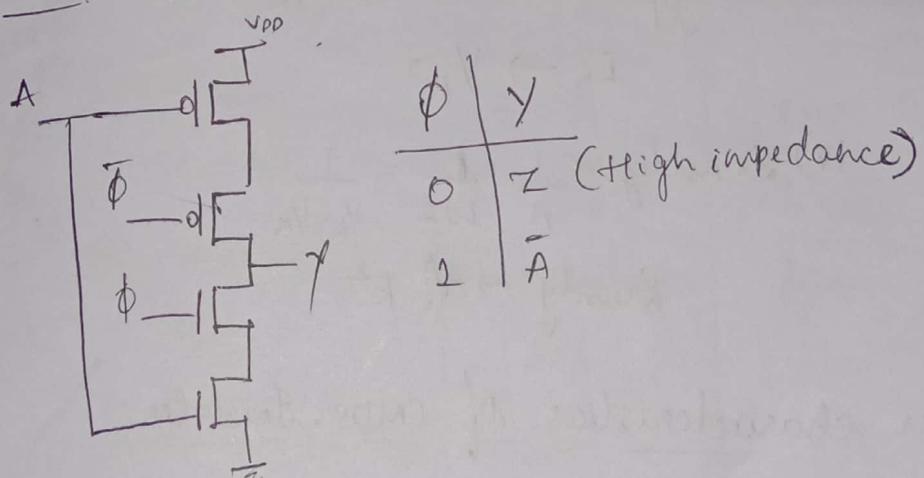
0/p of Q appears only if it satisfies setup & hold-time



## D-flip flop:



## Tri-state CMOS inverter:



Fabrication: Refer T.D.

- Scaling:
- i) Constant electric field scaling,  $L=1$ .
  - ii) Constant voltage scaling,  $V=1$
  - iii) Generalized scaling.

- a) Linear dimensions,  $- l, w, t_{ox}, x_j$  are scaled by  $\frac{1}{k}$   
 where  $k > 1$ ; let  $k = 2$ .
- b) In const.  $V_g$  scaling,  $E$  is scaled by  $\frac{1}{k}$   
 in "  $E$  scaling,  $V$  is scaled by  $\frac{1}{k}$
- c) Doping scaled by  $k$ .

Device

$$\left\{ \begin{array}{l} d) I_D = \mu C_{ox} \frac{W}{L} \left[ (V_{gs} - V_t) - \frac{V_{ds}}{2} \right] V_{ds} \\ \quad I_D \rightarrow \text{scaled by } \frac{1}{k} \\ e) C = \frac{\epsilon A}{d} = \cancel{\left( \frac{\epsilon}{d} \right)} \frac{w \cdot L}{t_{ox}} \propto \frac{1/k}{1/k} \rightarrow \text{scaled by } \frac{1}{k} \end{array} \right.$$

Circuit performance:

i)  $\tau = \text{delay} = R_C = \frac{V}{I} C = \frac{1/k}{1/k} \frac{1/k}{1/k} = C \rightarrow \frac{1}{k}$

ii) Power =  $V \cdot I = \frac{1}{k} \cdot \frac{1}{k}$

Power  $\rightarrow \frac{1}{k^2}$

iii) Energy = Power  $\cdot \tau = \frac{1}{k} \cdot \frac{1}{k}$

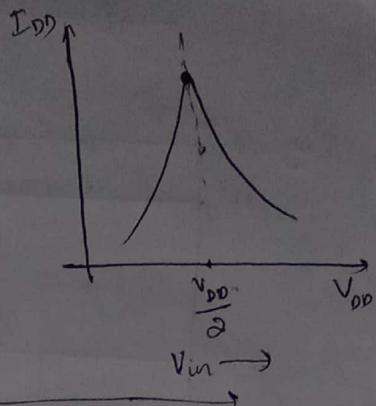
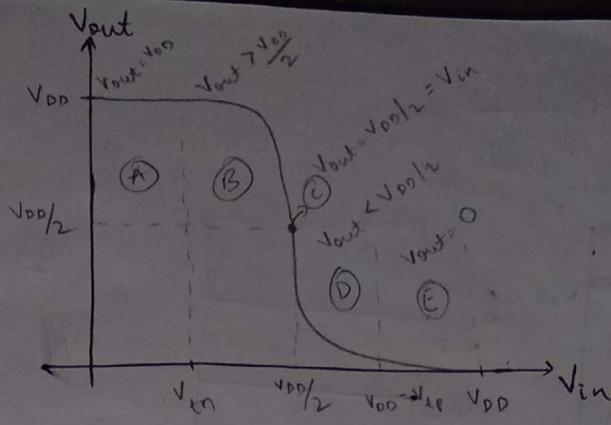
Energy  $\rightarrow \frac{1}{k^3}$

iv) Density  $\propto \frac{1}{A} = \frac{1}{wL} = \frac{1}{1/k \cdot 1/k}$

Density  $\rightarrow \frac{1}{k^2}$

DC-Transfer characteristics of CMOS-Inverter:

scaled by  $\frac{1}{k}$



n-mos.

Cut-off

$$V_{gs} < V_{tn}$$

$$V_{in} < V_{tn}$$

Linear

$$V_{gs} > V_{tn}$$

$$V_{in} > V_{tn}$$

$$V_{ds} < V_{gs} - V_{tn}$$

$$V_{out} < V_{in} - V_{tn}$$

Saturation

$$V_{gs} > V_{tn}$$

$$V_{in} > V_{tn}$$

$$V_{ds} > V_{gs} - V_{tn}$$

$$V_{out} > V_{in} - V_{tn}$$

p-mos.

$$V_{gs} > V_{tp}$$

$$V_{in} > V_{tp} + V_{DD}$$

$$\begin{aligned} \therefore V_{gs} &> V_{tp} \\ V_g - V_s &> V_{tp} \\ V_{in} - V_{DD} &> V_{tp} \\ V_{in} &> V_{DD} + V_{tp} \end{aligned}$$

Regions

$$V_{gs} < V_{tp}$$

$$V_{in} < V_{tp} + V_{DD}$$

$$V_{DS} > V_{gs} - V_{tp}$$

$$V_{out} > V_{in} - V_{tp}$$

$$(V_{out} > V_{DD})$$

n MOS

$$V_{gs} < V_{tp}$$

$$V_{in} < V_{tp} + V_{DD}$$

$$V_{ds} < V_{gs} - V_{tp}$$

$$V_{out} < V_{in} - V_{tp}$$

$$(V_{out} < V_{DD})$$

p MOS

(A)

$$0 < V_{in} < V_{tn}$$

cut off

linear

Assume

$$V_{DD} = 3V$$

$$V_{tn} = |V_{tp}| = 0.3V$$

& compare

(B)

$$V_{in} < V_{in} < V_{DD}/2$$

$$\begin{aligned} V_{gs} &< V_{DD}/2 \\ V_{gs} &> V_{DD}/2 \end{aligned}$$

Saturation

linear

(C)

$$V_{DD}/2$$

Sat

sat

(D)

$$V_{DD}/2 < V_{in} < V_{DD} - V_{tp}$$

linear

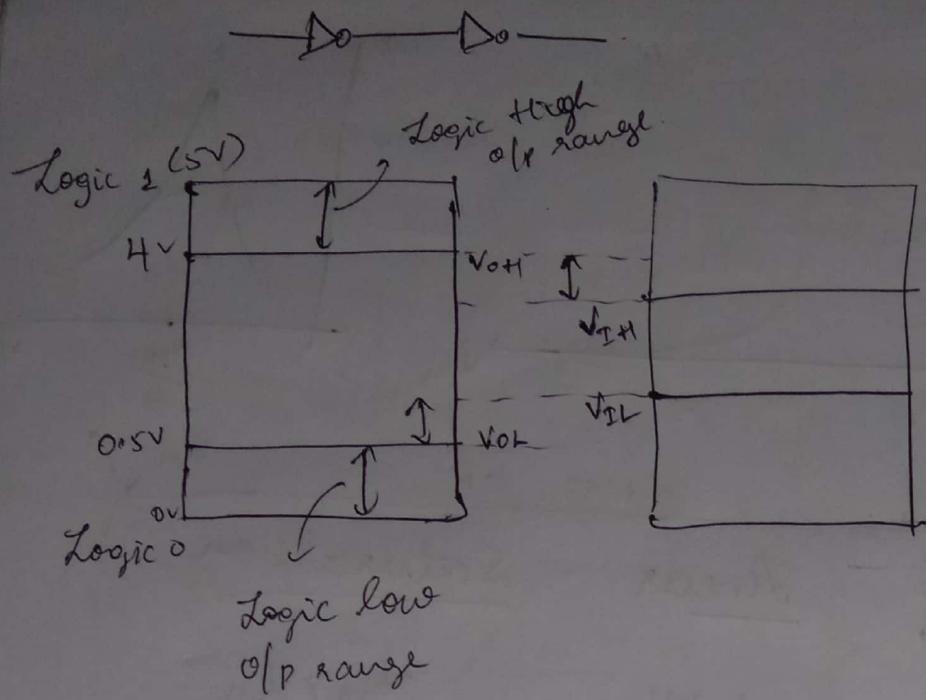
Sat

(E)

$$V_{DD} - V_{tp} < V_{in} < V_{DD}$$

linear

cut off



$$V_{IL} - V_{OL} = \text{Noise margin (L)}$$

$$V_{OH} - V_{IH} = \text{Noise Margin (H)}$$

For the inverter ckt,  $V_{O1}$  is the o/p vtg of inverter 1 &  $V_{I2}$  i/p vtg to inverter 2. Both inverters have following characteristic.  $V_{IL} = 1.3 \text{ V}$ ,  $V_{IH} = 3.15 \text{ V}$ ,  $V_{OL} = 0.29 \text{ V}$ ,  $V_{OH} = 3.84 \text{ V}$

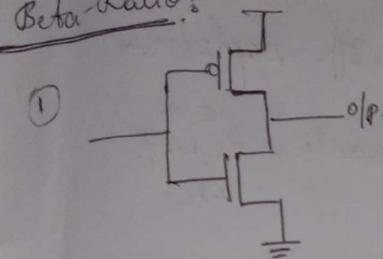
What are the inverter's low & high noise margin.  
Can the ckt tolerate 1V of noise b/w  $V_{O1}$  &  $V_{I2}$ ?

$$NM_H = V_{OH} - V_{IH} = 3.84 - 3.15 = 0.69 \text{ V}$$

$$NM_L = V_{IL} - V_{OL} = 1.3 \text{ V} - 0.29 = \cancel{0.95} \quad 1.01 \text{ V}$$

Since  $NM_H$  is in range of 1V, high vtg can be transferred. but  $NM_L$  is  $> 1\text{V}$ , low vtg cannot be transferred.

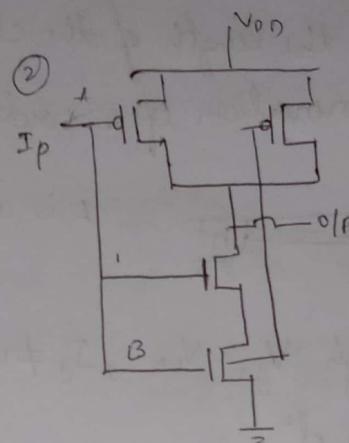
Beta-Ratio:



$$\beta_P = \beta_N$$

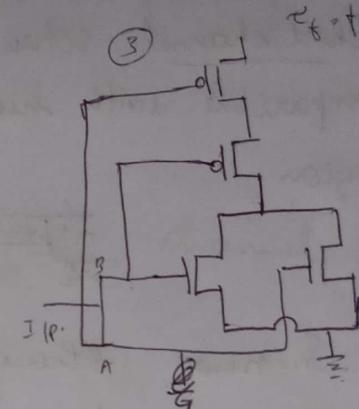
$$\frac{\beta_P}{\beta_N} = 1$$

$$\tau_n = \tau_f$$



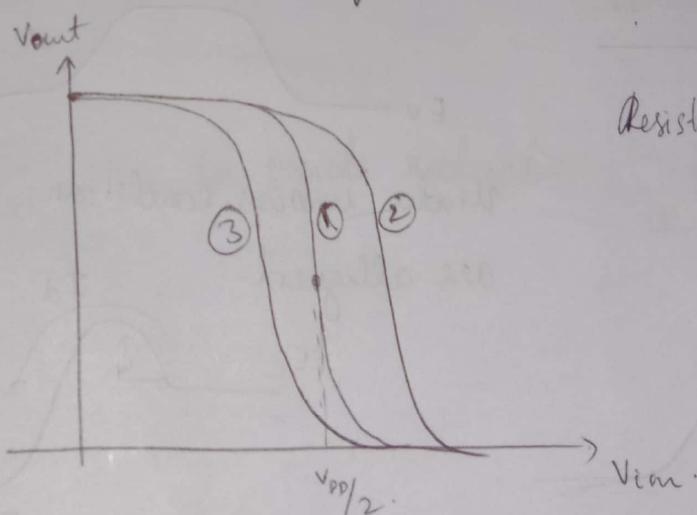
$$\frac{\beta_P}{\beta_N} = 2$$

$$\tau_n < \tau_f$$



$\tau_n$  = rise time  
 $\tau_f$  = fall time

$$\tau_n > \tau_f$$

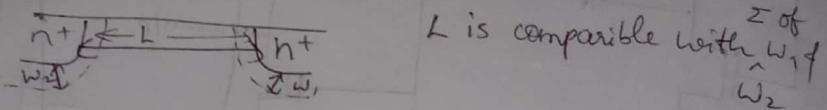


Resistance & Length

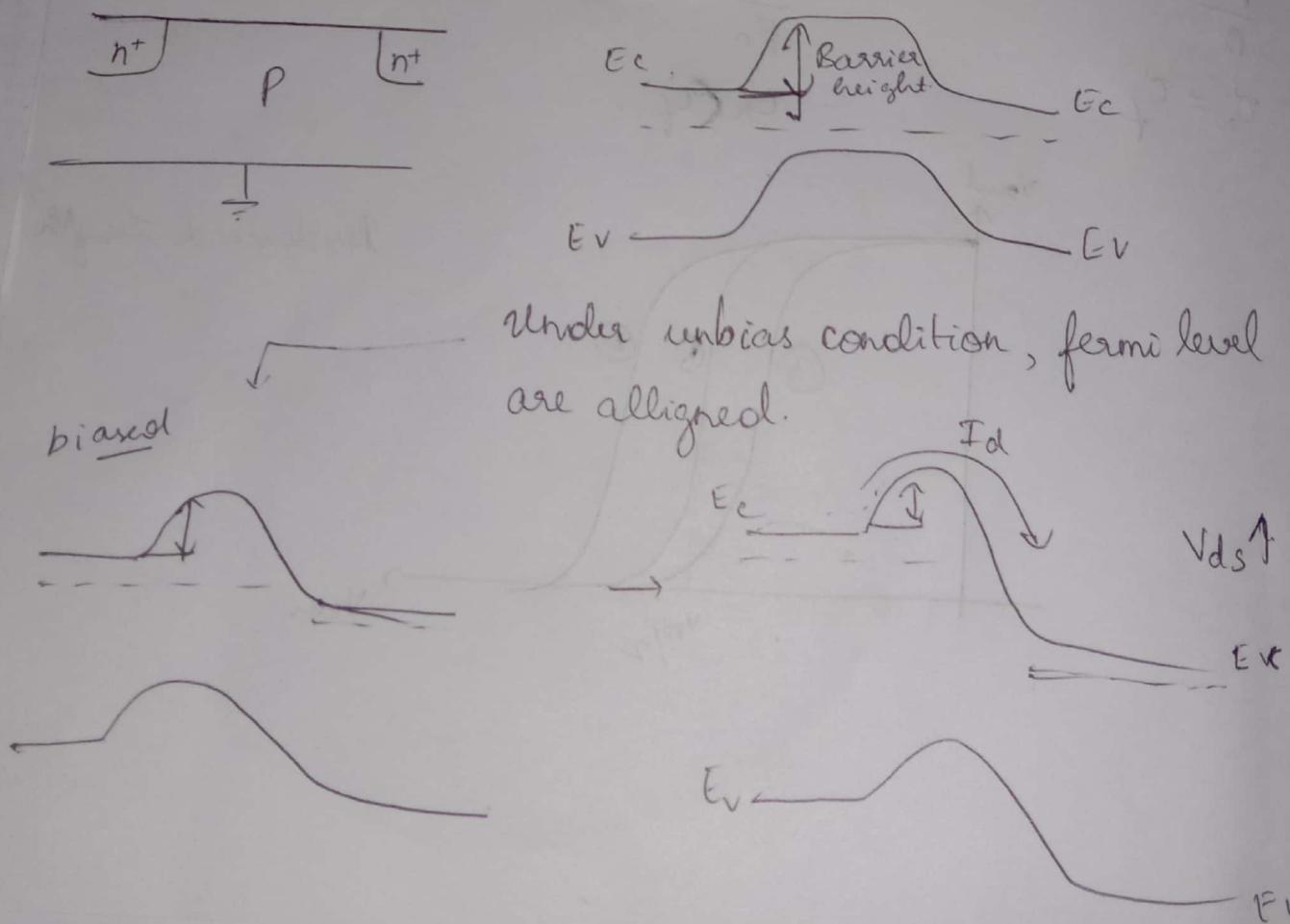
Non-Ideal IV characteristics: (secondary effects)  
are w.r.t short-channel transistor

- Logic 1  
H.v  
0.5  
Logic  
Base
- a.) Channel length modulation.
- b.) Body effect.
- c.) Velocity saturation & Mobility degradation.
- d.) Junction leakage.
- e.) Tunnelling.
- f.) Temperature effect.
- g.) Subthreshold conduction.

Short channel: When the length of the channel is comparable with summation of 2 width of depletion region



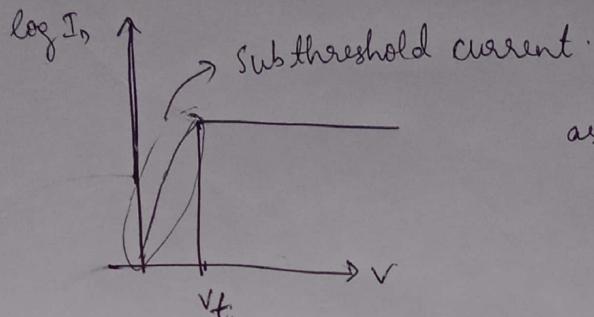
Suppose, In nmos, Although  $V_{gs} < V_{th}$ ,  $I_d \neq 0$ , this is known as subthreshold condn.



- \* conduction starts as we increase  $V_{ds}$  from 0 to +
- \* At source, the barrier height is very less, some charge carriers flow from S to D which constitutes current.  
i.e., even when  $V_{gs} < V_{th}$ ,  $I_D \neq 0$ .

→ DIBL (Drain induced barrier lowering): as  $V_{ds} \uparrow$ , Barrier near Source decreases.

$$I_{os} = I_{D_s} e^{\frac{V_{gs}-V_t}{kT}} \left[ 1 - e^{-\frac{V_{ds}}{kT}} \right]$$

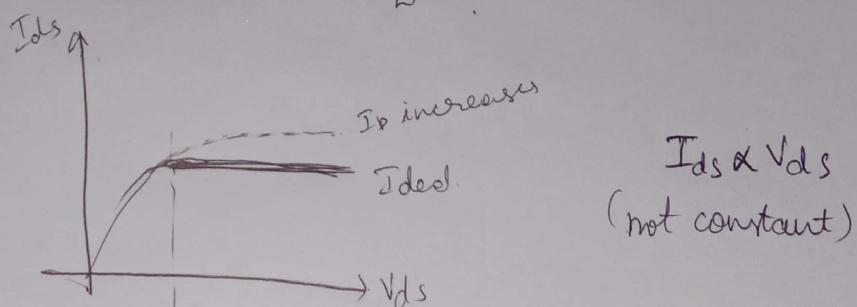


as  $V_t$  decreases, there is current flowing.

### Channel length modulation:

As  $V_{ds} \uparrow$  i.e., at  $V_{ds} > V_{gs} - V_{th}$ , channel length increases & reduces.

$$\text{Diagram of channel length modulation: } L_{eff} = L - \Delta L$$



Tunneling: Due to oxide reduction,  $I_g$  is constituted & flows into channel.