DIGITAL LOGIC DESIGN

Course Code - Category: CSE 114 - ES **Credits:3**

L	T	P	E	O
3	0	0	1	3

Sessional Marks:40

End Exam: 3 Hours End Exam Marks:60

Course Outcomes:

By the end of the course student should be able to:	
CO1	Perform number conversions between different number systems and codes and apply Boolean algebra to minimize logic expressions up to three variables.
CO2	Apply K-map method, tabulation method to minimize logic expressions up to four variables and design a combination logic circuit like decoders, encoders, multiplexers, and de-multiplexers etc. for a given specification and verify the correctness of the design.
CO3	Implement the given Boolean functions (upto four variable) using Programmable logic devices.
CO4	Analyze the operation of sequential circuits built with various flip-flops by finding the Boolean function or truth table and design various sequential circuits like registers, counters etc.
CO5	Design and Analyze synchronous and asynchronous sequential circuits as per given specifications.

SYLLABUS

UNIT-I **9 periods**

Digital Systems, Boolean Algebra and Logic Gates

Digital Systems, Binary Numbers, Number Base Conversions, Complements of numbers, Signed Binary Numbers, Binary Codes, Binary Logic. Basic Definitions, Axiomatic Definition of Boolean Algebra, Basic Theorems and Properties of Boolean Algebra, Boolean Functions, Canonical and Standard Forms, Different Logic Operations, Digital Logic Gates.

UNIT-II **9 periods**

Gate-Level Minimization

The Map Method, Four variable K-map, POS simplification, Don't-Care Conditions, NAND and NOR Implementation.

Combinational Logic

Combinational Circuits, Analysis Procedure, Design Procedure, Binary adder-subtractor circuit, Decimal adder circuit, Binary Multiplier, Magnitude Comparator, Decoders, Encoders, Multiplexers, Demultiplexers.

UNIT-III **9 periods**

Programmable Logic Devices

Programmable Logic Devices : PROM, PLA, PAL, realization of switching functions using PROM, PLA and PAL; comparison of PROM, PLA and PAL, Programming tables of PROM, PLA and PAL.

UNIT-IV **9 periods**

Sequential logic circuits

Sequential Circuits, Latches, Flip-Flops, Analysis of Clocked Sequential Circuits, Flip-Flop Conversions.

Registers and Counters

Registers, Shift Registers, Ripple Counters, Synchronous Counters, Johnson and Ring counters.

UNIT V **9 periods**

Synchronous Sequential Logic

Basic Design Steps, Serial Adder Example, State Reduction & Assignment Problem. **Asynchronous Sequential Logic**

Introduction, Analysis Procedure, Design Procedure, reduction of state and flow table.

Text Books:

1. **M. Morris Mano** *"Digital Design"* 3rd Edition, Pearson Publishers, 2001.
2. **Z Kohavi** *"Switching and Finite Automata Theory"* 2nd edition, TMH, 1978

Reference Books:

1. **William I. Fletcher** "*An Engineering Approach to Digital Design"* PHI, 1980.
2. **John F. Wakerly** "*Digital Design Principles and Practices*" 3rd Edition,Prentice Hall, 1999.
3. **Charles H Roth Jr and Larry L. Kinney** *"Fundamentals of Logic Design"* Cengage learning, 7th Edition, 2013
4. **R.P Jain** "*Modern Digital Electronics*" 3rd Edition, TMH, 2003.