Final Year Project review

Madhu Varshan

Objective:

- To simulate randon patterns using Pseudo Random Pattern generator with LFSR and transmit it using a channel having white guassian noise and calculate the error produced using a pattern matcher having error count register

Elements:

- lsfr module
- main module(this has connection with the above top layers)
- serializer module
- CDC module
- synchronizer module
- define module

PATTERN GENERATOR

noisy channel

- contains a pattern matcher curcuit inside it
- deserializer
- CRC checker
- define modules
- Main module
- Error count module

PATTERN MATCHER

Progress after 1st review

- Completed code for the following modules:
  a. Sychronizer
  b. Serializer
  c. Pattern generator main module
  d. CRC generator
  e. Error count
  f. Active white gaussian noise channel
- Research paper went through:
  - G. Castagnoli, S. Brauer and M. Herrmann, "Optimization of cyclic redundancy-check codes with 24 and 32 parity bits,"

Works for this week:

- Syncronize all the modulle that has been generated so far
- Test the simulation using Quartus software
- Go through the company tools for simulation

Works for next week:

- Go through SPYGLASS software for simulations
- Create the module for pattern matcher
- Integrate all three modules