VISVESVARAYA TECHNOLOGICAL UNIVERSITY

BELAGAVI-590 018

A Seminar Report on

"TRANSFORMER LESS GRID TIE PHOTOVOLTAIC INVERTER USING DUAL STAGE BOOST AND BUCK CONVERTERS"

Submitted for partial fulfillment of the requirement for the award of the degree of

Bachelor of Engineering

in

Electrical and Electronics Engineering

Submitted by

Name	USN
MADHU GOWDA H K	**4AD18EE015**

Under the Guidance of

Dr. Sathish K R, ME, Ph.D.

Assistant Professor, Department of EEE, ATMECE, Mysuru

Department of Electrical and Electronics Engineering

ATME COLLEGE OF ENGINEERING

13 KM STONE, MYSURU KANAKAPURA BENGALURU ROAD, MYSURU-570028

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ATME College of Engineering, Mysuru-570028

Department of Electrical and Electronics Engineering

CERTIFICATE

Certified that the seminar titled **"TRANSFORMER LESS GRID TIE PHOTOVOLTAIC INVERTER USING DUAL STAGE BOOST AND BUCK CONVERTERS"** presented by **MADHU GOWDA H K: 4AD18EE015** is a **bonafide** student of **ATME College of Engineering, Mysuru -570028.**

The presentation is in partial fulfilment for the award of **Bachelor of Engineering** in **Electrical and Electronics Engineering,** of the **Visvesvaraya Technological University, Belagavi - 590018 during** the year 2021-2021. It is certified that all corrections/suggestions indicated for the Internal Assessment have been incorporated in the report deposited in the departmental library. The Seminar report has been approved as it satisfies the academic requirements in respect of work prescribed for the said Degree.

Dr. Sathish K R	Dr. Parthasarathy L	Dr. L Basavaraj
Internal Guide	**Head of the Department**	**Principal**

External Examiners

Name of the Examiner	**Signature with Date**
1.	
2.	

DECLARATION

I, **MADHU GOWDA H K: 4AD18EE015** student of VIII semester, **Department of Electrical and Electronics Engineering**, **ATME College of Engineering, Mysuru-570018** declare that the Seminar titled **"TRANSFORMER LESS GRID TIEPHOTOVOLTAIC INVERTER USING DUAL STAGE BOOST AND BUCK CONVERTERS"** has been successfully completed. This work is submitted to **Visvesvaraya Technological University, Belagavi-590018**, in partial fulfillment of the requirements for the award of Degree of **Bachelor of Engineering in Electrical and Electronics Engineering** during the academic year 2021-2022.

Name	USN	Signature with date
MADHU GOWDA H K	**4AD18EE015**	

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MADHU GOWDA H K 4AD18EE015

ABSTRACT

Due to swift growth of photovoltaic (PV) power generation, highly efficient and cost effective pure sine wave inverters are greatly demanded in the local market. This thesis paper explores a topology for transformer less pure sine wave grid tie photovoltaic inverter for residential application using dual-stage Boost converter. My proposed gird tie inverter employs dual-stage switch mode boost converter, dual-stage switch mode buck converter, an H bridge inverter, and a T-LCL Immittance conversion circuit. The switching technique of proposed inverter consists with a combination of sinusoidal pulse width modulation (SPWM) and square wave along with grid synchronization condition. As the suggested method is entirely transformer less, it ridiculously reduces total harmonic distortion (THD) which is less than0.1%, minimizes size and swells inverter efficiency up to 97%. T-LCL Immittance conversion circuit provides a nearly constant output current which stabilize system rapidly and reduces harmonics generated by inverter. Overall performance of the proposed inverter is simulated through the PSIM. The simulation results are analysis through PSIM and MATLAB software. The results of simulation show that this new method can be eliminated vast harmonics and is highly efficient. Therefore it may able to meet the challenges of power crises in Bangladesh.

The photovoltaic inverter is one of the most important elements of the solar photovoltaic systems. In the last years the transformer less grid connected inverters are preferred for photovoltaic applications. The current paper aims to present an analysis of a new topology of this type of inverters, as well as to prove its operating ability and control of the process of injecting of solar power from photovoltaic panels into utility grid. The topology is based on theoretical model which is not investigated in details till now. This topology is symmetric with flying inductor and can be implemented in inverters that are able to operate in all modes buck boost and boost in both half-waves, as well as in some combinations of them. Also it has a possibility to change the behavior in dependence of the grid voltage.

Keywords: boost and buck converters , voltage divider , T-LCL immittance converter , grid tie inverter(GTI)

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CHAPTER 1

INTRODUCTION

1.1 Background

With the world energy demand increasing at an exponential rate, the search for energy sources other than fossil fuels is no longer a luxury. Although the fossil fuels offer a temporary solution to this energy crisis, they cause the emission of carbon dioxide and other greenhouse gases, which are harmful to the environment. This has paved the way for research on renewable energy technology and other researches in the fields of power electronics and hence, the cost of utilizing the renewable energy is at an ever decreasing rate.

One such source of renewable energy, the Sun, offers unlimited energy for harnessing and for this very reason, Photovoltaic (PV) systems consisting of PV modules, for generating environmental friendly power are gaining more and more recognition with each passing day. The PV modules comprise of several solar cells, which convert the energy of the sunlight directly into electricity, and are connected as required to provide desired levels of DC current and voltage. They produce electricity due to a quantum mechanical process known as the "photovoltaic effect".

The major drawback with these PV systems is that their cost is much high compared to the conventional sources such as fossil fuels and their efficiency are also quite low. Power semiconductor devices represent the heart of the modern power electronics, and are being extensively used in power electronic converters in the form of a matrix of on or off switches, and help to convert power from one form to another. There are four basic conversion functions that normally can be implemented such as AC to AC, AC to DC, DC to AC and DC to DC. Inverter is one of the converter families which are called DC to AC converter. It converts DC power to AC power to a symmetric AC output voltage at desired magnitude frequency. .

Inverter is widely used in industrial applications such as variable. speed AC motor drives, induction heating, standby power supplies and uninterruptible power supplies. The DC power input of inverter is obtained from the existing power supply network. digitize the power so that a sequence of voltage pulses can be generated by the on and off of the power switches.

The pulse width modulation inverter has been the main choice in power electronic for decades, because of its circuit simplicity and rugged control scheme. SPWM switching technique is commonly used in industrial applications . SPWM techniques are characterized by constant amplitude pulses with different duty cycle for each period. The width of this pulses are modulated in order to obtain inverter output voltage control and to reduce its harmonic.

In this proposed paper, recommended PV configuration consists of five main components:
1) a PV array for energy conversion solar to electrical,
2) dual-stage DC-DC boost converterwith MPPT,
3) an H-bridge DC-AC inverter to acquire AC voltage,
4) a T-LCL immittance converter to deliver a nearly constant output current
5) dual-stage AC-DC buck converter which is used at gate signal by combining SPWM and square wave for switching of inverter shown in Fig.1.1.

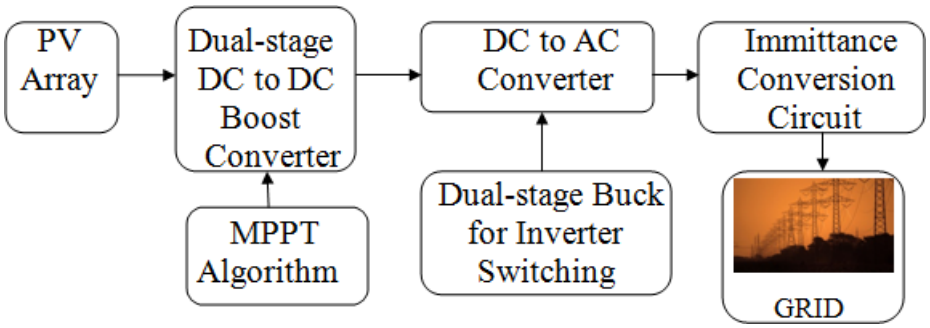


Fig. 1.1: Block diagram of transformer less GTI

1.2 Problem Statement

Inverter is one of power conversion device that widely used in the world to convert DC input voltage to AC output voltage. The output voltage waveforms of ideal inverters should be sinusoidal. However, the waveform of practical inverter is non-sinusoidal and contains harmonics. Then, for this project, it should get closer sinusoidal waveform within +- 1% harmonics contains. Harmonic contents in inverter output depends more to number of pulses per cycle. As an example, square wave switching method will produce more harmonic contents in inverter output compared to pulse width modulation switching technique.

This is due to number of pulses per cycle of pulse width modulation can be modified on thefrequency of triangular carrier waveform. The frequency of triangular waveform can be modified from lower frequency to higher frequency. If higher frequency is used, the number of pulses per cycle also increased and at the same time it will reduce the harmonic contents of the inverter. In switching losses problem, the number of pulses per cycle also affected. The use of high switching technique will contribute to the high power losses and it also needs to take care on
the inverter switching design.

The following factors are to be considered in order to meet the Requirements.

Factors:

i. Cost of equipment
ii. Size filter
iii. Total harmonic distortion
iv. Power loss in switching elements

In order to fulfill the requirement, the new switching technique had been analyzed and recommended in this thesis, namely SPWM which is generated with combination of high frequency triangular wave and square wave. Then T-LCL filter is used which will be provided a nearly constant output current which stabilize system rapidly and reduces harmonics generated by inverter.

1.3 Objectives

The aim of this research is mainly to design and develop the SPWM switching pulse for single phase Grid-Tie Inverter (GTI) application. The main objectives of this research can be summarized as:

- To design and implement switching strategy for inverter application, which are simple, reliable, low cost and high efficiency.
- To use the power electronics simulation software, PSIM version 9.001 to simulate the designed circuits with variety switching conditions to obtain optimum performance
- To develop gate pulse switching of GTI with combination of SPWM and square wave To develop a complete prototype of inverter with 2500W power rating for photovoltaic application.

- To compare and analyze the simulated results
- As transformers are bulky, heavy weighted and expensive so the paper target is to implement an inverter circuit without transformer which will help to provide pure sine wave AC output voltage while maximizing efficiency and reducing the total harmonic distortion (THD).

1.4 Research Methodology

The methods that will use to finish this thesis are illustrated through the flow chart showninFig.1.2:

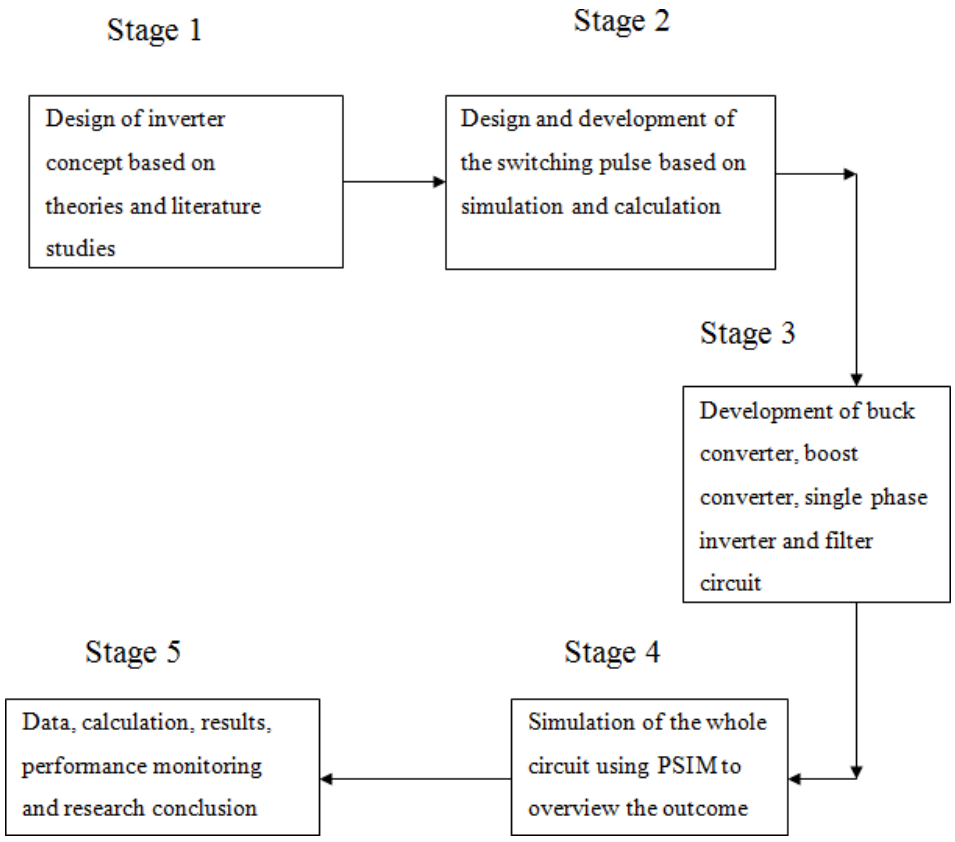


Fig. 1.2:Research Methodology1

1.5 Organization of this Report

This consists of five chapters. A short explanation is introduced here:

Chapter 1: Introduction

This chapter discuss about the issue relating to the background of the thesis objectives , methodology and research structure.

Chapter 2: Literature Review

This chapter discusses mainly about PV array, buck converter, boost converter, new technique of sinusoidal pulse width modulation, different inverter technique, converter topology, and application. Some of literature regarding this thesis topic is also included in this chapter.

Chapter 3: Design and circuit analysis

The Chapter 3 describes in detail the ideal Grid-Tie Inverter, design value and the circuit analysis of the DC-DC boost converter, DC-DC buck converter, T-LCL type immittance converter which includes the derivation of the input-output current and voltage equations and the efficiency equations.

Chapter 4: Simulation of Inverter

The chapter 4 will focus on mainly to the procedure, method, and theory implementation through simulation designing and of proposed PV inverter related to the thesis topic.

Chapter 5: Result and Discussion

The PV inverter is simulation tested, and verified. The tests include the efficiency of the designing DC-AC PV system and its performance.

Chapter 6: Conclusion

Finally, a conclusion on the obtained results is presented. This also includes the novelties within the work, and suggestions for future work.

CHAPTER-2
LITERATURE REVIEW

2.1 Analysis Design of PV Array

When sun rays diving into PV cell it converts solar energy into electricity. There exists two layer in a PV array, N-type layer and P-type layer, the two layers work together and generate electricity when photon exceeds band gap of solar cell. The equivalent circuit of a solar cell can be described as a current source is parallel with a diode and shown in Fig.2.1.

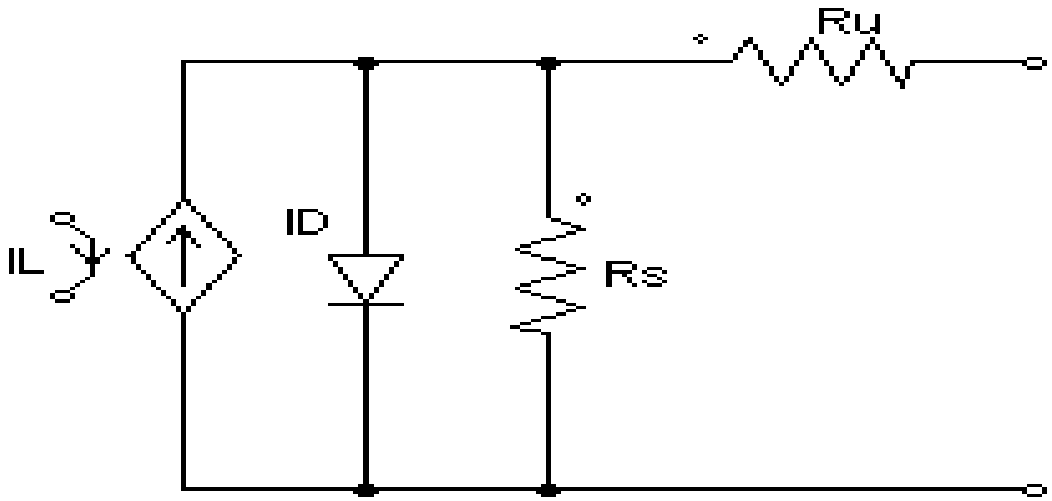


Fig .2.1:.Equivalent circuit of solar cell

This research discus the control algorithm of PV system by using simple model which ignoring insignificant voltage losses through series and parallel resistor of PV array, thus the V-I characteristics formula is simplified as following formula.

2.1 Photovoltaic system (PV) in Building Environment

Renewable energy sources (RES) are considered as a technological option for significantly contributing to the sustainable energy supply in Europe. PV energy generates electricity from solar radiation and, at present, represents one of the RES emerging technologies due to the continuous cost reduction and technological progress. The minimum element in the manufacturing of PV systems is the PV module. A typical panel is composed of 30–36 series-connected solar cells, with an open-circuit voltage (Voc) near 20 V and a short circuit current (Isc) around 3–4 A. For most applications, e.g., integration in building environment and autonomous applications, the power of one PV module is not enough.

As a result, it becomes necessary to group PV modules until the desired current and voltage levels are achieved. The efficiency of commercial PV modules is about 14%–16%. However, PV systems show additional losses that are important in many cases. If not considered during the PV design phase, unreal estimations will be foreseen, and public image of PV energy could be damaged.

Issues carried out by the University of Tokyo over 71 Japanese PV systems have shown losses of up to 25%. Causes are varied, ranging from load mismatching.
(although most PV systems have maximum power point tracking (MPPT) incorporated), differences in current–voltage (I–V) characteristics, shadows, dust, losses in PV inverter, low-radiation losses, and MPPT losses .

Various alternatives architectures for grid connected PV system configurations are available, such as centralized module, AC module and modular configuration where the last topology perfectly fits with an intelligent PV module concept. A few possible configurations of grid connected PV systems are shown in Fig.1. A centralized inverter configuration is illustrated in Fig. 2.2(a) that interfaced huge number of PV modules.

But, there are some severe limitations in the design of centralized inverters, such as power loss for using a central MPPT, PV modules with mismatch losses due to the high voltage dc cabling connecting the PV modules with the inverter, string diode loss etc. Fig. 2.2(b) shows the AC module configuration, which is a simplified version of the centralized inverter topology. A single string of PV module is connected with an inverter. Each string can be applied with a separate MPPT, as there is no loss attributed to string diodes. In comparison to the centralized inverter the overall efficiency is increased. Fig.2.2(c) shows the modular configuration. A common inverter is joined with multiple strings connected to individual DC-DC converter. The benefit of this modular configuration over centralized system is that each string can be controlled individually and ensure less cabling loss thereby enhancing the overall system efficiency.

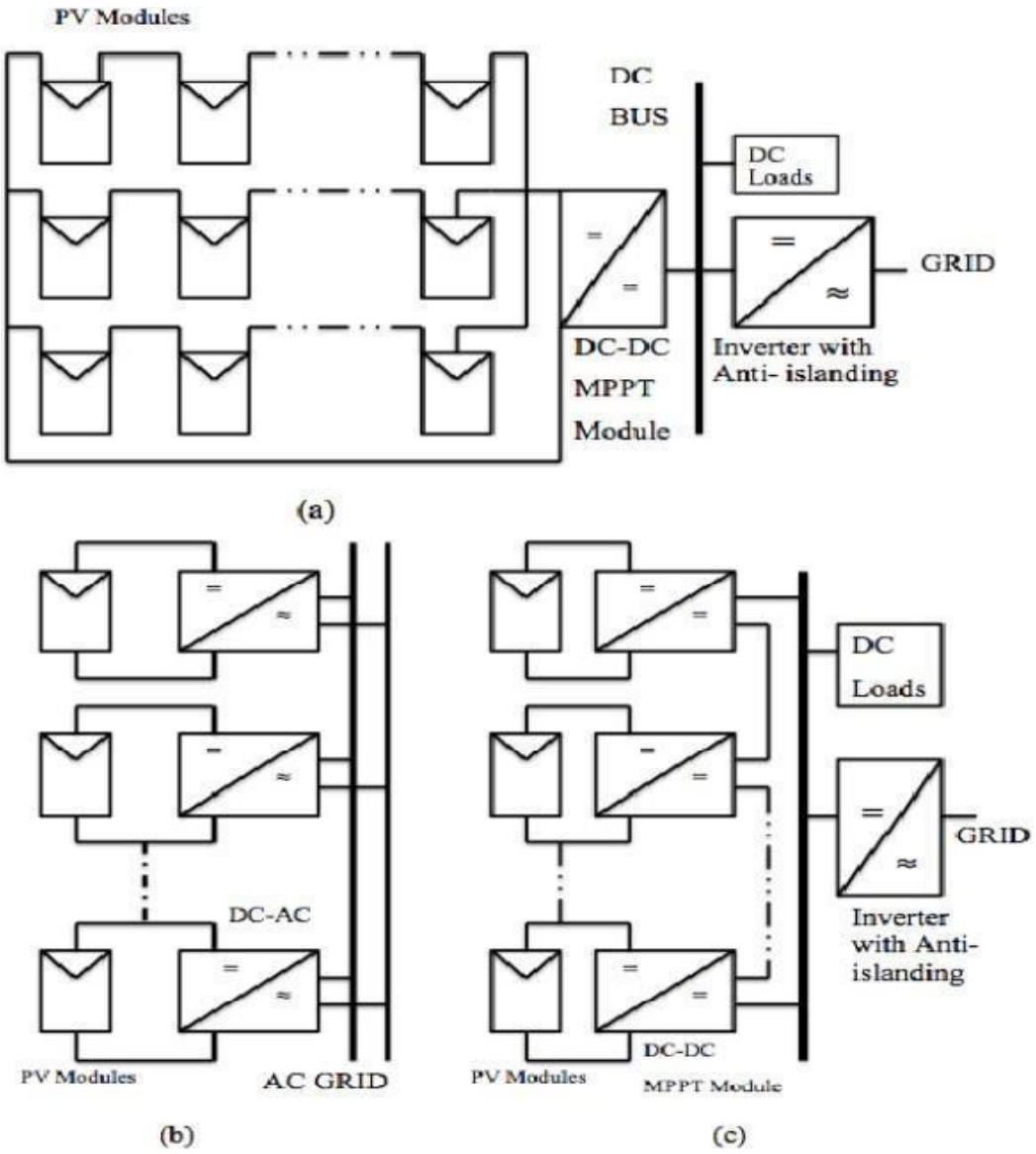


Fig.2.2. Grid connected PV system configurations (a) Centralized module (b) AC-Modules (c)Modular system

2.3 Control Strategy for MPPT Perturbation & Observation (P&O) Algorithm

There subsists different algorithm for MPPT design such as: Perturb -and-observe algorithm, Open and short circuit algorithm, Incremental conduction algorithm, Fuzzy logic algorithm among all algorithms P&O is one of the best because of its simple design and high reliability. It is just following "Trial and Error". The algorithm is driving periodically by compared output power with the previous cycle. Depending on output power perturbing cycle ether rises or fall.

If output power is increasing the cycle will continue by remaining unchanged and enters into the next cycle, else the perturbation cycle way will be reversed. Therefore array terminal voltage is perturbed for every MPPT cycle. Thus when maximum power is determined P&O will be started to oscillate around it.The flow chat of P&O algorithm is given in Fig.2.3.

In P&O method at first P (N) is calculated from present value of voltage V (N) and current I (N). Subsequently P (N) is compared with the next level of power P (N+1). If the power increases then the voltage is changed through the same direction as the previous changes else the change will be reversed.

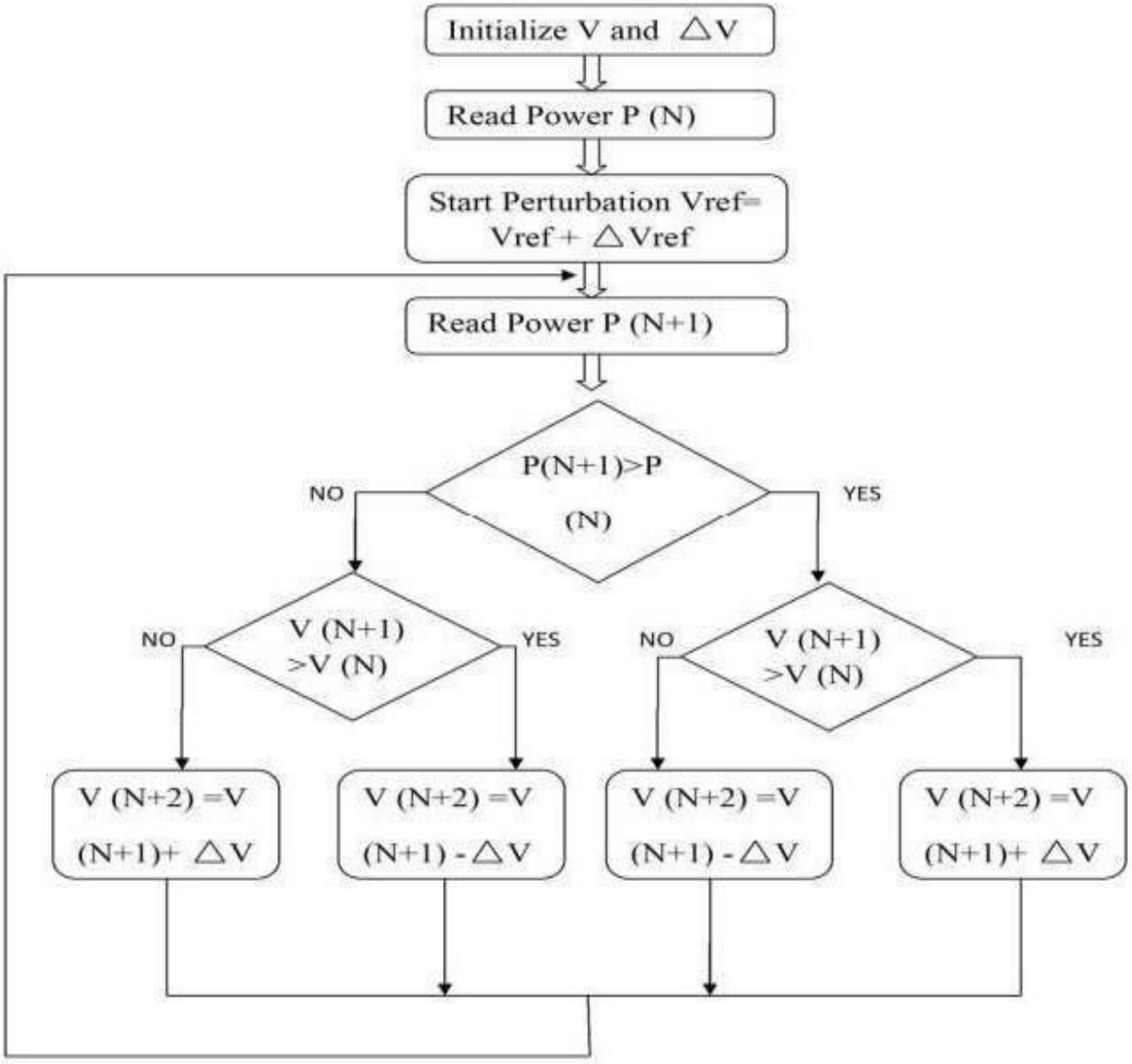


Fig.2.3. MPPT Perturbation &Observation (P&O) Algorithm

2.4 Power Electronics

Power electronics to process and control the flow of electric energy by supplying voltage and current in from that is optimally suited for user load. In power electronics, an electrical device should be able to achieve the highest efficiency compare to the linear electronics. Linear electronics utilize semiconductor devices that operate at their active region and a transformer just for electrical isolation. Fig.2.4 shows the power electronics systems that utilize a close loop operation.

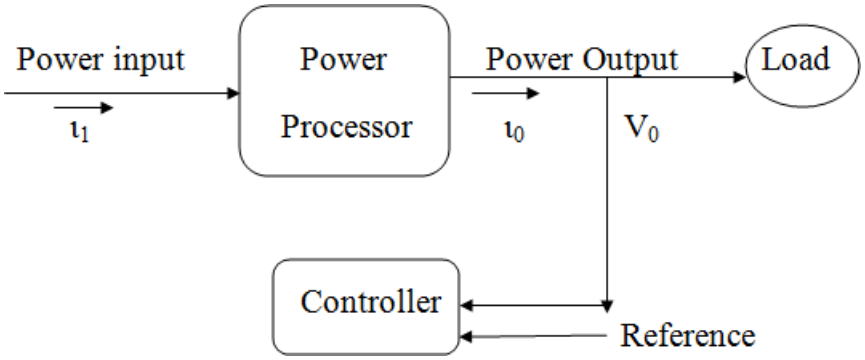


Fig.2.4. Power electronic system

In managing the energy consumed by load, power electronics system utilized switching methods to minimize the appearance of active region in semiconductor device. Although it is impossible to remove all power dissipated by semiconductor, switching mode has greatly reduced the power consumed in semiconductor devices. Therefore, the power consumed in semiconductor is then proportional to the switching frequency. Power electronics is the field The power source can be a DC source or an AC source (single-phase or three-phase with line frequency of 50 or 60 Hz), an electric battery, a solar panel, an electric generator or a commercial power supply.

A power converter takes the power provided by the source and converts it to the form required by the load. The power converter can be an AC-DC converter, a DC-DC converter, a DC-AC inverter or an AC-AC converter depending on the application .

2.5 Dual-stage DC-DC Boost converter

A DC to DC converter is a type of power converters which converts a source of direct current (DC) from one voltage level to another, by storing the input energy momentarily and then releasing that energy to the output at a different voltage. The storage should be in electric field storage components or in magnetic field storage components. There are three basic types of converter: buck converter, boost converter, and buck-boost converter. In my proposal, DCDC boost converter is used for converting unregulated voltage to a fixed level regulated voltage. In my design I preferred boost converter in case of steady environmental condition that successfully amplify PV arrays voltage into required level that is shown in Fig.2.6. This power converter is controlled by Pulse Width Modulation (PWM) and applied through transistor. To achieve desire output from power converter the duty cycle of the PWM should be large and from datasheet it is found conventional transistors will not response at that level of high duty cycle . Therefore to make convenience duty cycle power conversion done.

through 2stage. Fig. 2.5 is shown boost power converter circuit of dual-stage boost power converter that operates via MPPT algorithm of an intellectual PV system and increases the power of solar system which ensures optimum load impedance by varying duty cycle.

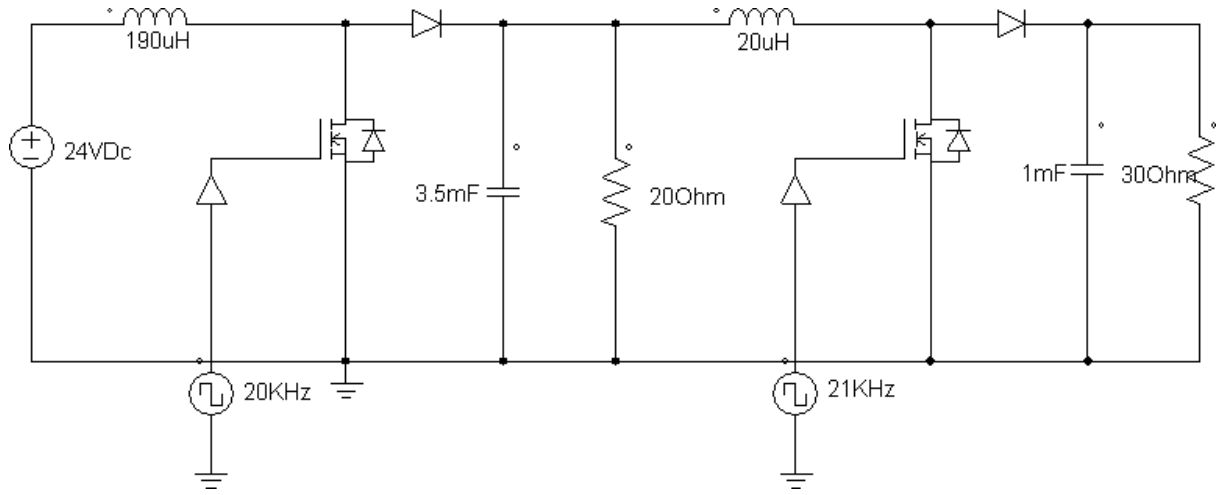


Fig.2.5. Dual-stage Boost Power Converter

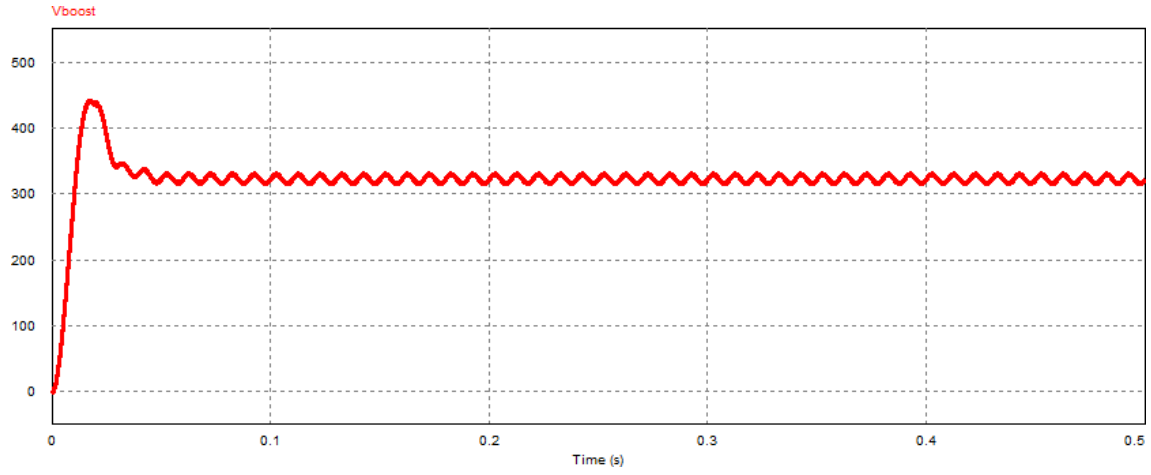
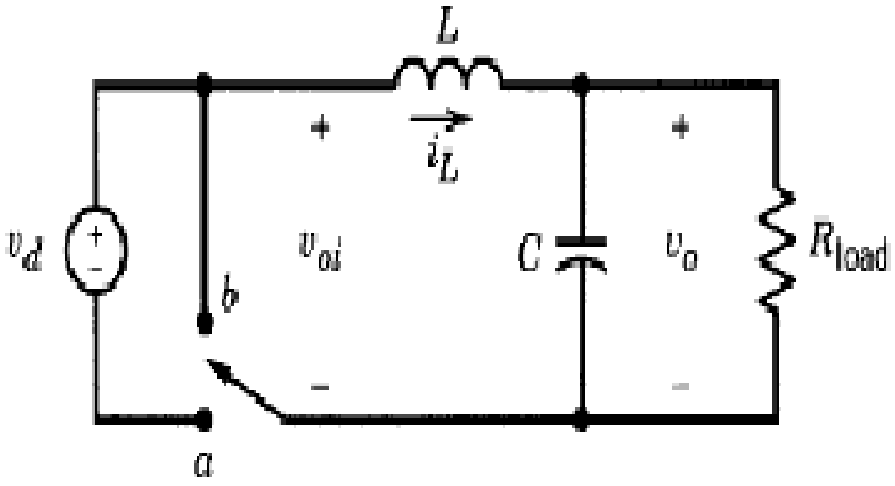


Fig.2.6. Dual-stage Boost converter output

The boost converter is used for 24V-312V conversion and it is used instead of transformer. Therefore in case of inverter use harmonics is the main consideration. If the harmonic of boost converter is more than transformer than it will be well to use transformer moreover transformer is bulky in size whereas boost converter circuit is light in weight.

2.6 Harmonics

In power electronics application, high switching mode can result harmonic components in output waveform. Harmonic of a wave is a component frequency that is an integer multiple of fundamental frequency.



(a)

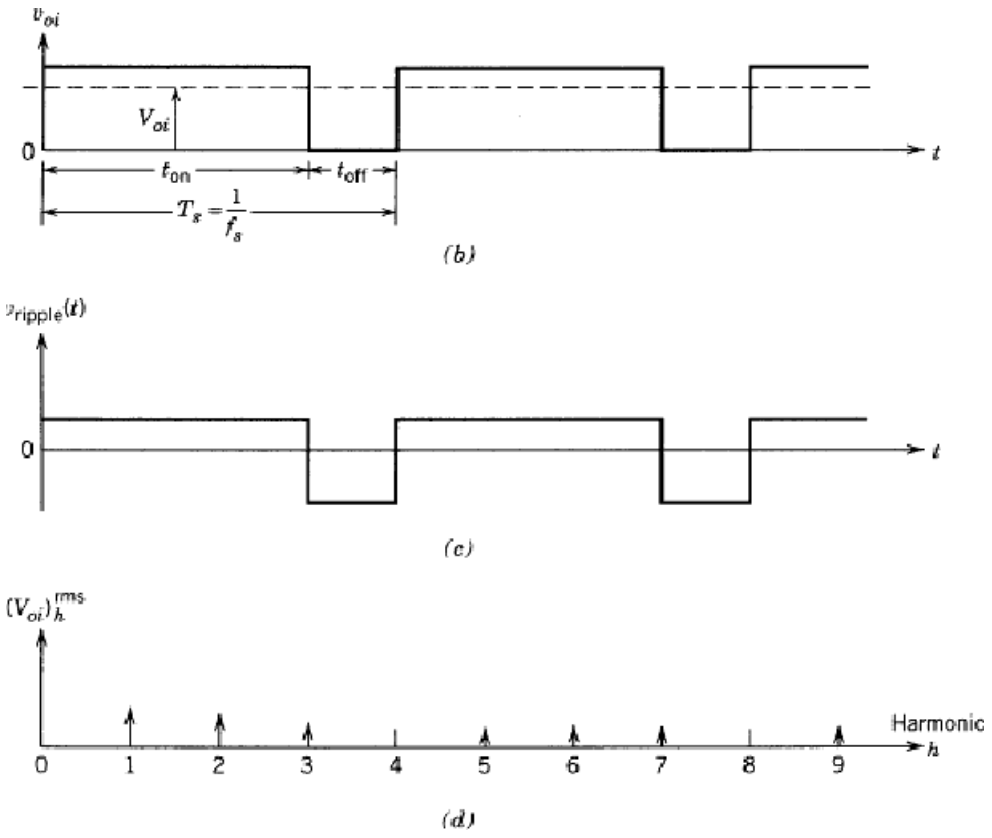


Fig.2.7. Harmonics happen at switching

Fig.2.7 (a) harmonic is created during fast switching mode. A DC voltage Voi is the desired output. While Vd(DC voltage) is the voltage source that is greater than Voi. Switching is used to get an average value of output waveform equal to Voi. The result waveform is depicted Fig.2.7 (b). Dashed Voi in Fig. 2.6 (c) known as fundamental component and Fig.2.7 (d) is known as its harmonics. The sum of fundamental and harmonic will result the actual waveform.

2.7 Dual-stage AC-DC Buck converter

In proposed buck power converter the input is taken from grid. And grid AC voltage is converted into pulse setting DC through full bridge rectifier shown in Fig.2.8. Subsequently pulse setting 220V DC is converted into 5V DC by using buck power converter. To achieve desire output from power converter the duty cycle of the PWM should be very small and from datasheet it is found conventional transistors will not response at that level of low duty cycle . Therefore to make convenience duty cycle power conversion done through dual- stage. The buck converter is used to take sample from grid. The sampled 5V pulse setting DC is used to generate the SPWM signal thus ensuring output voltage from GTI will have same frequency as the grid . Fig.2.9. illustrates output signal of buck converter.

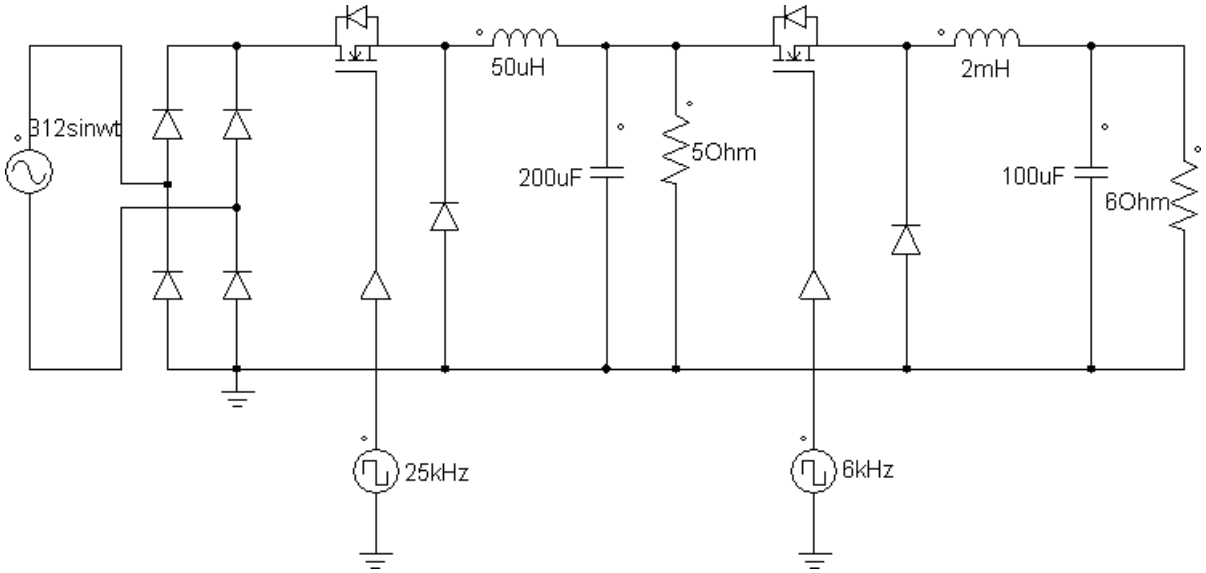


Fig.2.8. Dual-stage Buck power converter

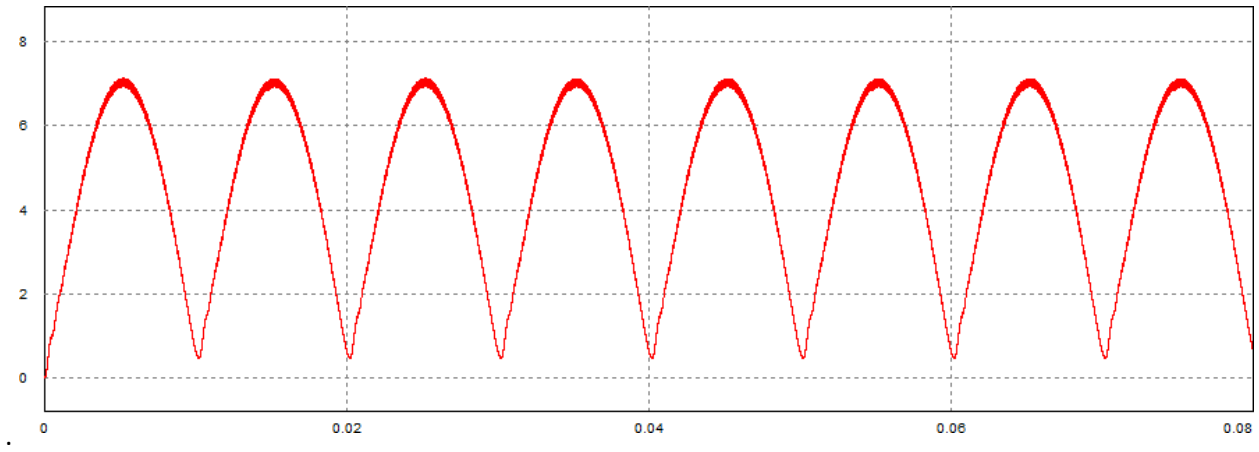


Fig.2.9. Dual- stage buck converter output (RMS 5V)

Buck converter is used for grid synchronization as well buck is used for gate drive circuit to reduce harmonics. As the input voltage of buck is taken from grid hence frequency of inverter output will be as equal as grid frequency. As microcontroller input is 5v therefore buck conversion is used to convert 312V-7.07V means RMS 220V-5V conversion.

2.8 Sinusoidal Pulse Width Modulation

In a conventional inverter design, normally the switching will used one type of the switching technique only. However, in this proposed design instate of using one type of switching signal to switch the inverter, a combination of SPWM and square wave is used [3]. With this kind of combination switching, the switching loss across the switches of the inverter will be greatly reduced due to reduce of switching frequency. The block diagram of the proposed switching circuit is as shown in Fig.2.10. In order to simplify the synchronizing process, instate of generating the sine wave from the analog oscillator or from microcontroller and digital-to- analog converter (DAC).

the sine wave of the proposed design will be sampled from the power grid by using the buck power converter to step down the 220V grid voltage to 5V is shown in Fig.2.7. With the sine wave sampled from the grid and used to generate the SPWM signal, the frequency of the output voltage from the GTI will be having the same frequency as the grid voltage where this is one of the most important requirement for the GTI as stated in the section2.7.

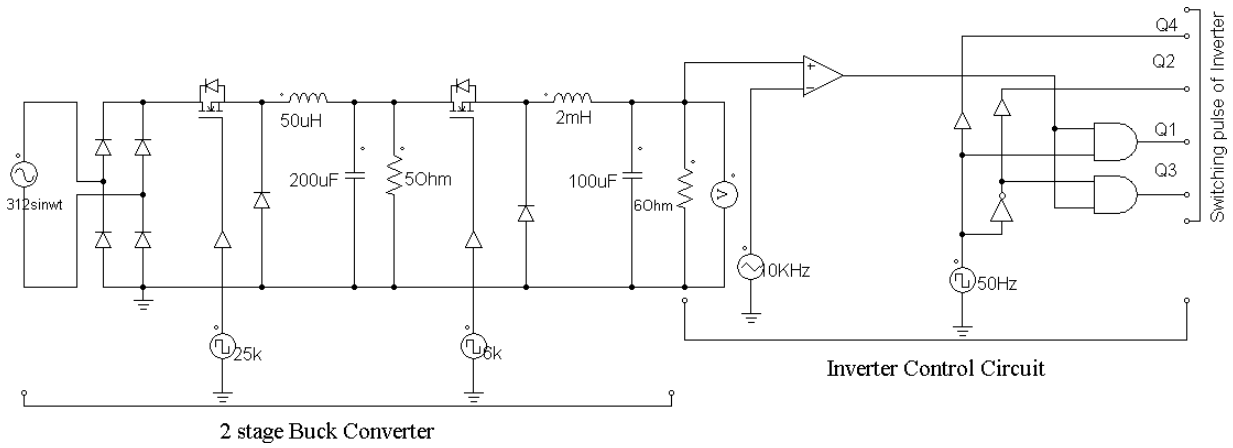


Fig.2.10. Block diagram of the proposed switching circuit

Besides processing the sampled sine wave, to produce a SPWM signal, a high frequency triangle wave also required. In this proposed design the high frequency triangle wave wills also generated by the analog oscillator and the frequency will be 10 kHz. The comparison of sampled grid rectified wave V Modulation and high frequency triangular wave Vtriis shown in Fig.2.11.

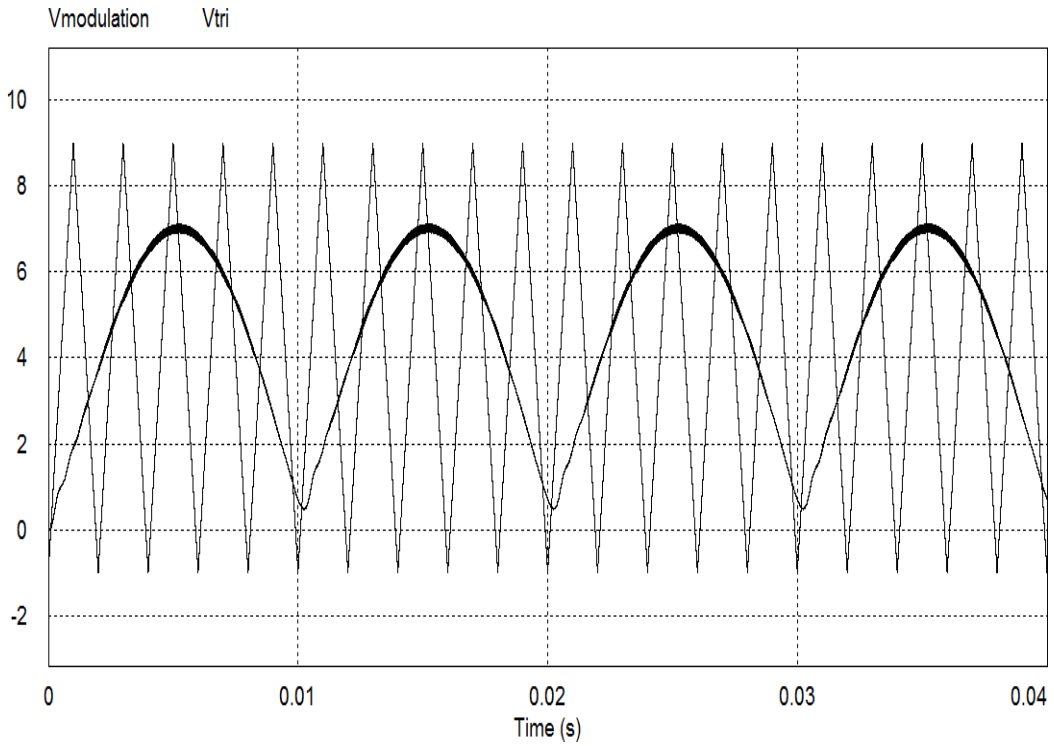


Fig.2.11. Sinusoidal pulse width modulation generation

These two signals will then pass though a comparator to produce SPWM for the switching signal. These two signals will produce a uni-polar SPWM as shown in Fig.2.12. The uni-polar SPWM signal have only positive value and will be change from +5V to 0V and back to +5V again.

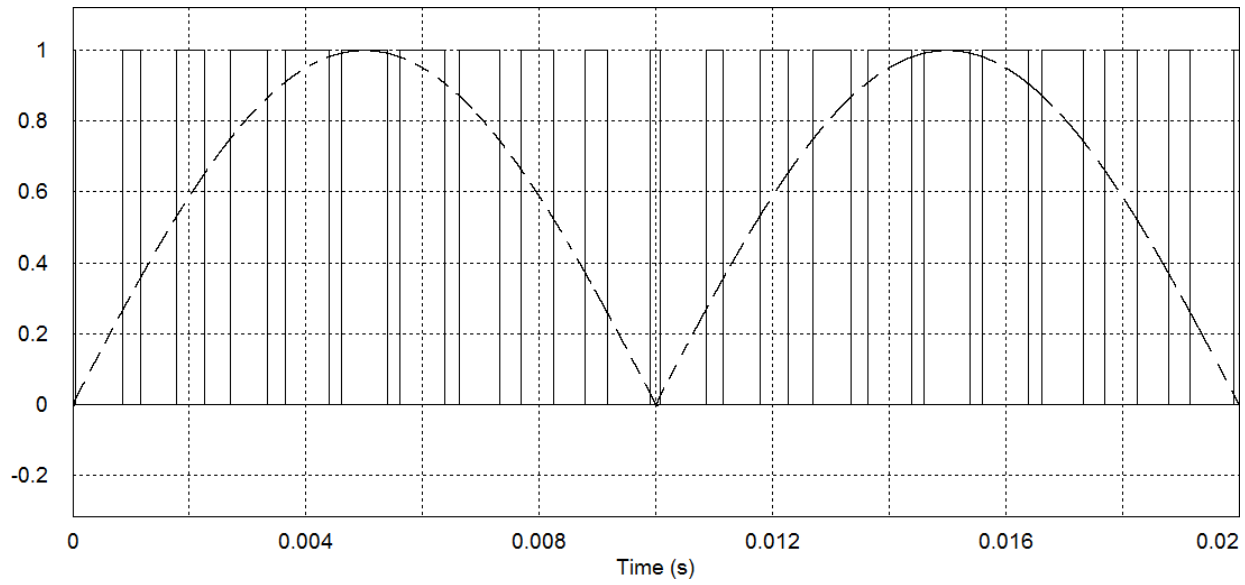


Fig.2.12.Uni-polar sinusoidal PWM switching signal.

After getting the SPWM signal for the switching of the IGBT as many conventional inverter circuits, the proposed GTI will also have square wave signal for the switching. This square wave signal will be in line frequency (50 Hz for Bangladesh) and in phase with the SPWM. This square wave signal will pass though a NOT gate and creating another set of signal which is 1800 out phase from the original square wave.

Therefore switching of the transistors is done independently which results in four intervals per cycle. For two intervals *VL* equals E or –E which forces the load current to increase exponentially in the positive or negative direction respectively. Uni-polar PWM method has the ability to produce less harmonics and at lower amplitudes than the bipolar method because of the uni-polar voltage switching difference of E is half the bipolar method of 2E. The other advantage is derived from the fact that the unipolar method effectively doubles the switching frequency of the bipolar method. To take advantage of this,

This results in the even harmonics having the same phase because the voltage waveform are displaced by 180° of the fundamental frequency. In addition, the sidebands of the switching frequency harmonics will also cancel as will the dominant harmonic at twice the switching frequency. The outcome of this setup is that the uni-polar method will only produce odd numbered harmonics.

The technique of this new switching method is used because; to match grid frequency grid voltage was sampled through buck power converter, to match grid phase sequence square wave was implied and the photovoltaic system was designed to operate using the uni-polar method over the bipolar method because of the advantage of reducing the inverter output harmonics.

Advantages of SPWM:

- Low power consumption.
- High energy efficient up to 90%.
- High power handling capability.
- No temperature variation-and ageing-caused drifting or degradation in linearity.
- Easy to implement and control.
- Compatible with today's digital microprocessors

Disadvantages of SPWM:

- Drastically increased switching frequencies that leads to greater stresses on associated Switching devices and therefore de-rating of those devices.

2.9 DC-AC Inverter

Inverter is an electrical device that converts a direct current DC into an alternating current .The basic principle is to convert a DC into an AC is by controlling the electrical switching components. Fig.2.13 represents the basic inverter circuit with ideal switch.

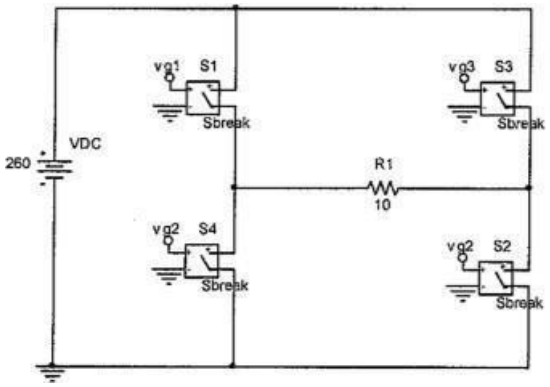


Fig.2.13. Basic inverter circuit with ideal switch

2.10 Inverter Design Requirement

The requirements for inverter go as follows:

- Output Voltage Equal to 220 Vrms
- Fixed Output Frequency of 50 Hz
- Capable of Supplying Power up to 2500W
- Maximum Load Current of 12 A
- Input DC Voltage Between 24 V
- Efficiency at Full Load Current Greater than 98%

2.11 Classification of Inverter

Inverters are basically two major types

- Single phase inverter
- Three phase Inverter

Again single phase inverter are further classified few more types that is discussed below

2.11.1 Square Wave Inverter

Square Wave units could be harmful to some electronic equipment, especially equipment with transformers or motors. The square wave output has a high harmonic content, which can lead such equipment components to overheat Square Wave units were the pioneers of inverter development and, like the horse and buggy, are no longer relevant for modern inverter.

2.11.2 Modified Sine Wave Inverter

The most common, general-use inverters available are "Modified Sine Wave". Usually available at more moderate pricing compared to pure sine wave models. Modified Square Wave (or “Modified Sine Wave” and “Quasi Sine Wave”) output inverters are designed to have somewhat better characteristics than Square Wave units, while still being relatively inexpensive. Although designed emulate a Pure Sine Wave output, Modified Square Wave inverters do not offer the same perfect electrical output. As such, a negative by-product of Modified output units is electrical noise, which can prevent these inverters from properly powering certain loads.

For example, many TVs and stereos use power supplies incapable of eliminating common mode noise. As a result, powering such equipment with a Modified Square Wave may cause a "grain" or small amount of "snow" on your video picture, or "hum" on your sound system. Likewise, most appliances with timing devices, light dimmers, battery chargers, and variable speed devices may not work well.

2.11.3 Pure Sine Wave Inverter

Pure or True Sine Wave inverters provide electrical power similar to the utility power you receive from the outlets in your home or office, which is highly reliable and does not produce electrical noise interference associated with the other types of inverters. With its "perfect" sine wave output, the power produced by the inverter fully assures that your sensitive loads will be correctly powered, with no interference. Some appliances that are likely to require Pure Sine Wave include computers, digital clocks, battery chargers, light dimmers, variable speed motors, and audio/visual equipment. If your application is an important video presentation at work, opera on your expensive sound system, surveillance video, a telecommunications application, any calibrated measuring equipment, or any other sensitive load, you must use a Pure Sine Wave inverter.

2.11.4 H-Bridge Inverter

A typical DC-AC converter is commonly named as inverter. This takes a DC input voltage and converts into sinusoidal ac output voltage and frequency as grid standard. Fig.2.14 shows a typical H-bridge inverter circuit diagram. The H-bridge inverter has high conversion efficiency, low stress and also easily interfaced with renewable energy source such as PV panel .

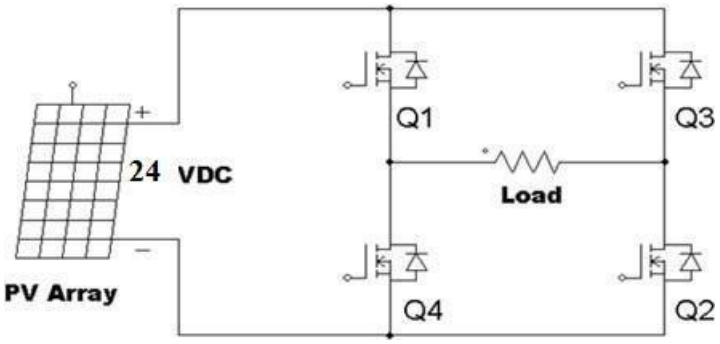


Fig.2.14. H-Bridge inverter circuit

In switching process, four switches are grouped into two groups, Q1 and Q2 are in one group and Q3 and Q4 are in another group. When Q1 and Q2 are switched, Q3 and Q4 are forced turned off. Similarly, when Q3 and Q4 are switched, Q1 and Q2 are forced off.

2.12 Inverter Applications

Everyday appliances such as microwaves, power tools, TVs and VCRs, lights, audio/visual load , you must use a Pure Sine Wave inverter.

Pure Sine Wave inverters are ideal for running sensitive test equipment such as communications equipment, oscilloscopes, scales, high end stereos & video equipment, communications equipment, etc.

The most useful use in renewable energy conversion such as to convert solar energy to electrical energy.

2.13 T-LCL filter

A lumped-constant reactor L and capacitor C can be used for the implementation of an immittance converter in a compact design. Some lumped-constant configurations of the immittance converter have been studied previously . There are four typical configurations of the immittance converter that consist of three lumped reactive elements namely T-LCL type, π-CLC type, T-CLC type and π-LCL type.

Converters with more than four reactive elements are bigger, heavier and costlier and their analysis and design is more complicated . Hence converters having more than four reactive elements have not been studied.

The T-LCL topology and its applications have been studied the most .The immittance conversion circuit or immittance converter is actually an impedance-admittance converter. It is thus named as in this particular topology; the impedance is converted into admittance. The input impedance is proportional to the output load and the output current is proportional to the source voltage. In the immittance circuit, the input current is alsoproportional to the output voltage. By means of an immittance converter, a constant voltage source is converted into a constant current source.

The immittance conversion circuit used in the proposed SWI is a T-LCL configuration .The T-LCL immittance conversion circuit is not only efficient in the reduction of harmonic distortion to produce a pure sinusoidal output but it also helps to maintain the desired constant current output is shown in Fig.2.15.

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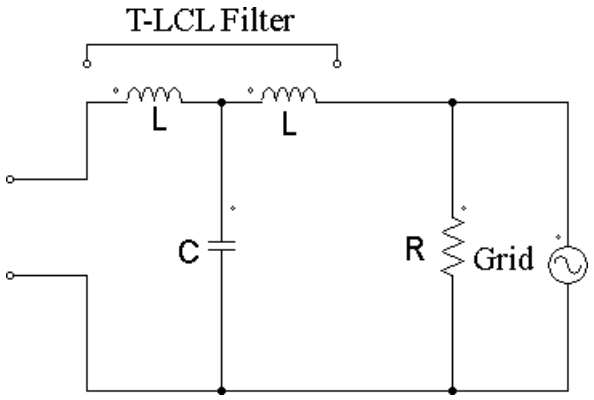


Fig.2.15.T-LCL filter

2.14 Power Inverter Protection Systems

According to their production technologies, solar power inverters can include many different protection systems. The most well known protection systems are:

Over temperature shutdown:

They are also known as thermal protection systems. When a power inverter converts power over the capacity it has or at values very close to this capacity it may overheat and break down. Electronic parts generally start to break down over 90 0C. In order to prevent this from happening, heat sensitive sensors are placed inside the power inverters, and this enables shutdowns at high temperatures or decrease of the power transmitted. These parts called PTC or NTC send the necessary temperature information to the central processing unit when high temperatures are reached and this activates the protection.

Automatic Overload Protection:

Overload protection which is another protection system, works in or der to prevent breakdowns caused by burns of the parts which are caused by power load which exceeds the capacity of the device. For example, if an inverter which has 4000W capacity is loaded with 4300W power, the protection system is activated and gives the necessary warning to the user such as closing the device and decreasing the transferred power.

Ground Fault Protection:

In high capacity solar cell power inverters, grounding systems are essential. In order to protect the devices that are connected to the system and in order for the inverter to work more efficiently, the grounding should be done properly. If a high capacity power inverter has not been grounded properly, by means of the protection system that it has inside, it will warn the user and carry out the necessary processes. If grounding is not done properly, ground, not short circuit connection is carried out automatically and thus the system is protected.

Short Circuit Protection:

By means of this protection system, the short circuit problem which is caused by the output cables touching one another due to user misuse is prevented. During short circuit, the device is immediately put on passive condition and is shut down. Other names for this protection system are known as AC Over current protection and DC Over current protection.

2.15 Powersim (PSIM) Software

PSIM provides an ultimate simulation environment for power conversion and control. It is mainly designed for power electronics, motor drives, analog and digital control, magnetic and dynamic system studies. It enables fast simulation and it is quite user-friendly. The PSIM simulation environment includes the PSIM Circuit Schematic, the Simulation engine and the SIMVIEW for viewing and analyzing the waveforms. The PSIM schematic program is highly interactive and user-friendly in building the circuit as well as editing it. The PSIM software has been used for carrying out all the simulations and analysis of the waveforms so obtained in the thesis.

CHAPTER-3

DESIGN &CIRCUIT ANALYSIS

3.1 Derivation of DC-DC Boost converter

In boost regulator the output voltage is greater than the input voltage-hence the name of the converter is "BOOST". The operation of the circuit is explained now. The essential control mechanism of the circuit in Fig. 2.4 is turning the power semiconductor switch on and off. When the switch is ON, the current through the inductor increases and the energy stored in the inductor builds up. When the switch is off, current through the inductor continues to flow via the diode D, the RC network and back to the source. The inductor is discharging its energy and the polarity of inductor voltage is such that its terminal connected to the diode is positive with respect to its other terminal connected to the source. It can be seen then the capacitor voltage has to be higher than the source voltage and hence this converter is known as the boost converter. It can be seen that the inductor acts like a pump, receiving energy when the switch is closed and transferring it to the RC network when the switch is open. When the switch is closed, the diode does not conduct and the capacitor sustains the output voltage. The circuit can be split into two parts, as shown in Fig. 3.1. As long as the RC time constant is very much larger than the on-period of the switch, the output voltage would remain more or less constant. .

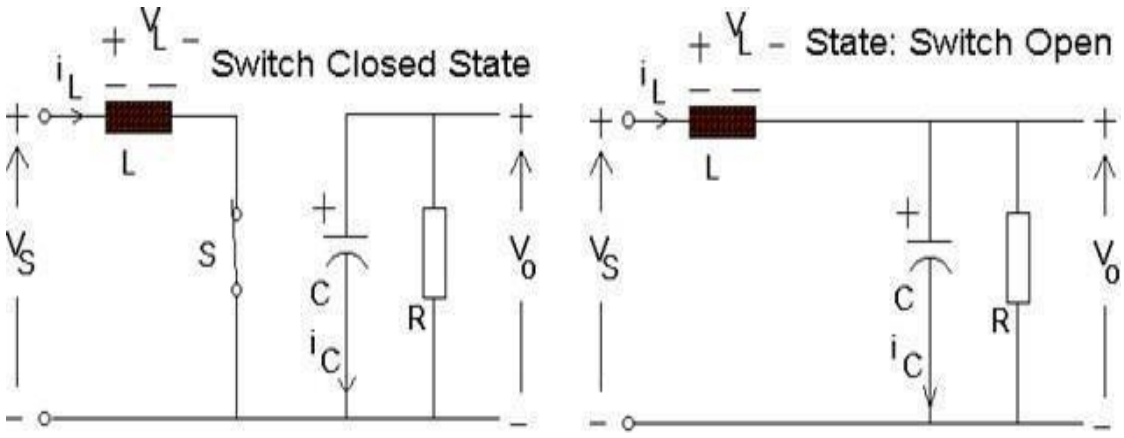


Fig.3.Fig.3.1. Equivalent circuits of boost converter

3.2 Design parameter of Boost Power Converter

Boost is designed in two stages (N=2), compared to straight boost converting this technique provides a more symmetrical duty cycle and reduced voltage stress on the MOSFET. Moreover in straight boost converter required duty cycle is tough to handle by switching. Therefore the conversion of boost converter is done based on conversion ratio which converted 24V DC to 86V DC then 86V DC to 312V DC . The design parameters of boost converters

Symbol	Actual Meaning	Value
V_{in}	Given input Voltage	24V
V_{out}	Desired average output Voltage	86V
f_s	Minimum switching frequency of the converter	20KHz
I_{LMax}	Maximum Inductor current	261A
ΔI_L	Estimated inductor ripple (1.75% of Inductor current)	4.55A
ΔV_{out}	Desired output voltage ripple (0.4% of output voltage)	0.44V
I_{out}	Maximum Output current(V_{out}/R)	4.3A

Table 3.1 Design parameters of first stage Boost converter

Table 3.2 Design parameters of second stage Boost converter

Symbol	Actual Meaning	Value
V_{in}	Given input Voltage	86V
V_{out}	Desired average output Voltage	312V
f_s	Minimum switching frequency of the converter	21KHz
I_{LMax}	Maximum Inductor current	260A
ΔI_L	Estimated inductor ripple (3.85% of Inductor current)	10A
ΔV_{out}	Desired output voltage ripple (0.1% of output voltage)	0.35V
I_{out}	Maximum Output current(V_{out}/R)	10.4A

Inductor Selection:

The smoothing Inductor is used to limit current ripple. As in conventional process inductor value have to chosen from recommended data sheets . But in this report I have to convert a large scale of voltage from 24V DC to 86V DC for this part no inductor range is given, the following equation is a good estimation for choosing right inductor value.

Capacitor selection:

In this report the following equations can be used to adjust the output capacitor values for a desired output voltage ripple .

3.3Derivation of Buck Converter

A buck converter or step-down switch mode power supply can also be called a switchmode regulator. Popularity of a switch mode regulator is due to its fairly high efficiency compact size and a switch mode regulator is used in place of a linear voltage regulator at relatively high output. In applications where size and efficiency are critical, linear voltage regulators cannot be used. The operation of the buck converter is explained first. This circuit can operate in any of the three states as explained below.

The first state corresponds to the case when the switch is ON. In this state, the current through the inductor rises, as the source voltage would be greater than the output voltage, whereas the capacitor current may be in either direction, depending on the inductor current and the load current. When the inductor current rises, the energy stored in it increases. During this state, the inductor acquiresenergy. When the switch is closed, the elements carrying current are shown in red color in Fig. 3.2, whereas the diode is in gray, indicting that it is in the off state. In Fig. 3.2, the capacitor is getting charged in first state, whereas it is discharging in second stage .

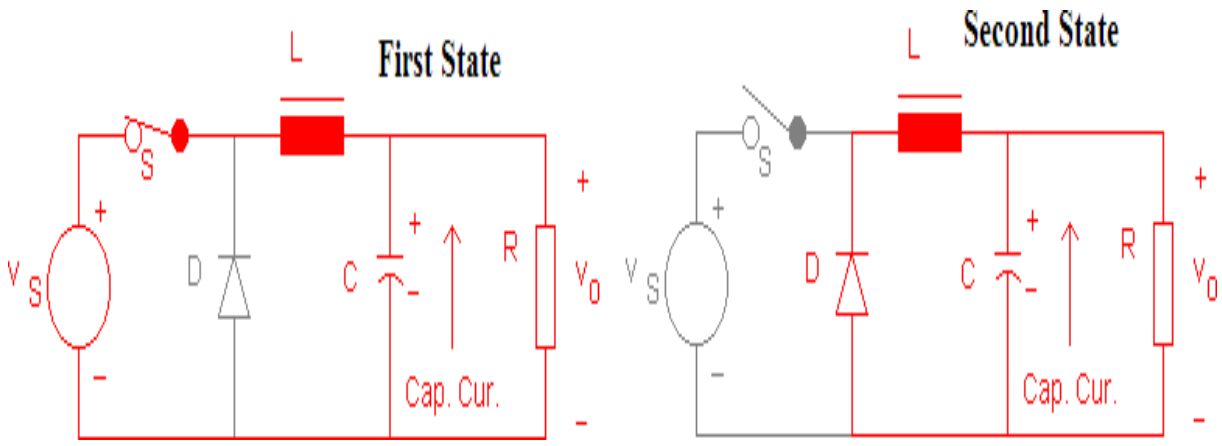


Fig.3.2. Equivalent circuits of buck converter

3.4 Design parameter of Buck power converter

Buck converter is designed in two stages (N=2), because in straight buck conversion desire duty cycle is very low and is impracticable to apply. Therefore the conversion of buck converter is done based on conversion ratio which converts RMS 220V AC to 33V DC then 33V DC to 5V DC . The design parameters of buck converters are listedin Table-
3.3 and Table-3.4:

Table 3.3 Operating parameter for first stage buck converter

Symbol	Actual Meaning	Value
V_{in}	Given RMS input voltage	220V
V_{out}	Desired output voltage	33V
f_s	Minimum switching frequency of the converter	25KHz
I_{Lmax}	Maximum inductor current	50A
ΔI_L	Estimated inductor ripple (4.4% of maximum inductor current)	2.2A
ΔV_{out}	Desired output voltage ripple (1.6% of output voltage)	0.05V

Table 3.4 Operating parameters of second stage buck converter

Symbol	Actual Meaning	Value
V_{in}	Given RMS input voltage	33V
V_{out}	Desired RMS output voltage	5V
f_s	Minimum switching frequency of the converter	6KHz
I_{Lmax}	Maximum inductor current	14A
ΔI_L	Estimated inductor ripple (3% of maximum inductor current)	0.35A
ΔV_{out}	Desired output voltage ripple (1.6% of output voltage)	0.05V

Inductor selection for buck converter:

The smoothing Inductor is used to limit current ripple. As in conventional process inductor value has to be chosen from recommended data sheets. But no inductor range is given for a large scale conversion like from 202V to 33V. Therefore, in the present design, the following equation is a good estimation for choosing right inductor value.

Capacitor selection for buck converter:

The basic selection of the output capacitor is based on the ripple current and ripple voltage, as well as on loop stability considerations. In the present design, the following equations can be used to adjust the output capacitor values for a desired output voltage ripple in 220V to 33V conversion ..

3.5 T-LCL Type Immittance Converter:

The circuit diagram of the T-LCL immittance converter is shown in Fig. 3.3. It consists of two inductors L1 and L2, and a capacitor C, in a T shape. The inductors are assumed to have series internal resistances r1 and r2 and the capacitor is assumed to be ideal. A load Z2 is connected across the output terminals . The input and output voltages and currents are as shown in the diagram.

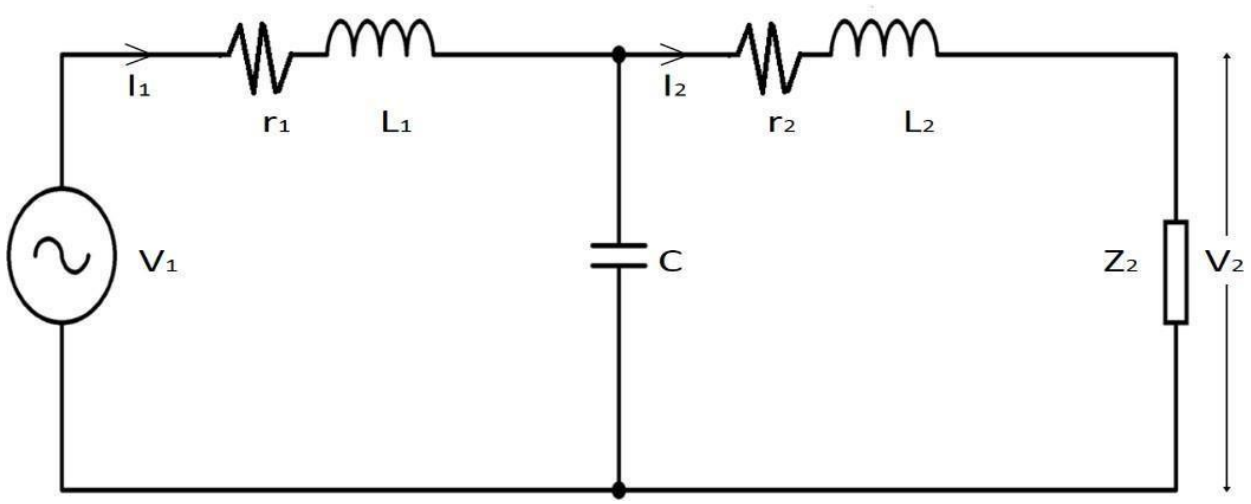


Fig.3.3. T-LCL type immittance converter

3.6 Design of T-LCL filter

From above derivation it is proved that the low pass filter is applied to suppress harmonic influence and to acquire pure sine wave at output of the inverter. In this article T –LCL immittance conversion circuit is applied as a filter circuit because it is not only capable in the reduction of harmonic distortion to produce a pure sinusoidal output but it alsohelps to sustain the desired constant current output.. shows that the output current does not depend on the load impedance and depends only on input voltage and characteristic impedance Z0 = √(L⁄C).

Therefore, in ideal condition, the immittance circuit will provide constant current or constant power. And the output voltage does not depend on the load impedance.

the output voltage does not depend on the load impedance but depends only on input current and characteristic impedance Z0. Therefore, the ideal immittance circuit will provide constant voltage.

CHAPTER-4

SIMULATION OF INVERTER

4.1 Introduction

Here proposed inverter design consists of firstly calculation and then simulation on PSIM software.

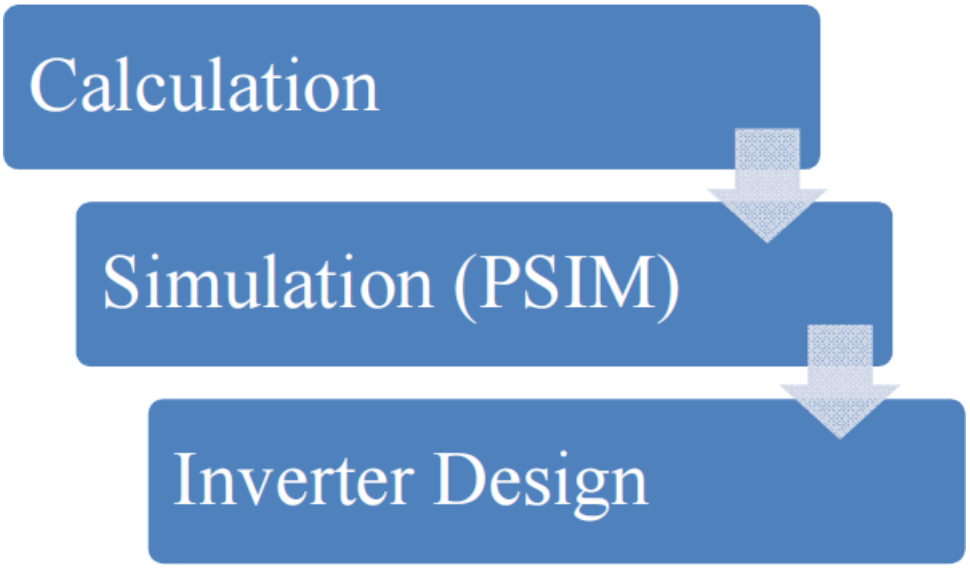


Fig.4.1: Methodology for Inverter Design

4.2 SWITCH SELECTION

MOSFET vs IGBT:

Two main types of switches are used in power electronics. One is the MOSFET, which his designed to handle relatively large voltages and currents. The other is the insulated gate bipolar transistor, or IGBT. Each has its advantages, and there is a high degree of overlap in the specifications of the two.

IGBTs tend to be used in very high voltage applications nearly always above200V,

and generally above 600V. They do not have the high frequency switching capability of MOSFETs, and tend to be used at frequencies lower than 29kHz. They can handle high currents, are able to output greater than 5kW, and have very good thermal operating ability, being able to operate properly above 100 Celsius. One of the major disadvantages of IGBTs is their unavoidable current tail when they turn off. Essentially, when the IGBT turns off, the current of the gate transistor cannot dissipate immediately, which causes a loss of power each time this occurs. This tail is due to the very design of the IGBT and cannot be remedied. IGBTs also have no body diode, which can be good or bad depending on the application. IGBTs tend to be used in high power applications, such as uninterruptible power supplies of power higher than 5kW, welding, or low power lighting.

MOSFETS have a much higher switching frequency capability than do IGBTs, and can be switched at frequencies higher than 200 kHz. They do not have as much capability for high voltage and high current applications, and tend to be used at voltages lower than 250V and less than 500W. MOSFETs do not have current tail power losses, which makes them more efficient than IGBTs. Both MOSFETs and IGBTs have power losses due to the ramp up and ramp down of the voltage when turning on and off (dV/dt losses). Unlike IGBTs, MOSFET shave body diode.

Generally, IGBTs are the sure bet for high voltage, low frequency (>1000V, <20kHz) uses and MOSFETs are ideal for low voltage, high frequency applications (<250V, >200kHz). In between these two extremes is a large grey area. In this area, other considerations such as power, percent duty cycle, availability and cost tend to be the deciding factors. Therefore in this simulation MOSFET is used as high frequency and 212 v are required.

4.3 Switching Circuit design

In conventional inverter design, Sinusoidal Pulse Width Modulation (SPWM) is generally used to get AC output. But in this article SPWM and square wave combination is used for inverter switching because this new technique reducing losses by reducing switching frequency. To accurately obey grid synchronization process the sine wave of the proposed design will be sampled from power grid by using buck power converter to step down the 220V grid voltage to 5V DC voltage . As a result the frequency of GTI output will be as same as grid frequency. After that a high frequency triangular wave (10Hz) is compared with sampled sine wave by using comparator to build SPWM as shown in Fig. 4.3. The square wave is used as per grid frequency (50 Hz in Bangladesh) and is in same phase with SPWM. The square wave is also passed through a NOT gate which produces a signal 1800 out of phase with the original signal. Both square wave signal shown in Fig.10. The inverter is required four sets of signal as it used four MOSFET in inverter circuit. Under this situation two sets of SPWM signal and two sets of AND gate operation is performed. Eventually four sets of signal can be labeled into two groups. The first group consists of MOSFETs Q1 and Q4 while second group consists of MOSFETs Q2 and Q3. When Q4 is switched on SPWM is appeared at Q1 at that time Q2 and Q3 switches are off. Again when Q2 is turned on SPWM is appeared at Q3 and that time Q1 and Q4 switches are remaining off. For Q1 and Q4 pair positive voltage is emerged across the load. Moreover for Q2 and Q3 pair negative voltage is emerged across the load . The switches in each branch is operated alternatively so that they are not in same mode (ON /OFF) simultaneously .In practice they are both OFF for short period of time called blanking time, to avoid short circuiting. These bridges legs are switched such that the output voltage is shifted from one to another and hence the change in polarity occurs in voltage waveform. If the shift angle is zero, the output voltage is also zero and maximal when shift angle is π.

The gate switching sequence is shown in Table-4.1. The gate pulses for switching of inverter are illustrated in Fig.4.5 and Fig.4.6.

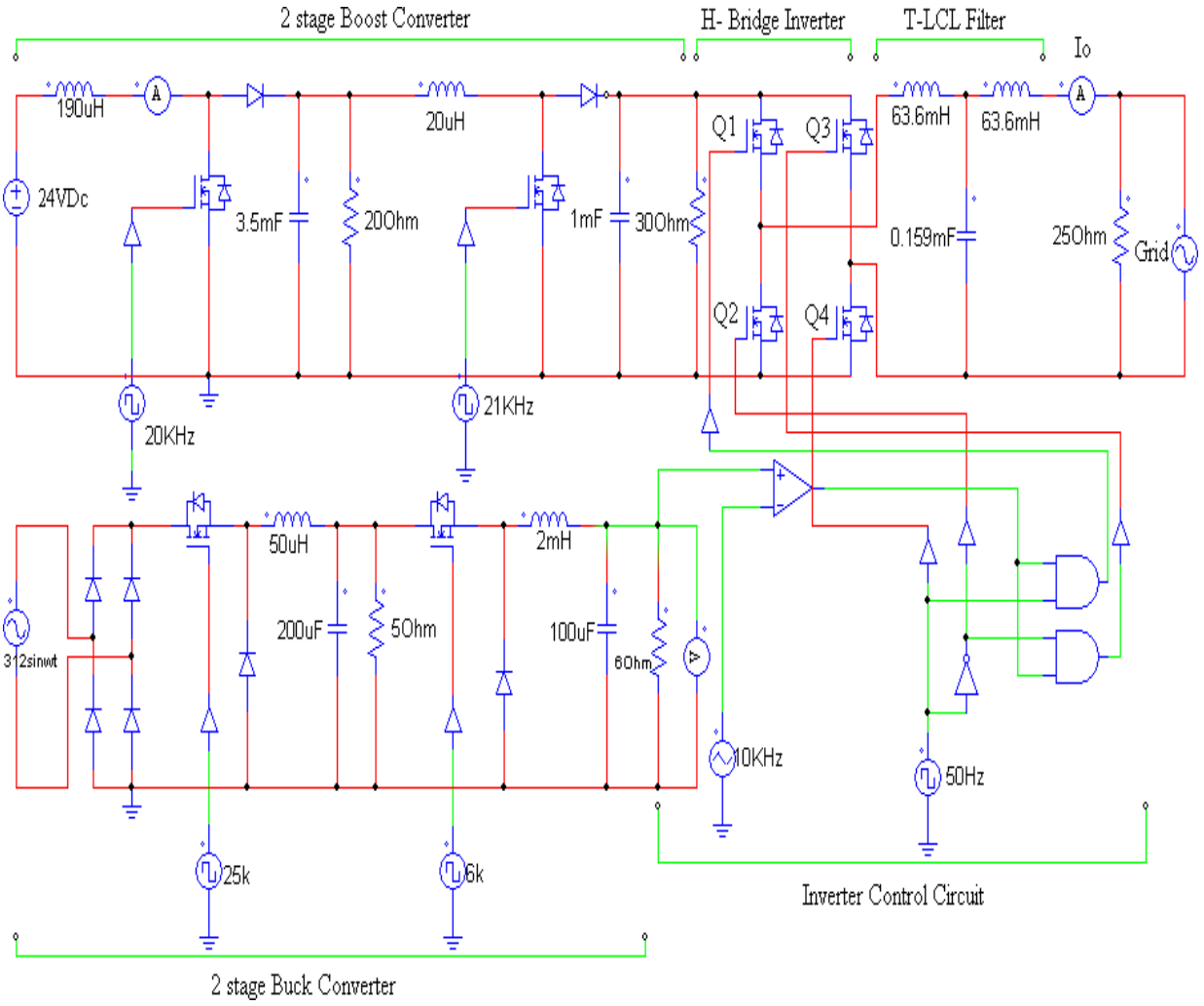


Fig.4.2. Schematic diagram of transformer less GTI for simulation in PSIM

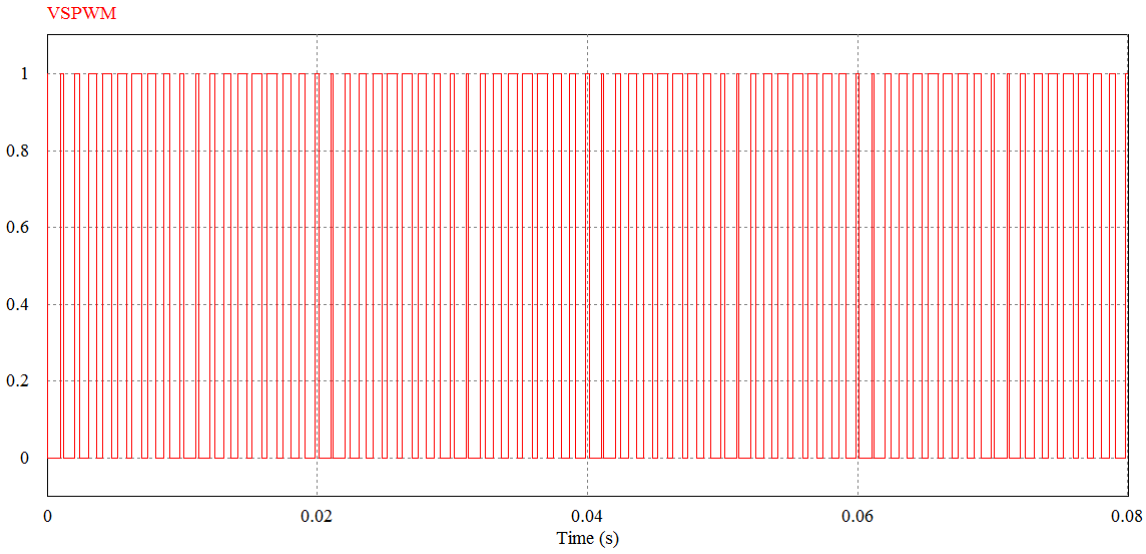


Fig.4.3. SPWM signal for switching

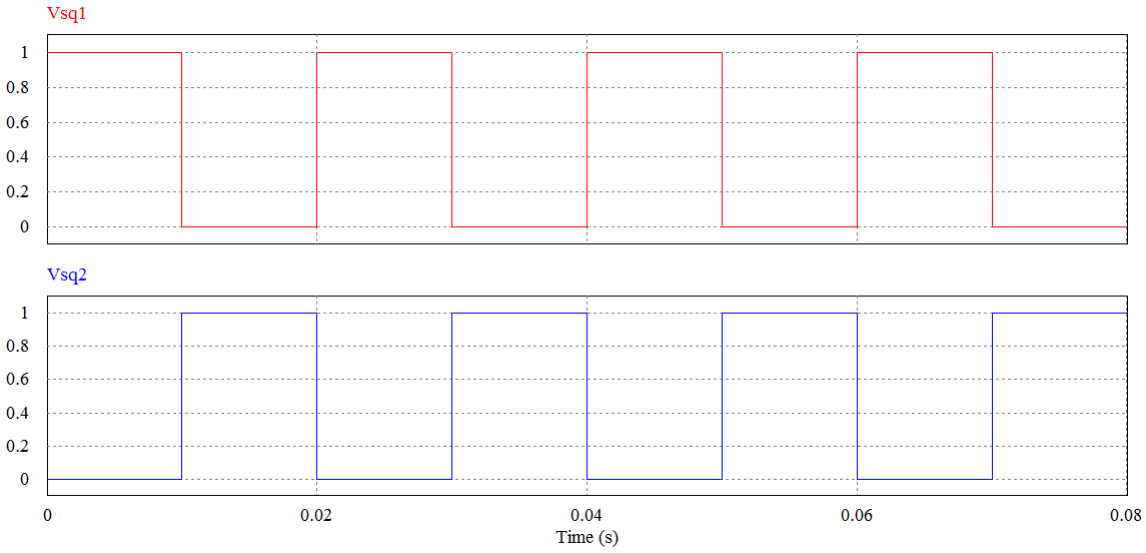


Fig.4.4. Square wave gate pulse 1800 phase difference

Table-4.1 the gate switch Sequence

Q1	Q2	Q3	Q4	V_{out}
ON	OFF	OFF	ON	+Vs
OFF	ON	ON	OFF	-Vs
ON	OFF	ON	OFF	0
OFF	ON	OFF	ON	0

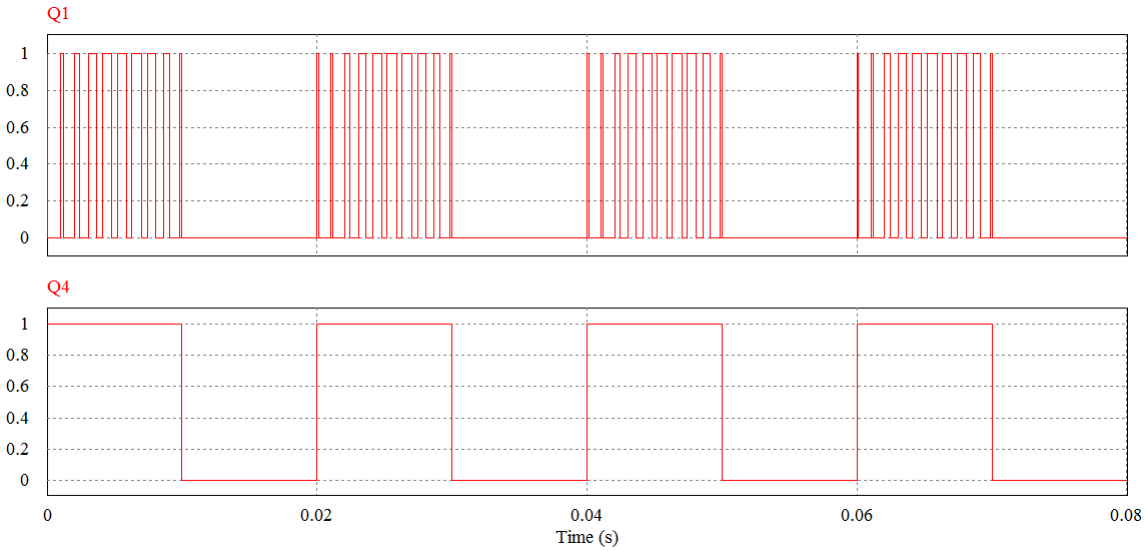


Fig.4.5. Switching signal from control circuit to MOSFETs Q1 and Q4

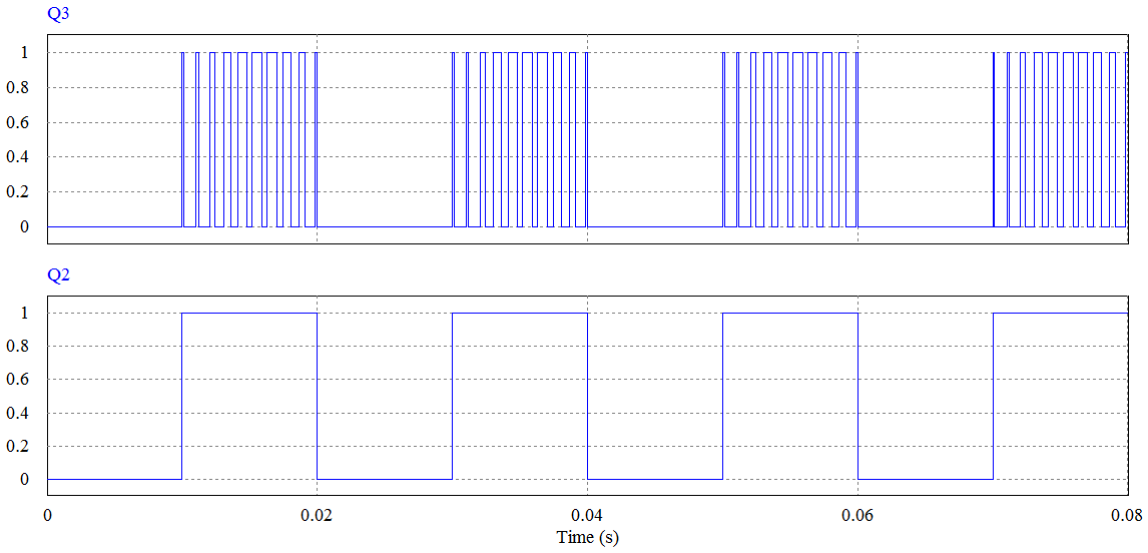


Fig.4.6 switching signal from control circuit to MOSFETs Q1 and Q4

4.4 Grid synchronization technique

The output voltage of a GTI inverter should maintain some fixed requirement so that it may provide power to grid [3]. The requirements are given below:

- The output voltage magnitude should be equal as grid.
- The frequency of inverter should be equal as grid frequency (50Hz in Bangladesh).
- The output phase should as same as grid.

In this proposal to follow the requirement, grid voltage is sampled and is used to set up for switching signal. GTI is directly tied with grid utility and where load is quite large than GTI. Therefore it is transmitted force to GTI for generating power from PV into grid. The real and reactive powers are given below .

4.5 Power transmitting

According to formula (4.2) the voltage angle of GTI should be grater than grid voltage to transmitting power from PV array to grid utility. Though the sine wave is sampled from grid it is passed through a phase shifter to obey the leading condition. From formula (4.1) it can be stated that for sending maximum power at grid phase angle Θ need to keep 900 . But in practical to stay the system in stabilize mood the angle is low than 900 . The load impedance is also very important in case of power transmitting. To reduce noise and maintain current in the output of GTI the article is proposed to employ T-LCL filter .

4.6 Design functions of GTI

In a GTI concern function are divided into two major parts: grid synchronization, power transmitting. For synchronizing frequency of GTI with the grid a sampled of sine wave is taken from grid. After ward the sampled sine wave is rectified and passed through a dual stage buck power converter and the output of buck converter is compared with high frequency triangular wave to build SPWM which ensures same frequency. To match same phase SPWM sets with phase-shift to zero. Then two sets of AND gate operation is performed with combination of SPWM and square wave to construct four individual signal for switching of inverter. The zero crossing detects when inverter output and grid voltage both in phase. Once zero crossing is detected inverter and grid connection is tied via connector is shown in Fig.4.7.

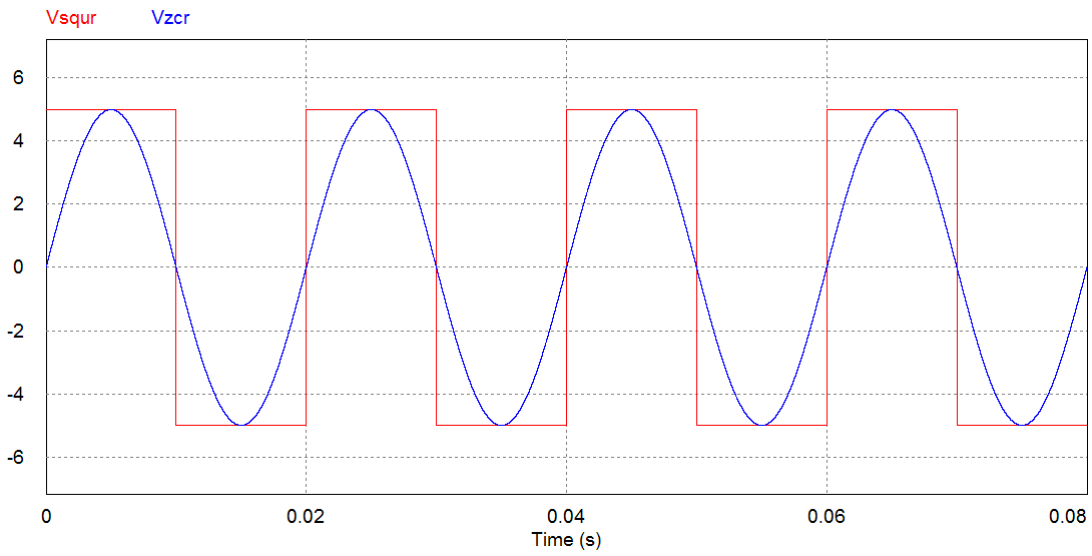


Fig.4.7. Zero crossing detection of Voltage (grid matching)

After inverter and grid connect mutually power starts to transmit from PV array to grid. Now for protection purpose to avoid transmission of power when grid is down due to unavoidable circumstances a relay circuit is employed to trip inverter circuit from grid at this particular situation. A current transformer takes measurement if any fault is occurred at grid relay circuit will be trip and circuit breaker will isolated inverter from grid. Thus measurement and protection purpose of inverter will be served.

The grid synchronization is matched through by following stages:

- As buck input is sampled from grid and buck output is building SPWM for gate signal of H-bridge inverter. Therefore inverter output signal frequency is as same as grid frequency.
- For zero crossing phase detection square wave combination is used with gate signal.Hence phase detection of inverter output is ensured through zero crossing detection.

- To make transformer less inverter boost converter is used which output is 312V and the voltage is used as input of Inverter. Therefore inverter output will be 312V which means RMS220V.
- Thus phase, frequency and amplitude of inverter will be matched with grid utility. And power transmission will be started from inverter to grid utility.

CHAPTER-5

RESULT AND DISCUSSION

5.1 Simulation Result

Fig. 5.1 shows the simulated output voltage waveform that is non-sinusoidal which isdistorted, contains excessive harmonics. Thus, a low pass T-LCL filter is employed atthe output terminal of the inverter to reduce the harmonics.

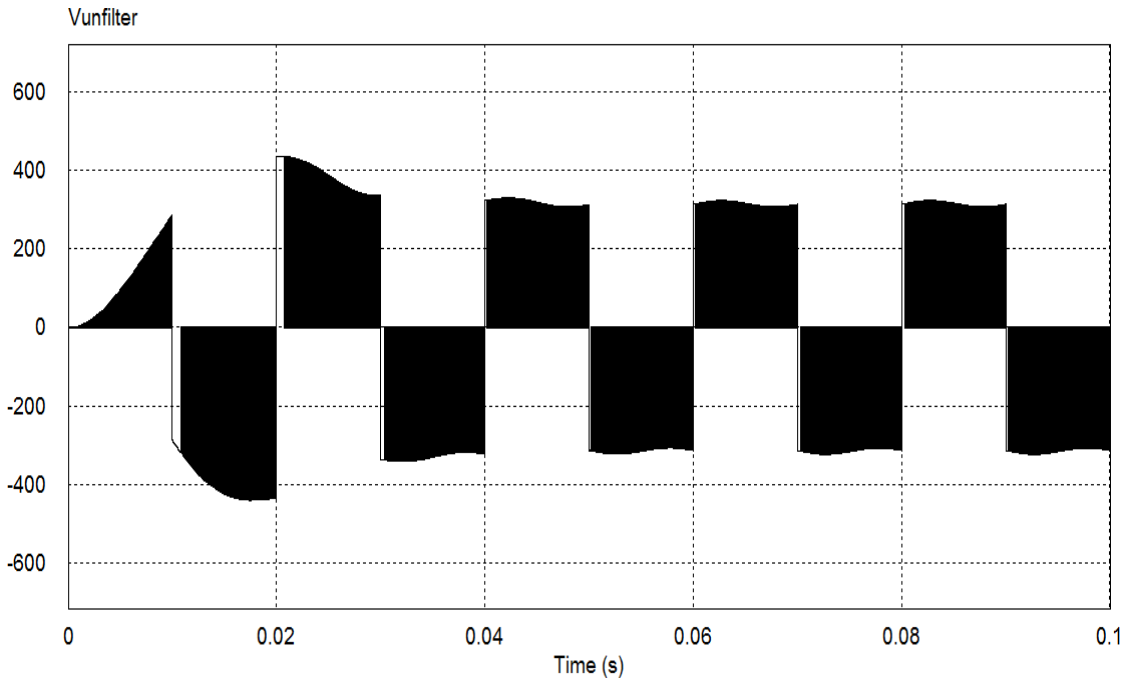


Fig.5.1. Output voltage waveform without filtering in PSIM

After filtering, we obtained 220V (RMS), 50Hz pure sine wave output voltage and current waveform that is shown in Fig. 5.2 and Fig. 5.3. The proposed design helps the output voltage and current to become stable after single cycle.

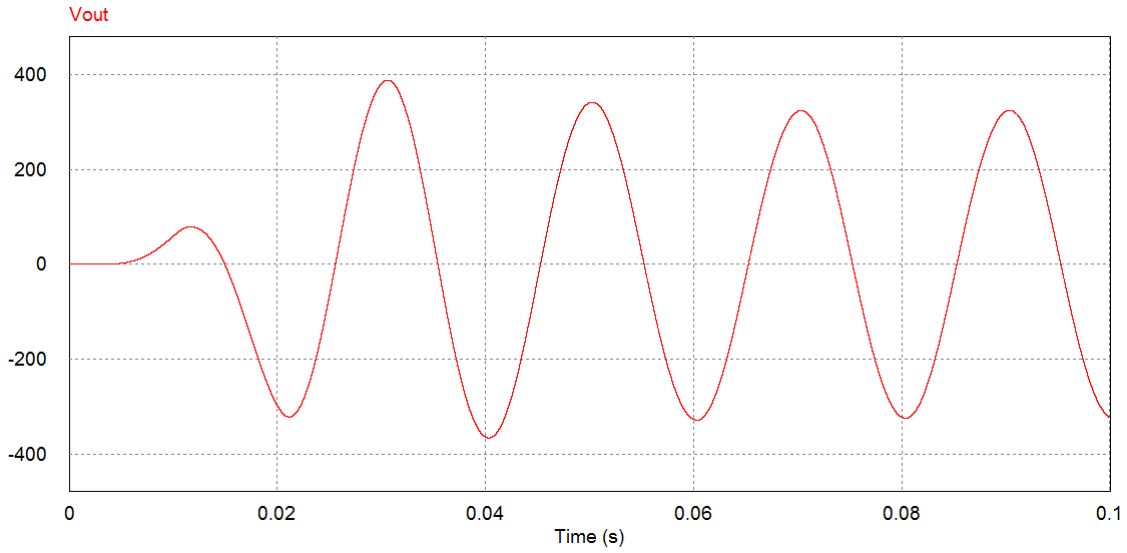


Fig. 5.2 Output voltages after filtering in PSIM

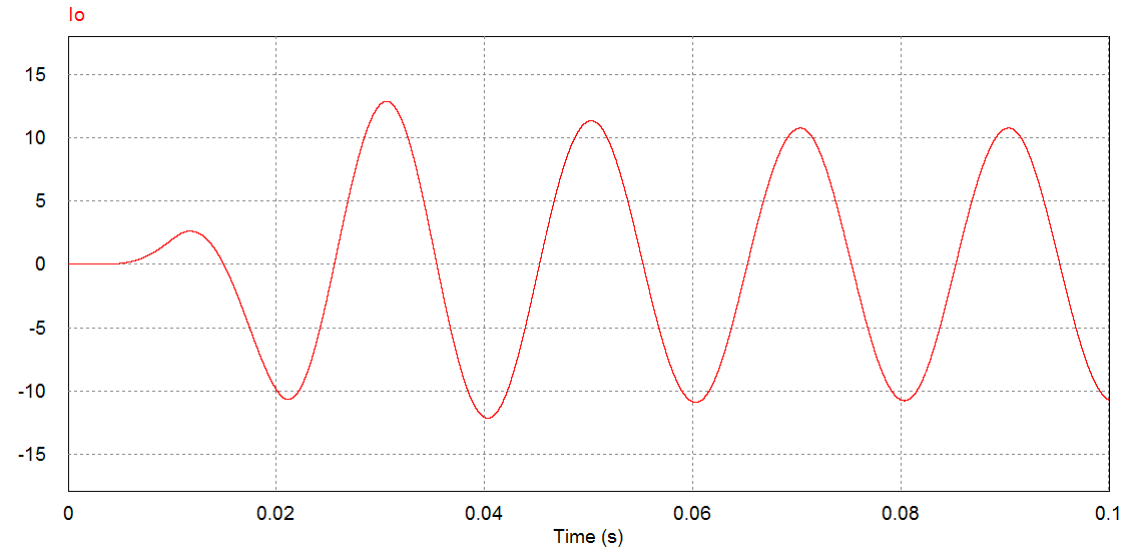


Fig.5.3. Output current waveform in PSIM

Fig. 5.4 presents the FFT analysis of output voltage unfiltered and filtered condition. The fast Fourier transform ensures that unfiltered inverter output has harmonics with mentioned value but filtered output has only fundamental harmonics which lies with in 50Hz and rest of harmonics are negligible.

After filtering the output has low level of THD less 0.1% because the proposed circuit is totally transformer less.

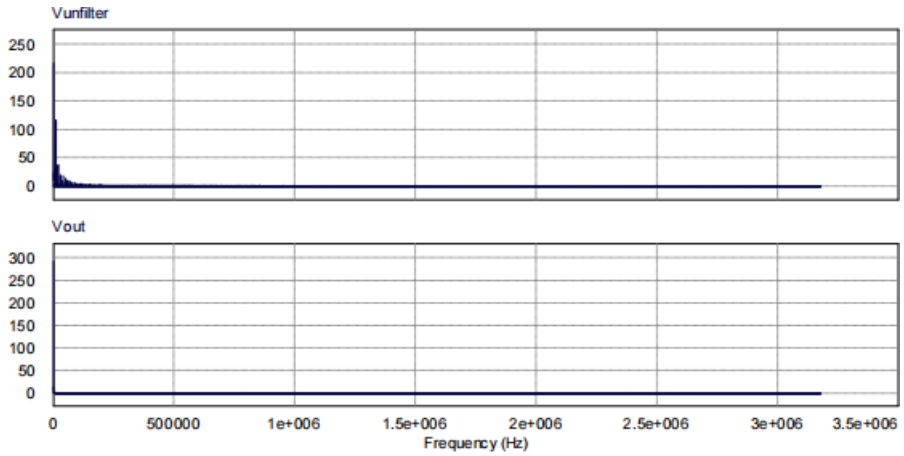


Fig.5.4. Output Voltage's FFT unfiltered and filtered condition in PISM

Fig.5.5 represents output currents with its FFT. Where again FFT demonstrates that fundamental harmonic component lies at 50 Hz and rest of them are eliminates.

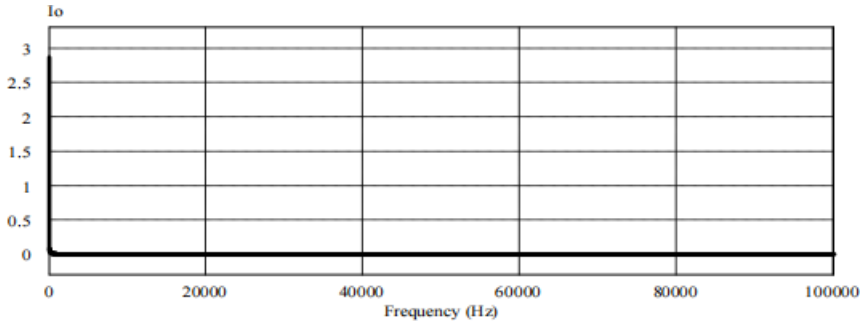
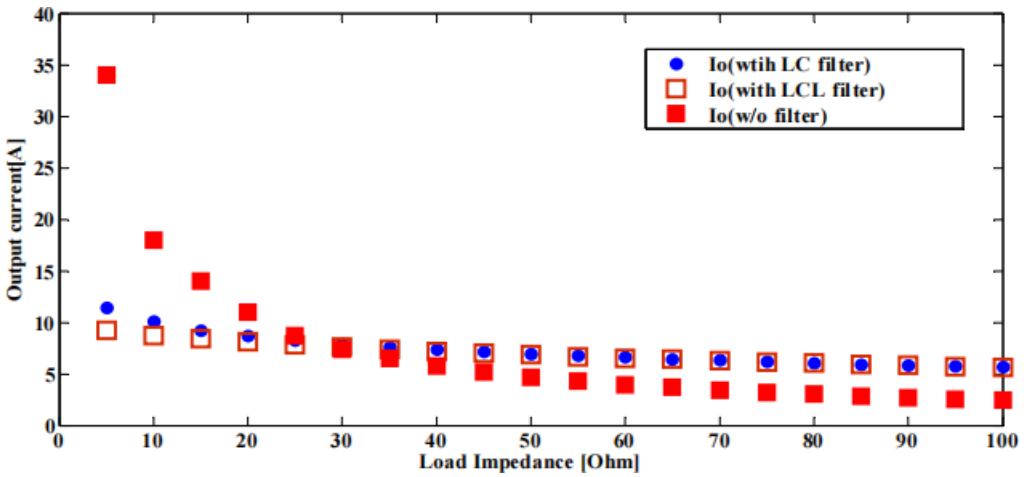


Fig.5.5. Output current's FFT in PSIM

5.2 Inverter Output current

The peak value of the inverter output current is an important factor in designing the inverter stack size. The inverter current rating is normally determined by the filter impedance and the rated load impedance in a steady state. The output current should maintained constant irrespective of load on the inverter and the output voltage is force to change..Therefore to maintain constant output current T-LCL filter is employed. It is found from filter equation output current of the inverter does not depend upon load.

Fig.5.6. Output current vs. load impedance



Here the load impedance was varied from 5Ω to 100 Ω by considering characteristics impedance Z0=20 Ω and current was measured from load without applying any filter circuit. Same procedure was applied for LC filter and T-LCL filter. It was observed that current across load without filter varying in a quite large range whereas in LC filter for varying load current changed in low scale and in T-LCL filter current is quite constant, which ensures longevity of appliances applied across the load of T-LCL filter and the graph is used data of Table5.1.

Table-5. 1 Inverter data for graphical representation.

Load value	Pout [LCL filter]	Pin [LCL filter]	Io	Pin [LC filter]	Pout [LC filter]	η% [LC]	Io	Io /wo filter	η% [LCL]
5	651	706	11.42	427	456	93.64	9.24	34	92.2
10	1021	1070	10.1	766	799	95.86	8.75	18	95.42
15	1286	1331	9.26	1061	1101	96.36	8.41	14	96.61
20	1513	1563	8.7	1318	1366	96.5	8.11	11	96.85
25	1708	1771	8.26	1543	1602	96.31	7.85	8.7	96.7
30	1883	1956	7.92	1742	1812	96.13	7.62	7.42	96.27
35	2041	2125	7.63	1919	2002	95.68	7.4	6.48	96
40	2185	2281	7.39	2077	2174	95.53	7.2	5.75	95.79
45	2313	2424	7.17	2220	2331	95.23	7.03	5.17	95.42
50	2432	2558	6.97	2348	2475	94.86	6.86	4.69	95.07
55	2540	2682	6.79	2464	2607	94.51	6.69	4.3	94.7
60	2639	2798	6.63	2570	2730	94.13	6.54	3.97	94.31
65	2729	2905	6.47	2666	2844	93.74	6.41	3.68	93.94
70	2813	3008	6.39	2754	2950	93.35	6.27	3.43	93.51
75	2888	3102	6.2	2834	3049	92.94	6.14	3.22	93.1
80	2957	3191	6.08	2907	3142	92.52	6.03	3.02	92.66
85	3023	3277	5.94	2975	3230	92.1	5.91	2.86	92.24
90	3096	3373	5.86	3042	3319	91.65	5.81	2.71	91.78
95	3166	3466	5.77	3112	3412	91.2	5.71	2.57	91.34
100	3236	3561	5.68	3184	3509	90.73	5.64	2.45	90.87

5.3 Inverter Efficiency

Efficiency means ratio of output and input. And by varying load it was monitored that the efficiency of T-LCL filter was higher than the efficiency of LC filter. The efficiency versus load impedance for LC and T-LCL filter is shown in Fig.5.7 and the graph is used data of Table5.7.

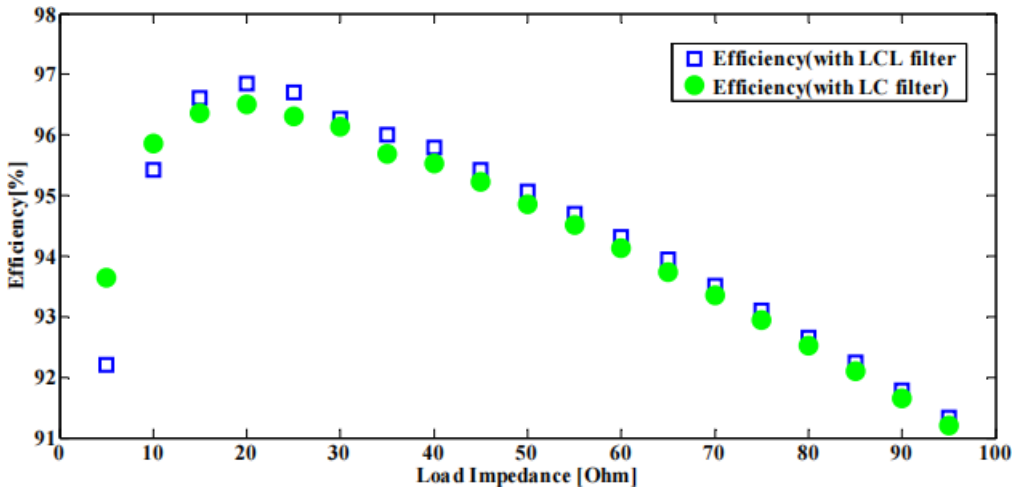


Fig.5.7. Efficiency vs. Load impedance

It is found that the proposed transformer- less GTI is highly efficient while it is transmitting power up to around 1000W to 2400W. At that time inverter efficiency is about 95% and in characteristic impedance the efficiency is 96.7% and when output RMS voltage is 220V and load impedance is 30Ω inverter efficiency is 96.3%.

By analysis PV array system, the paper proposed a dual-stage intelligent PV system, which is similar to modular configuration topology. In an intelligent PV module instead of interconnection between modules they are interconnected with associated DC-DC converter for MPPT tracking which ensures optimal operations of PV module.

Various MPPT algorithms exist in different literatures. This research is proposed perturb and observe (P&O) method to extract maximum possible power from solar panel. A dual stage Boost power converter is proposed instead of transformer which will be helped the whole system.

To make highly efficient, cost effective and light weighted and the whole system efficiency will be rise up to 96.7% with less than 0.01% THD. To make the inverter grid-tie a dual-stage Buck power converter is proposed in this research proposal.

CHAPTER-6

CONCLUSION AND FRAME WORK

6.1 Conclusion

In looking at the components selected and the simulations created before the actual construction of the inverter, everything was built in mind for the purpose of efficiency and keeping power losses to a minimum. In this paper design of a transformer-less grid-tie inverter using new sinusoidal pulse width modulation along with immittance conversion topology and dual stage boost converter and dual stage buck converter have been presented. The simulation results obtained were quite satisfactory and the frequency obtained was in line with the grid. A pure sinusoidal output waveform was obtained and the output current did not change much with the change in the load impedance. The proposed inverter is suitable for constant current load or a dynamic load. It can be conclude that the proposed inverter circuit proved that it is a highly efficient an d cost effective product for renewable energy . This project is a stepping stone to a cheaper and efficient pure sine wave inverter, by using the data collected in this report as well as the schematics and recommendations the product produced here can be improved upon.

A dc–ac voltage source converter has been proposed and studied both theoretically and experimentally. According to our opinion, the boost inverter is suitable for applications where the output ac voltage needs to be larger than the dc input and can offer economic and technical advantages over the conventional VSI.

6.2 Future work

The proposed design can be turned into a fully functional grid - tie inverter for establishing connection between the source and the grid for sending power to an electrical grid. The hardware of the proposed grid-tie inverter would also be constructed with the help of a micro controller and the experimental results would be compared with the ones obtained from the simulation. The simulation results would also be extended in order to expand the horizon of the research.

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Single-Phase Two-Stage Transformerless Grid-Connected Inverter For Photovoltaic Applications

Naser Vosoughi Kurdkandi
Department of Electrical Power Engineering and Mechatronics
Tallin University of Technology
Tallin, Estonia.
naser.vosoughi@taltech.ee

Milad Ghavipanjeh Marangalu
Electrical and Computer Engineering Department
University of Tabriz
Tabriz, Iran.
milad.ghavipanjeh@yahoo.com

Tala Hemmati
Electrical and Computer Engineering Department
University of Tabriz
Tabriz, Iran.
talahemmati@tabrizu.ac.ir

Seyed Hossein Hosseini
Electrical and Computer Engineering Department
University of Tabriz
Tabriz, Iran.
hosseini@tabrizu.ac.ir

Oleksandr Husev
Department of Electrical Power Engineering and Mechatronics
Tallin University of Technology
Tallin, Estonia.
oleksandr.husev@taltech.ee

Arash Khsokhbar-sadigh
School of Electrical Engineering and computer scince Department
Pensylvania State University
Pensylvania, USA.
kzs1012@psu.edu

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***Abstract*—This paper introduces a single dc source five-level grid-tied photovoltaic (PV) inverter. In the proposed topology generates a five-level output voltage waveform using only one input dc source. It causes reduction in the overall size and cost. In addition, the dc-dc buck-boost converter is applied to regulate the voltage of the utilized capacitor around it's reference value. The adjusted capacitor voltage leads to high quality output voltage and current. The output five-level voltage is favorable in high voltage applications and it generates lower total harmonic distortion (THD) in comparison with three-level inverters. In addition to these advantages, the presented topology is capable of providing reactive power supporting which is essential according to grid regulations. Peak current control (PCC) method is used to control both active and reactive powers. Also, in the in order to generate the switching gate pulses of the introduced inverter the PCC strategy is applied. In addition, a completely controlled sinusoidal current can be pumped to the power grid. In order to highlight the advantages of the proposed system, the proposed inverter is compared with other topologies. The effectiveness of the introduced configuration is validated by MATLAB/Simulink when, the proposed topology is connected to the power grid. Finally, the paper is concluded.**

Keywords—multilevel inverters, grid-connected inverters, two-stage, reactive power, dc-dc boost converter, PCC strategy.

I. INTRODUCTION

Multilevel inverters have taken considerable attention during last decades in renewable energy systems. Their staircase output voltage, close to sinusoidal waveform, results in lower THD. Furthermore, they require components with low voltage stress and mitigate electromagnetic interference. To benefit from these advantages, researchers have introduced many structures. Cascaded H-bridge (CHB), neutral point-clamped (NPC) and flying capacitor (FC) converters form the main dc-ac multilevel topologies each structure has its own pros and cons [1-3]. PV grid-connected multilevel inverters, as the main interfaces between the PV panels and the power system, should meet the serious grid regulations imposed by system operators which needs sophisticated control process [4-6]. Usually, an extra dc-dc converter [7-9] is added to perform some tasks along with the main dc-ac multilevel inverter. It leads to two-stage scenario and facilitates the control scheme efficiently though increasing the overall size and volume. It improves the MPPT scheme and the harvested energy even in low values of input voltage resulting from low solar irradiance. This reference points to economic importance of connecting 1500VDC inverter to 800VAC grid with a dc-dc converter, while it is not mandatory in 400VAC. In [10], it is emphasized that a dc-dc stage is necessary in micro inverters. In [11], the dc-dc buck converter is used to regulate the input dc-link capacitors voltage. In this way, the input voltage is balanced and the output voltage has no extra harmonics. Reference [11] describes the MPPT control method through a dc-dc buck converter in a PV stand-alone system. In [12], the dc-dc boost converter tackles the problem of voltage reduction under heavy loads in switched-capacitor based cascaded H-bridge multilevel inverter.

On the other hand, in two-stage models, the dc-ac inverter usually is controlled in a way that it satisfies the grid standards. One of the principle requirements in PV grid-tied multilevel inverters is controlling active and reactive power[13]. Consequently, it is vital to design a structure to be capable of exchanging active and reactive power with the grid and a convenient control procedure is necessary. Reference [13, 14] introduces PCC as a simple way to inject/absorb reactive power.

In this paper, a five-level two-stage inverter is presented. The dc-dc stage is applied in the proposed structure to adjust the dc link voltage while MPPT and the dc-ac conversion is done in the second stage. PCC technique is applied which makes the topology capable of providing reactive power [15]. In the next section, the structure and the switching method will be completely described. In section III, the control system of the proposed topology will be introduced. Section IV, presents a comparison of the proposed inverter with some other topologies. In order to validate the performance of the proposed topology, simulation results are presented in section V using MATLAB/Simulink. Finally, the overall work is concluded in section V.

II. THE PROPOSED STRUCTURE AND THE OPERATION MODES

The introduced a single dc-source five-level inverter is indicated in Fig. 1. Considering this figure, the proposed topology composes of two main parts: the buck-boost dc-dc converter, and five-level inverter. The dc-dc buck-boost converter concludes one unidirectional power switch with anti-parallel diode, one power diode (D_b), one capacitor (C_b) and one inductor (L_b).In the proposed two-stage topology, the dc-dc converter is applied to balance the voltage of capacitor C_b around it's reference value. The five-level inverter has six power switches with antiparallel diodes ($S_1 \sim S_6$), two power diodes (D_1, D_2). The switching states of the proposed five-level inverter is presented in Table I. considering this table, in order to generate each output levels only two power switches are in ON-state. By assuming the same polarity for grid voltage and injected grid to the current, six operation modes can be described for the proposed two-stage inverter. The operation modes of the proposed five-level inverter are presented in Fig. 2(a)-(f).

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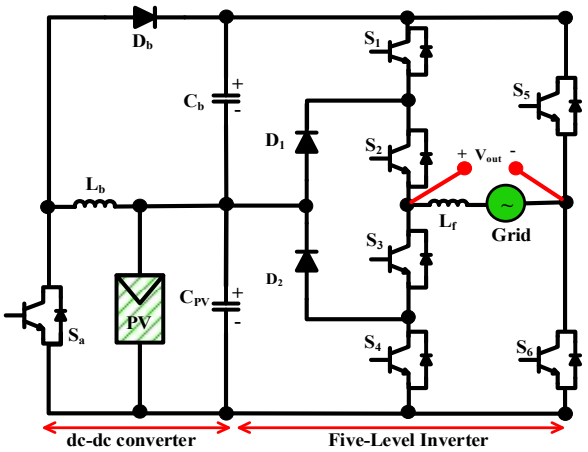


Fig. 1. The proposed two-stage five-level inverter

TABLE I. Switching States of the proposed multilevel inverter

Switching States								V_{out}
S_1	S_2	S_3	S_4	S_5	S_6	D_1	D_2	
on	on	off	off	off	on	off	off	$2V_{dc}$
off	on	off	off	off	on	on	off	V_{dc}
off	off	on	on	off	on	off	off	0^+
on	on	off	off	on	off	off	off	0^-
off	off	on	off	on	off	off	on	$-V_{dc}$
off	off	on	on	on	off	off	off	$-2V_{dc}$

Positive half cycle:

A. First operation mode

The equivalent electrical circuit of the first operation mode is shown in Fig. 2(a).considering this figure, during this mode the switches S_3, S_4, and S_6 are in ON-state. Also, the each utilized power diodes (D_1 and D_2) are disconnecting. So that the zero level of output voltage waveform during positive half cycle is generated.

B. Second operation mode

The second operation mode of the proposed inverter during positive half cycle is illustrated in Fig. 2(b). In the first operation mode, the switches S_2 and S_6 are turned on. The diode D_1 is in forward bias. So that the PV panel is in series with the power grid. Therefore, the output voltage becomes V_{dc} .

C. Third operation mode

The electrical circuit of the third operation mode is shown in Fig. 2(c). Considering this figure, the switches S_1 , S_2 and S_6 are turned on. Therefore the capacitor C_b and C_{PV} is in series and the stored energy of these capacitors is injected to the output. So that, the output voltage of inverter is equal to $2V_{dc}$.

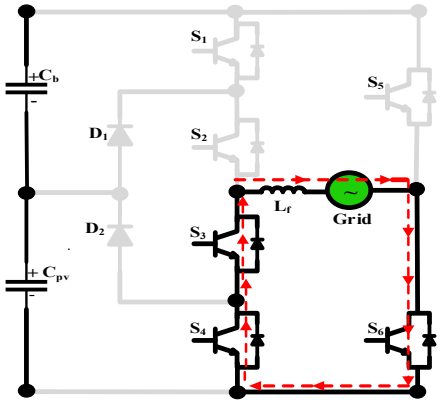
Negative half cycle:

D. Forth operation mode

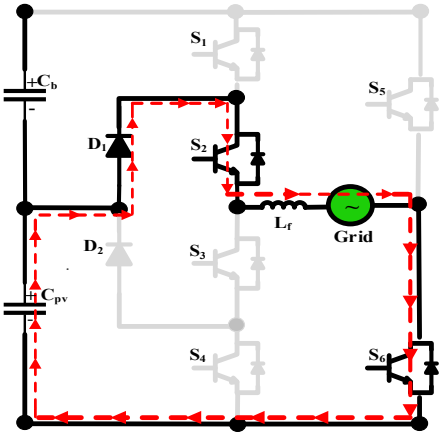
The electrical circuit of the forth operation mode is indicated in Fig. 2(d). Considering this figure, the witches S_1, S_2 and S_5 are in ON-state. So that, during the negative half cycle the zero level of output voltage waveform is generated.

E. Fifth operation mode

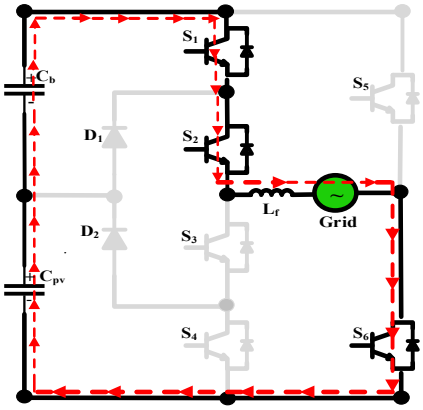
The electrical equivalent circuit of the fifth operation is indicated in Fig. 2(e). Based on this figure, in order to generate first level during negative half cycle of the output voltage waveform, the power switches S_3, and S_5 should be in ON-state. Also, in this mode the power diode D_2 is connecting. So that, the output voltage is equal to $-V_{dc}$.



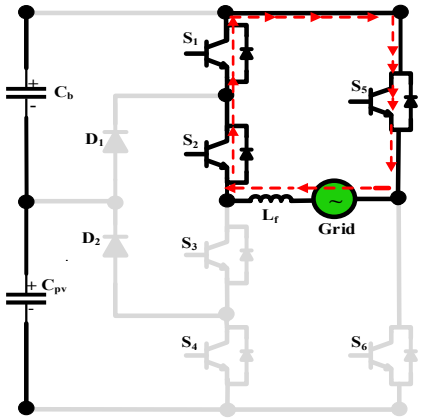
(a)



(b)



(c)



(d)

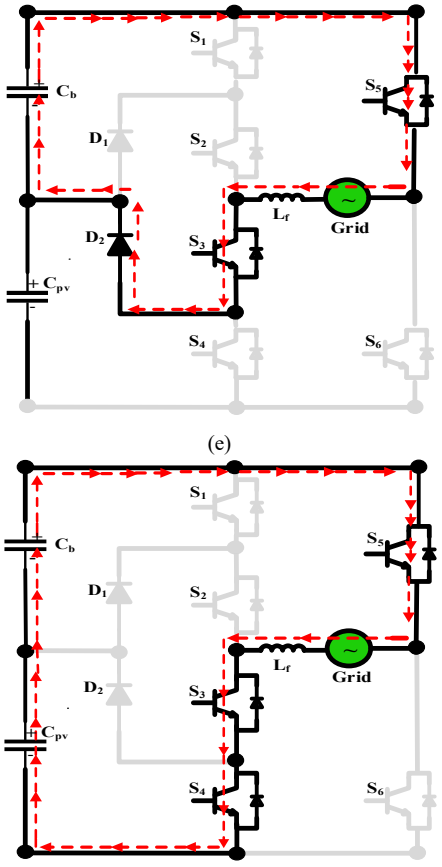


Fig. 2. Operation modes of the proposed five-level inverter

F. *Sisxth operation mode*

The electrical circuit with injected grid current path is indicated in Fig. 2(f). With respect to this figure, the switches S_3, S_4 and S_5 are in ON-state. Also, during this mode both of the utilized diodes are in disconnected mode. So that, the second level of the output voltage waveform of the proposed inverter during negative half cycle is generated. Therefore, the output voltage of the inverter is equal to $-2V_{dc}$.

III. CONTROL SYSTEM OF THE PROPOSED TWO-STAGE INVERTER

In this section, the simple control strategy utilized for the dc-dc buck-boost converter and also the applied peak current control method for five-level inverter is described.

A. *Control method of the buck DC-DC converter*

As mentioned, the dc-dc converter is applied to adjust the capacitor C_b voltage. So that, the simple control method shown in Fig. 3(a) could be used. Based on this figure, the measured voltage of the capacitor C_b (V_{Cb}) is subtracted from its reference value (V_{ref}). A proportional-integral (PI) controller is then applied to generate the duty cycle of the dc-dc converter from the voltage error (V_{error}). As the duty cycle is generated, the switching signal could be generated by comparing the output signal of PI controller with a high-frequency triangular. It should be noted that the duty cycle is between 0 and 1, the high-frequency waveform also oscillates between 0 and 1.

B. *Control system of the proposed inverter*

Fig. 3(b) indicates the control block diagram based on PCC technique to trigger the power switches and also adjust the active and reactive powers. Due to the use of photovoltaic panel as the input voltage source, maximum power point tracking is required. Among different methods available, conventional Perturb & Observation (P&O) technique has been applied since it is simple. By measuring the grid voltage amplitude and phase, P&O method gives the maximum power. A phase locked loop (PLL), as a synchronization unit, is used to detect the grid voltage phase.

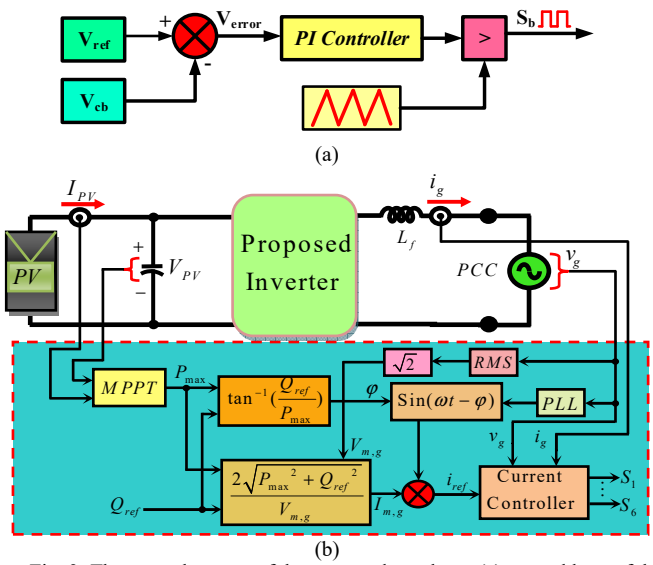


Fig. 3: The control system of the proposed topology: (a) control loop of the applied dc-dc converter (b) PCC control system of the inverter

Filter-based PLL systems like Enhanced PLL (EPLL) [9] or Second Order Generalized Integrator (SOGI) [10] are proposed in this part based on fast and dynamic capability of current injection to the grid. Then, according to the required active and reactive power, the amplitude and phase of reference current (I_{ref}) are defined. In the next stage, the current passed through the L-type filter, named L_f, is measured as the grid current (i_g). In the PCC technique, I_{ref} is compared with i_g in a sampling time of T_{sample} which is half of the maximum switching frequency ($1/2f_s$), and the result provides the signal of power switches gates. The performance of this method depends on the polarity of the grid voltage (V_g) and it causes the injected current to track a sinusoidal waveform of reference current correctly. It is worth mentioning that there is no Proportional-Resonant (PR) or Proportional Integrator (PI) controller in this control block. Therefore, the current injected to the grid is fast enough under dynamic grid condition. Fig. 3(a) depicts the control method which is applied to adjust C_b voltage. Firstly, the voltage across C_b is measured (V_{cb}). Then, it is subtracted from reference voltage. The difference (V_{error}) is tuned by a PI block and is compared with a triangular carrier waveform. In this way, the gate signal of S_b is generated with a proper duty cycle to charge the boosting capacitor.

IV. COMPARISON STUDY

Table II investigates some five-level inverters from the view point of boosting capability and device count. Similar to the proposed structure, references [16] and [17] use single dc supply. However, they use more power switches for the same output voltage levels which is a considerable negative property in terms of power loss.

Moreover, ref. [16] fails to boost the voltage. On the contrary, ref. [18] applies no diode or capacitor while the introduced topology possesses three power diodes and two capacitors. It does not take noticeable attention when considering the boosting feature and input voltage source count. References [19], [17] and [20] can increase the amplitude of the output voltage. In return, the devices number remains a concern. Overall, this table confirms the strength of the suggested five-level inverter in comparison with other ones regarding the above-mentioned features.

TABLE II. COMPARISION OF THE PROPOSED TOPOLOGY WITH OTHER FIVE-LEVEL INVERTERS

Topology	Switches	Diodes	Capacitors (Without output filter)	DC-Sources	Inductors (Without output filter)	Boosting capability
[18]	8	-	-	2	-	no
[19]	8	7	2	3	3	yes
[16]	12	-	3	1	-	no
[17]	12	-	4	1	-	yes
[20]	8	4	2	2	2	yes
Proposed	7	3	2	1	1	yes

V. SIMULATION RESULTS

The validation of the proposed topology and the control method is tested through simulation with MATLAB/Simulink. In the simulation, the five-level inverter is connected to the power grid. Leading, lagging and unity PF are considered to verify the PCC method in active injecting reactive power to the grid. The capacitance of the utilized capacitor C_b is equal to $2200\mu F$. Also, the magnitude of the input dc source is considered 200V. The inductance of the output filter is about 3mH (L_f=$3mH$). Fig. 4 (a) shows the voltage across capacitor C_b. Considering this figure, the voltage of capacitor C_b is balanced to 200V. Also, the five-level output voltage waveform of the proposed inverter with grid voltage waveform is illustrated in Fig. 4(b). With respect to this figure, the peak value of the output voltage is equal to 400V. In addition, the inverter output voltage and injected gird current waveforms are presented under unity power factor (PF=1), leading PF and lagging PF in Fig. 5(a), (b) and (c), respectively. Considering this figure, the peak value of injected grid current is equal to 6A. So that, the value of injected power grid is equal to 933W. Also, from Fig. 5, it can be seen that the proposed inverter has good tracking ability of the reference current. Furthermore, the grid voltage waveform along with injected grid current are depicted under PF=1, leading PF and lagging PF are shown in Fig. 6(a), (b) and (c), respectively. Considering this figure, the proposed inverter supports the reactive power. Also, it can be seen that the proposed inverter which uses the PCC strategy can inject the sinusoidal current under different conditions of PF.

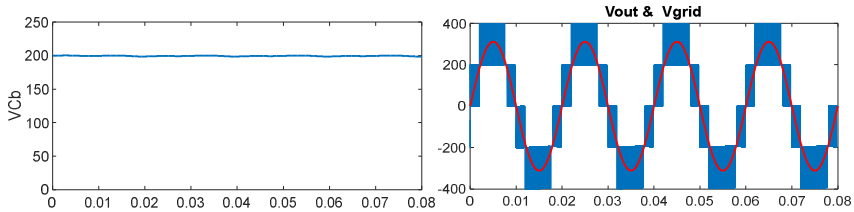


Fig. 4. Simulation results: (a) capacitor C_b voltage, (b) fivel-level outout volatge with grid voltage waveform.

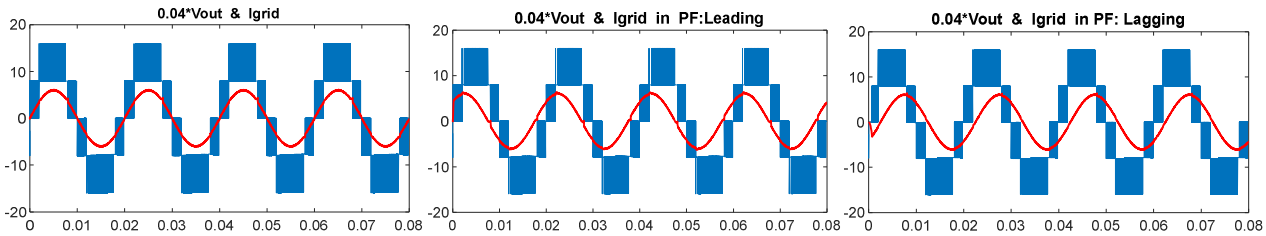


Fig. 5. Five-level output voltage and injected grid current waveforms under different conditions of PF: (a) PF=1 (b) leading PF (c) lagging PF.

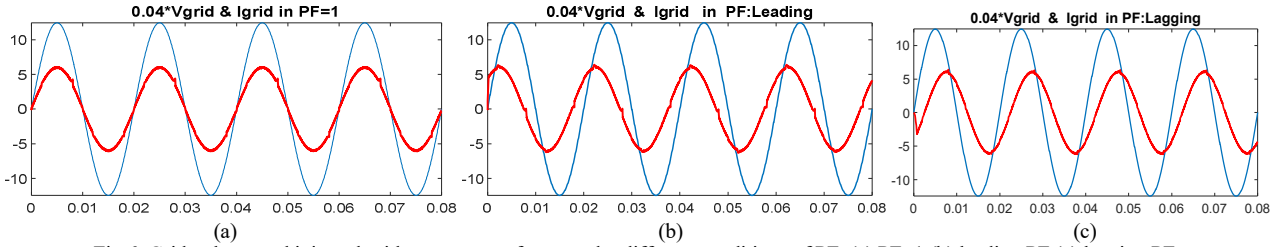


Fig.6. Grid voltage and injected grid current waveforms under different conditions of PF: (a) PF=1 (b) leading PF (c) lagging PF.

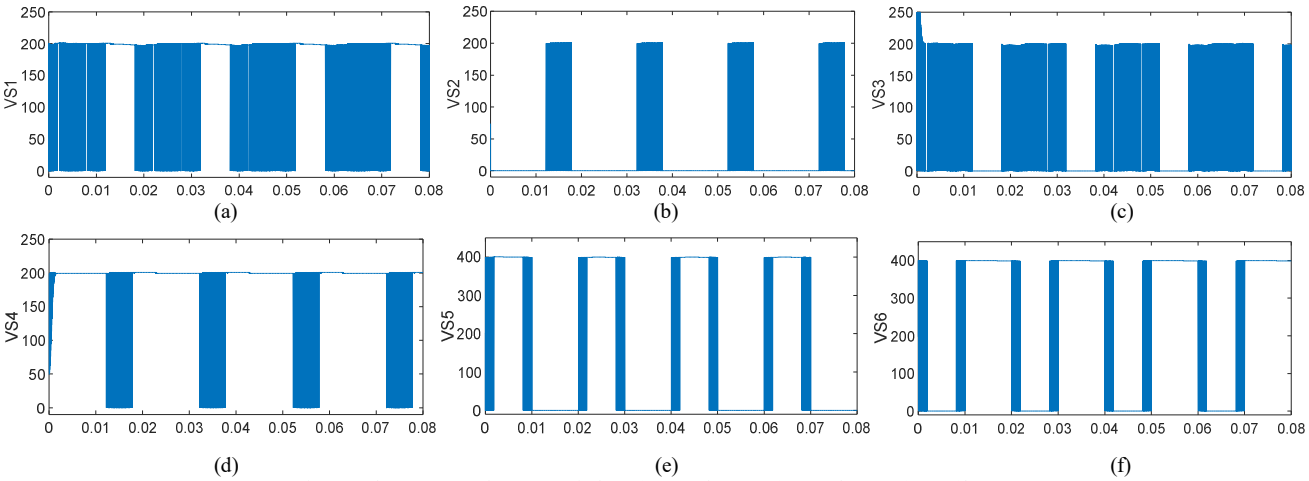


Fig.7. Voltage stress of power switches: (a) V_{S1} (b) V_{S2} (c) V_{S3} (d) V_{S4} (e) V_{S5} (f) V_{S6}.

The voltage stress of the each utilized power switches in the proposed inverter are illustrated in Fig. 7(a)-(f). The voltage stress of switch S_1 is shown in Fig. 7(a). Regarding this figure, it can be understood that the maximum blocked voltage of this switch is equal to input voltage of the inverter (V_{S1}=200V). The voltage stress of the switch S_2 is illustrated in Fig. 7(b). Considering this figure, the peak value of blocked voltage of S2 is 200V. The voltage stress of switch S_3 is depicted in Fig. 7(c). Based on this figure, the peak standing voltage on S_3 switch is 200V. Also, the voltage stress of switches S_4, S_5 and S_6 are shown in Fig. 7(d), (e) and (f), respectively. Considering this figures, the standing voltage of switches S_4, S_5 and S_6 are equal to 200V, 400V, and 400V, respectively. It can be concluded that the maximum blocked voltage of the switch is $2V_{PV}$ or 400V. Also, the total standing voltage of the inverter is equal to $12V_{PV}$.

VI. Conclusion

This paper presented a single dc source five-level grid-tied photovoltaic (PV) inverter. In the proposed inverter, the dc-dc buck-boost converter was applied to adjust the voltage of capacitor. In addition, Peak current control (PCC) method was used to control both active and reactive powers. Also, a completely controlled sinusoidal current can be injected to the power grid by using PCC strategy. In order to highlight the advantages of the proposed system, the suggested inverter was compared with other structures. The effectiveness of the proposed inverter was confirmed by MATLAB/Simulink software.

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A NewTransformerless Inverter for Grid Connected Photovoltaic System With Low Leakage Current

Monirul Islam[1*], Mahamudul Hasan[2], Parvez Akter[1], Md. Mizanur Rahman[3]
[1]Department of Electrical Engineering, University of Malaya, Kuala Lumpur, 50603 Malaysia
[2]Department of Mechanical Engineering, University of Malaya, Kuala Lumpur, 50603 Malaysia
[3]Department of Electrical and Electronic Engineering, CUET, Chittagong, Bangladesh
*E-mail: monir04eee@yahoo.com

Abstract—**Transformer-less inverters are more attractive for grid-tied photovoltaic (PV) system due to its higher efficiency and lower cost. But unfortunately, a leakage current flows through the system. So transformer-less PV inverter have to be tackled carefully. In this paper, a new transformer-less PV inverter topology with low leakage current has been proposed. Proposed circuit structure and detail operation principle are presented in this paper. One additional switch with conventional full H- Bridge and a diode clamping branch make sure the disconnection of PV module from the grid at the freewheeling mode and clamp the short circuited output voltage at the half of DC input voltage. Therefore, the common mode (CM) leakage current is minimized. The relationship between H5 topology and proposed topology has been analyzed in this paper. The proposed inverter topology is simulated by MATLAB / Simulink software to validate the accuracy of the theoretical analysis. Finally, a 1kW prototype has been built and tested.**

Keywords—Common mode voltage, Converter, Grid connected, Leakage current, Photovoltaic, Transformerless.

I. INTRODUCTION

Transformer-less grid-tied inverters have many advantages such as higher efficiency, lower cost, smaller size, and weight. However, there is a galvanic connection between the power grid and the PV module; this may cause fluctuation of the potential between the solar cell array and the ground. This CM voltage V_{cm} shown in equation (1) may induce a leakage current, $i_{Leakage}$ flowing through the loop consisting of the parasitic capacitors (C_{pvg1} and C_{pvg2}), the filter inductors, the bridge, and the utility grid [1]. As a result, the grid current harmonics and losses are increased. A person, who touch the PV array and connected to the ground, may conduct by the capacitive current. At the same time, conducted and radiated interference will be brought in by the ground current [2]. The instantaneous CM voltage V_{cm} in the full bridge topology shown in Figure 1 is defined as follows [3].

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} \quad (1)$$

In order to eliminate the leakage current, the CM voltage must be kept constant during all operation modes and many solutions have been proposed [2-10] as follows:

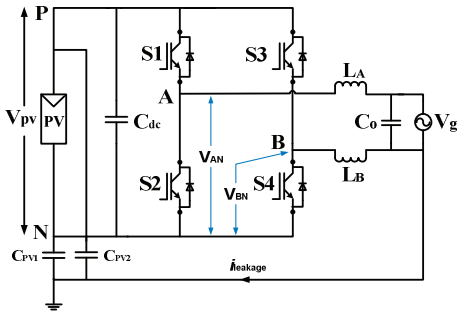

Figure 1. leakage current and parasitic capacitance in transformer-less grid connected PV system

1. Bipolar sinusoidal pulse width modulated (SPWM) full bridge inverter: The bipolar SPWM modulation can be used to solve the problem of the leakage current in the full bridge inverter. This inverter can keep constant CM voltage during the whole operation. However, the current ripples across the filter inductors and also the switching losses are large. Furthermore, it is critical to maintain a good synchronization among the gate signals of the bridge transistors [1].

2. Unipolar sinusoidal pulse width modulated (SPWM) full bridge inverter: The most common modulation used in this topology is unipolar SPWM, because it presents a lot of advantages in comparison to bipolar modulation such as higher dc voltage utilization, lower current ripple at high frequencies, better efficiency, lower electromagnetic interferences emission, etc. However, when unipolar SPWM is employed in the transformer-less conventional full H-bridge inverter; in active mode, the CM voltage V_{cm} is equal to $0.5V_{pv}$ but in the freewheeling mode V_{cm} is equal to V_{pv} or zero depending on the leg midpoints (point *A* and *B* in Figure 1) connected to the positive or negative terminal of the input. Therefore, the CM voltage of conventional unipolar SPWM full-bridge inverter varies with high frequency, which leads to high leakage current [2].

To solve the aforementioned problem, the PV module should be separated from the grid during the freewheeling period and a lot of depth researches have been done to minimize the leakage current. Most of the topology has been proposed in the literature based on the structure of freewheeling path, where a new freewheeling path has been created [2-10].

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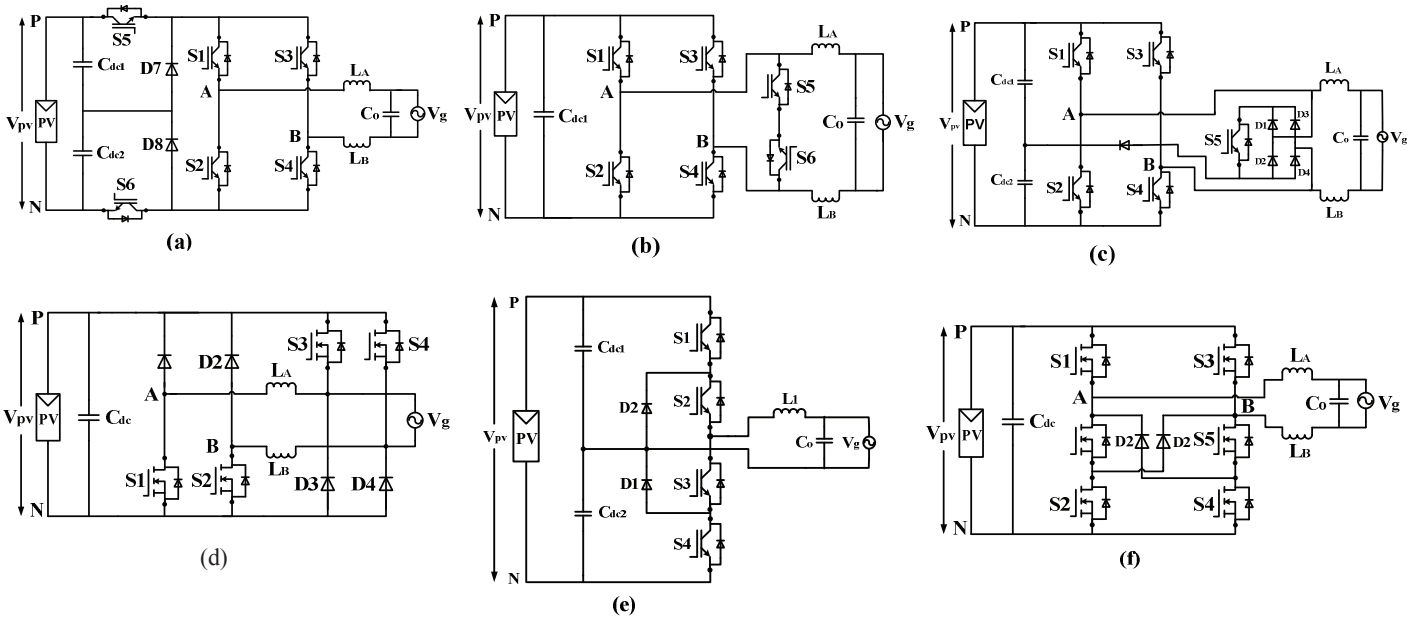


Figure 2. Some existing transformer-less topologies for grid-tied PV inverter (a) H6 topology proposed in [3] (b) HERIC topology proposed in [11] (c) HB-ZVR topology proposed in [7] (d) Dual-Paralleled-Buck inverter topology proposed in [12] (e) NPC topology proposed in [13] (f) H6 type topology proposed in [14]

In this paper, a new structure of transformer-less inverter has been proposed based on H5 topology. The proposed inverter ensures that the freewheeling voltage is clamped to the half of DC input voltage and the PV module is separated from the grid during the freewheeling period by adding an extra switch and a capacitor divider. As a result, the CM mode voltage kept constant during the whole operation period and the generated leakage current is almost zero. Also unipolar SPWM is applied to the proposed topology with three-level output voltage. The efficiency of the proposed inverter, H6 inverter and HERIC inverter are calculated and compared. Simulation and experimental results show that the proposed inverter operates with high efficiency and low leakage current.

This paper is prepared as follows: A review of single phase transformer-less topology is described in section II. CM voltage and leakage current of H5 topology is presented in section III. The proposed improved converter structure and operation principle with unipolar SPWM control scheme are investigated in section IV. Simulation and experimental results are presented in section V and section VI concludes the paper

II. SINGLE PHASE TRANSFORMER-LESS TOPOLOGIES

A. H6 topology:

Full-bridge inverter with dc bypass (FB-DCBP) topology has been proposed in [3] shown in Figure 2(a). Two extra switches are added into the conventional full H-bridge inverter in order to decouple dc bus from the grid during freewheeling period. Also a capacitive divider and two diodes are added to clamp the common mode voltage at half of the dc input voltage. The active voltage vector is achieved by switching S5 and S6 with high frequency. Switches S1 & S4 are switched with the grid frequency and in anti-parallel to S2 & S3, depending on whether the reference voltage is in the positive or negative half period. The output voltage has three levels. The main drawback of FB-DCBP topology is that it suffers more conduction losses from the inductor current flowing through four switches in the active mode [3].

B. HERIC Topology:

Full-bridge inverter with ac bypass (FB-ACBP) topology has been proposed in [11] as shown in Figure 2(b), called Highly Efficient and Reliable Inverter Concept (HERIC). Two switches are added in the ac side to provide the path of freewheeling current. The PV module is decoupled from the grid during the freewheeling period because the switches S1, S2, S3, and S4 are turned-off. The output voltage of the inverter has three levels and the current ripple at output is very lower. The inverter generates constant CM voltage; therefore, the leakage current through the parasitic capacitance is minimized to safe level. Furthermore, the inverter efficiency is kept high because the load current is short circuited via S5 or S6 during the freewheeling period.

C. HB-ZVR Topology:

Another full-bridge inverter topology with ac bypass is proposed in [7], where the midpoint of the dc link is clamped by means of a diode rectifier and one bidirectional switch. An extra diode is used to protect from short-circuiting the lower dc-link capacitor. The operational principle is same as HERIC topology. The zero voltage state is generated by short-circuiting the output of the inverter and clamping them to the midpoint of the dc-link. Three-level output voltage has been achieved by employing unipolar SPWM. The main disadvantage of this topology is the necessity of dead time which increases the distortion of output current [7].

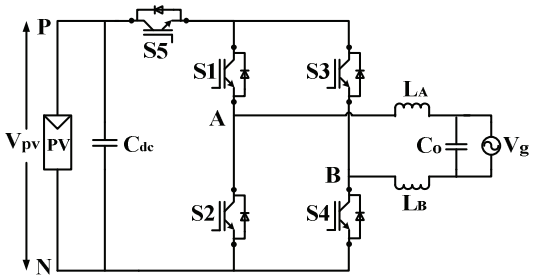


Figure 3. Power circuit structure of H5 topology

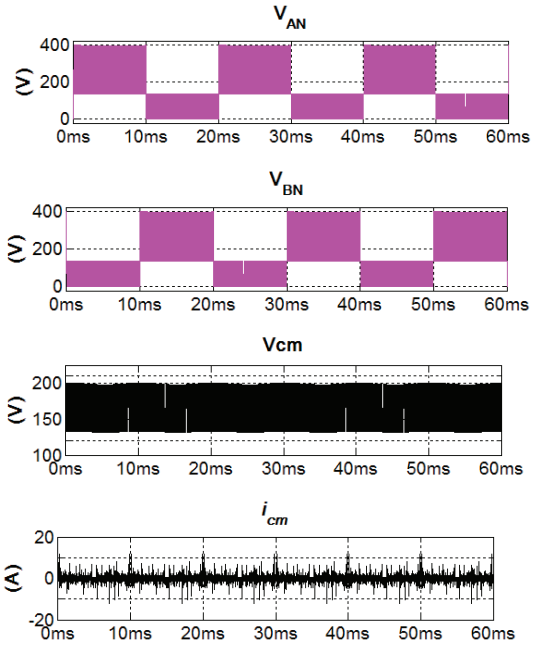


Figure 4. Simulated waveform of V_{AN}, V_{BN}, Vcm, and i_{cm} of H5 topology

III. H5 TRANSFORMER-LESS TOPOLOGY

A. Circuit Configuration and Operation Principle:

An inverter topology proposed in [6] is called H5 topology which is shown in Figure 3. It is made up by adding an extra switch S5 with standard H-Bridge topology. L_A, L_B, and C_o constructs the LCL type filter which is coupled to the grid. In this topology, unipolar SPWM is applied with three-level output voltage. This topology can meet the condition of eliminating CM leakage current. In the positive half cycle of grid current, switch S5 and S4 are commutates with switching frequency. During the zero voltage vectors, S5 and S4 are turned-off and the freewheeling current flows through S1 and the anti-parallel diode of S3. In the negative half cycle, S5 and S2 are commutates with switching frequency and the freewheeling current flows through S3 and the anti-parallel diode of S1.

B. Common Mode Voltage and Leakage Current:

The CM voltage and the leakage current for H5 topology can be calculated using equation (1) and (2).

$$V_{CM} = \frac{V_{Ao} + V_{Bo}}{2} \tag{1}$$

$$i_{CM} = c_{PV} \frac{dV_{CM}}{dt} \tag{2}$$

where, V_{AN} and V_{BN} are the voltages of the full-bridge inverter from mid-point A and B of the bridge leg to the reference terminal N. Figure 4 shows the waveform of CM voltage and leakage current of H5 topology. We can see that a small variation of CM voltage is existed and as a result, a non-negligible leakage current is generated.

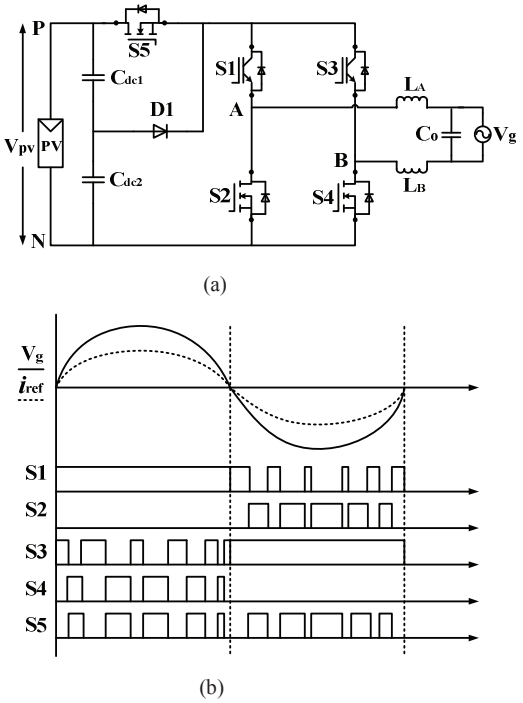


Figure 5. Proposed transformers-less grid-tied PV inverter (a) Proposed circuit configuration (b) Switching signals with unity power factor

IV. PROPOSED TOPOLOGY

A. Circuit Structure:

In order to de-couple the converter from the grid in the freewheeling mode, an extra MOSFET switch is added into the conventional full H-Bridge topology and the two lower high frequency IGBT switches of two phase legs are replaced by MOSFET switches in this paper which is shown in Figure 5(a). Also a diode and a capacitor divider are added to clamp the short circuited output voltage at the mid-point of DC link voltage. L_A, L_B, and C_o constructs the LCL type filter coupled to the grid. This topology can achieve three-level output voltage with unipolar SPWM.

B. Operation Principle analysis:

Grid tied photovoltaic system generally operate at unity power factor. Figure 5(b) shows the waveform of the switching pattern for the proposed topology. The operation principle is very similar to the H5 topology shown in Figure 6. Consequently, four operational modes are proposed that produce the output voltage states of $+V_{PV}$, 0, and $-V_{PV}$.

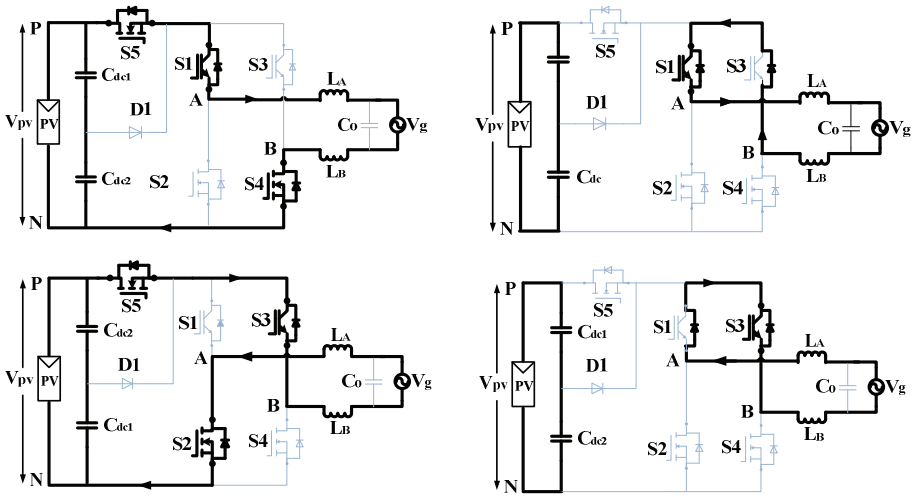


Figure 6. Operation principle of the proposed topology (a) active mode and (b) freewheeling mode in the positive half cycle of grid current (c) active mode and (d) freewheeling mode in the negative half cycle of grid current

1) Mode 1 is the active mode in the positive half cycle of grid current. When S1, S4 and S5 are turned-on, the voltage $V_{AN} = V_{PV}$ and $V_{BN} = 0$, thus $V_{AB} = V_{PV}$ and the CM voltage, $V_{cm} = (V_{AN} + V_{BN})/2 = V_{PV}/2$.

2) Mode 2 is the freewheeling mode in the positive half cycle of grid current as shown in Figure 6(b). The freewheeling current flows through S1 and body diode of S3. In this mode, the freewheeling output voltage is clamped to the half of DC input voltage thorugh diode D1, thus $V_{AN} = V_{BN} = V_{PV}/2$, $V_{AB} = 0$ and the CM voltage, $V_{cm} = (V_{AN} + V_{BN})/2 = V_{PV}/2$.

3) Mode 3 is the active mode in the negative half cycle of grid current. Like as mode 1, when S2, S3 and S5 are turned-on, the voltage $V_{AN} = 0$ and $V_{BN} = V_{PV}$, thus $V_{AB} = -V_{PV}$ and the CM voltage, $V_{cm} = (V_{AN} + V_{BN})/2 = V_{PV}/2$.

4) Mode 4 is the freewheeling mode in the negative half cycle of grid current. When S5 and S2 are turned-off, the freewheeling current flows through S3 and body diode of S1. In this mode, $V_{AN} = V_{BN} = V_{PV}/2$, thus $V_{AB} = 0$ and the CM voltage, $V_{cm} = (V_{AN} + V_{BN})/2 = V_{PV}/2$.

As analysis above, the CM voltage remains constant during the whole operation period of the proposed inverter and equals to $V_{PV}/2$. As a result, the inverter is hardly to generate CM leakage current.

V. RESULTS

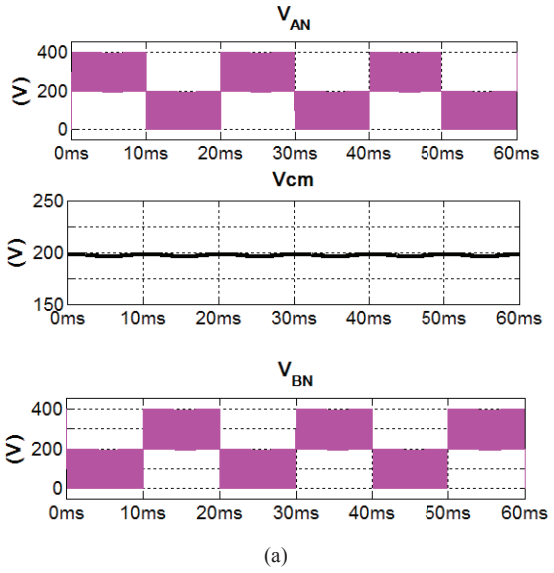
In order to verify the theoretical analysis, the proposed topology has been simulated by MATLAB/Simulink software using the parameters given in Table I. Figure 7 shows the simulated and experimental waveform of V_{AN}, V_{BN}, and Vcm. From figure 7(a), it can be seen that the CM mode voltage kept constant at the half of DC input voltage 200V. As a result, the generated leakage current is almost zero which is shown in Figure 8(c). Experimental Results of CM mode voltage are shown in Figure 7(b), which shows the same characteristics as simulation. Experimental result of leakage current is shown in Figure 9, which shows that the peak and RMS values are successively limited within 45mA and 8mA, respectively.

Figure 8 shows the simulated waveform of grid current, grid voltage, differential-mode voltage, and leakage current. From Figure 8(a) and Figure 9, it is clear that the output voltage and current of the proposed inverter has low harmonic distortion which can meet the requirements of IEEE STD 1547.1™-2005 [15]. The proposed inverter has three-level output voltage $+V_{PV}$, 0, and $-V_{PV}$ which is shown in Figure 8(c). It designates that the proposed topology is modulated with unipolar SPWM with excellent differential-mode characteristics.

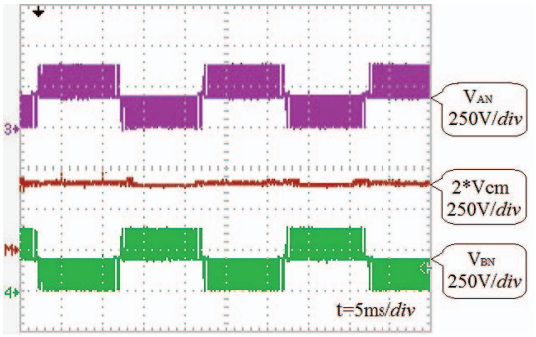
The efficiency comparison among the proposed, HERIC and H6 topologies with the same parameter is illustrated in Figure 10. Note that the presented efficiency diagram covers the total device losses but it does not include the losses for control circuit. It is clear that the efficiency of the proposed topology is higher than the H6 topology and almost same to the HERIC topology.

TABLE I. PARAMETERS USED IN SIMULATION

Inverter Parameter	Value
Input Voltage	400VDC
Grid Voltage / Frequency	230V / 50Hz
Rated Power	1000 W
AC output current	4.1A
Switching Frequency	20kHz
DC bus capacitor	470µF
Filter capacitor	2.2µF
Filter Inductor L_A, L_B	3mH
PV parasitic capacitor Cpv1, Cpv2	75nF



(a)



(b)

Figure 7. Simulated waveform of CM voltage and leakage current (a) V_{AN}, Vcm, V_{BN} (b) i_{cm}

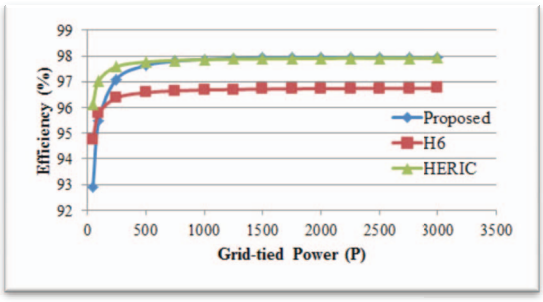
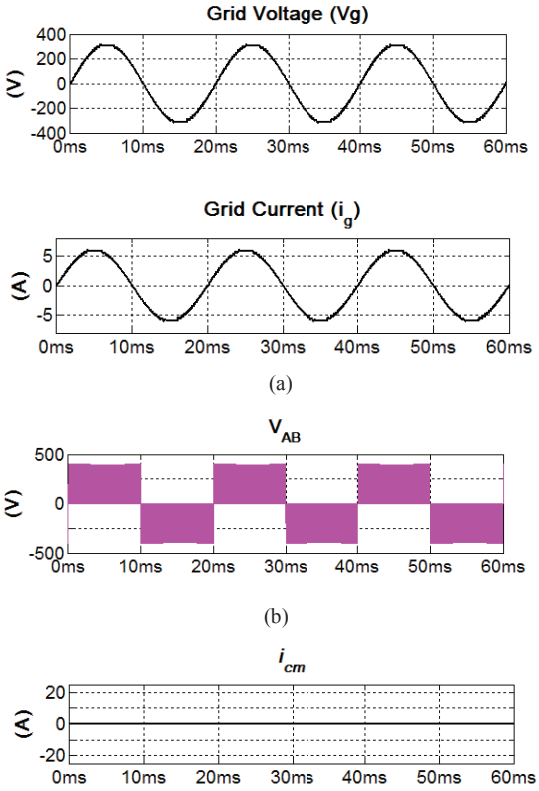


Figure 10. Efficiency comparison of proposed, H6, and HERIC topology



(a)

(b)

(c)

Figure 8. Simulated waveform of output voltage (a) grid voltage and grid current (b) differential output voltage (c) Leakage current

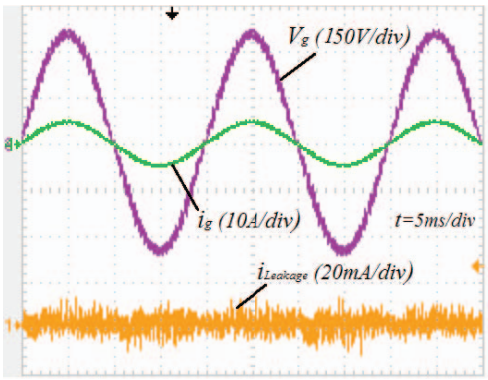


Figure 9. Simulated waveform of output voltage (a) grid voltage and grid current (b) differential output voltage

VI. CONCLUSION

In this paper, a new single phase transformer-less inverter for grid connected PV system have been presented. Also major transformer-less topologies are reviewed based on leakage current, advantages, and disadvantages. It is found that these topologies have some drawbacks such as leakage current and efficiency. However, The CM voltage of the proposed topology is clamped to half of DC input voltage, thus leakage current is well suppressed. The inverter output voltage has three levels by employing unipolar SPWM with good differential mode characteristics. The waveform of output current shows that the proposed inverter can convert the solar power to a high quality ac power to inject into utility grid.

Furthermore, the proposed inverter achieved higher efficiency. Therefore, it can be concluded that the proposed inverter is very suitable for single phase grid connected PV system.

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