1.

Suppose the following processes arrive at the times indicated. The total available memory is 35 units. OS occupies 10 units and the remaining 25 units for user process. Assume all processes are CPU bound and the content switch time is 1.

Process	Arrival Time	CPU Burst Time	Memory Required (Units)
P1	0	5	3
P2	3	3	5
P3	7	9	8
P4	12	10	12
P5	18	16	2
P6	25	2	6
P7	29	8	9

- Calculate the turnaround time for each process using FCFS scheduling policy.
- Draw the memory map if First-fit allocation policy is used and processes are scheduled using FCFS.
- Draw the memory map if Best-fit allocation policy is used and processes are scheduled using FCFS.

2.

Consider a computer system which uses paging. Assume the system also has associative registers.

a. Distinguish logical address and physical address.

b. Explain how logical addresses are translated to physical addresses.

c. Calculate the effective memory access time given:

associative register access time = 50 nanosec.

memory access time = 250 nanosec.

hit ratio = 80%

d. With the above associative register and memory access times, calculate the minimum hit ratio to give an effective memory access time less than 320 nanoseconds.

Why are Translation Look-aside Buffers (TLBs) important? In a simple paging system, what information is stored in a typical TLB table entry? Draw a flow-chart to cover all the situations that arise in the operation of logical memory paging with a TLB.

3.

A computer has 192 bytes of memory organized into 64 byte blocks. The following addresses are accessed in the order specified:

50, 306, 96, 194, 141, 298, 90, 275, 133, 265, 9

How many pages of memory are accessed?

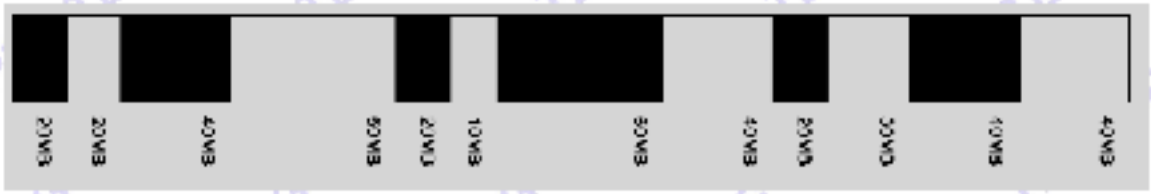
How many frames of memory are accessed?

Calculate the physical memory address in multi-partition memory allocation if base register is 9055 and limit register is 2000 for the following program address:

100, 200, 2002, 300, 324, 5000

4.

a) A system uses a dynamic partitioning scheme, and the current memory configuration is as shown below.



The shaded areas are allocated blocks. The unshaded areas are free blocks. The next three memory requests are for 40MB, 20MB, and 60MB. Indicate the starting address for each of the three blocks using the first-fit, best-fit and worst-fit placement algorithm.

b) Detail the various methods for free space management.

Consider the following free space bitmap block 1000 0000 0000 0000 (the first block is used for the root directory). The system always searched for the free blocks starting at the lowest numbered block. Show the bitmap after each of the following additional actions:

i) File A is written, using 4 blocks

ii) File B is written, using 6 blocks

iii) File A is deleted

iv) File C is written, using 8 blocks

v) File B is deleted.

5.

What do you mean by locality of reference? A student in a compiler course proposes to the professor a project of writing a compiler that willproduce a list of page references that can be used to implement the optimal page replacementalgorithm. Is this possible? Why or why not?

6.

Assume that you have a page-reference string for a process with m frames (initially all empty). The page-reference string has length p; n distinct page numbers occur in it. What is a lower bound and upper bound on the number of page faults for any page replacement algorithms?

7.

What is page fault? Explain the actions taken by the Operating System when page fault occurs. Consider the following page reference string:

1, 2, 3, 4, 2, 1, 5, 6, 2, 1, 2, 3, 7, 6, 3, 2, 1, 2, 3, 6.

How many page faults would occur for the following replacement algorithms, assuming one, two, three, frames? Remember all frames are initially empty, so your first unique pages will all cost one fault each. Is FIFO suffers from Belady's Anomaly?

LRU replacement

FIFO replacement

Optimal replacement

8.

a) Assume we have a memory that have the following holes in increasing memory start address order: Hole1 = 20 KB, Hole2 = 8 KB, Hole3 = 40 KB, Hole4 = 36 KB, Hole5 = 14 KB, Hole6 = 18 KB, Hole7 = 24 KB, Hole8 = 30 KB. Which hole is taken for successive segment requests of 24 KB, 20 KB and 18 KB, if we use:

   First-fit, best-fit, worst-fit

b) Draw up a flow-chart to cover all the situations that arise in the operation of virtual memory paging with a TLB. Ignore the detail of running another waiting process whilst waiting for a missing page to be read in from the swap/paging disk area.

9.

Consider a simple paging system with the following parameters:

- 2^{32} byes of physical memory
- Page size of 2^{10} bytes
- 2^{16} pages of logical address space

1. How many bits are in a logical address?
2. How many bytes in a frame?
3. How many bits in the physical address specify the frame number?
4. How many entries in the page table?
5. How many bits in each page table entry? Assume each page table entry includes a valid/invalid bit.

10.

Consider a demand paging system. We measure the various resource utilizations and see:

CPU utilization 20%

Paging disk 99%

Which of these (if any) should improve the CPU utilization? Why?

- Get a faster CPU.
- Get a bigger disk.
- Get a faster disk.
- Increase the degree of multiprogramming.
- Decrease the degree of multiprogramming.

11.

. When do page faults occur? List the actions taken by the operating system when a page fault occurs. Consider the following sequence of memory references from a 460 bytes size program: 10, 11, 104, 170, 73, 309, 185, 245, 246, 434, 458, 364. (i) Give the reference string, assuming a page size of 100 bytes. (ii) Find the page-fault rate for the reference string in part (i), assuming 200 bytes (2 frames) of main memory is available to the program and a FIFO replacement algorithm. (iii) Calculate the page-fault rate if the page replacement algorithm is LRU.

12.

What is the difference between physical and virtual addresses? Is it reasonable to have the following situations:

(i) physical address space > virtual address space

(ii) virtual address space > physical address space

(iii) virtual address space = physical address space

13.

Consider a system where the virtual memory page size is 2K (2048 bytes), and main memory consists of 4 page frames. Now consider a process which requires 8 pages of storage. At some point during its execution, the page table is as shown below:

Virtual page	Valid	Physical page
0	No	
1	No	
2	Yes	1
3	No	
4	Yes	3
5	No	
6	Yes	0
7	Yes	2

- List the virtual address ranges for each virtual page.
- List the virtual address ranges that will result in a page fault.
- Write the main memory (physical) addresses for each of the following virtual addresses (all numbers decimal): (i) 8500, (ii) 14000, (iii) 5000, (iv) 2100.

b) Consider a system with the following specification:

- Total available physical memory frame: 1200KB
- Frame Size is 4 KB
- Total processes : 6
- The frame needed by each process has the following format (Process ID, Total frame). (0, 40), (1, 60), (2, 100), (3, 20), (4, 80), (5, 100)

Unfortunately the total available frames are limited. The system cannot supply all the requested frames to every process.

i) Determine total frames given to each process if the system uses equal allocation mechanism.

ii) Determine total frames given to each process if the system uses proportional allocation algorithm.

14.

. Explain why sharing a reentrant module is easier when segmentation is used than when pure paging is used. A virtual memory system has a page size of 1024 bytes, eight virtual pages, and four physical page frames. The page table is as follows:

Virtual page Number	Page Frame Number	Validity Bit
0	1	V
1	0	V
2	3	V
3	2	I
4	0	I
5	2	V
6	1	I
7	2	I

- What is the size of the virtual address space? How many bits in a virtual address?
- What is the size of the physical address space? How many bits in a physical address?
- What are the physical addresses corresponding to the following decimal virtual addresses: 0, 3728, 1023, 1024, 1025, 7800, 4096?

15.

What is the difference between physical address and virtual address? A computer has 40 bytes of memory organized into pages with size 10 bytes. The following virtual addresses are accessed in the order specified:

21, 61, 65, 14, 20, 10, 17, 32, 45, 66, 70, 58, 39, 13, 41

How many pages of virtual memory are accessed? How many frames of memory are available?

16.

A computer keeps its page tables in memory. The time required to read a word from the page table is 50ns. To reduce this overhead, the computer has a TLB, which holds 32 (virtual page, physical page frame) pairs and can do a look up in 10ns. On a TLB miss, the OS accesses the memory to get the page table entry and updates the TLB (the update time of the TLB is included in the 50ns of the page table access). What hit rate is needed to reduce the mean access time to 20ns?

17.

Consider a server with two clients running independent multi-threaded databases. Client_1 has paid for 75% of the available CPU resources, while Client_2 has paid for 25%. How would you ensure that each client got their requested (paid for) share of CPU resource?

18.

Consider a system with the following specification:

- Total available physical memory frame: 1200KB
- Frame Size is 4 KB
- Total processes : 6
- The frame needed by each process has the following format (Process ID, Total frame). (0, 40), (1, 60), (2, 100), (3, 20), (4, 80), (5, 100)

Unfortunately the total available frames are limited. The system cannot supply all the requested frames to every process.

i) Determine total frames given to each process if the system uses equal allocation mechanism.

ii) Determine total frames given to each process if the system uses proportional allocation algorithm.

20.

You are designing the memory mapping hardware for a new machine. The memory addressing will have segments that are paged. The machine has a 64-bit virtual address. Each process can have up to 64K (65536) segments, and page size is 64K bytes. The segment tables (ST) and page tables (PT) are stored in main memory. ST's and PT's can start at any byte address. Each segment table entry (STE) points to a page table. Each page table entry (PTE) points to a page in real memory. Each PTE will also have: a "read-enable" bit, a "write-enable" bit, and a bit that is set on each reference to the page.

This machine will support physical memories up to 64 gigabytes.

i. Draw a diagram of this memory map. Show how the pieces of the virtual address are used to reference each of the tables, and to generate the physical address. Indicate the size of each field, where it comes from, and where it is used. Also indicate where page faults or memory protection traps will be indicated.

ii. How large (in bytes) is a full-sized ST?

iii. Is it a good idea to have a "bounds" field in your STE's? Why or why not? Should this bounds field be in units of bytes or pages?

What happens if we double the page size (while still keeping a 64 bit virtual address)?

iv. Now, add a TLB to the memory mapping architecture that described above. This cache should be 4-way set associative and will have 256 rows. Draw a diagram of the TLB, showing the size of each field in the TLB. Indicate how bits of the VA are used for input to the TLB, and describe the outputs from the TLB.

21.

Consider a computer is equipped with associative memory that can hold 16 entries of the page table and can be accessed in 10 nanoseconds. The hit ratio is the percentage of the page table entry can be found in the associative memory. The CPU takes total 130 nanoseconds to search the page entry and access a data item when the page entry is not in the associative memory.

- Find a formula that expresses the effective access time as a function of the hit ratio (h).
- What hit ratio is needed to achieve the effective access time to 82 nanoseconds?

22.

Consider the following factors:

internal fragmentation
process table size
I/O overhead
locality of reference

Which of these factors could be used to argue for a large page size, and which could be used to argue for a smaller page size? Why?

23.

A computer has 192 bytes of memory organized into 64 byte blocks. The following virtual addresses are accessed in the order specified:

50, 306, 96, 194, 141, 298, 90, 275, 133, 265, 9

- How many pages of memory are accessed?
- How many frames of memory are accessed?
- Determine the number of page faults that will occur for the above virtual addresses access, using the following page replacement algorithms: (a) FIFO (b) LRU (c) Optimal. Assume that all page frames are initially empty.

24.

Consider a system with the following specification:

- Total available physical memory frame: 1200KB
- Frame Size is 4 KB
- Total processes : 6
- The frame needed by each process has the following format (Process ID, Total frame). (0, 40), (1, 60), (2, 100), (3, 20), (4, 80), (5, 100)

Unfortunately the total available frames are limited. The system cannot supply all the requested frames to every process.

i) Determine total frames given to each process if the system uses equal allocation mechanism.

ii) Determine total frames given to each process if the system uses proportional allocation algorithm.

25.

Suppose the access times are as follows.

Associative memory Hit:

To read associative memory1ns

To read main memory 6 ns

Associative memory Miss:

To read associative memory 1ns

To add the page number to the page table origin register 2ns

To read page table 6 ns

To read main memory6 ns

(i) Calculate the effective access time for a hit rate of 93 per cent.

(ii) If the page fault service time is 1.2 ms, what is the maximum page fault rate that the system can tolerate without incurring more than 15 percent degradation?