RISC AND CISC

- 19PW13
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* Reduced Instruction Set Architecture (RISC):

Makes Hardware simpler by using an instruction set composed of few basic steps for loading, evaluating and storing operations just like a load command will just load data.

Increases CPU performance by reducing cycles per instruction at cost of number of instructions per program.

Characteristics:

1. Simpler Instruction, hence simple decoding
2. Instruction come under size of one word
3. Instruction take single clock cycle to get executed.
4. More number of general purpose registers
5. Simple Addressing Modes
6. Less Data types
7. Pipeline can be acheived.

* Complex instruction set architecture (CISC)

single instruction will do all loading, evaluating and storing operations. Hence its complex.

. Attempts to minimize no: of instructions per program but at the cost of increase in number of cycles per instruction.

characteristics :

1. Complex instruction, complex decoding
2. Instruction are larger than one word size
3. Instruction may take more than single clock cycle to get executed.
4. Less number of general purpose registers as operations get performed in memory itself.
5. Complex addressing Modes
6. More Datatypes.

EXAMPLE - suppose we have to add 2 8 bit numbers.

- CISC approach - single instruction for this like ADD which will perform task
- RISC approach - programmer will write first load command to load data in registers then use suitable operator and store result in desired location

* DIFFERENCE

	RISC	CISC
1.	Focus on software	Focus on Hardware
2.	Uses only Hardwired control unit	Uses both hardwired and microprogrammed control unit.
3.	Transistors are used for more registers	Transistors are used for storing complex instructions.
4.	Fixed sized instructions	Variable sized instructions
5.	Can perform only register to register arithmetic operations	Can perform REG to REG, REG to MEM or MEM to MEM
6.	Requires more number of registers	Requires Less no: of registers
7.	code size is large	code size is small
8.	Instruction execute in single clock-cycle	Takes more than one clock cycle.
9.	Instruction fit in one word	Instructions are larger than size of one word.