PSG College of Technology, Coimbatore – 641004

Department of Computer Applications

18MX25 Microprocessors and Embedded Systems

Worksheet on CO1 and CO2

1.Generate the machine code for the following instruction.

   MOV CX, [BX + SI + 45H]

2.Determine the contents of registers AX, BX ad CX after execution of the following code.

                        MOV CL,3

                        MOV AX, 7FH

                        MOV BX, 0505H

                        ROL AX, CL

                        AND AH, BH

                        OR BL, AL

3. Explain internal architecture of X86 processor. Discuss in detail how instruction
    pipelining improves the performance. Discuss the various addressing modes supported by
    X86 architecture
4.A String is given as an input. Write an ALP to find the number of characters in that string

and the frequency of occurrence of each character in that string.

5.Why doesn't make sense to use REP prefix with the LODS instruction
6.Explain various parameters passing mechanism supported by 8086 processor with suitable
    example.
7. Write an ALP procedure which implements the below algorithm for a number N between
    1 and 10.
            IF N=1 THEN FACT = 1
            ELSE
                    FACT = 1
            REPEAT
                    FACT = FACT * N
                    DECREMENT N

UNTIL N=0.

8. Explain various parameter passing mechanism in X86.

9. Write a Procedure which removes leading and duplicate blank characters in the string passed by reference through stack. Write an interactive program which reads the input string of text and using the above procedure eliminates the extra blank spaces and prints the changed text as a blinking string. (8) The output of your program should be,

INPUT   :   ####ASSEMBLY   #########   LANGUAGE####   PROGRAM

OUTPUT   :   ASSEMBLY#LANGUAGE#PROGRAM

blank space

10. Write the sequence of command words that are used to initialize an 8259 with a base address of FF10H as follows: edge-triggered; only one 8259; 8086 system; interrupt type 40 corresponds to IR0 input; normal EOI; nonbufferd mode, not special fully nested mode; IR1 and IR3 unmasked

11. Explain sequence of actions performed when an interrupt call occurs?(5)

12. Explain the need for support chips by X86 processor. Explain the block diagram of Programmable Interrupt Controller with different control words and words sent to 8259PIC.

NOTE:

Prepare yourself for test 1 and semester exam

Write in your class work or as assignment and submit the same on reopening date.

Any clarifications you can contact me through mail or whatsapp.