Bitonic Counting Network -Assignment3

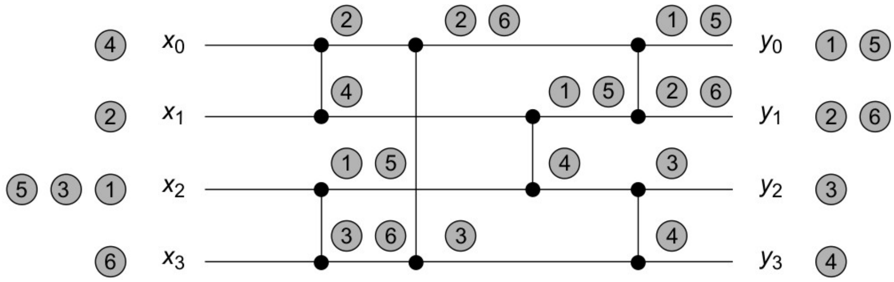
-2018101116,Lakshmi Madhuri

<u>Introduction of Counting Networks:-</u>

Usually,a balancing network is constructed by connecting some balancer's output wires to other balancer's input wires.A balancing network of width w has input wires x 0 , x 1 , . . . , x w−1 (not connected to output wires of balancers), and w output wires y 0 , y 1 , . . . , y w−1 (similarly unconnected). The balancing network's depth is the maximum number of balancers one can traverse starting from any input wire.

In general,any balancing network that satisfies the below property(Step Property) is Counting Network:-

y i = (n/w) + (i mod w)   if n=sigma(xi)



Each vertical line represents a balancer, and each balancer's two input and output wires are the horizontal lines it connects to at the dots. In this sequential execution, tokens pass through the network, one completely after the other in the order specified by the numbers on the tokens. We track every token as it passes through the balancers on the way to an output wire. For example,token number 3 enters on wire 2, goes down to wire 1, and ends up on wire 3. Notice howthe step property is maintained in every balancer, and also in the network as a whole.

Bitonic Counting Network:-

This Bitonic Counting Network is the generalization of the above network , where we extend it width defined as "**any power of 2"**.

Merger[2k] network as follows:-

With width k , we take two input sequences :- x and x`

With width 2k, we output sequence :- y

where a sequence x= x0,x1,x2,......xk-1

When k is equal to 1, the Merger [2k] network is a single balancer. For k > 1, we construct

the Merger [2k] network with input sequences x and x` from two Merger [k] networks and k balancers

We take outputs of two Merger[k] networks z,z` defined as

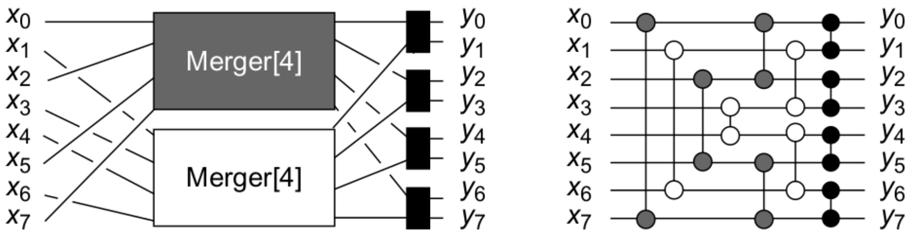
z is the output of (even subsequence of x + odd subsequence if x`)  =x0,....xk-2,x`1,...x`k-1

z` is the output of (odd subsequence of x + even subsequence if x`) =x1,....xk-1,x`0,...x`k-2

The final stage of the network combines z and z` by sending each pair of wires zi and z`i into a balancer whose outputs yield y 2i and y 2i+1 .

The Bitonic [2k] network is constructed by passing the outputs from two Bitonic [k] networks into a Merger [2k] network.This construction gives us a network consisting of (log 2k+1 2) layers each consisting of k balancers.

Below figure depicts the procedure explained above.



On the left-hand side we see the logical structure of a M ERGER [8] network, into which feed two B ITONIC [4] networks, as depicted in Fig. 12.12. The gray M ERGER [4] network has as inputs the odd wires coming out of the top B ITONIC [4] network, and the even ones from the lower B ITONIC [4] network. In the lower M ERGER [4] the situation is reversed. Once the wires exit the two M ERGER [4] networks, each pair of identically numbered wires is combined by a balancer. On the right-hand side we see the physical layout of a M ERGER [8] network. The different balancers are color coded to match the logical structure in the left-hand figure.