ALU POWER OPTIMIZATION USING CLOCK GATING AND CLOCK SCALING

Introduction

The Arithmetic Logic Unit (ALU) forms the core computational block of a processor, executing arithmetic and bitwise logic operations essential for instruction processing. As a key part of the CPU's data path, it interacts continuously with registers, control units, and memory. To maintain synchronized execution, ALU operations are controlled by precise control signals, with outputs updating critical status flags for branching and interrupts.

In modern pipelined and superscalar architectures, the ALU functions as an execution unit, enabling parallel and out-of-order instruction processing. In specialized domains like DSP, extended ALU capabilities support fixed-point and saturation arithmetic. The reduction of Power, Performance, and Area (PPA) in ALU design is crucial: lowering power consumption reduces thermal loads and improves energy efficiency, critical for mobile, embedded, and large-scale data center applications; optimizing performance ensures minimal latency and supports higher clock frequencies needed for real-time and high-throughput systems; minimizing area saves silicon real estate, enabling higher integration densities and cost-effective chip production.

Techniques such as carry-lookahead adders, Booth multipliers, and conditional sum logic are employed to balance these PPA factors, directly impacting the processor's competitiveness in terms of efficiency, scalability, and system reliability.

Objective

The objective of this project is to design and implement a power-optimized 32-bit Arithmetic Logic Unit by strategically integrating fine grained clock gating and clock scaling methodologies, targeting dynamic power reduction, performance retention, and efficiency, aligning with modern low-power VLSI design standards.

Industry standard tools used: Cadence Genus Synthesis solution, Xilinx Vivado

Code

Module 1: ALU

```
`timescale 1ns / 1ps
module ALU_32bit (
    input [31:0] A, B,
    input [2:0] Opcode,
    input [1:0] Power_Mode,
    input Clk,
    input Enable,
    output reg [31:0] Result,
    output reg Cout
```

```
);
    wire [31:0] CLA_Sum;
    wire CLA_Cout;
    wire Clk_Scaled;
    wire Clk_Gated_CLA, Clk_Gated_Logic;
    wire [31:0] B_comp_isolated;

// for subtraction
    assign B_comp_isolated = (Opcode == 3'b001) ? ~B + 1 : B;

    // CLA Adder instantiation
    CLA_Adder_32bit CLA (
        .A(A),
        .B(B_comp_isolated),
        .Cin(1'b0),
        .Sum(CLA_Sum),
        .Cout(CLA_Cout)
    );

    // Clock Scaling
    ClockScaler clk_div (
        .Clk(Clk),
        .Power_Mode(Power_Mode),
        .Clk_Scaled(Clk_Scaled)
    );

    // Clock Gating Cells
    clockgating cla_gate (
        .Clk(Clk_Scaled),
        .Enable(Enable && (Opcode == 3'b000 || Opcode == 3'b001)),
        .Gated_Clk(Clk_Gated_CLA)
    );

    clockgating logic_gate (
        .Clk(Clk_Scaled),
        .Enable(Enable && (Opcode >= 3'b010 && Opcode <= 3'b101)),
        .Gated_Clk(Clk_Gated_Logic)
    );

    // Arithmetic Operations (ADD/SUB)
    always @(posedge Clk_Gated_CLA) begin
    case(Opcode)
    3'b000: {Result , Cout} = { CLA_Sum , CLA_Cout};
    3'b001: {Result , Cout} = { CLA_Sum , ~CLA_Cout};
    default : $display("invalid input");
    endcase
    end
```

```
    // Logic Operations (AND, OR, XOR, NOT)
    always @(posedge Clk_Gated_Logic) begin
        case (Opcode)
            3'b010: Result <= A & B;
            3'b011: Result <= A | B;
            3'b100: Result <= A ^ B;
            3'b101: Result <= ~A;
            default: Result <= 32'b0;
        endcase
        Cout <= 1'b0;
    end
endmodule
```

Module 2: Carry Lookahead Adder for highly computable arithmetic operations

```
module CLA_Adder_32bit (
    input [31:0] A, B,
    input Cin,
    output [31:0] Sum,
    output Cout
);
    wire [31:0] G, P;
    wire [31:0] C;

    assign G = A & B;
    assign P = A ^ B;

    assign C[0] = Cin;

    genvar i;
    generate
        for (i = 0; i < 31; i = i + 1) begin : carry
            assign C[i+1] = G[i] | (P[i] & C[i]);
        end
    endgenerate

    assign Sum = P ^ C[31:0];
    assign Cout = C[31];
endmodule
```

Module 3 : ClockScaling using frequency division based on the power mode

```
module ClockScaler (
    input wire Clk,
```

```
    input wire [1:0] Power_Mode,
    output reg Clk_Scaled
);
    reg [1:0] count;

    always @(posedge Clk) begin
        case (Power_Mode)
            2'b00: count <= count + 2'd1;
            2'b01: count <= count + 2'd2;
            2'b10: count <= 2'd0;
            default: count <= 2'd0;
        endcase
    end

    always @(*) begin
        case (Power_Mode)
            2'b00: Clk_Scaled = (count == 2'b11);
            2'b01: Clk_Scaled = count[0];
            2'b10: Clk_Scaled = Clk;
            default: Clk_Scaled = Clk;
        endcase
    end
endmodule
```

Module 4: Latch-based Clock Gating Implementation

```
module clockgating (
    input wire Clk,
    input wire Enable,
    output wire Gated_Clk
);
    reg Enable_latched;

    always @(posedge Clk)
        Enable_latched <= Enable;

    assign Gated_Clk = Clk & Enable_latched;
endmodule
```

Testbench

```
module ALU_32bit_tb;

    reg [31:0] A, B;
    reg [2:0] Opcode;
```

```
    reg [1:0] Power_Mode;
    reg Clk, Enable;
    wire [31:0] Result;
    wire Cout;

    // Instantiate ALU
    ALU_32bit uut (
        .A(A),
        .B(B),
        .Opcode(Opcode),
        .Power_Mode(Power_Mode),
        .Clk(Clk),
        .Enable(Enable),
        .Result(Result),
        .Cout(Cout)
    );

    // Clock generation
    initial begin
        Clk = 0;
        forever #5 Clk = ~Clk;
    end

    initial begin
        $dumpfile("ALU_optimized.vcd");
        $dumpvars(0, ALU_32bit_tb);

        // Initial state
        Enable = 1;
        Power_Mode = 2'b10;
        // ADD
        Opcode = 3'b000; A = 32'd5; B = 32'd3; #20;
        $display("ADD: A=%d, B=%d, Result=%d, Cout=%b", A, B, Result,
Cout);

        // SUB
        Opcode = 3'b001; A = 32'd5; B = 32'd3; #20;
        $display("SUB: A=%d, B=%d, Result=%d, Cout=%b", A, B, Result,
Cout);

        // AND
        Opcode = 3'b010; A = 32'hFF00FF00; B = 32'h0F0F0F0F; #20;
        $display("AND: Result=%h", Result);

        // OR
        Opcode = 3'b011; A = 32'hFF00FF00; B = 32'h0F0F0F0F; #20;
        $display("OR: Result=%h", Result);
```

```
        // XOR
        Opcode = 3'b100; A = 32'h12345678; B = 32'h87654321; #20;
        $display("XOR: Result=%h", Result);

        // NOT
        Opcode = 3'b101; A = 32'hFFFFFFFF; #20;
        $display("NOT: Result=%h", Result);

        // Disable ALU
        Enable = 0; Opcode = 3'b000; A = 32'd10; B = 32'd5; #20;
        $display("Disabled ALU: Result=%d, Cout=%b", Result, Cout);

        $finish;
    end
endmodule
```

Simulation results:

- Generated using Xilinx Vivado.

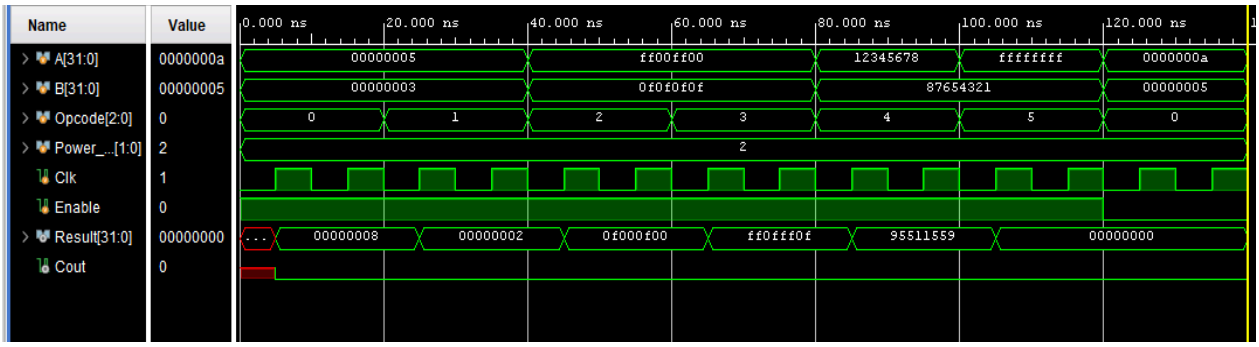

Figure 1. Xilinx Vivado Simulation Result

Synthesis Results:

- Generated using Cadence Genus Synthesis Solution

Module 1: ALU 32-bit

1. **Schematic after synthesis:**

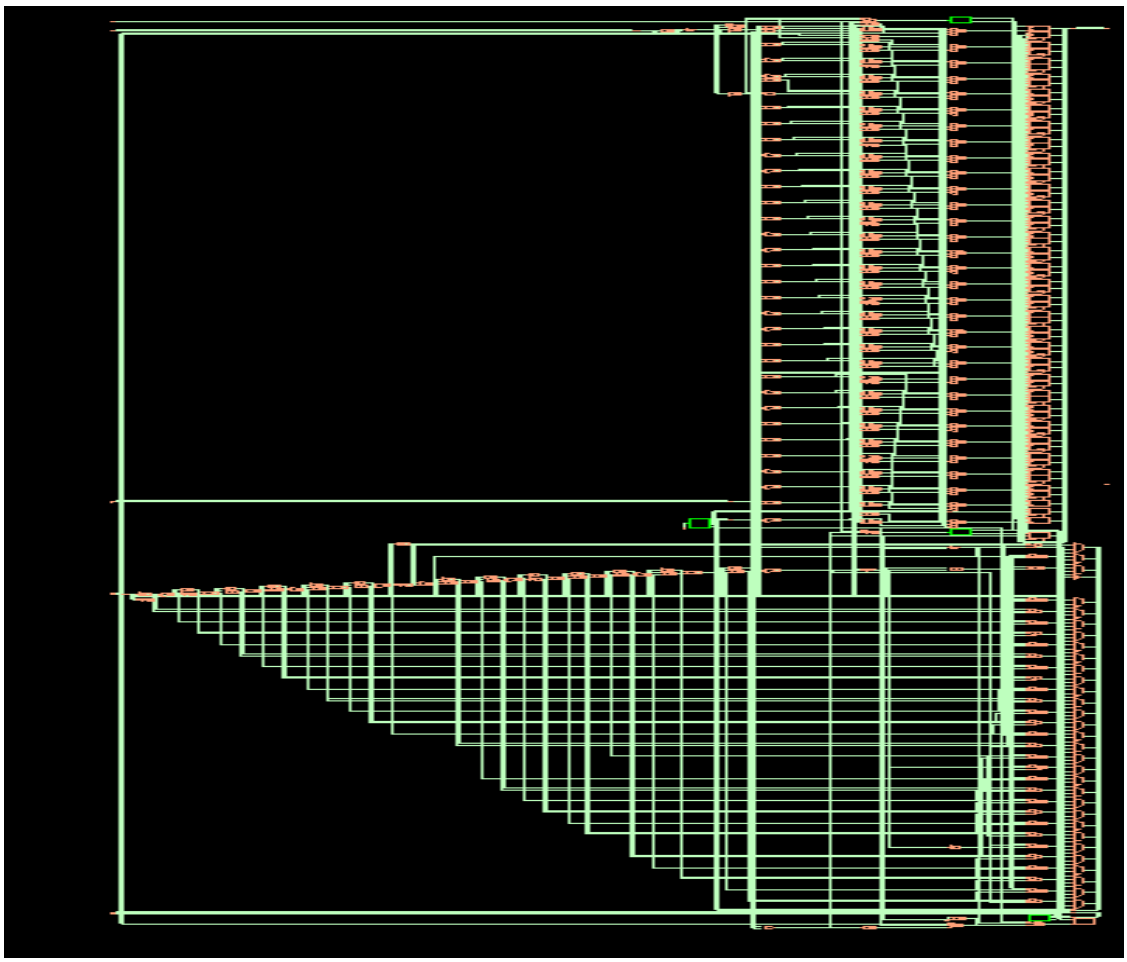

Figure 2. ALU 32-bit Synthesized Schematic

2. QOR Report:

a. Timing Analysis:

```
  Module:                 ALU_32bit
  Technology library:     slow_vdd1v0 1.0
  Operating conditions:   PVT_0P9V_125C (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================

Timing
--------

Clock  Period
--------------
clk   10000.0


  Cost    Critical         Violating
 Group   Path Slack  TNS     Paths
-------------------------------------
default    No paths   0.0
-------------------------------------
Total                 0.0          0
```

Figure 3. ALU 32-bit Timing Analysis Report

b. Area Analysis:

```
  Module:                 ALU_32bit
  Operating conditions:   PVT_0P9V_125C (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================


  Gate    Instances   Area       Library
------------------------------------------
AND2X1            2    2.736    slow_vdd1v0
AOI21XL          48   82.080    slow_vdd1v0
BUFX2             1    1.710    slow_vdd1v0
DFFHQX1          33  180.576    slow_vdd1v0
INVX1            17   11.628    slow_vdd1v0
INVXL             2    1.368    slow_vdd1v0
MX2XL            31   74.214    slow_vdd1v0
NAND2X2           1    1.710    slow_vdd1v0
NAND2XL          47   48.222    slow_vdd1v0
NAND3BXL          1    1.710    slow_vdd1v0
NOR2BX1           2    2.736    slow_vdd1v0
NOR2XL           47   48.222    slow_vdd1v0
OA21X1           15   30.780    slow_vdd1v0
OAI211X1          1    1.710    slow_vdd1v0
OAI222XL         32   87.552    slow_vdd1v0
OR2X1             2    2.736    slow_vdd1v0
OR2X2             2    3.420    slow_vdd1v0
SDFFQX1          32  240.768    slow_vdd1v0
XNOR2X1           1    2.394    slow_vdd1v0
------------------------------------------
total           317  826.272


     Type      Instances   Area  Area %
----------------------------------------
sequential            65 421.344   51.0
inverter              19  12.996    1.6
buffer                 1   1.710    0.2
unresolved             4   0.000    0.0
logic                232 390.222   47.2
physical_cells         0   0.000    0.0
----------------------------------------
total                321 826.272  100.0
```

Figure 4. ALU 32-Bit Area Analysis Report

c. Power Analysis:

```
Instance: /ALU_32bit
Power Unit: W
PDB Frames: /stim#0/frame#0
  ------------------------------------------------------------------------
    Category         Leakage     Internal    Switching        Total     Row%
  ------------------------------------------------------------------------
       memory     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
     register     7.76194e-09  4.71550e-07  5.26500e-09  4.84577e-07  56.45%
        latch     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
        logic     6.01569e-09  2.55168e-07  1.12671e-07  3.73855e-07  43.55%
         bbox     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
        clock     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
          pad     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
           pm     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
  ------------------------------------------------------------------------
    Subtotal     1.37776e-08  7.26719e-07  1.17936e-07  8.58432e-07 100.00%
  Percentage           1.60%       84.66%       13.74%      100.00% 100.00%
  ------------------------------------------------------------------------
```

Figure 5. ALU 32-bit Power Analysis Report

Module 2: Carry Lookahead Adder

1. **Schematic after synthesis**

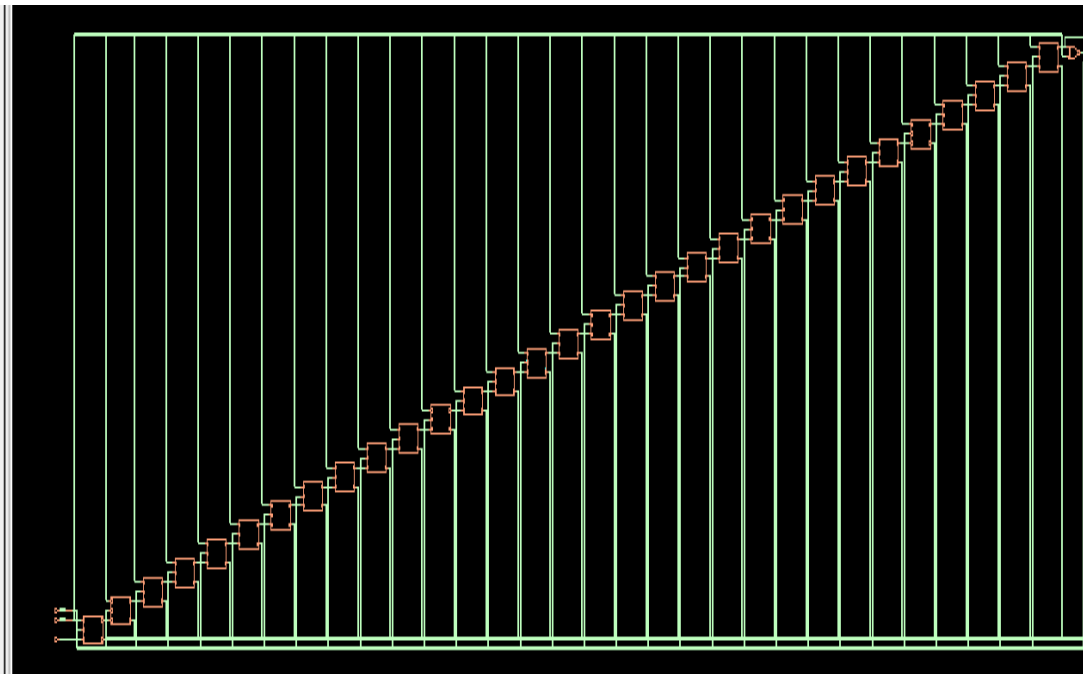

Figure 6. Carry Lookahead Adder Synthesized Schematic

2. **QOR Report:**

   a. **Timing Analysis:**

```
Timing
--------

Clock  Period
--------------
clk   10000.0


  Cost    Critical         Violating
 Group   Path Slack  TNS     Paths
-------------------------------------
default    No paths   0.0
-------------------------------------
Total                 0.0          0
```

Figure 7. Carry Lookahead Adder Timing Analysis Report

b. Area Analysis:

```
  Module:                 CLA_Adder_32bit
  Operating conditions:   PVT_0P9V_125C (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================


  Gate    Instances   Area       Library
------------------------------------------
ADDFX1           31  159.030    slow_vdd1v0
XNOR2X1           2    4.788    slow_vdd1v0
------------------------------------------
total            33  163.818


     Type      Instances   Area  Area %
---------------------------------------
logic                 33 163.818  100.0
physical_cells         0   0.000    0.0
---------------------------------------
total                 33 163.818  100.0
```

Figure 8. Carry-lookahead Adder Area Analysis Report

c. Power Analysis:

```
Instance: /CLA_Adder_32bit
Power Unit: W
PDB Frames: /stim#0/frame#0
 ------------------------------------------------------------------------------
   Category         Leakage     Internal    Switching        Total     Row%
 ------------------------------------------------------------------------------
     memory     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
   register     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
      latch     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
      logic     3.25863e-09  2.58639e-07  7.04092e-08  3.32307e-07 100.00%
       bbox     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
      clock     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
        pad     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
         pm     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
 ------------------------------------------------------------------------------
   Subtotal     3.25863e-09  2.58639e-07  7.04092e-08  3.32307e-07 100.00%
 Percentage           0.98%       77.83%       21.19%      100.00% 100.00%
 ------------------------------------------------------------------------------
```

Figure 9. Carry Lookahead Adder Power Analysis Report

Module 3 : Clock scaling

1. Schematic after synthesis

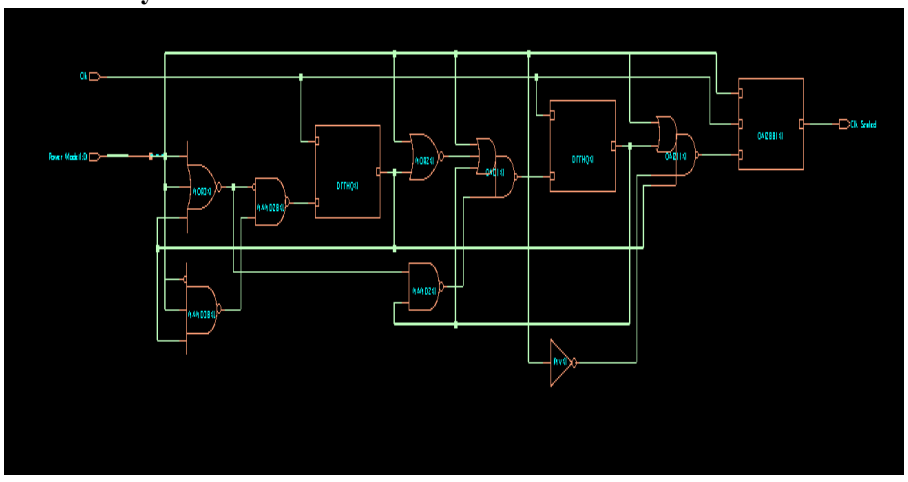

Figure 10. Clock Scaling Synthesised Schematic

2. QOR Report:

a. Timings Analysis:

```
  Module:                 ClockScaler
  Operating conditions:   PVT_0P9V_125C (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================


Path 1: MET (9336 ps) Setup Check with Pin count_reg[1]/CK->D
     Startpoint: (R) count_reg[0]/CK
          Clock: (R) clk
       Endpoint: (R) count_reg[1]/D
          Clock: (R) clk

                    Capture       Launch
       Clock Edge:+   10000            0
      Src Latency:+       0            0
      Net Latency:+       0 (I)        0 (I)
          Arrival:=   10000            0

            Setup:-      33
    Required Time:=    9967
     Launch Clock:-       0
        Data Path:-     631
            Slack:=    9336
```

Figure 11. Clock Scaling Timing Analysis Report

b. Area Analysis:

```
  Module:                 ClockScaler
  Operating conditions:   PVT_0P9V_125C (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================


   Gate    Instances   Area      Library
-----------------------------------------------
DFFHQX1            2  10.944    slow_vdd1v0
INVX1              1   0.684    slow_vdd1v0
NAND2BXL           1   1.368    slow_vdd1v0
NAND2X1            1   1.026    slow_vdd1v0
NAND3BXL           1   1.710    slow_vdd1v0
NOR2X1             1   1.026    slow_vdd1v0
NOR3X1             1   1.710    slow_vdd1v0
OAI211X1           1   1.710    slow_vdd1v0
OAI2BB1X1          1   1.710    slow_vdd1v0
OAI31X1            1   2.052    slow_vdd1v0
-----------------------------------------------
total             11  23.940


     Type      Instances  Area  Area %
---------------------------------------
sequential             2 10.944   45.7
inverter               1  0.684    2.9
logic                  8 12.312   51.4
physical_cells         0  0.000    0.0
---------------------------------------
total                 11 23.940  100.0
```

Figure 12. Clock Scaling Area Analysis

c. Power Analysis:

```
Instance: /ClockScaler
Power Unit: W
PDB Frames: /stim#0/frame#0
  ------------------------------------------------------------------------
    Category         Leakage     Internal    Switching        Total    Row%
  ------------------------------------------------------------------------
      memory     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
    register     2.40947e-10  4.65017e-07  2.60080e-08  4.91266e-07  58.51%
       latch     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
       logic     2.30765e-10  9.75703e-08  4.96861e-08  1.47487e-07  17.57%
        bbox     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
       clock     4.76440e-11  1.52227e-07  4.86000e-08  2.00875e-07  23.92%
         pad     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
          pm     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
  ------------------------------------------------------------------------
    Subtotal     5.19356e-10  7.14814e-07  1.24294e-07  8.39628e-07 100.00%
  Percentage           0.06%       85.13%       14.80%      100.00% 100.00%
  ------------------------------------------------------------------------
```

Figure 13. Clock Scaling Power Analysis

Module 4 : Clock Gating

1. Schematic after synthesis

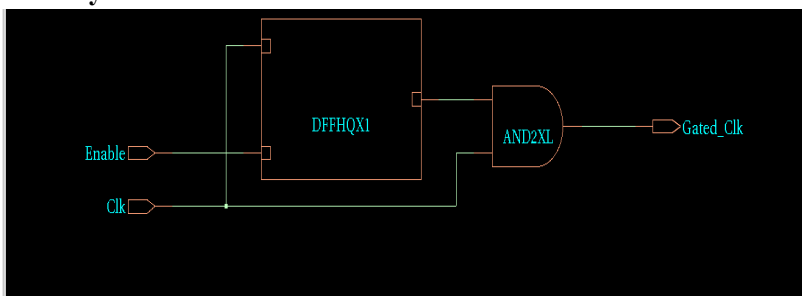

Figure 14. Clock Gating Synthesized Schematic

2. QOR Report:

a. Timing Analysis:

```
  Module:                 clockgating
  Operating conditions:   PVT_0P9V_125C (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================


Path 1: MET (9602 ps) Clock Gating Setup Check at pin g12__2398/A
     Startpoint: (R) Enable_latched_reg/CK
          Clock: (R) clk
       Endpoint: (F) g12__2398/A
          Clock: (R) clk

                    Capture       Launch
       Clock Edge:+   10000            0
      Src Latency:+       0            0
      Net Latency:+       0 (I)        0 (I)
          Arrival:=   10000            0

  Gate Check Setup:-       0
     Required Time:=   10000
      Launch Clock:-       0
         Data Path:-     398
             Slack:=    9602

Exceptions/Constraints:
  output_delay             0             clk_gating_check_4
```

Figure 15. Clock Gating Timing Analysis Report

b. Area Analysis:

```
  Module:                 clockgating
  Operating conditions:   PVT_0P9V_125C (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================


  Gate    Instances  Area      Library
------------------------------------------
AND2XL            1  1.368    slow_vdd1v0
DFFHQX1           1  5.472    slow_vdd1v0
------------------------------------------
total             2  6.840


     Type       Instances  Area Area %
---------------------------------------
sequential              1 5.472   80.0
logic                   1 1.368   20.0
physical_cells          0 0.000    0.0
---------------------------------------
total                   2 6.840  100.0
```

Figure 16. Clock Gating Area Analysis Report

c. Power Analysis:

```
Instance: /clockgating
Power Unit: W
PDB Frames: /stim#0/frame#0
  ------------------------------------------------------------------------
    Category         Leakage     Internal    Switching        Total    Row%
  ------------------------------------------------------------------------
      memory     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
    register     1.20340e-10  2.11544e-07  4.05000e-09  2.15714e-07  72.79%
       latch     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
       logic     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
        bbox     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
       clock     2.39910e-11  4.82165e-08  3.24000e-08  8.06405e-08  27.21%
         pad     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
          pm     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
  ------------------------------------------------------------------------
    Subtotal     1.44331e-10  2.59760e-07  3.64500e-08  2.96355e-07 100.00%
  Percentage           0.05%       87.65%       12.30%      100.00% 100.00%
  ------------------------------------------------------------------------
```

Figure 17. Clock Gating Power Analysis Report

Conclusion:

1. This project successfully implemented a power-optimized 32-bit ALU using clock gating and clock scaling techniques.
2. By selectively controlling the clock and adapting the frequency to performance needs, significant dynamic power reduction was achieved without compromising functionality.
3. The use of a Carry Lookahead Adder (CLA) ensured fast arithmetic operations, supporting the overall low-power design goals.
4. Simulation and synthesis results validated the effectiveness of these optimizations, demonstrating their importance in modern low-power VLSI systems.