A design of CMOS Operational Amplifier in TMEC 0.8 µm technology

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***Abstract*—This paper proposes a basic two stage CMOS operational amplifier (opamp) design in TMEC 0.8 µm technology. The designkits of TMEC technology was supported on Tanner EDA v15.1 tools. The opamp operates on a single supply of 5V. Simulation results show a unity gain frequency of 4MHz, a gain of 65-dB with 65º phase margin, and power consumption of 582µW. The basic opamp was implemented for instrumentation amplifier. The gain of instrumentation amplifier was varied by R_g form 1-Ω to 400-kΩ for 60 dB to 0 dB, respectively. The post layout simulation of instrumentation amplifier was varied by R_g form 1-Ω to 350-kΩ for 43.7 dB to 0 dB, respectively. The objective of this paper is to verify TMEC's design kits using an opamp as design example.**

Keywords—Operational amplifier (opamp); Instrumentation Amplifier; TMEC 0.8 µm technology; Tanner EDA tools.

I. INTRODUCTION

The basic opamp is used in building block of analog and mixed signal circuit. The general two stage opamp block diagram [1]-[2] consists of input differential amplifier stage, high gain stage, output buffer, bias circuitry and compensation circuitry. The output buffer may be needed in some applications.

The IC design development trend is featured small CMOS technology and several techniques of circuit and layout design. CMOS technology was scaled down the supply voltage with reducing transistor channel length, bring about to several low power applications such as portable devices, wireless communication products, and consumer electronics. While the performance of CMOS building block is degraded. The CMOS opamp design challenge depends on the several techniques of circuit design and technology for the best performance.

This paper presented the basic opamp [2] designed using RC compensation for stability using a TMEC 0.8 µm CMOS technology. The current reference circuit [3] is widely used in many integrated circuit applications. The precision and stability of reference circuit is degraded by supply voltage, temperature variation and the large parasitic capacitor in current mirror circuit. The precision and stability is difficult for process compensation technique. Several techniques are usually based on optimal transistor matching and intelligent layout design [4]. The proposed opamp was applied for instrumentation amplifier to amplify TMEC pressure sensor signal in the same technology. This work has been done using tanner EDA v15.1 tools. The schematic has been made using S-Edit while the netlist was being created using T-Spice and results were viewed using W-Edit. This step was supported by tmec08_model_rc04d.md file. Backend design (design and verify layout) has supported by TMEC08.tdb in L-Edit. L-Edit Extract generates a SPICE netlist by TMCN082p3M_EXT.ext file for LVS comparison and post-layout simulation in T-Spice. The outline of paper: Section 2 presents the proposed CMOS circuit. Section 3 presents the circuit and post-layout simulation results. The final section is the conclusion.

II. PROPOSED CMOS CIRCUIT DESIGN

The circuit proposed was designed regarding general specifications of basic CMOS opamp [2], such as the open loop dc-gain, output voltage swing, input offset voltage, CMRR, PSRR, the unity-gain bandwidth, setting time, slew rate, etc. The designing of high performance CMOS opamp is becoming the most essential analog circuit design for instrumentation amplifier application to interface sensors in TMEC technology.

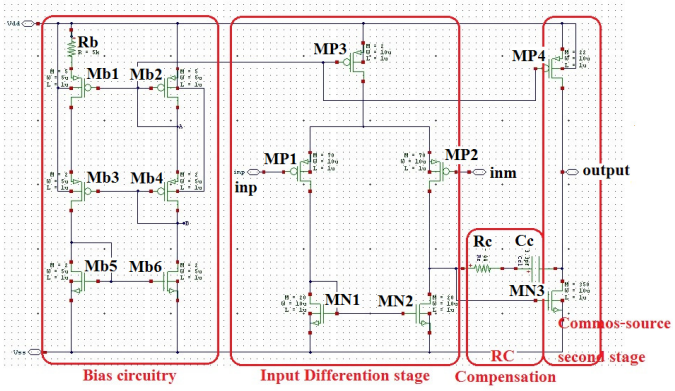


Fig. 1. *Schematic of CMOS opamp*

Fig.1 shows a CMOS opamp structure for general specification of

- Open loop dc-gain ≥ 60 dB
- Phase Margin ≥ 60 dB
- A single supply voltage range is 3 volt to 5 volt
- Maximum 5 V of output voltage

The design procedure can be constructed as follows.

A. *First stage: Input differential amplifier stage*

The first stage is a differential input with current mirror load. P-channel input pair (MP1 and MP2) have lower noise as compared to N-channel. These differential currents are applied to a current mirror circuitry of the MN1 and MN2 transistors to the differential voltage. MP3 transistor provides biasing for the entire opamp. Therefore, symmetry and matching consists of $W/L_{MP1}=W/L_{MP2}$ and $W/L_{MN1}=W/L_{MN2}$.

$$I_o = g_{MP1}\left(V_{in+} - V_{in-}\right) \tag{1}$$

And

$$g_{MP1} = \sqrt{2K_p'\left(\frac{W}{L}\right)I_{d1}} \tag{2}$$

First stage gain, $A_{v1} = -\dfrac{g_{MP1}}{\left[g_{ds,MP2} + g_{ds,MN2}\right]}$ (3)

B. *Second stage: Voltage gain stage*

The common source second stage is simply designed with MN3 and MP4 transistors. MP4 transistor is loaded by a current sink load, which converts the current to voltage at the output.

Second stage gain, $A_{v2} = -\dfrac{g_{MP4}}{\left[g_{ds,MP4} + g_{ds,MN3}\right]}$ (4)

Therefor; $A_v=A_{v1}+A_{v2}$

Gain Bandwidth $= \dfrac{g_{MP1}}{C_c}$ (5)

Zero $z_1 = \dfrac{g_{MP4}}{C_c}$ (6)

Output pole $p_2 = -\dfrac{g_{MP4}}{C_L}$ (7)

The slew rate is $SR = \dfrac{I_{D_{MP3}}}{C_C}$ (8)

The minimum value of $C_c > 0.22C_L$ is chosen, this is for a 60° phase margin (generally considered acceptable for most applications). This value is determined by the pole-zero pattern of the transfer function. It also determines the time response analysis.

C. *Bias circuitry*

The current reference value is about 20 µA for opamp in Fig.1. The main specification of circuit is low r_{out} and low PVT sensitivity (Process, Voltage, and Temperature) [3].

$$I_{ref}\frac{2}{\mu_p C_{ox}\left(\frac{W}{L}\right)}\frac{1}{R_b^2}\left(1-\frac{1}{\sqrt{K_p}}\right)^2 \tag{9}$$

D. *RC Compensation circuitry*

The RC compensation circuitry has been proposed in [1] and [2]. A capacitor, C_c is used for frequency compensation. That is to achieve stability for phase margin. A resistor, R_c, in series with the compensation capacitor, C_c, has effect to the RHZ translating into the left-plane. In [5] shows several frequency compensation techniques. In this paper, R_c and C_c are used between gate and drain of M_{N3} to improve the phase margin and hence stability of the opamp.

The typical instrumentation amplifier (In-Amp) is widely used in many industrial and measurement applications [6]. In-Amp is needed for sensor interface circuit. In-Amp performs a pre-amplification of a weak sensor signal to a level that can be suited for subsequent processing as well as reject a certain level of unwanted noise [7]. The total power dissipation of low-power systems can be realized that commercially available In-Amp topologies. In-Amp is a precision closed-loop gain block. Typical expected characteristics of an In-Amp are: low noise, low offset, high gain, high input impedance and high CMRR.

The basic instrumentation amplifier is shown in Fig.2, it is made up of three opamps and six resistors. The voltage gain is control by external resistor (R_g).

$$V_{out} = V_{in}\left(1+\frac{2R_2}{R_g}\right) \tag{10}$$

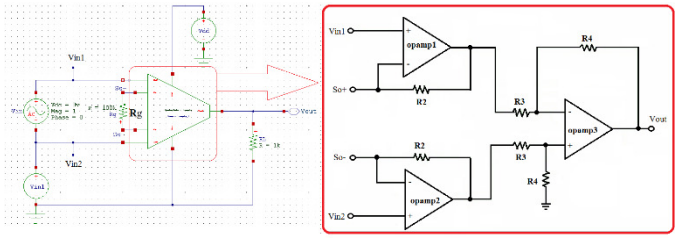


Fig. 2. *The instrumentation amplifier*

Table I shows that the aspect ratios of all transistor of opamp and instrumentation amplifier.

TABLE I. **DEVICE PARAMETERS OF OPAMP AND IN-AMP CIRCUITRY**

opamp circuitry [W/L (µm)]			
MP1,MP2	700/1	MN1,MN2	200/1
MP3	20/1	MN3	3500/1
MP4	220/1	Rc	44 Ohm
		Cc	3.3 pF
Bias circuit parameters [W/L (µm)]			
Mb1 to Mb6	10/1	Rb	10 k-ohm
Instrumentation amplifier circuitry			
Rg	Range of 1 ohm to 400 k-ohm		
R2	100 k-ohm	R3	10 k-ohm

III. SIMULATION RESULTS

The proposed circuit was design using TMEC 0.8 µm CMOS 2P2M standard process and carried out in Tanner tools (T-Spice, S-Edit, W-Edit, L-Edit and LVS (Standard LVS for layout versus schematic)). Table II shows the TMEC process parameters.

TABLE II. TMEC PROCESS PARAMETERS (0.8 MICRON)

Process parameters	NMOS	PMOS
V_t (V)	7.345e-01	-9.0978e-01
Gain factor (µA/V^2)	6.833e-01	4.617e-01

The opamp simulation was done using a 5V supply. Fig. 3 shows the simulation output frequency response of 65-dB loop gain, 65º phase margin, a unity gain frequency of 4-MHz. Fig.4 shows signal swing of two inputs and output. The slew rate simulation shows in the Fig. 5. The simulation results of designed opamp are shown in Table III compared with [7], [8], [9], and [10]. Post-layout simulation is performed successfully for 65.7 dB gain, 73.9 of CMRR, 90 dB of PSRR+, and 65.2 dB of PSRR-. This opamp performance is not better than [7], while it is better than [10] in the same technology.

TABLE III. **OP-AMP PERFORMANCE COMPARISON**

	[8]	**[9]**	**[10]**	**[7]**	**This work** Sim/Post-layout sim
Technology (µm)	TSMC 0.18	TSMC 0.18	0.8	AMS 0.8	TMEC 0.8
Vdd (V)	1.8	+/- 1.8	2	5	5
Open-loop gain (dB)	55.5	70	61	70	65 / 65.7
Unity-gain bandwidth (Hz)	12.6 M	8 M	1.09 M	11 M	4 M / 6.64 M
Phase margin(º)	60º	75º	61º	79º	65º / 64.2 º
CMRR (dB)	-	-	60.3	105	72.3 / 73.9
-PSRR (dB)	-	-	110	71	65 / 65.2
+PSRR (dB)	-	-	108	88	92.2 / 90
Power (W)	300u	19.5u	16.8u	1.3m	582u
Year/ EDA Tools	2014 P-spice	2013 Tanner	2010 Mentor	2008 Cadence	2018 Tanner

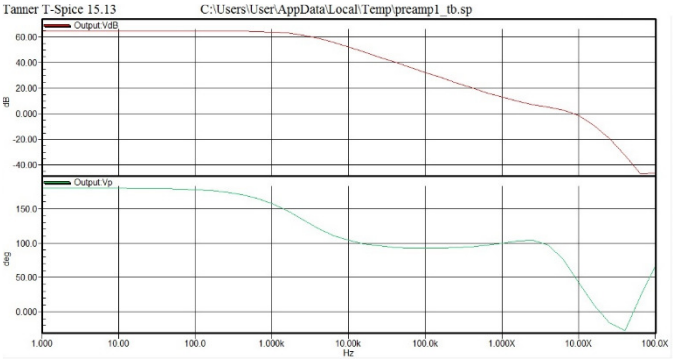


Fig. 3. *Frequency response of opamp.*

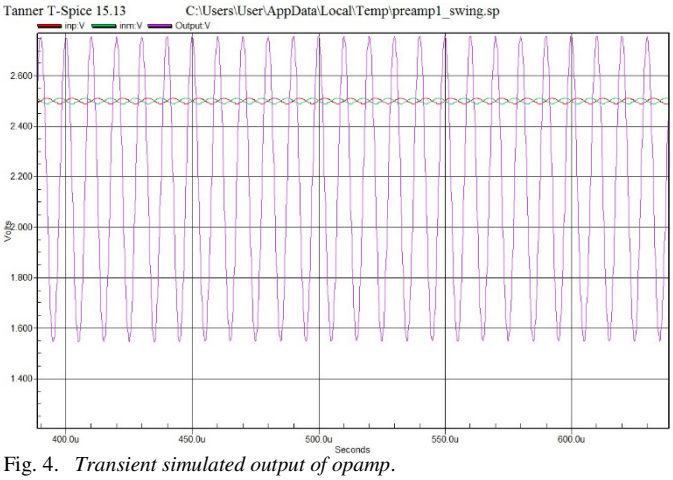


Fig. 4. *Transient simulated output of opamp.*

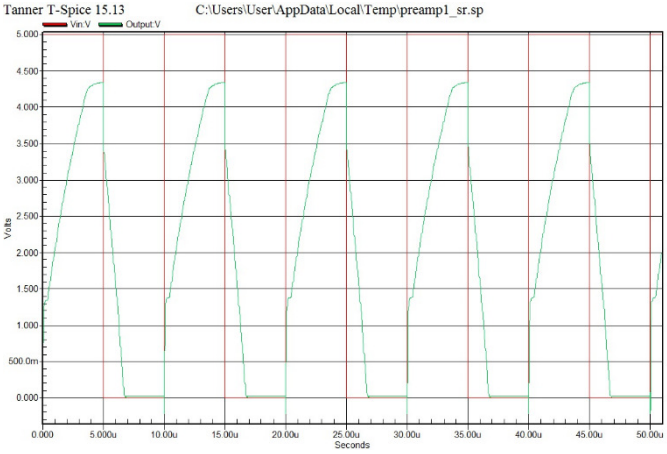


Fig. 5. *Plus waveform simulation for Slew rate output of opamp.*

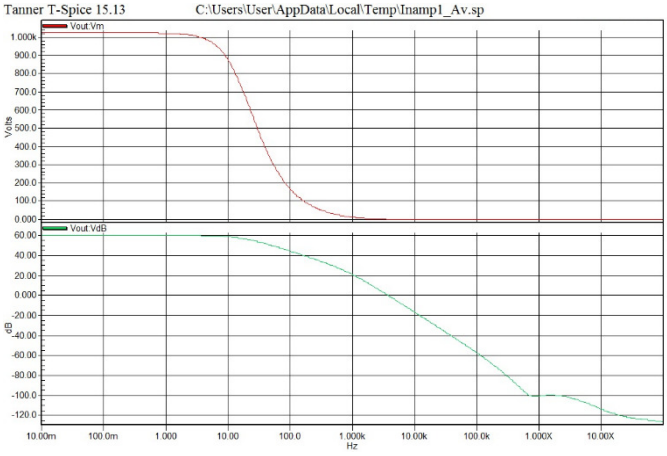
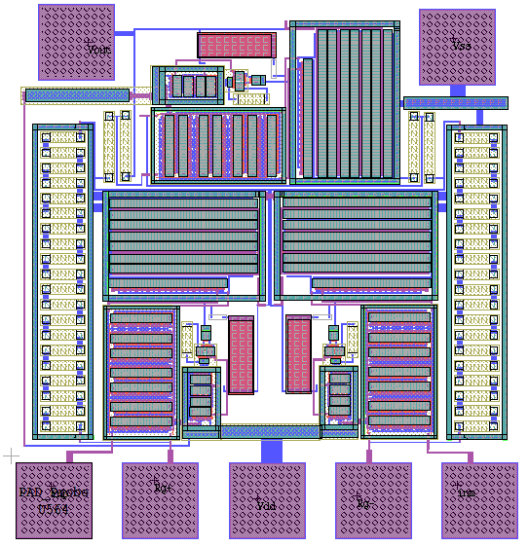


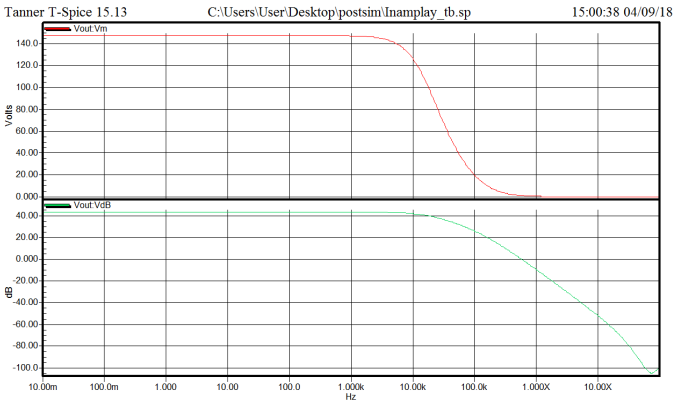
Fig. 6. *In-amp simulation of amplify Gain at R_g=1-Ohm*

The power dissipation can be calculated by using transient analysis to measure the rise/fall time of Op-amp, Power report results as: VVdd from time 1e-009 to 5.1e-005 and Average power consumed -> 5.825410e-004 watts. The In-Amp simulation exhibits of Gain range of R_g in Fig. 6, which R_g=400 kΩ: gain = 0 dB and when R_g=1Ω: gain ≈ 60 dB.

Fig. 7 (a) and (b) exhibit In-amp layout design for 573x690 µm of area while a single opamp area is 250x330 µm. The layout is designed and verified by L-Edit of Tanner tools in TMEC technology. Fig. 7 (b) shows post-layout simulation for gain range, which R1=1Ω: gain ≈ 43.7 dB or R1=350 kΩ: gain = 0 dB.



(a)



(b)

Fig. 7. *(a) In-amp layout design and (b) Post-layout simulation of amplify gain at R_g=1-Ohm*

IV. Conclusions

This paper proposed the TMEC 0.8µm process technology for integrated circuit design. A basic two stage CMOS operational amplifier and instrumentation amplifier were used for this work. Simulation and Post-layout simulation results confirm in the TMEC process technology to design and support the CMOS integrated circuit. In the future, this circuit will be used to interface transducer bridge sensors (TMEC sensors) on the same die and is fabricated in Thailand.

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