Application Note for
2 Stage CMOS OPAMP (avsdopamp 3v3)

By

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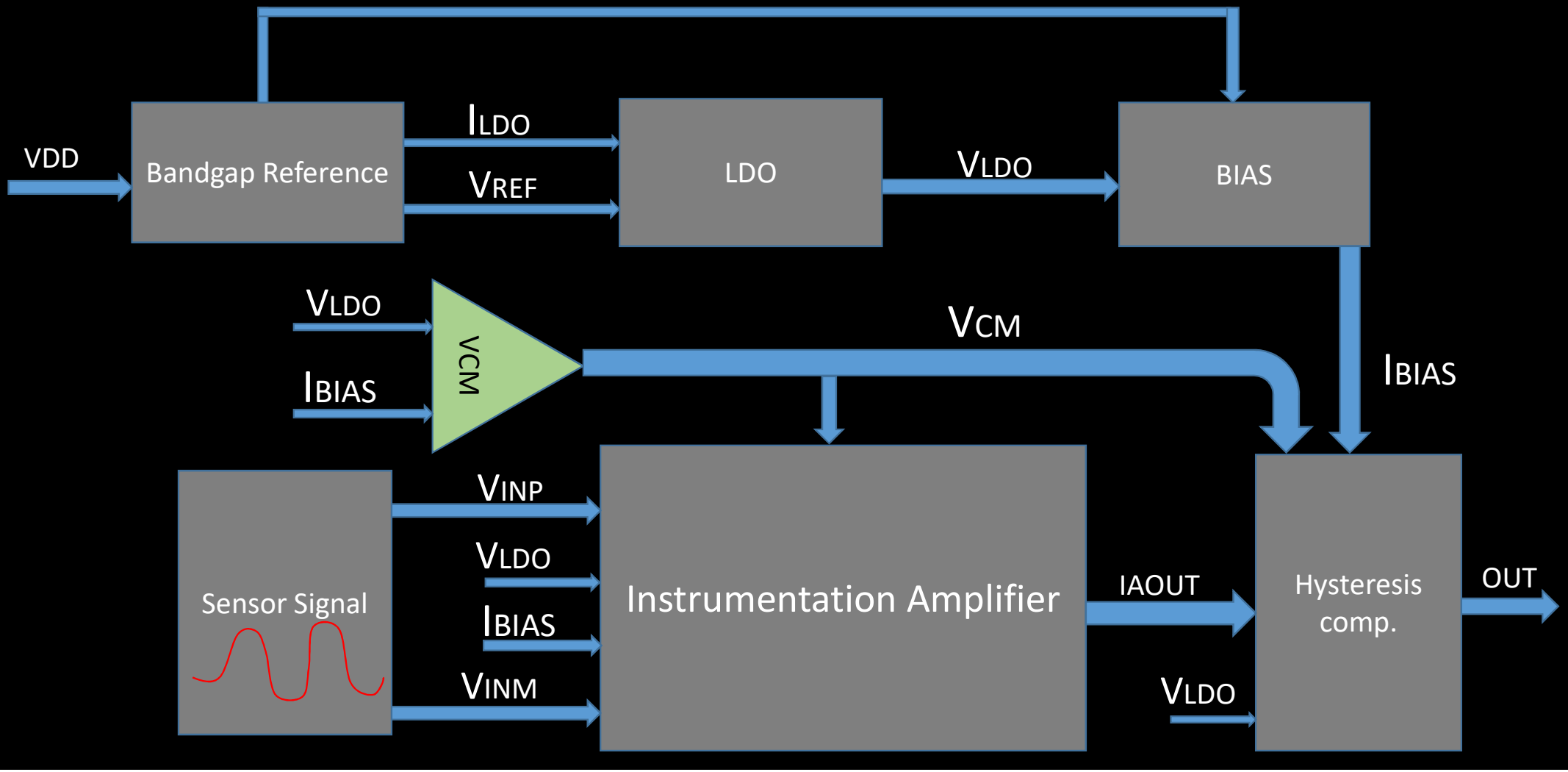
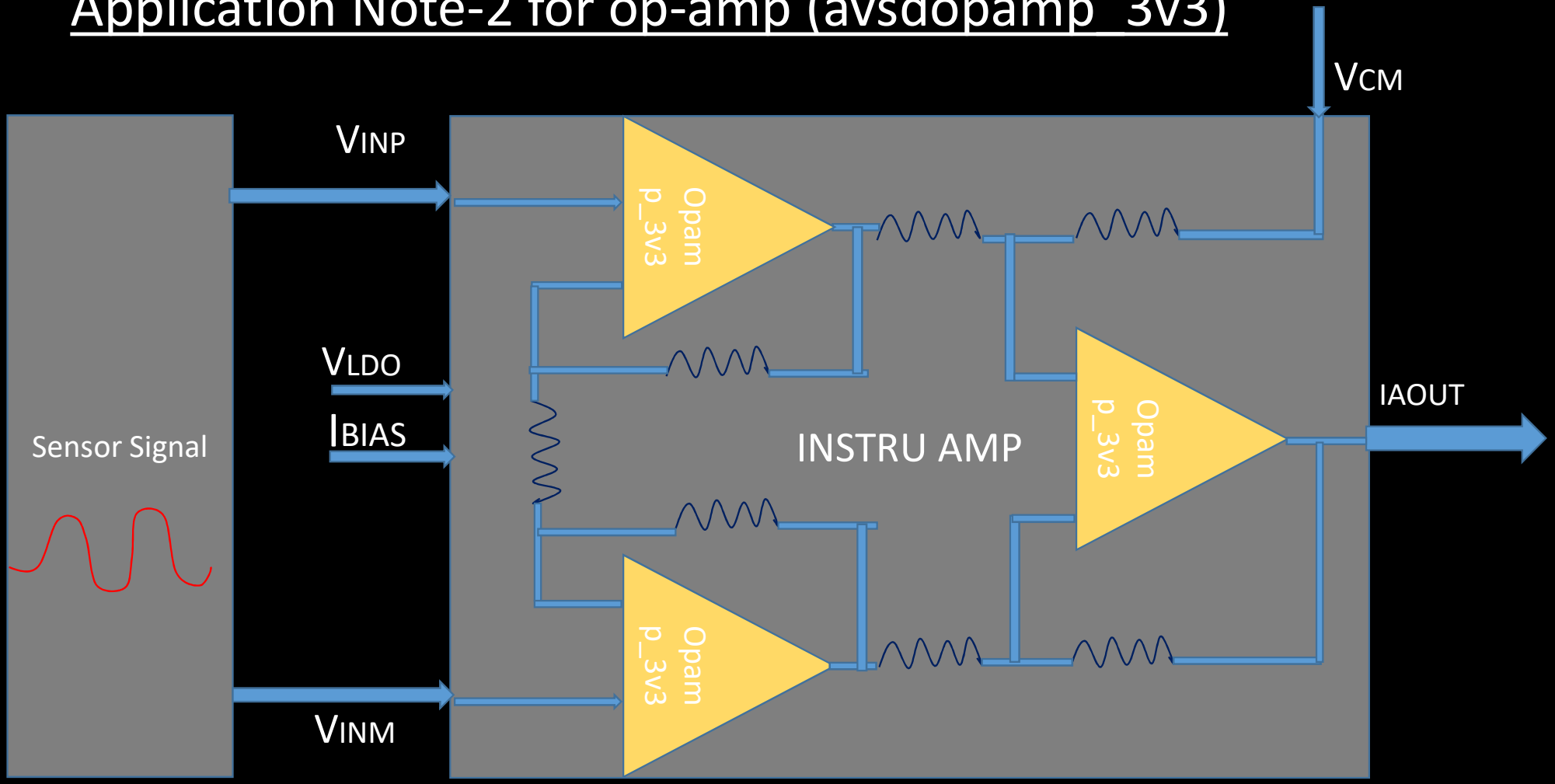
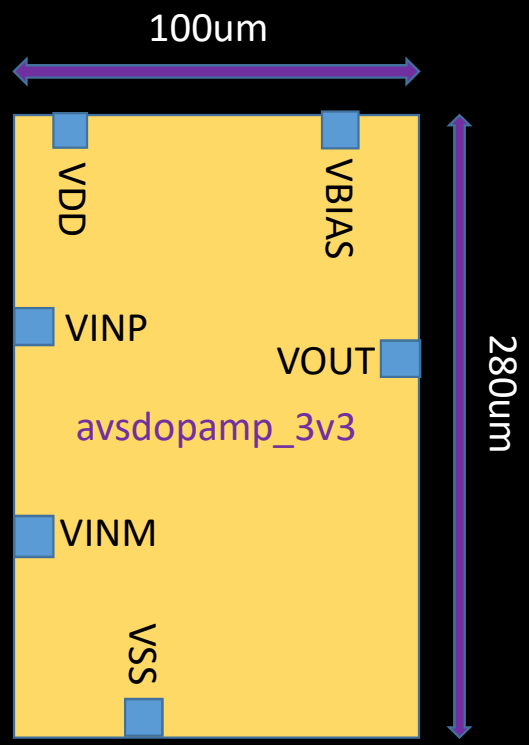
Application Note-1 for op-amp (avsdopamp_3v3)



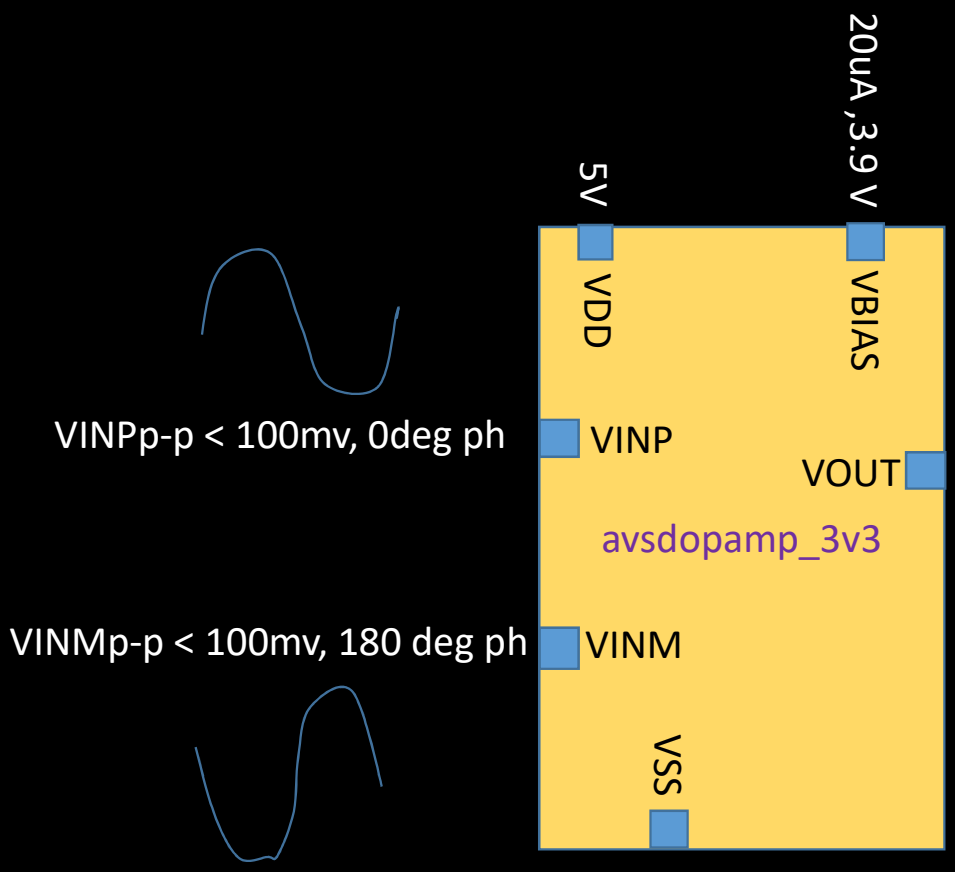
Application Note-2 for op-amp (avsdopamp_3v3)

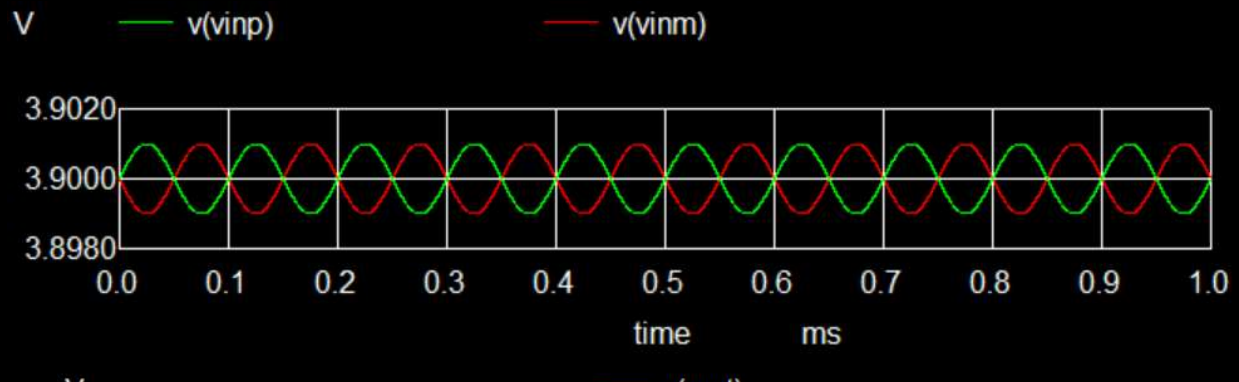


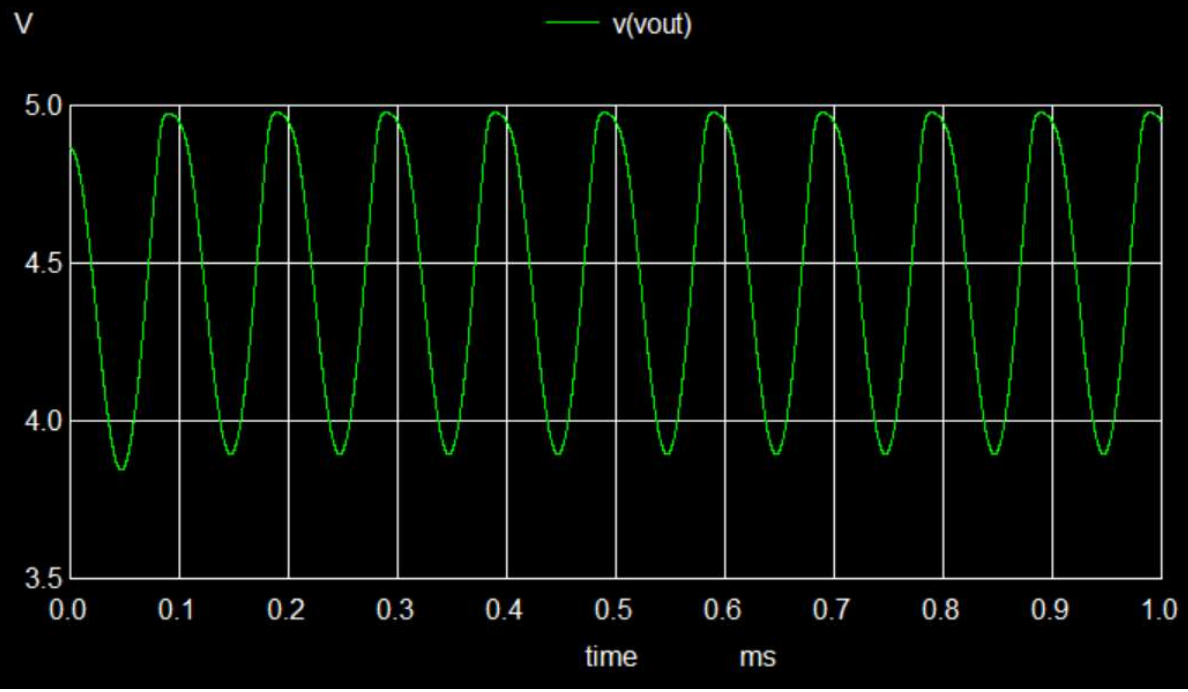
avsdopamp_3v3 Pin layout and preferred dimensions



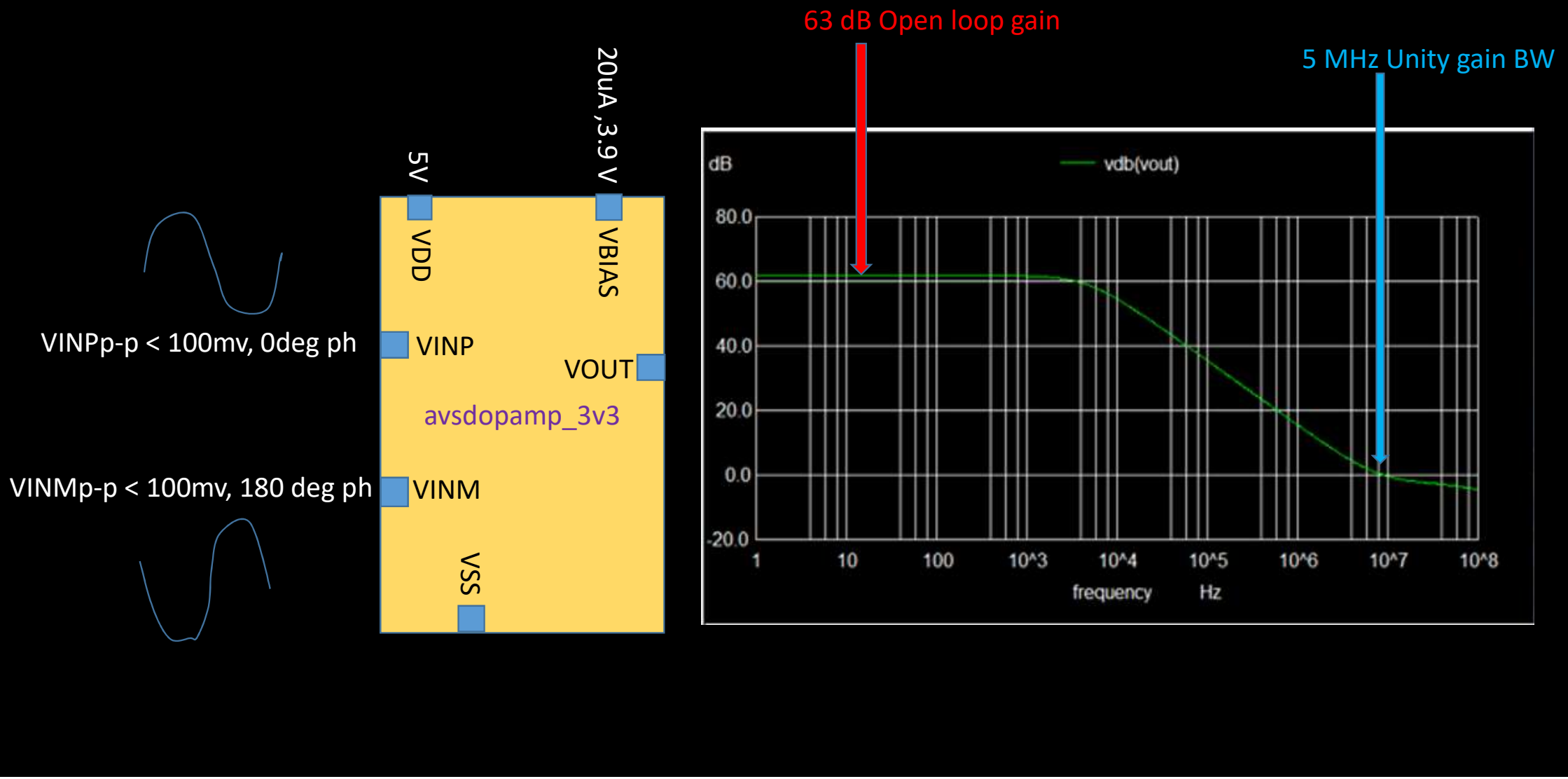
avsdopamp 3v3 Transient Response







avsdopamp_3v3 Frequency Response



avsdopamp 3v3 Plots and values needed

1) CMOS OPAMP Bias voltage VBIAS = 3.9 V with IBIAS = 20 uA

2) OPAMP open loop gain = 63 dB

3) Unity Gain Bandwidth = 5 MHz

4) Common mode rejection ratio (CMRR) = 65 dB

5) Power dissipation = 590 uW