# EXPERIMENTT NO 9

## Design and Implementation of Magnitude Comparator

**Objective:-**

To design and implement

2 – Bit magnitude comparator using basic gates.

**Parts required:-**

| Sl.No. | COMPONENT | SPECIFICATION | QTY. |
|---|---|---|---|
| 1. | AND GATE | IC 7408 | 2 |
| 2. | X-OR GATE | IC 7486 | 1 |
| 3. | OR GATE | IC 7432 | 1 |
| 4. | NOT GATE | IC 7404 | 1 |

**Apparatus:-**

- Trainer/ proto board
- Wire cutter
- Patch Cords
- Voltmeter

**THEORY:**

The comparison of two numbers is an operator that determines one number is greater than, less than (or) equal to the other number. A magnitude comparator is combinational circuits that compares two numbers A and B and determine their relative magnitude. The outcome of the comparator is specified by three binary variables that indicate whether

A>B, A=B or A<B.

$A = A_3\ A2\ A1\ A0$

$B = B_3\ B2\ B1\ B0$

The equality of the two numbers and B is displayed in a combinational circuit designated by the symbol (A=B).

This indicates A greater than B, then inspect the relative magnitude of pairs of significant digits starting from most significant position. A is 0 and that of B is 0.

We have A<B, the sequential comparison can be expanded as

$$A>B = A3B_3{}^1 + X_3A_2B_2{}^1 + X_3X_2A_1B_1{}^1 + X_3X_2X_1A_0B_0{}^1$$

$$A<B = A_3{}^1B_3 + X_3A_2{}^1B_2 + X_3X2A_1{}^1B_1 + X_3X_2X_1A_0{}^1B_0$$

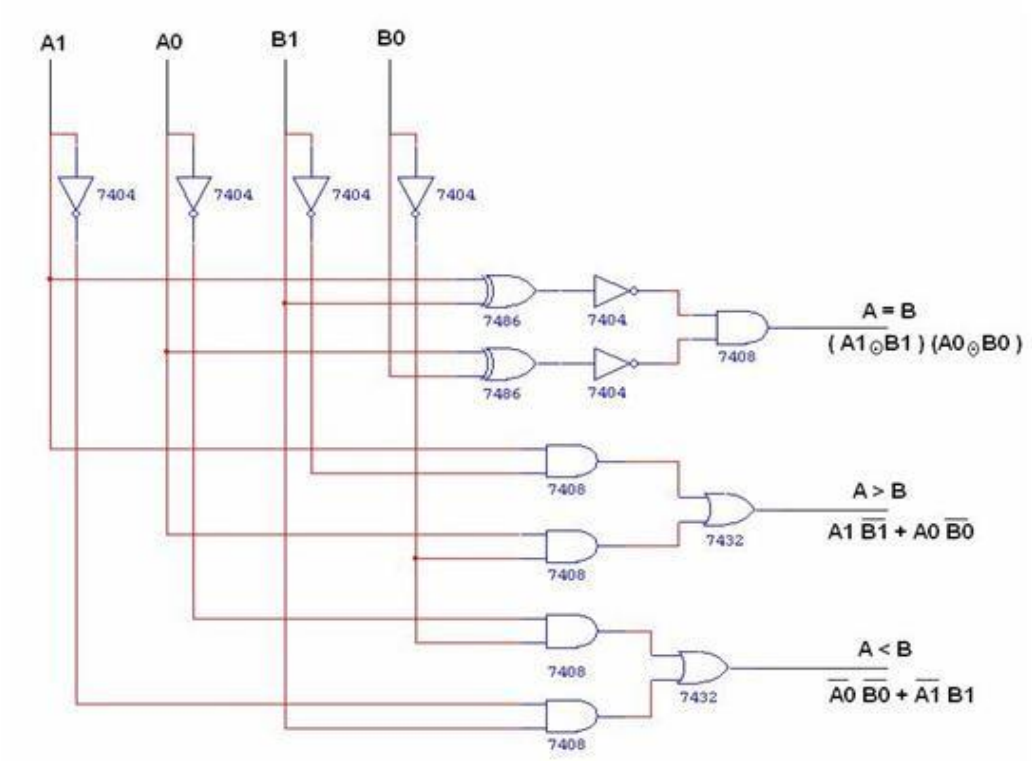
The same circuit can be used to compare the relative magnitude of two BCD digits. Where, A = B is expanded as,

$$A = B = (A_3 + B_3)\,(A_2 + B_2)\,(A_1 + B_1)\,(A_0 + B_0)$$

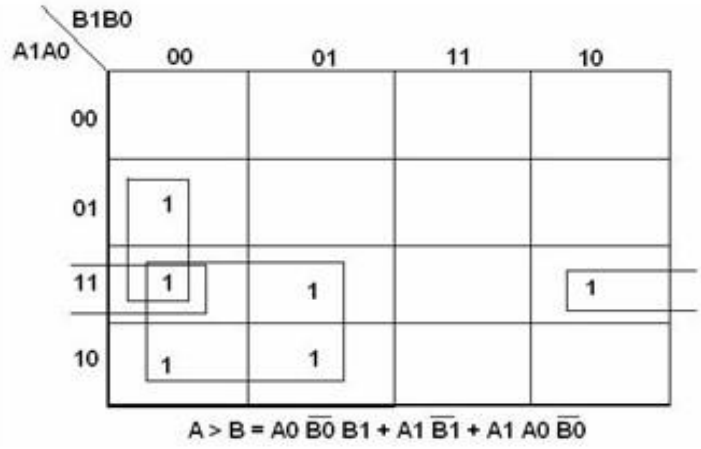
$x_3$ x2 x1 x0

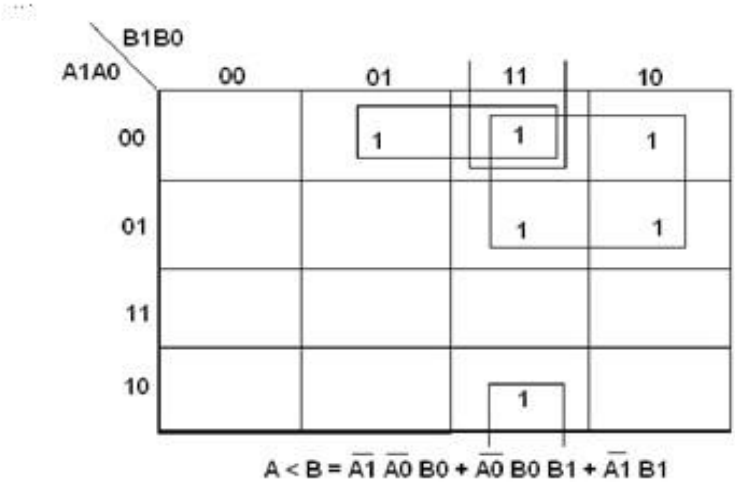
**LOGIC DIAGRAM:**

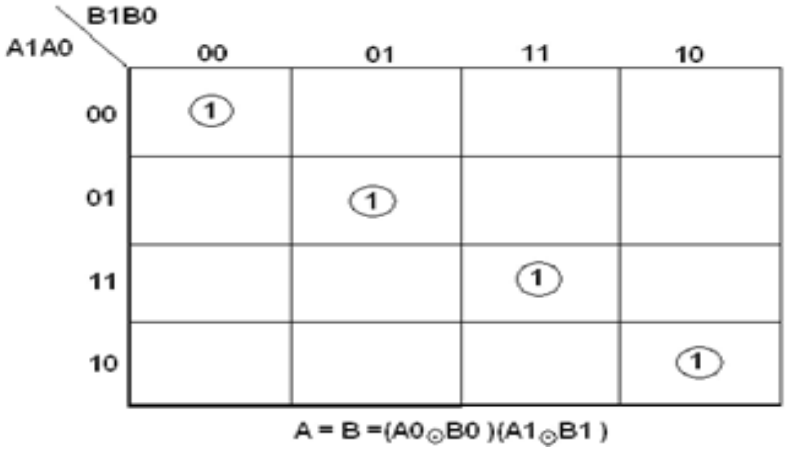
**2 BIT MAGNITUDE COMPARATOR**



## K MAP


B1B0
A1A0
00
01
11
10
1
A > B = A0 $\overline{B0}$ B1 + A1 $\overline{B1}$ + A1 A0 $\overline{B0}$


B1B0
A1A0
00
01
11
10
1
A < B = $\overline{A1}$ $\overline{A0}$ B0 + $\overline{A0}$ B0 B1 + $\overline{A1}$ B1


B1B0
A1A0
00
01
11
10
1
A = B =(A0⊙B0 )(A1⊙B1 )

**TRUTH TABLE**

| A1 | A0 | B1 | B0 | A > B | A = B | A < B |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 |

**PROCEDURE:**

(i) Verify the gates

(ii) Connections are given as per circuit diagram.

(iii) Logical inputs are given as per circuit diagram.

(iv) Observe the output and verify the truth table.

**Questions:**