EXPERIMENT NO: 5

Implementation of Adder Half Adder and Full Adder

APPARATUS:

7486, 7432, 7408, 7404 IC's, logic kit and connecting leads.

HALF ADDER:

Half Adder is combinational logic circuit that generates the sum of two binary numbers (each having 1 bit length). The logic circuit has two inputs and two outputs i.e. Sum & Carry abbreviated as S_{HA} & C_{HA} respectively.

First of all, we shall construct Truth Table of Half Adder

Inputs		Outputs			
		$S_{HA} = x'y+xy'$		$C_{HA} = x\ y$	
x	y	Actual	Observed	Actual	Observed
0	0				
0	1				
1	0				
1	1				

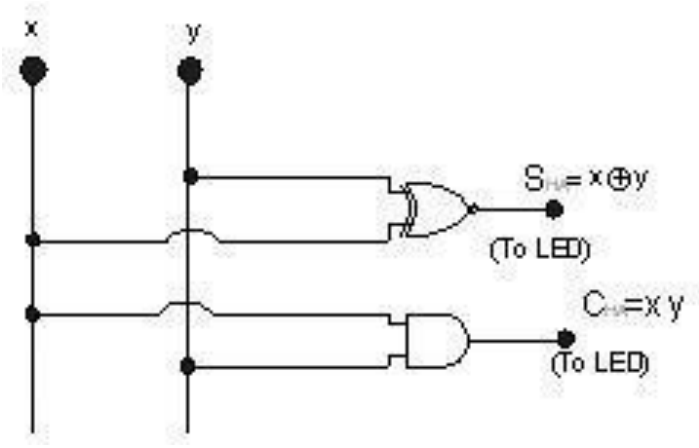
Now we write Boolean function from above Truth Table as

$$S_{HA} = x'y +$$

$$xyC_{HA} = xy$$

IMPLEMENTATION

Now we implement above Boolean expression by basic logic gates i.e.



Now we shall check this logic circuit by the Truth Table of Half Adder.

Lab Exercise:

1. Students are required to write outputs of Full adder using Basic logic gates..
2. Then implement Half Adder using basic logic gates.

FULL ADDER:

Full Adder is combination logic circuit that performs the sum of 3 input binary numbers, (each having 1 bit length). Two of the binary input variables are x and y represent the two significant bits to be added the third input z, represents the carry from previous lower significant position. Outputs of Full Adder are Sum and Carry represented as S_{FA} and C_{FA} respectively.

First of all, we shall construct Truth Table of Full Adder i.e.

Truth Table

Inputs			Outputs			
x	y	z	S_{FA}		C_{FA}	
			Actual	Observed	Actual	Observed
0	0	0				
0	0	1				
0	1	0				
0	1	1				
1	0	0				
1	0	1				
1	1	0				
1	1	1				

Now we write Boolean expression for Sum and Carry of Full Adder.

1) **Sum** = $x'y'z+x'yz'+xy'z'+xyz$

Simplifying by using Boolean Postulates & theorems/k-map, we get

$$Sum = (x'y+xy')'.z + (x'y+xy').z'$$

$$S_{FA} = (x \oplus y) \oplus z$$

2) $Carry = x'yz + xy'z + xyz'+xyz$

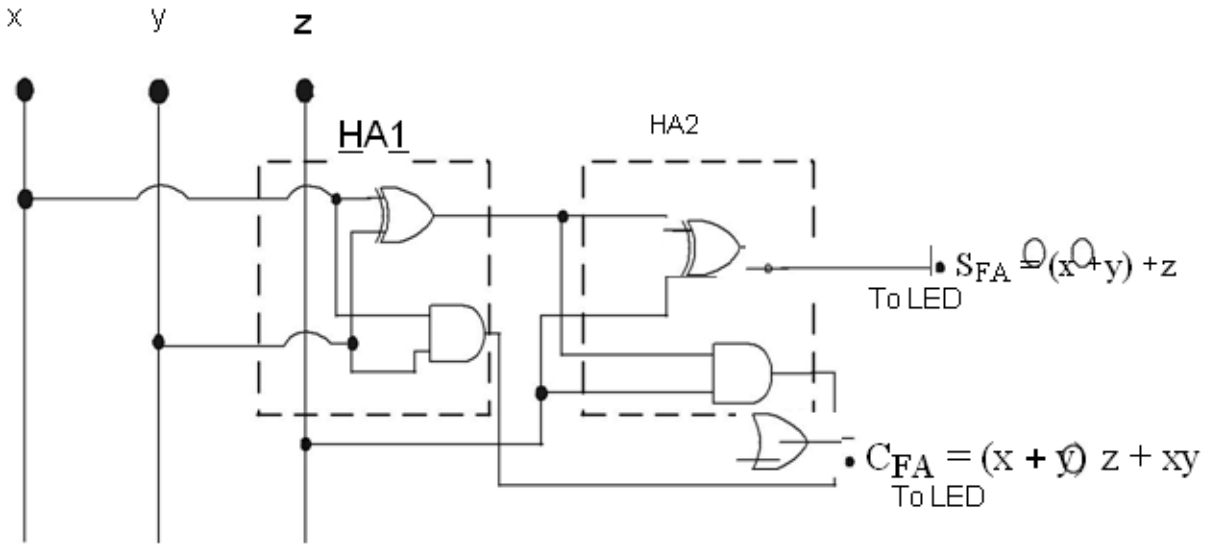
Simplifying by using Boolean Postulates & theorems/k-map, we get

Carry = $(x'y+xy').\ z+xy$

$$\mathbf{C_{FA} = (x \oplus y)\ z + xy}$$

Implementation

Now we implement simplified Boolean expressions of S_{FA} & C_{FA} i.e.



We shall check this logic circuit by the Truth Table of Full Adder