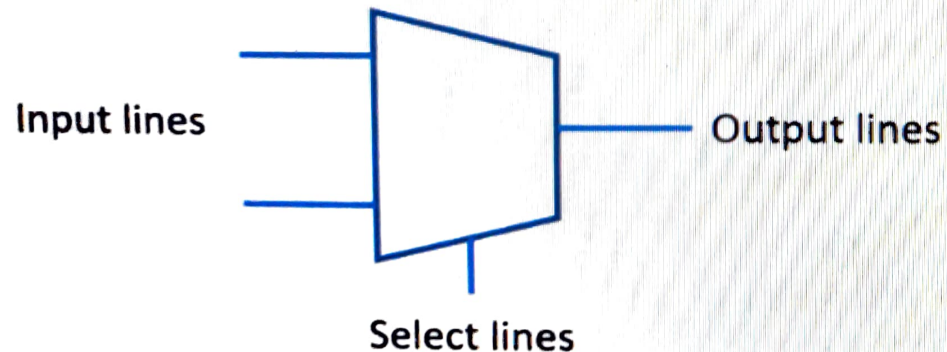
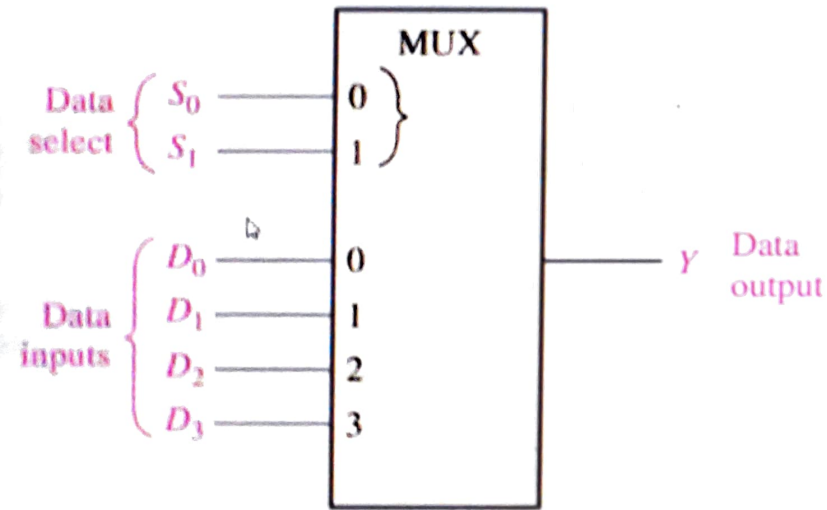


# Multiplexer (Data selector)

- MUX
- Combinational circuit that selects binary information from one of many input lines and directs it to a single output line
- The selection of a particular input line is controlled by a set of selection lines.
- Normally, there are  $2^n$  input lines and  $n$  selection lines whose bit combinations determine which input is selected.
- A two-to-one-line multiplexer connects one of two 1-bit sources to a common destination



# Multiplexer



Data selection for a 1-of-4-multiplexer.

Data-Select Inputs		Input Selected
$S_1$	$S_0$	
0	0	$D_0$
0	1	$D_1$
1	0	$D_2$
1	1	$D_3$

The data output is equal to  $D_0$  only if  $S_1 = 0$  and  $S_0 = 0$ :  $Y = D_0\bar{S}_1\bar{S}_0$ .

The data output is equal to  $D_1$  only if  $S_1 = 0$  and  $S_0 = 1$ :  $Y = D_1\bar{S}_1S_0$ .

The data output is equal to  $D_2$  only if  $S_1 = 1$  and  $S_0 = 0$ :  $Y = D_2S_1\bar{S}_0$ .

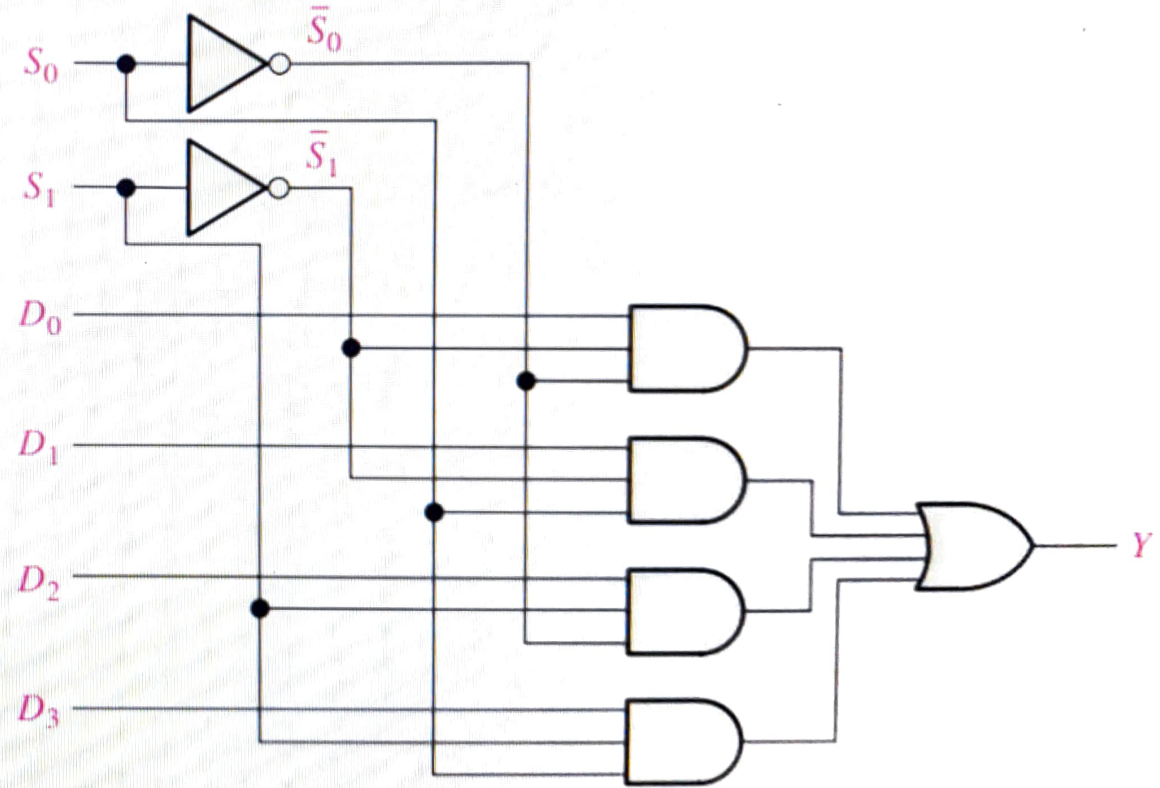
The data output is equal to  $D_3$  only if  $S_1 = 1$  and  $S_0 = 1$ :  $Y = D_3S_1S_0$ .

the total expression for the data output is

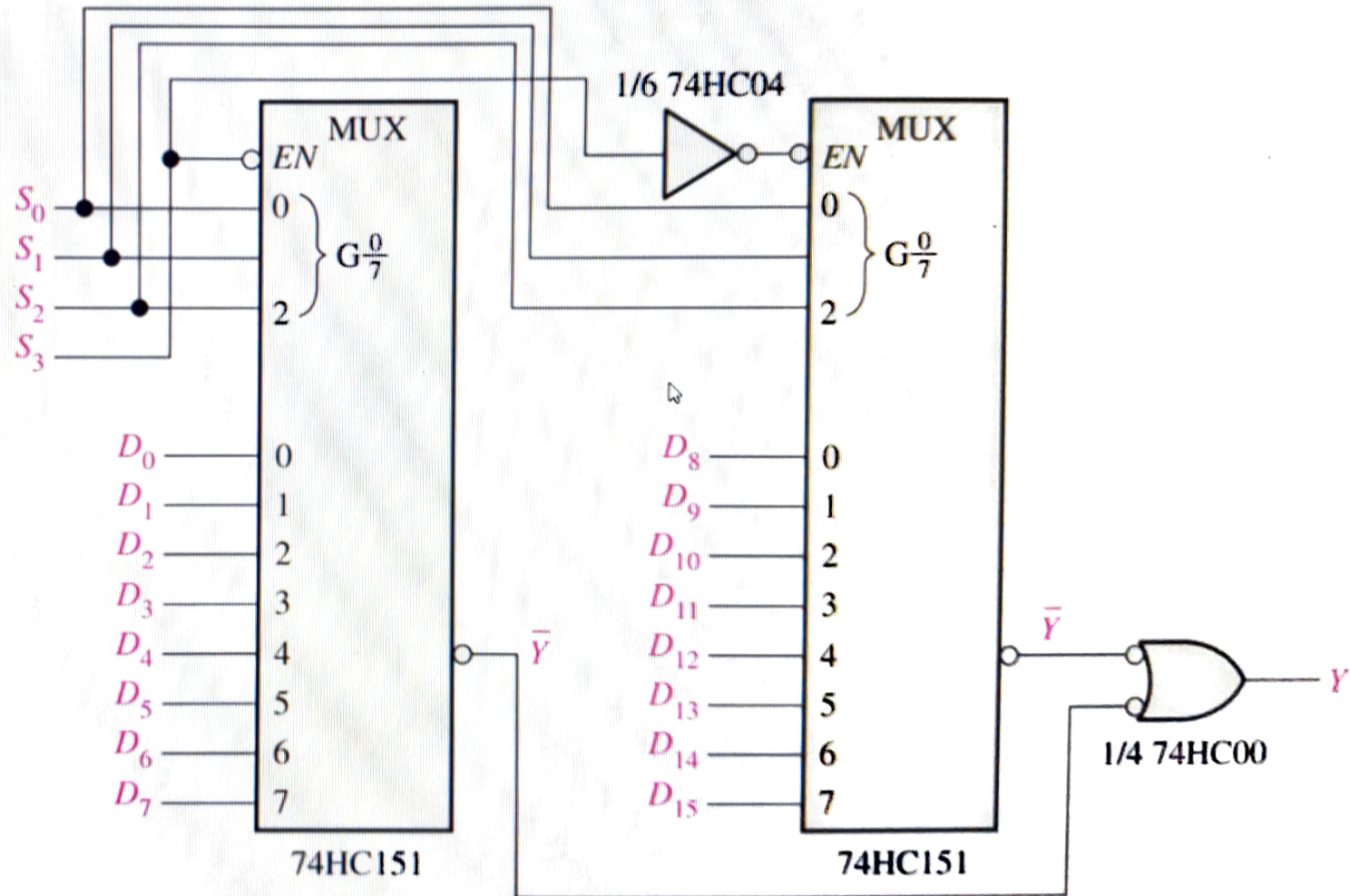
$$Y = D_0\bar{S}_1\bar{S}_0 + D_1\bar{S}_1S_0 + D_2S_1\bar{S}_0 + D_3S_1S_0$$

# Multiplexer

$$Y = D_0\bar{S}_1\bar{S}_0 + D_1\bar{S}_1S_0 + D_2S_1\bar{S}_0 + D_3S_1S_0$$



# A 16-input MUX

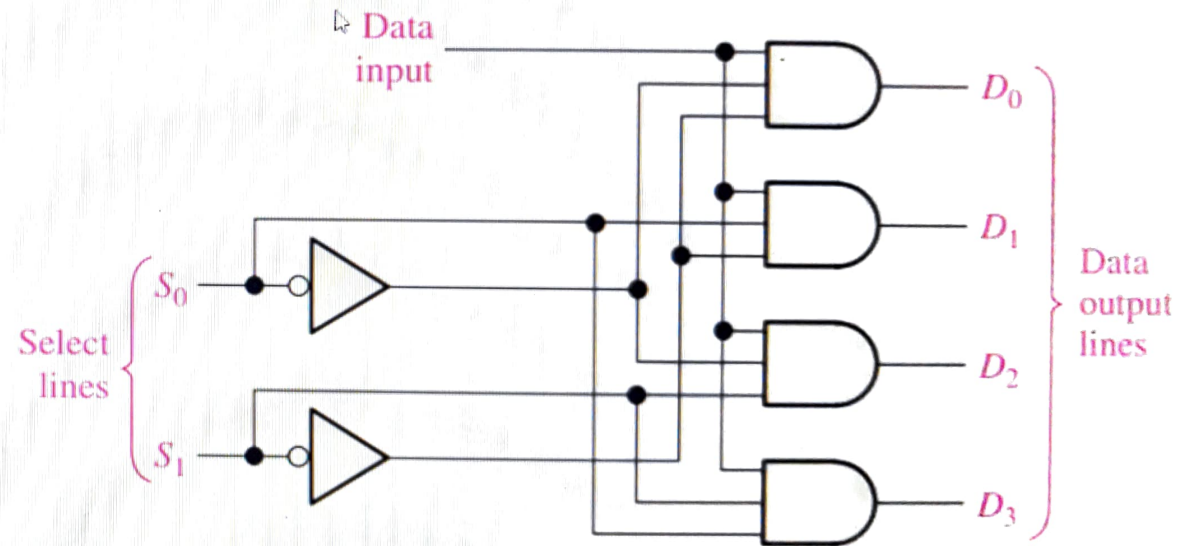




# Demultiplexers

- **DEMUX**

- reverses the multiplexing function.
- It takes digital information from one line and distributes it to a given number of output lines.
  - The demultiplexer is also known as a data distributor.
- Decoders can also be used as demultiplexers



# Parity generator/checker

- Nibble (4 bits)
- XOR is also called modulo-2 addition
- $A \oplus B = 1$  only when there are an odd number of 1's in (A,B). The same is true for  $A \oplus B \oplus C$  also
- **Basic Parity Logic**
  - The sum (disregarding carries) of an even number of 1s is always 0
  - The sum of an odd number of 1s is always 1

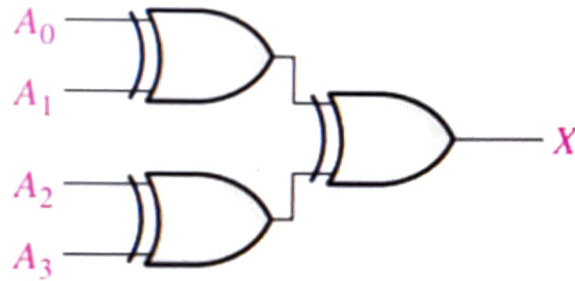
A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

# Modulo-2 sum

- The modulo-2 sum of two bits can be generated by an exclusive-OR gate
- The modulo-2 sum of four bits can be formed by three exclusive-OR gates



(a) Summing of two bits



(b) Summing of four bits