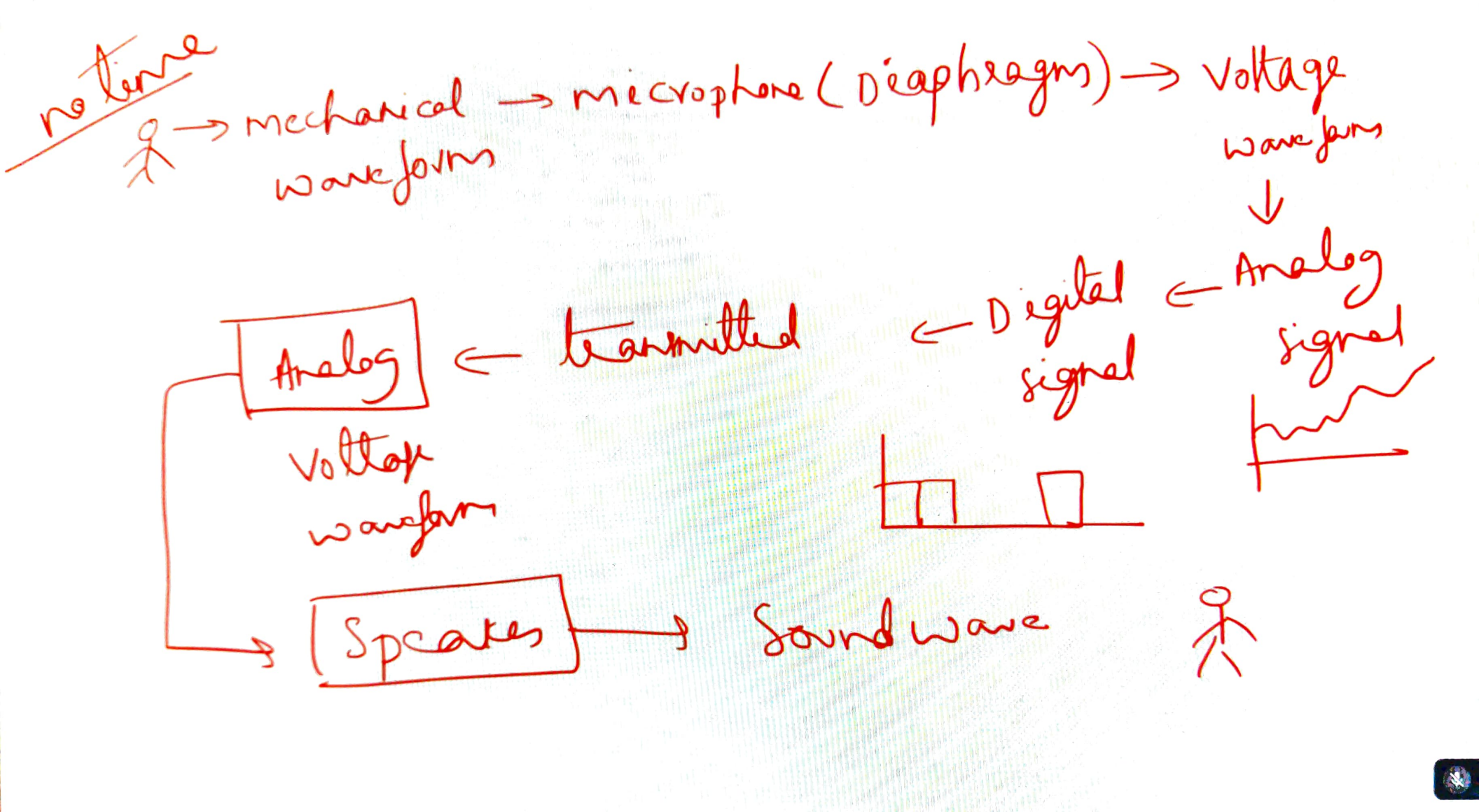
ADC & DAC


no time
mechanical waveforms
microphone (Diaphragm)
Voltage waveforms
Analog signal
Digital signal
transmitted
Analog
Voltage waveform
Speaker
Sound wave

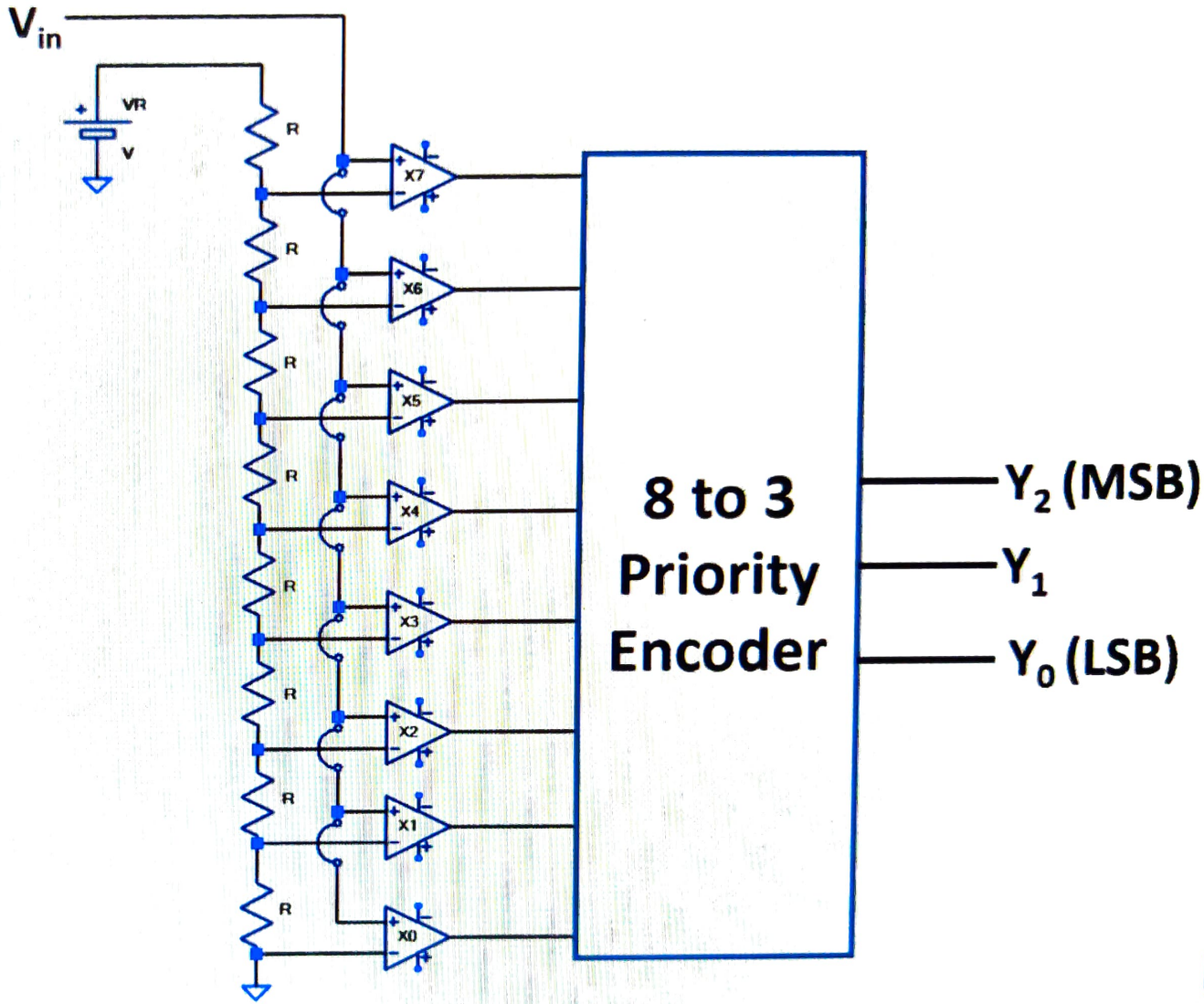
3-bit Analog to Digital converter

Flash/Parallel ADC

Resistive divider network

Total comparators = 2^3

8 to 3 Priority Encoder

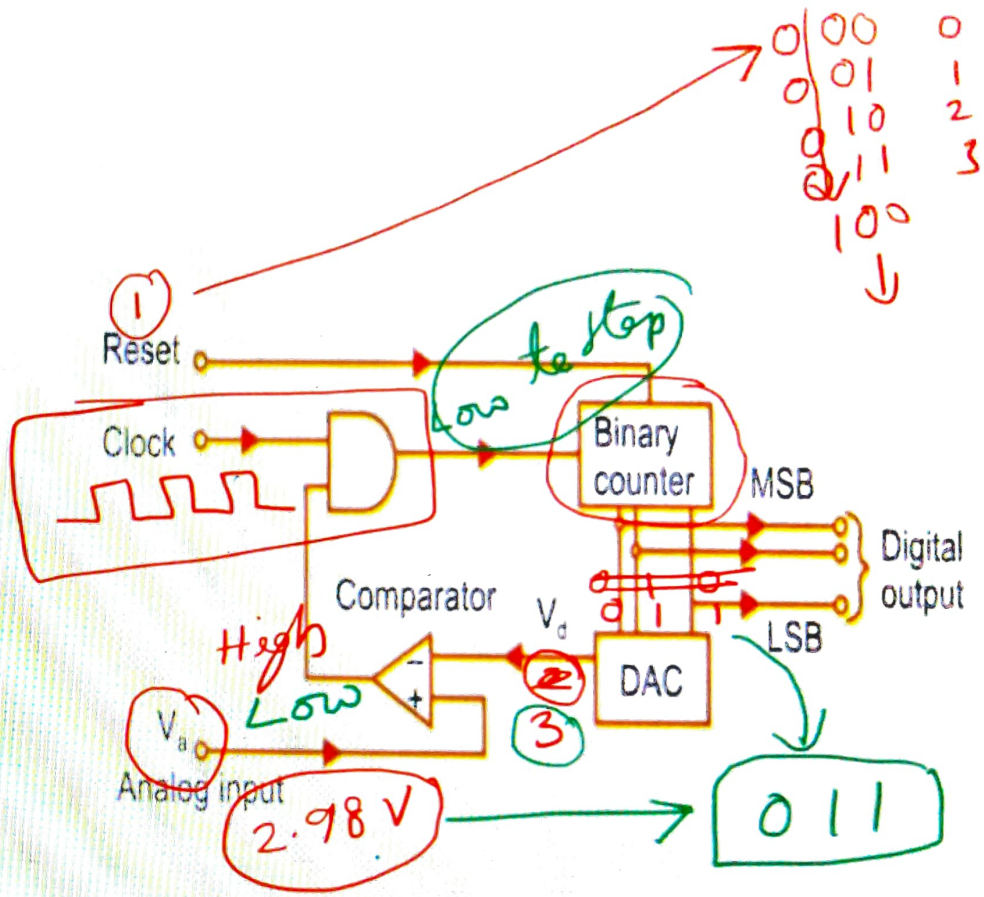


ADC

- An integrated circuit which converts analog (continuous) signal to digital (discrete) form.
- Analog signals are directly measurable quantities

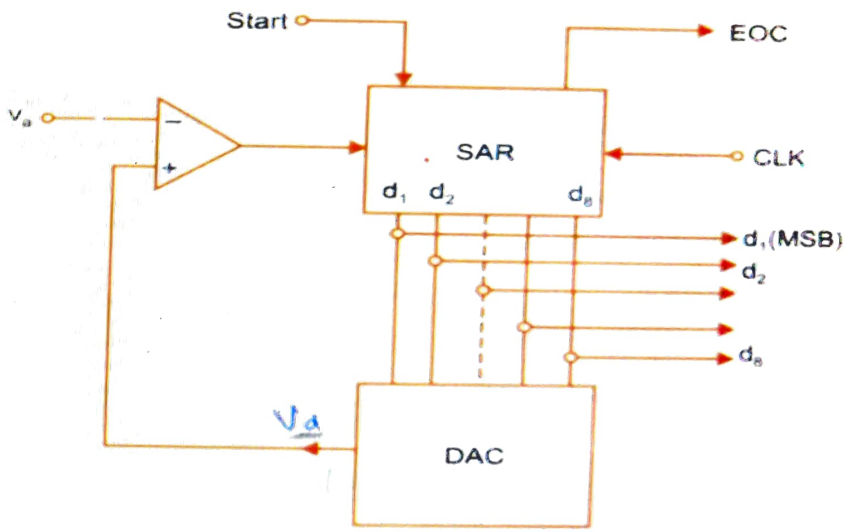
Counter type ADC

- A counter type ADC produces a digital output, which is approximately equal to the analog input by using counting (Binary counter) operation internally
- Initially reset the counter to zero
- Start the clock signal generator
- The counter gets incremented by one for every clock pulse and its value will be in binary (digital) format.
- The output of the counter is given to DAC.



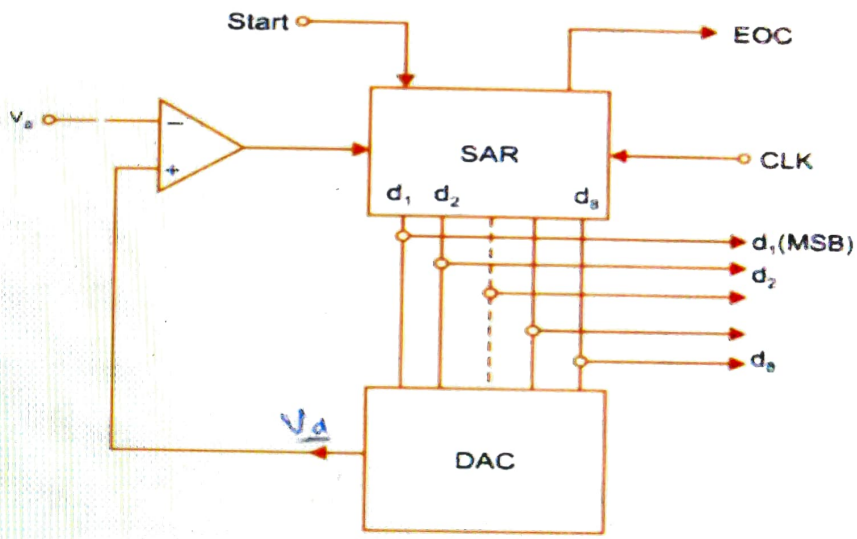
Succesive approximation ADC

- Clock signal generator, Successive Approximation Register (SAR), DAC, comparator and Control logic
- One of the most common analog-to-digital converters



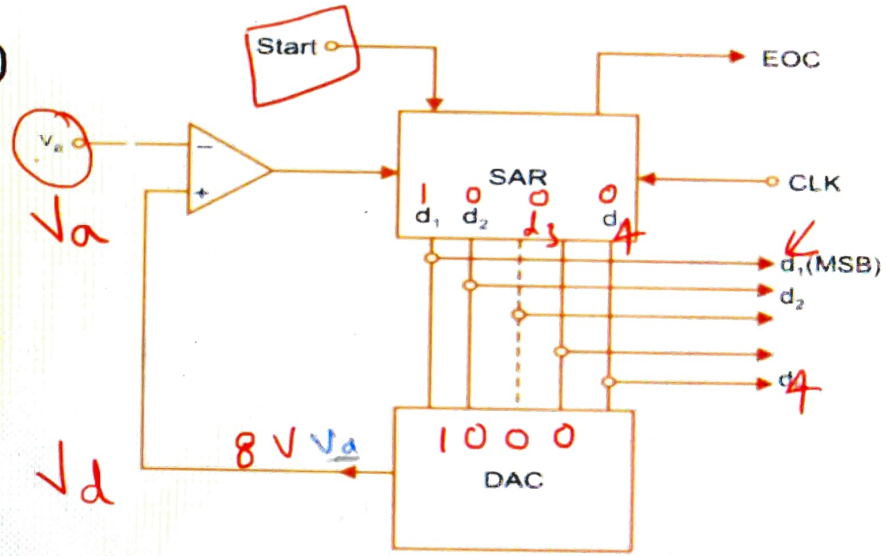
Succesive approximation ADC

1) Successive approximation uses an efficient “code search” strategy to complete n-bit conversion in just n-clock periods.
2) Thus it takes much shorter conversion time than counter type ADC.
3) Figure shows the block diagram of successive approximation DAC.
4) A four bit converter would require eight clock pulses to obtain a digital output.



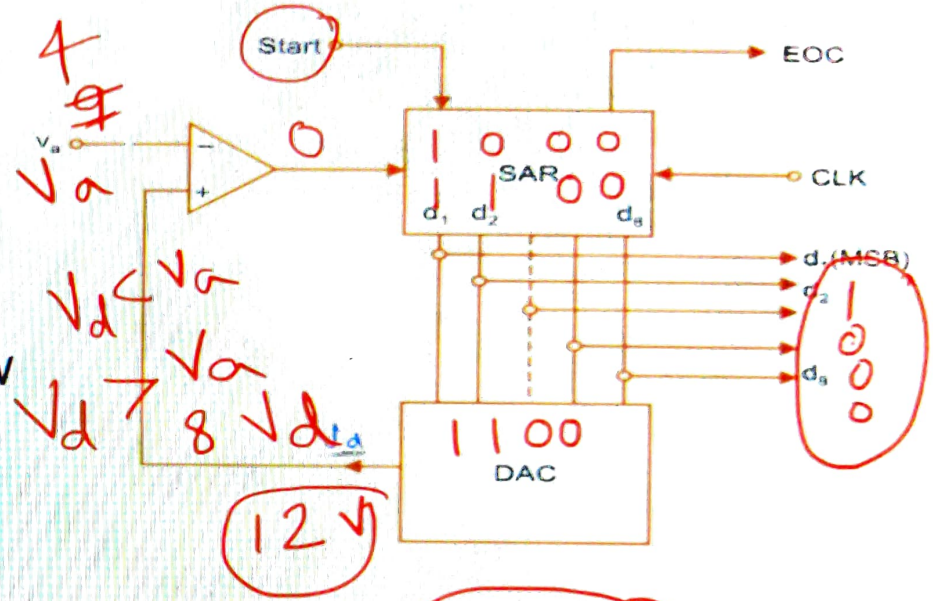
Succesive approximation ADC

- To start conversion “Start” input is made 1.
- SAR will set MSB to 1 and all other bits to 0 so that trial code output of SAR is D1,D2,D3,D4 = 1000.
- The output of SAR is then applied to DAC. The corresponding output DAC V_d is applied to comparator.



Succesive approximation ADC

- If $V_d < V_a$ i.e trial code is less than input signal, then output goes high which is applied to SAR.
- In response to high comparator output, MSB D1 is maintained at 1 and the next bit D2 is made 1. The trial code at the SAR output now becomes 1100. The corresponding DAC output is compared with *Va* and the process continues.
- However for the first trial code, $V_d > V_a$, then the comparator output will go low i.e. 0. The SAR will respond to it by reseting its MSB bits D1 to 0 and next bit D2=1 so that the new trial code is 0100.



numerical Analysis