# Sequential circuits

Dr. E. Paul Braineard

SAMRAT B
Good Evening Sir

RAMESH PALTHYA
good evening sir

Sai Kasyap
Good evening sir

JESWIN SAM
Good evening sir

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Raise hand

Turn on captions

Paul Brain
is present

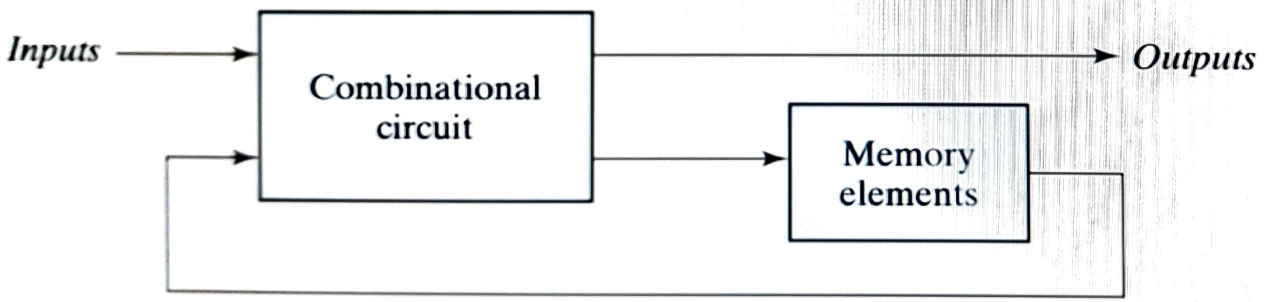
# Outline

- Latches
- Flip-Flops
  - SR
  - D
  - JK
  - T
- Timers

- Set
- Reset
- Monostable
- Bistable
- Astable

# Sequential circuits

- Combinational circuit + storage element in the feedback path
- Storage element (Memory)
  - Device capable of storing binary information
- State
  - The binary information stored in these elements at any given time




Block diagram of Sequential circuit

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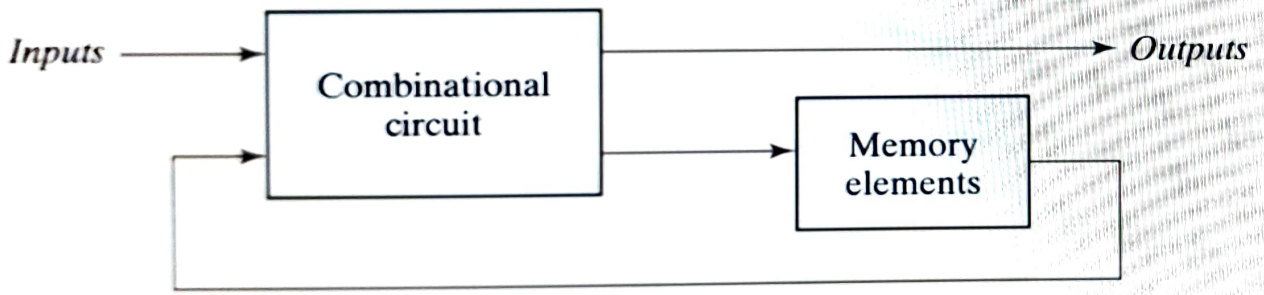


Block diagram of Sequential circuit

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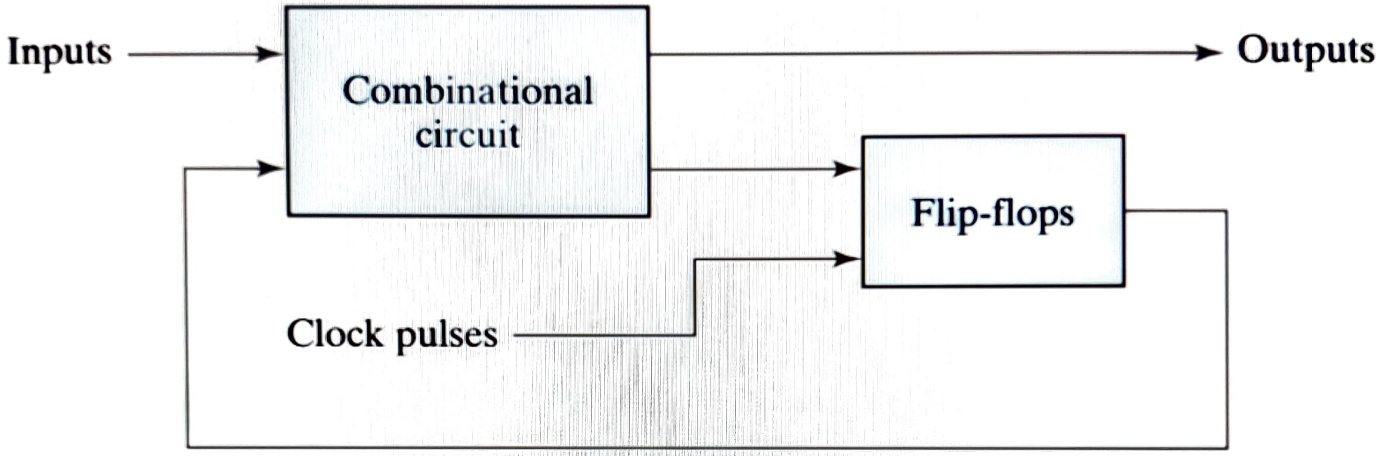
# Synchronous Sequential circuit




Block diagram of Synchronous Sequential circuit

Timing diagram of clock pulses

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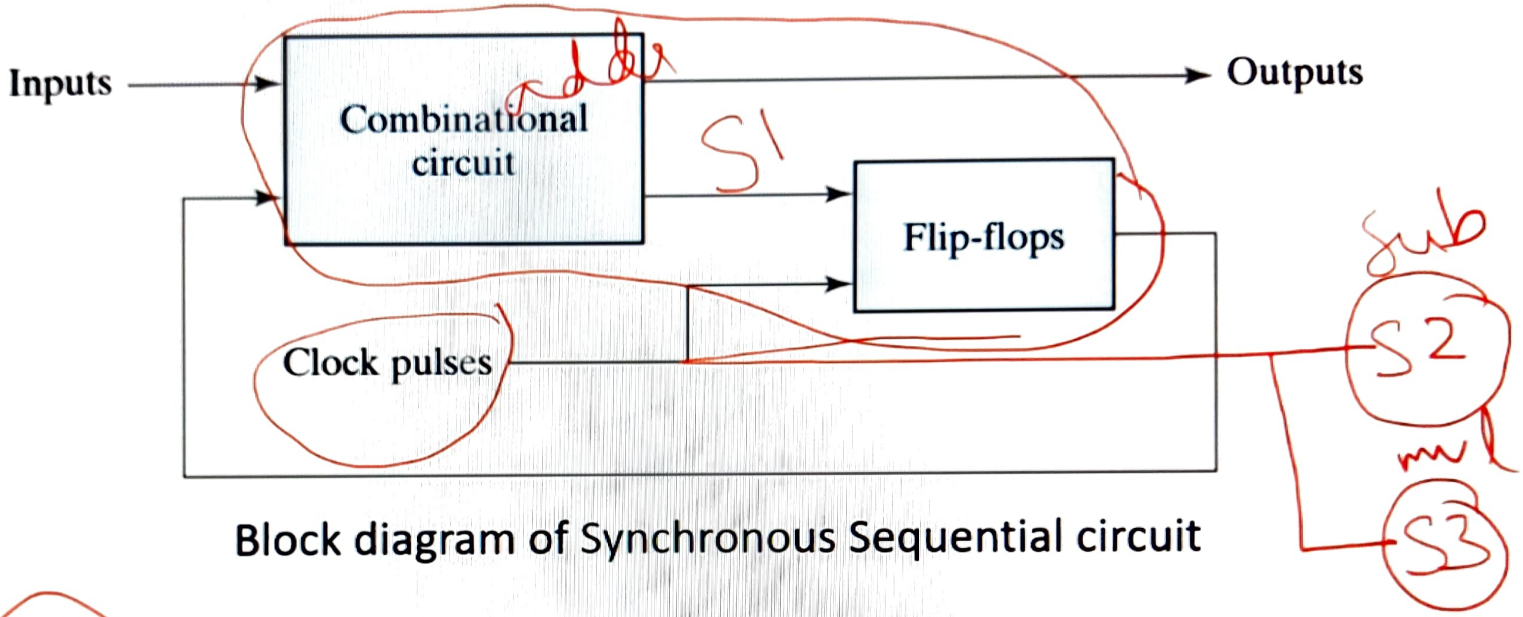
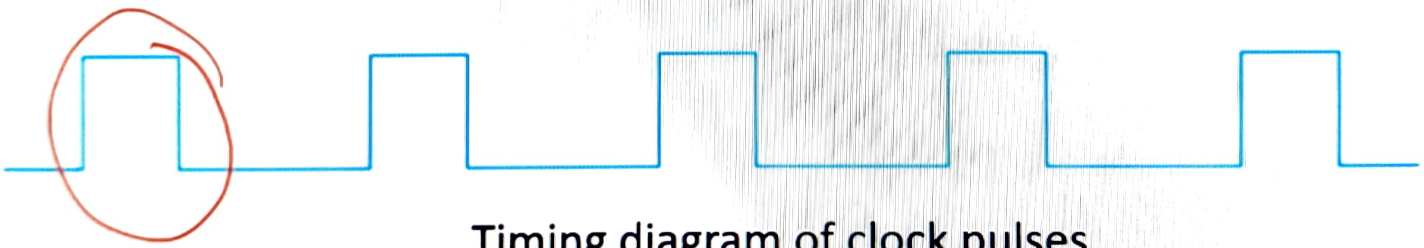
# Synchronous Sequential circuit




Block diagram of Synchronous Sequential circuit



Timing diagram of clock pulses

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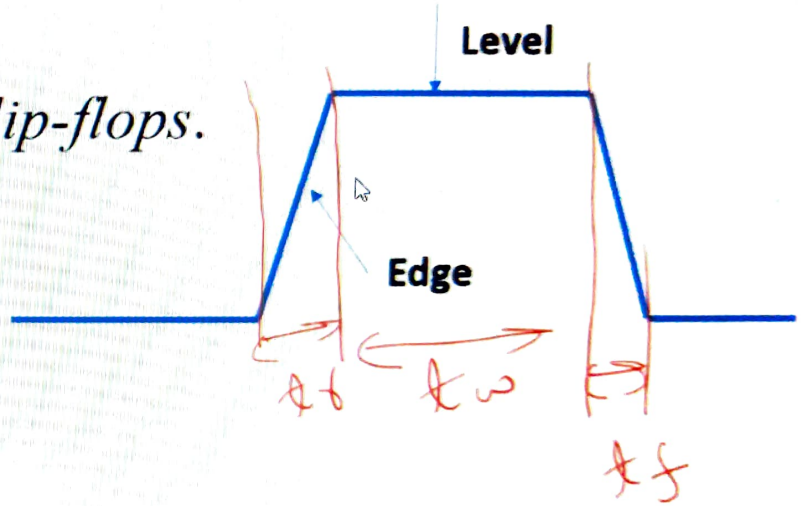
# Latches and flipflop

- *Storage elements that operate with signal levels are referred to as latches*
  - Latches are said to be level sensitive devices

- *Those controlled by a clock transition are flip-flops.*
  - Flip-flops are edge-sensitive devices.

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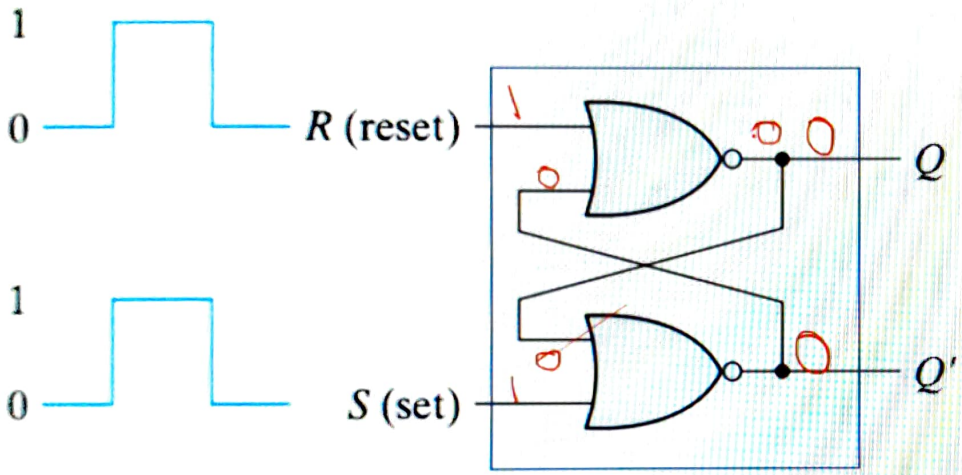
# SR Latch with NOR gates




| $S$ | $R$ | $Q$ | $Q'$ | |
|---|---|---|---|---|
| 1 | 0 | 1 | 0 | |
| 0 | 0 | 1 | 0 | (after $S = 1, R = 0$) |
| 0 | 1 | 0 | 1 | |
| 0 | 0 | 0 | 1 | (after $S = 0, R = 1$) |
| 1 | 1 | 0 | 0 | (forbidden) |

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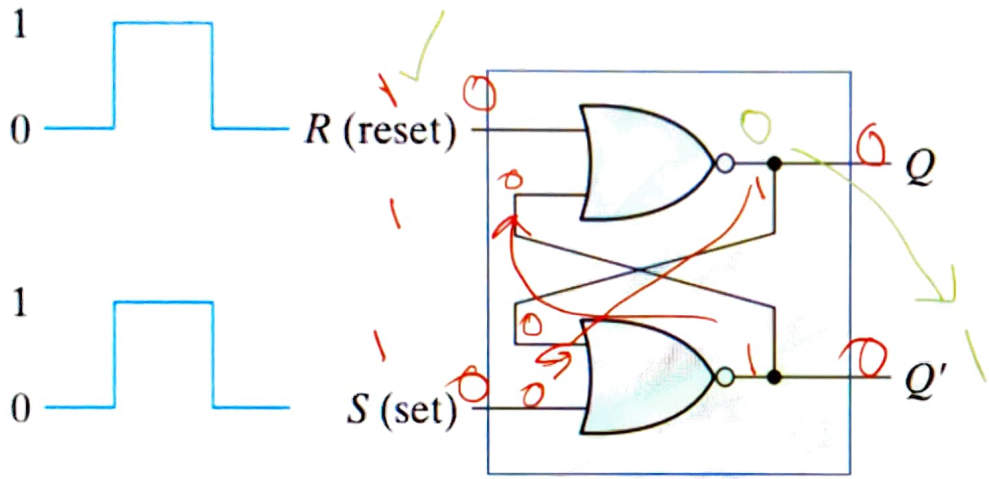
# SR Latch with NOR gates


| $S$ | $R$ | $Q$ | $Q'$ | |
|---|---|---|---|---|
| 1 | 0 | 1 | 0 | |
| 0 | 0 | 1 | 0 | (after $S = 1, R = 0$) |
| 0 | 1 | 0 | 1 | |
| 0 | 0 | 0 | 1 | (after $S = 0, R = 1$) |
| 1 | 1 | 0 | 0 | (forbidden) |

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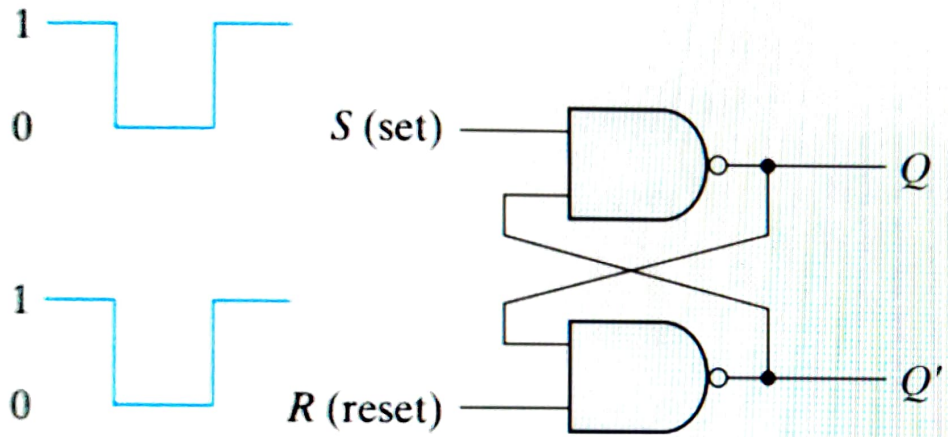
# SR Latch with NAND gates




| $S$ | $R$ | $Q$ | $Q'$ | |
|---|---|---|---|---|
| 1 | 0 | 0 | 1 | |
| 1 | 1 | 0 | 1 | (after $S = 1, R = 0$) |
| 0 | 1 | 1 | 0 | |
| 1 | 1 | 1 | 0 | (after $S = 0, R = 1$) |
| 0 | 0 | 1 | 1 | (forbidden) |

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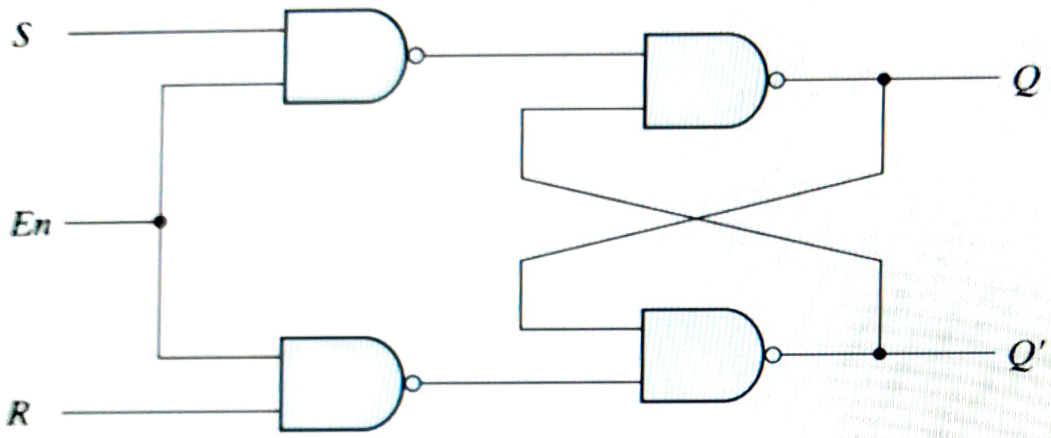
# SR Latch with control input




(a) Logic diagram

| *En* | *S* | *R* | Next state of *Q* |
|---|---|---|---|
| 0 | X | X | No change |
| 1 | 0 | 0 | No change |
| 1 | 0 | 1 | $Q = 0$; reset state |
| 1 | 1 | 0 | $Q = 1$; set state |
| 1 | 1 | 1 | Indeterminate |

(b) Function table

- In either case, when En returns to 0, the circuit remains in its current state.
- An indeterminate condition occurs when all three inputs are equal to 1

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