Welcome to ECE Lab

Latches & Flip-flops

There are two types of memory elements based on the type of triggering that is suitable to operate it.

1. Latches

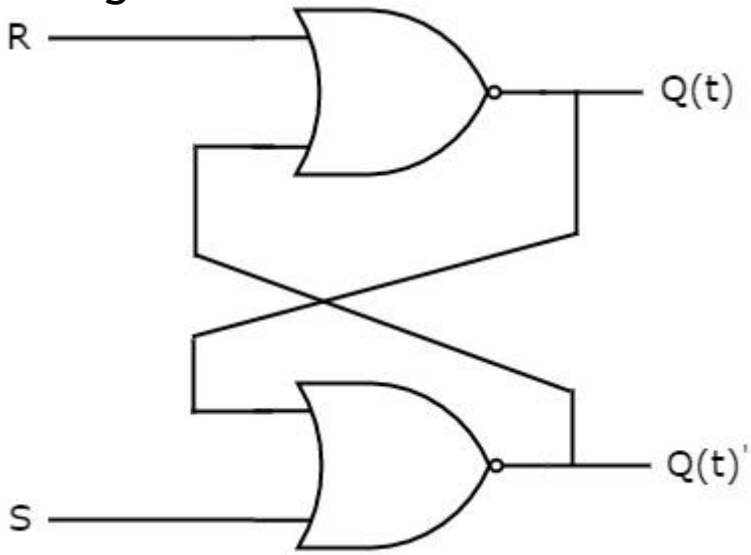
2. Flip-flops

Latches operate with enable signal, which is **level sensitive**. Whereas, flip-flops are edge sensitive.

Latches	Flip Flops
Latches are building blocks of sequential circuits and these can be built from logic gates	Flip flops are also building blocks oof sequential circuits. But, these can be built from the latches.
Latch continuously checks its inputs and changes its output correspondingly.	Flip flop continuously checks its inputs and changes its output correspondingly only at times determined by clocking signal
The latch is sensitive to the duration of the pulse and can send or receive the data when the switch is on	Flipflop is sensitive to a signal change. They can transfer data only at the single instant and data cannot be changed until next signal change. Flip flops are used as a register.
It is based on the enable function input	It works on the basis of clock pulses
It is a level triggered, it means that the output of the present state and input of the next state depends on the level that is binary input 1 or 0.	It is an edge triggered, it means that the output and the next state input changes when there is a change in clock pulse whether it may a +ve or -ve clock pulse.

SR Latch

An **SR latch** (Set/Reset) is an asynchronous device. It works independently of control signals and relies only on the state of the S and R inputs. In the image we can see that an SR latch can be created with two NOR gates that have a cross-feedback loop. SR latches can also be made from NAND gates, but the inputs are swapped and negated.

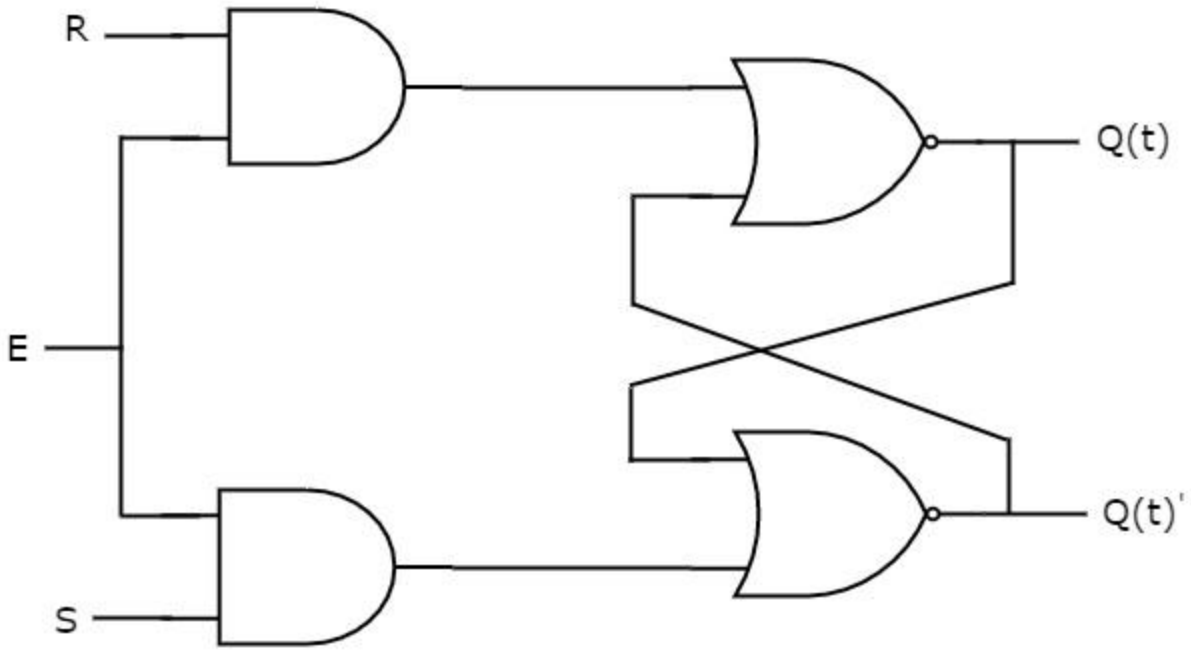


Truth Table

S	R	Q	$\overline{Q}$
0	0	Latched	
0	1	0	1
1	0	1	0
1	1	Illegal	

Gated SR Latch

The **gated SR latch** is a simple extension of the SR latch which provides an *Enable* line which must be driven high before data can be latched

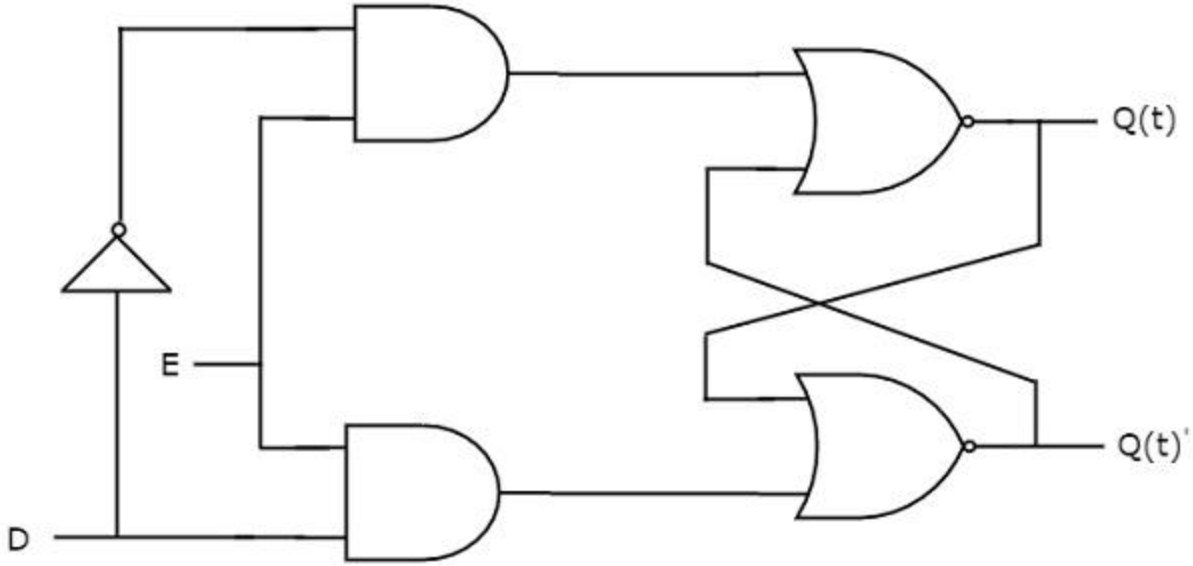


Truth Table

Enable	S	R	Q	$\overline{Q}$
0	0	0	Latched	
0	0	1	Latched	
0	1	0	Latched	
0	1	1	Latched	
1	0	0	Latched	
1	0	1	0	1
1	1	0	1	0
1	1	1	Illegal	

D Latch

There is one drawback of SR Latch. That is the next state value can't be predicted when both the inputs S & R are one. So, we can overcome this difficulty by D Latch. It is also called as Data Latch. The D latch or transparent latch is a simple extension of the gated SR latch that removes the possibility of invalid input states.

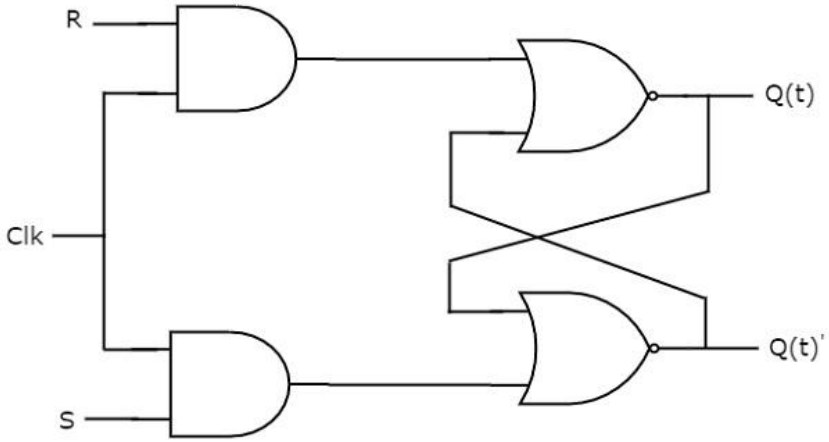


Truth Table

Enable	D	Q	$\overline{Q}$
0	0	Latched	
0	1	Latched	
1	0	0	1
1	1	1	0

SR - Flip-Flop

Circuit Diagram

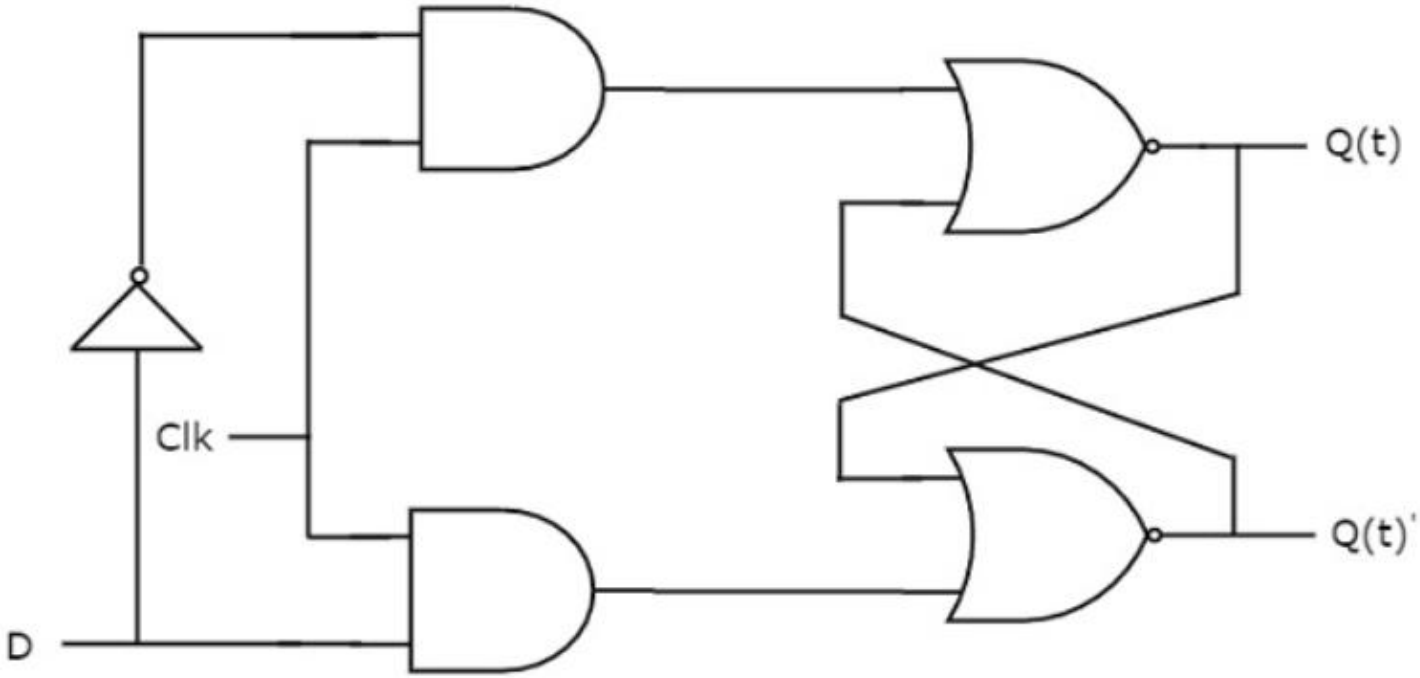


Truth Table

INPUTS			OUTPUT	STATE
CLK	S	R	Q	
X	0	0	No Change	Previous
↑	0	1	0	Reset
↑	1	0	1	Set
↑	1	1	-	Forbidden

D Flip-flop

Circuit Diagram



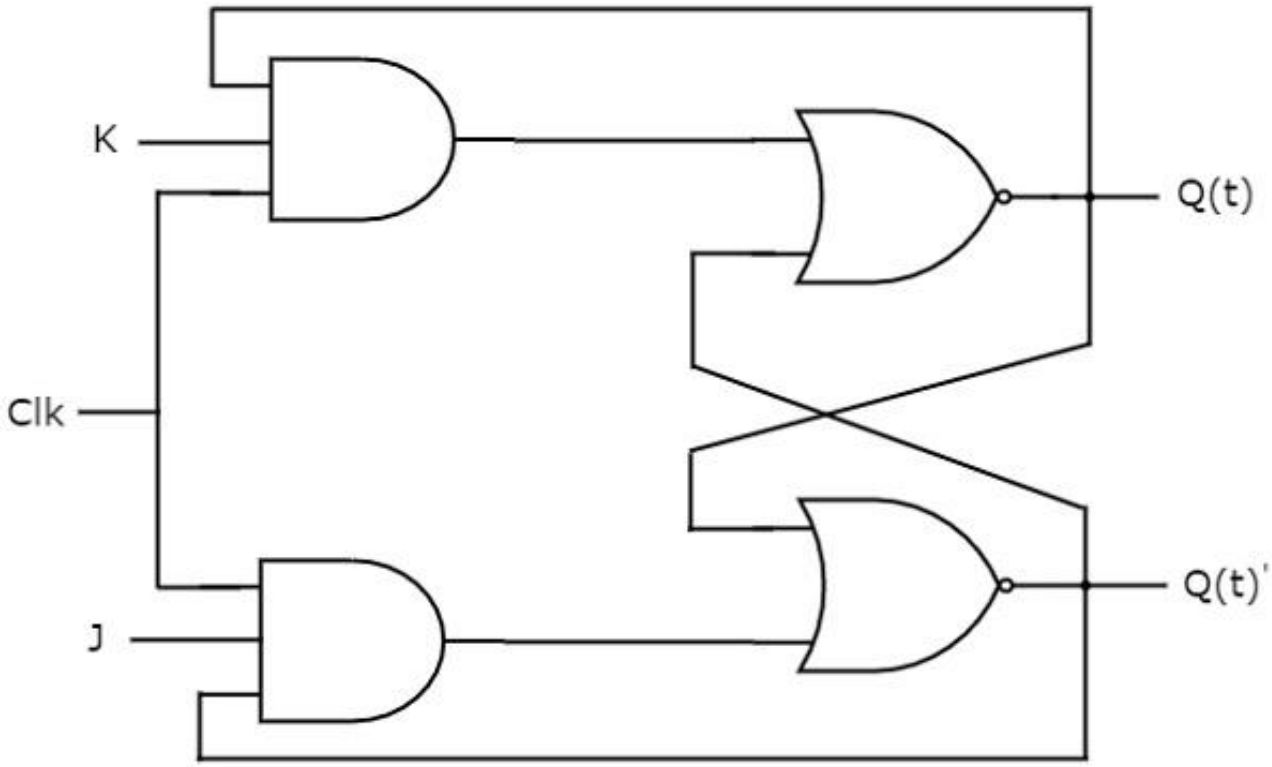
Truth Table

D Flip Flop with Preset and Clear Inputs

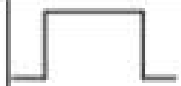
Inputs				Output		Comment
$\overline{PR}$	$\overline{CR}$	CLK	D	Q_{n+1}	$\overline{Q_{n+1}}$	
0	0	X	X	$\overline{Q_n}$	Q_n	Avoid
0	1	X	X	1	0	Preset
1	0	X	X	0	1	Clear
1	1	0	X	Q_n	$\overline{Q_n}$	No Change
1	1	1	0	0	1	Reset
1	1	1	1	1	0	Set

JK Flip-flop

Circuit Diagram



JK Flip-Flop Truth Table

		Inputs			Output
PR	CLR	CLK	J	K	Q
0	0	X	X	X	Race Condition
0	1	X	X	X	1
1	0	X	X	X	0
1	1	X	0	0	No change
1	1		0	1	0
1	1		1	0	1
1	1		1	1	Toggle

Thank You