Gate-Level Minimization
Karnaugh map or K-map

Gate-Level Minimization

- Design task of finding an optimal gate-level implementation of the Boolean functions describing a digital circuit
- The complexity of implementing digital logic gates is directly related to the complexity of the algebraic expression
- Simple straightforward procedure for minimizing Boolean functions is
  - Karnaugh map or K-map

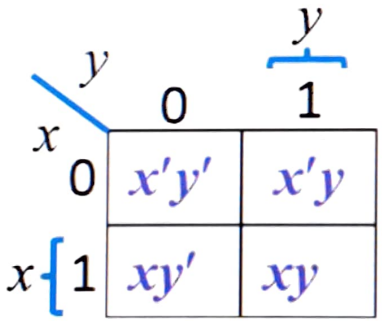
Karnaugh map

- Diagram of squares
- Each square represents one minterm of the function that is to be minimized

Two-variable K-map

- Two variables
- Four minterms
- The K-map consists of four squares, one for each minterm

m_0	m_1
m_2	m_3



00	01
10	11

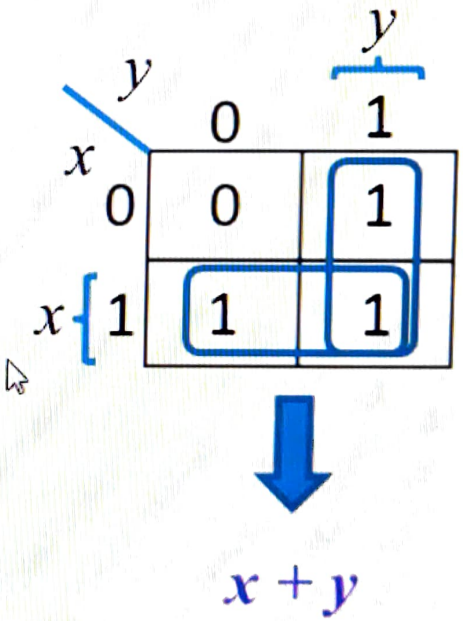
0	0
0	1
1	0
1	1

Two-variable K-map

- Minimize the function $m_1 + m_2 + m_3$
- $m_1 + m_2 + m_3 = x'y + xy' + xy = x + y$

m_0	m_1
m_2	m_3

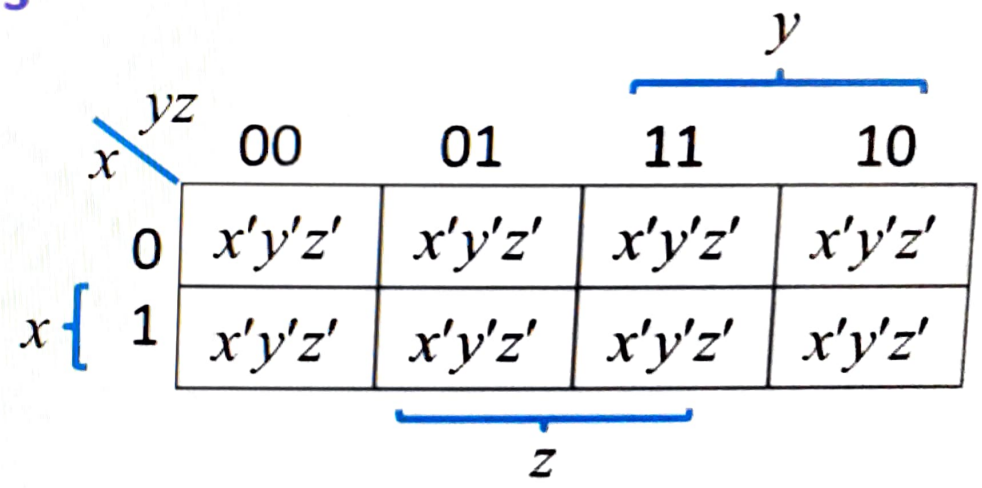
$x'y'$	$x'y$
xy'	xy



Three-variable K-map

- Three variable K-map
- There are eight minterms
- ∴ Eight squares
- Characteristic: **Only one bit changes**

m_0	m_1	m_3	m_2
m_4	m_5	m_7	m_6



Three-variable K-map

- Simplify the Boolean function F(x, y, z) = Σ(2, 3, 4, 5)
- xy′ + x′y