Clock responses

(a) Response to positive level

(b) Positive-edge response

(c) Negative-edge response

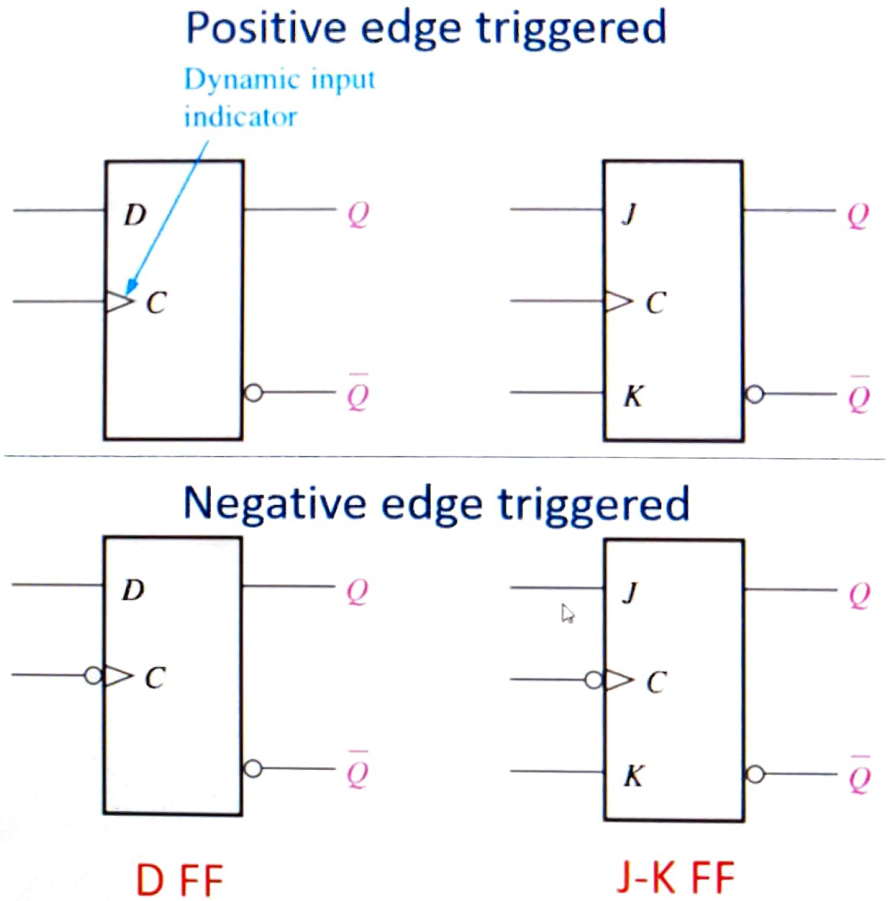
Clock response in latch and flip-flop

Dr. E. Paul Braineard

Raise hand
Turn on captions
Paul Brai
is prese

Edge-triggered flip-flop

- Changes state either at the positive edge (rising edge) or at the negative edge (falling edge) of the clock pulse
- Sensitive to the inputs only at this transition of the clock
- Two types of edge-triggered flip-flops are covered in this section
  - D FF
  - J-K FF

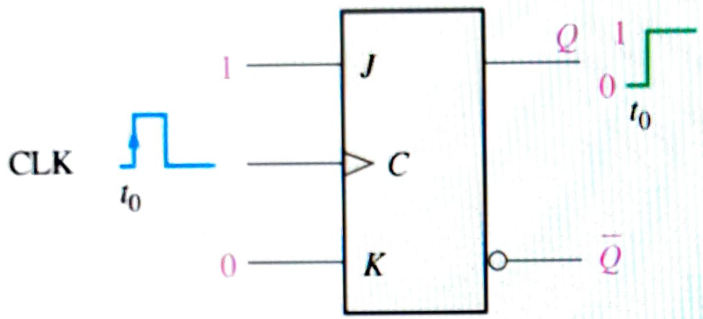


Graphic symbols

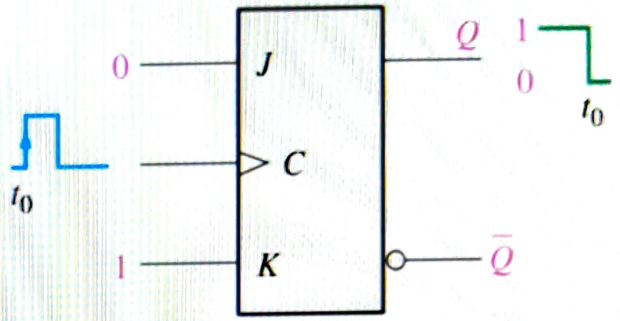
Dr. E. Paul Braineard

Feb2021)
Raise hand
Turn on captions
Paul Brainea
is presentin

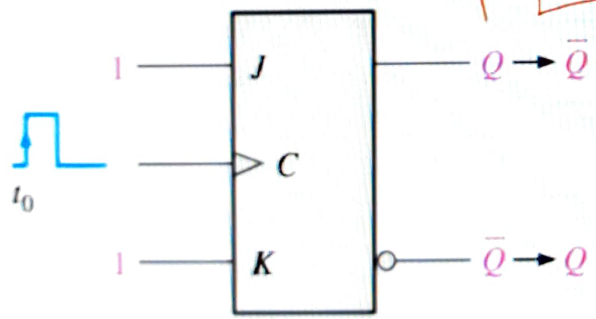
Operation of a positive edge-triggered J-K flip-flop



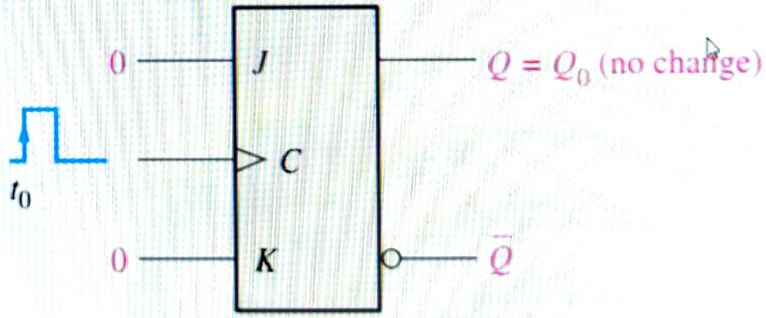
(a) $J = 1$, $K = 0$ flip-flop SETS on positive clock edge. (If already SET, it remains SET.)



(b) $J = 0$, $K = 1$ flip-flop RESETS on positive clock edge. (If already RESET, it remains RESET.)



(c) $J = 1$, $K = 1$ flip-flop changes state (toggle).



(d) $J = 0$, $K = 0$ flip-flop does not change. (If SET, it remains SET; if RESET, it remains RESET.)

Dr. E. Paul Braineard

eb2021)
Raise hand
Turn on captions
Paul Brain
is preser

J-K Flip-flop

Truth table for a positive edge-triggered J-K flip-flop.

Inputs			Outputs		
J	K	CLK	Q	$\overline{Q}$	Comments
0	0	↑	Q_0	$\overline{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	$\overline{Q}_0$	Q_0	Toggle

↑ = clock transition LOW to HIGH

Q_0 = output level prior to clock transition

021)

Raise hand

Turn on captions

Paul is p

Problem

- Determine the Q and $\bar{Q}$ output waveforms of the flip-flop in Figure 1 for the J-K and CLK inputs in Figure 2. Assume that the positive edge-triggered flip-flop is initially RESET.

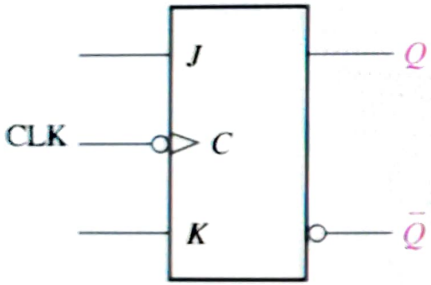


Figure 1

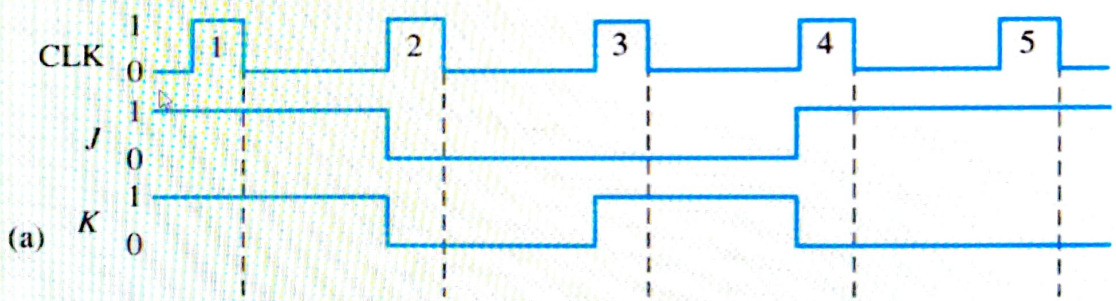


Figure 2

2021)

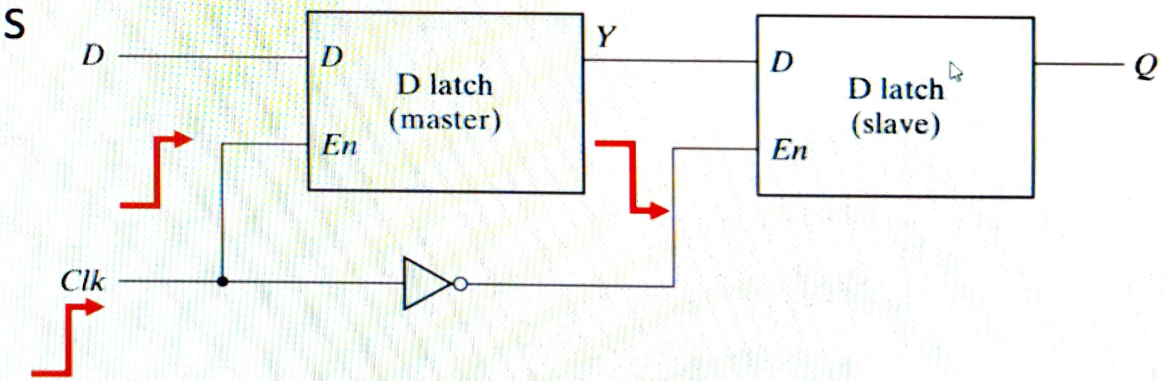
Raise hand

Turn on captions

Paul Brain
is preser

Master–slave *D* flip-flop

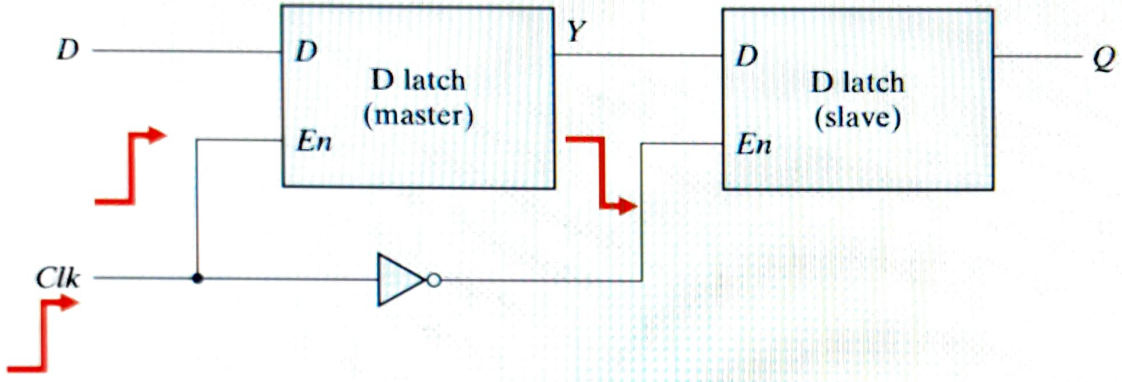
- Only the change in Master latch will bring change in Slave latch, hence called master slave
- master slave flip flop is triggered either on the rising edge of the clock signal or on falling edge of clock signal depending on the design
- When rising edge of clock is there at master, there will be falling edge of the clock at slave

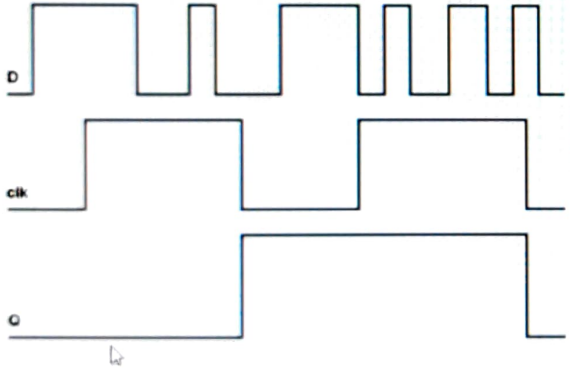


Dr. E. Paul Braineard

2021)
Raise hand
Turn on captions
Paul Brair
is preser

Master–slave *D* flip-flop





What is the application of master slave FF?
Simulate this FF in logisim

Dr. E. Paul Braineard

b2021)
Raise hand
Turn on captions
Paul Brai
is prese

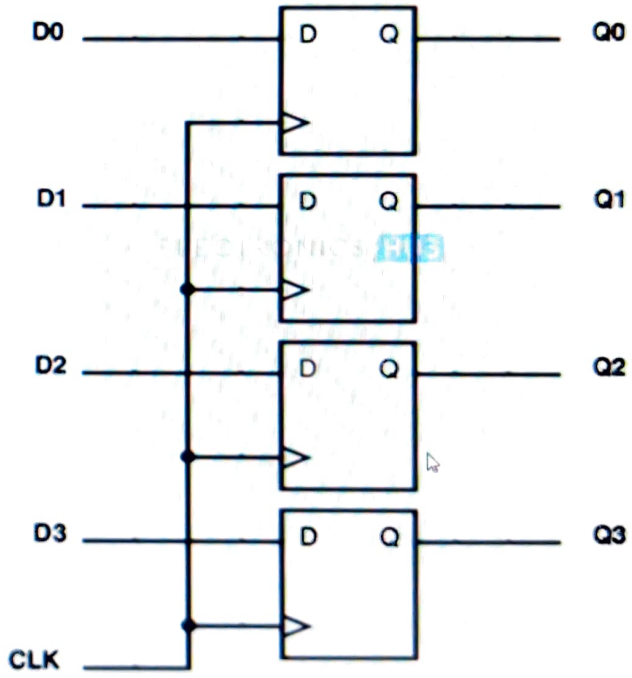
Applications of D-Flip flop

- Data storage
- Data transferring as shift register
- Frequency division circuits

Dr. E. Paul Braineard

2021)
Raise hand
Turn on captions
Paul Bra
is prese

D FF: Data storage

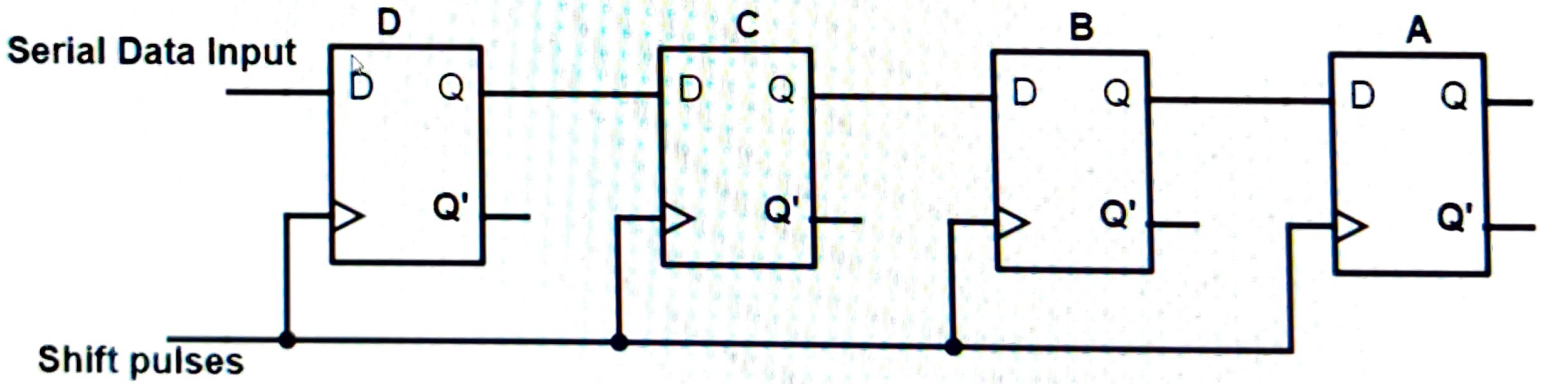


Dr. E. Paul Braineard

Raise hand
Turn on captions

D FF: Data transferring as shift register

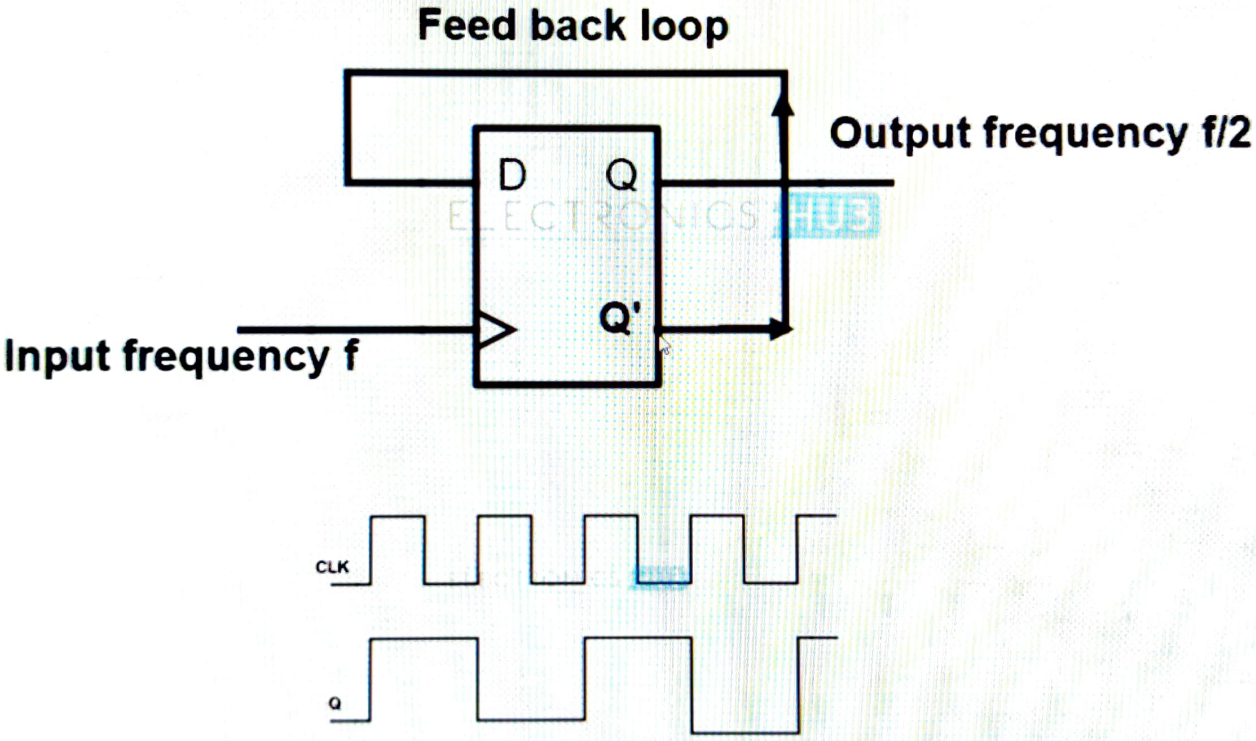
- D flip – flops are connected to form a shift register.
- A cascade connection of D flip – flops with same clock signal will form a shift register.
- A shift register can shift the data without changing the sequence of bits.
- When a clock pulse is applied, the one bit data is shifted or transferred. Shift registers can store the data temporarily.



Dr. E. Paul Braineard

Raise hand
Turn on captions
Paul Br
is pres

D FF: Frequency division circuits



Dr. E. Paul Braineard

b2021)
Raise hand
Turn on captions
Paul Bra
is prese