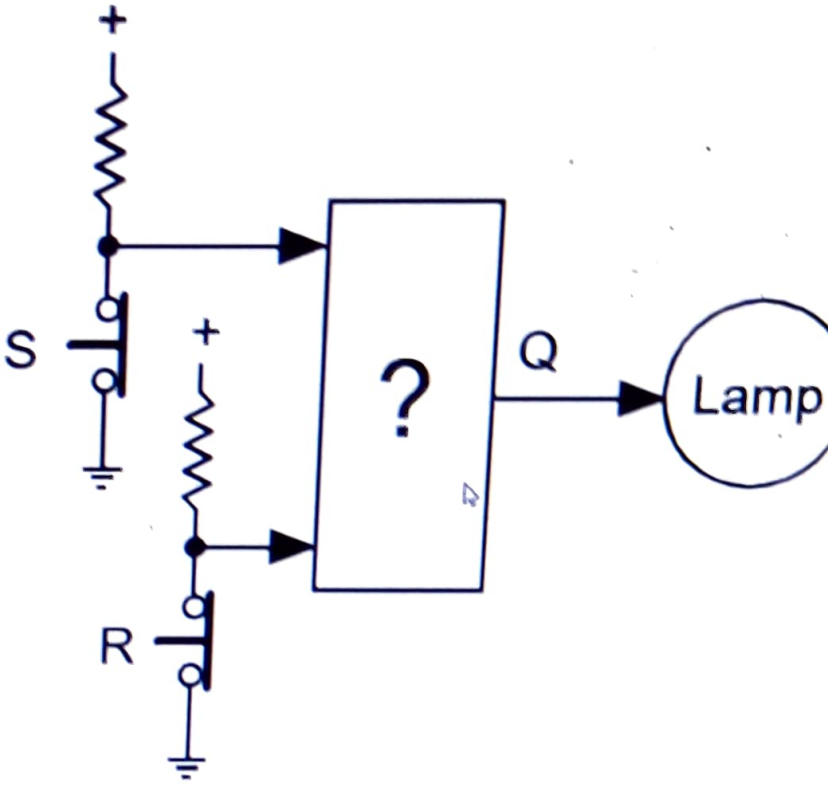
SR latch example: Calling an air hostess

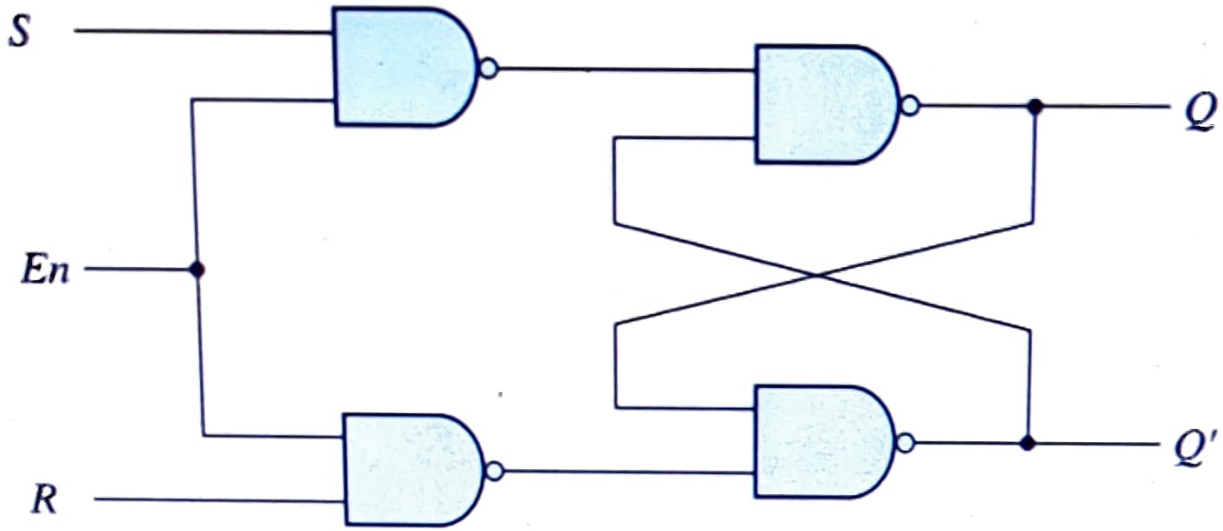
- Design a network to control a lamp from two pushbutton switches labeled S and R.
  - If we push switch S the light should turn on.
    - If we then release S, the light should stay on.
  - If we push switch R, the lamp should turn off
    - If we release R the lamp should stay off.

  Assume that both S and R are not pushed at the same time.



Dr. E. Paul Braineard

SR Latch with control input



(a) Logic diagram

En	*S*	*R*	Next state of *Q*
0	X	X	No change
1	0	0	No change
1	0	1	$Q = 0$; reset state
1	1	0	$Q = 1$; set state
1	1	1	Indeterminate

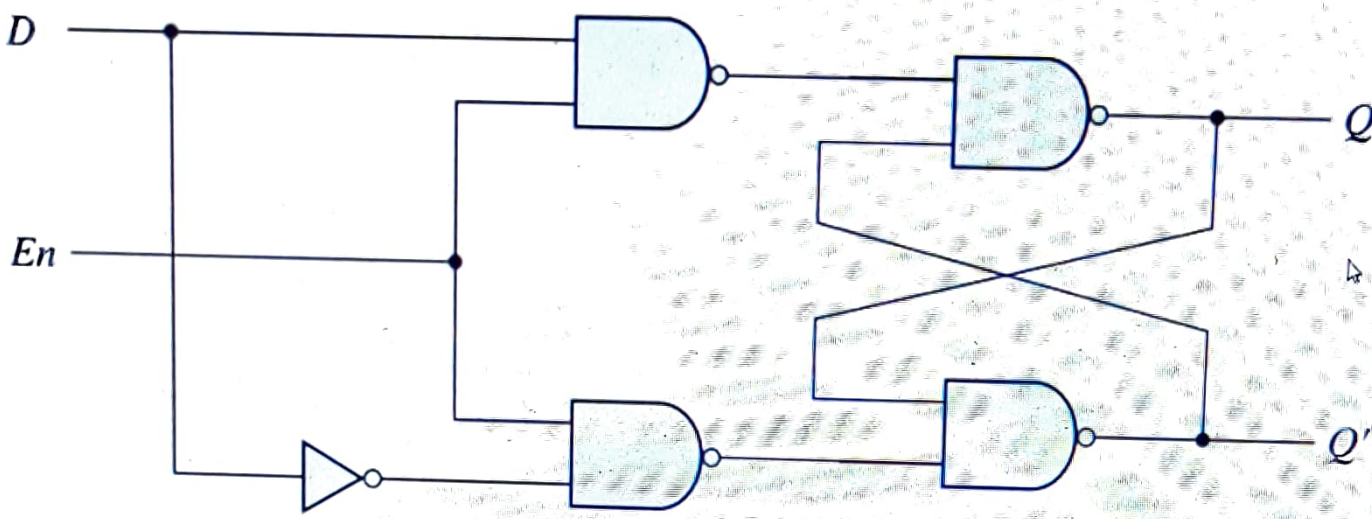
(b) Function table

- In either case, when En returns to 0, the circuit remains in its current state.
- An indeterminate condition occurs when all three inputs are equal to 1

Dr. E. Paul Braineard

D Latch

- One way to eliminate the undesirable condition of the indeterminate state in the SR latch is to ensure that inputs S and R are never equal to 1 at the same time. This is done in the D latch



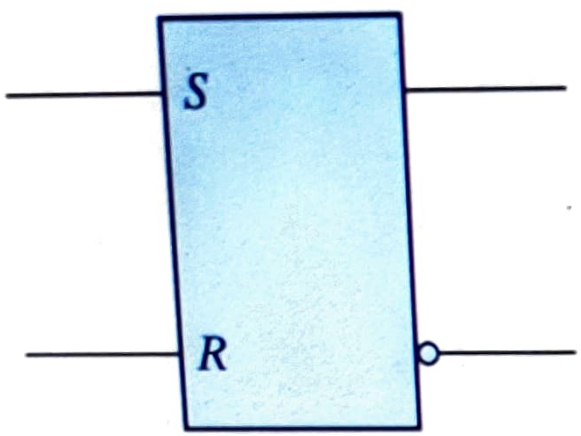
(a) Logic diagram

En	D	Next state of Q
0	X	No change
1	0	Q = 0; reset state
1	1	Q = 1; set state

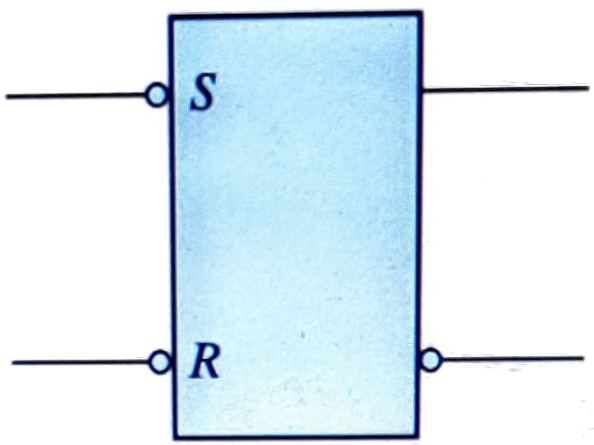
(b) Function table

Dr. E. Paul Braineard

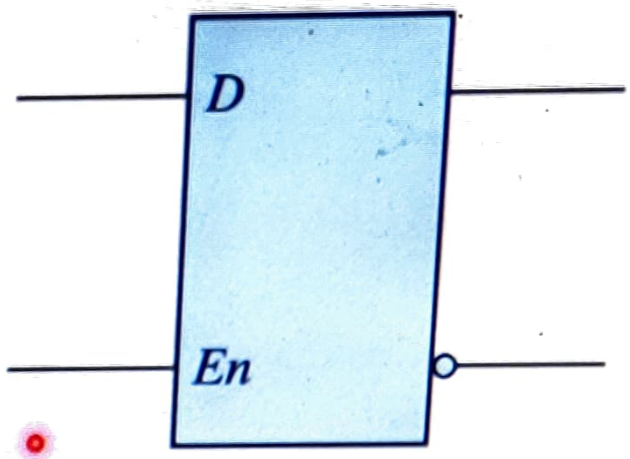
Graphic symbols for SR, S′R′ and D latch



SR



$\overline{S}\overline{R}$



D

Dr. E. Paul Braineard

Storage elements: Flip-flops

- The state of a flip-flop is changed by switching the control input.
- This momentary change is called a trigger
  - The transition it causes is said to "trigger the flip-flop".
- Flip-flops are synchronous bistable devices
  - Also known as *bistable multivibrators*
  - Synchronous: the output changes state only at a specified point (leading or trailing edge) on the triggering input called the **clock** (CLK)
  - which is designated as a control input, *C*
  - Output changes in synchronization with the clock
  - FFs are edge-triggered
  - Latches are level triggered
- A **flip-flop**, that stores one bit
- Combine that block to build multi-bit storage – a **register**

TEJADITYA NACHIKETA P has left the meeting

Dr. E. Paul Braineard

Clock responses

(a) Response to positive level

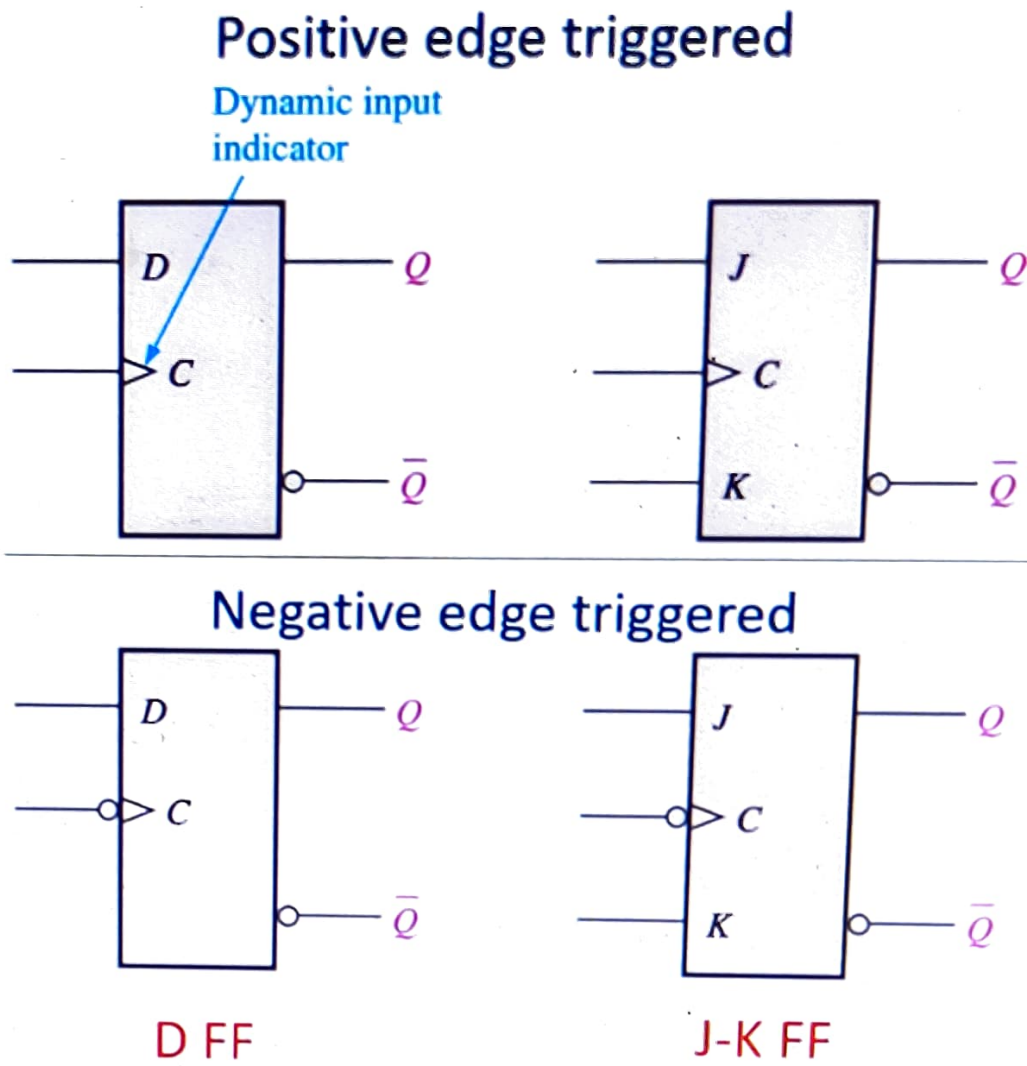
(b) Positive-edge response

(c) Negative-edge response

Clock response in latch and flip-flop

Edge-triggered flip-flop

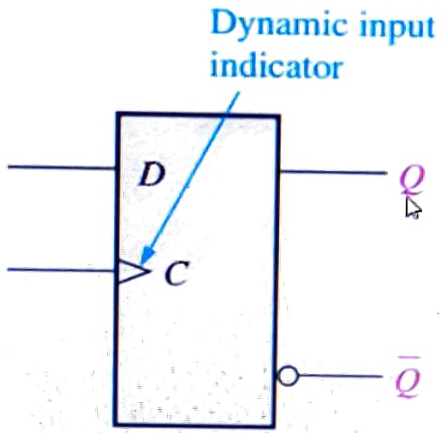
- Changes state either at the positive edge (rising edge) or at the negative edge (falling edge) of the clock pulse
- Sensitive to the inputs only at this transition of the clock
- Two types of edge-triggered flip-flops are covered in this section
  - D FF
  - J-K FF



Dr. E. Paul Braineard

D Flip-Flop

- The *D* input of the **D flip-flop** is a **synchronous**
- **D**ata on the input are transferred to the flip-flop's output only on the triggering edge of the clock pulse.
- When *D* is HIGH, the *Q* output goes HIGH on the triggering edge of the clock pulse, and the flip-flop is SET.
- When *D* is LOW, the *Q* output goes LOW on the triggering edge of the clock pulse, and the flip-flop is RESET



Dr. E. Paul Braineard

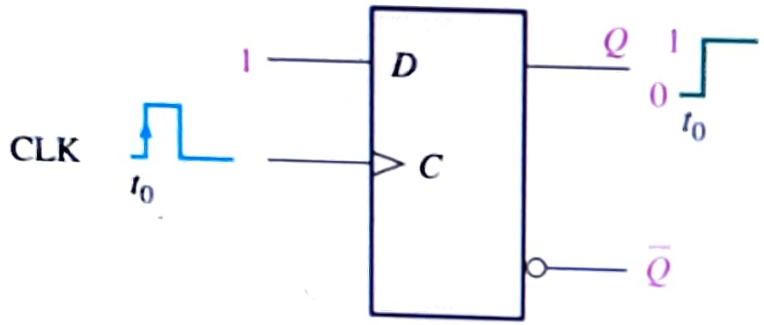
Operation of a positive edge-triggered D flip-flop

- The flip-flop cannot change state except on the triggering edge of a clock pulse

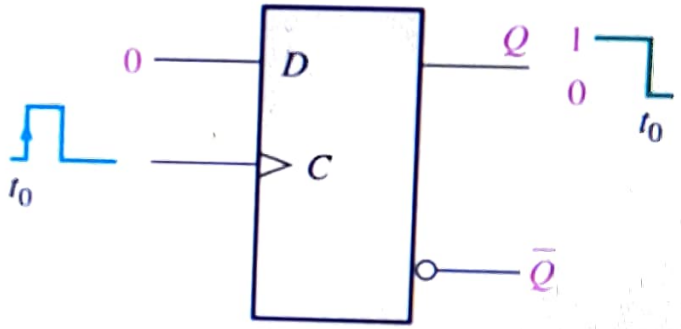
Truth table for a positive edge-triggered D flip-flop.

Inputs		Outputs		
D	CLK	Q	$\bar{Q}$	Comments
0	↑	0	1	RESET
1	↑	1	0	SET

↑ = clock transition LOW to HIGH



(a) $D = 1$ flip-flop SETS on positive clock edge. (If already SET, it remains SET.)



(b) $D = 0$ flip-flop RESETS on positive clock edge. (If already RESET, it remains RESET.)

Dr. E. Paul Braineard

Problem

- Determine the Q and $\bar{Q}$ output waveforms of the flip-flop in Figure 1 for the D and CLK inputs in Figure 2. Assume that the positive edge-triggered flip-flop is initially RESET.

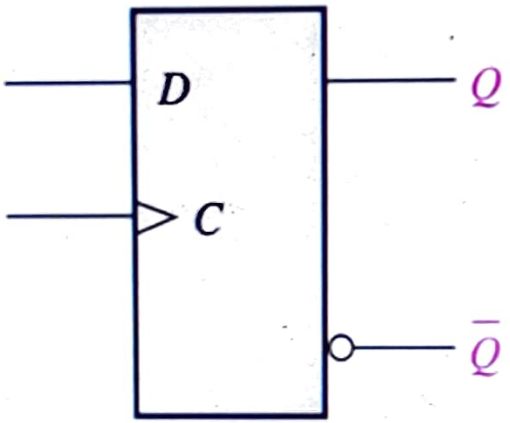


Figure 1

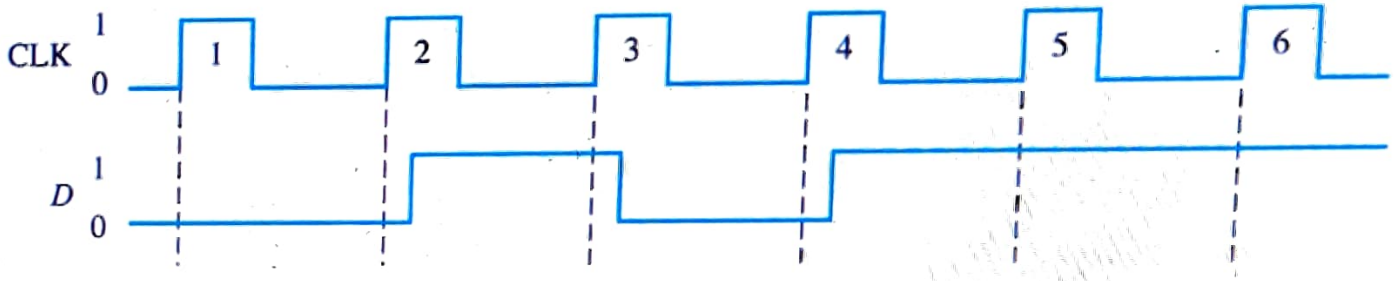
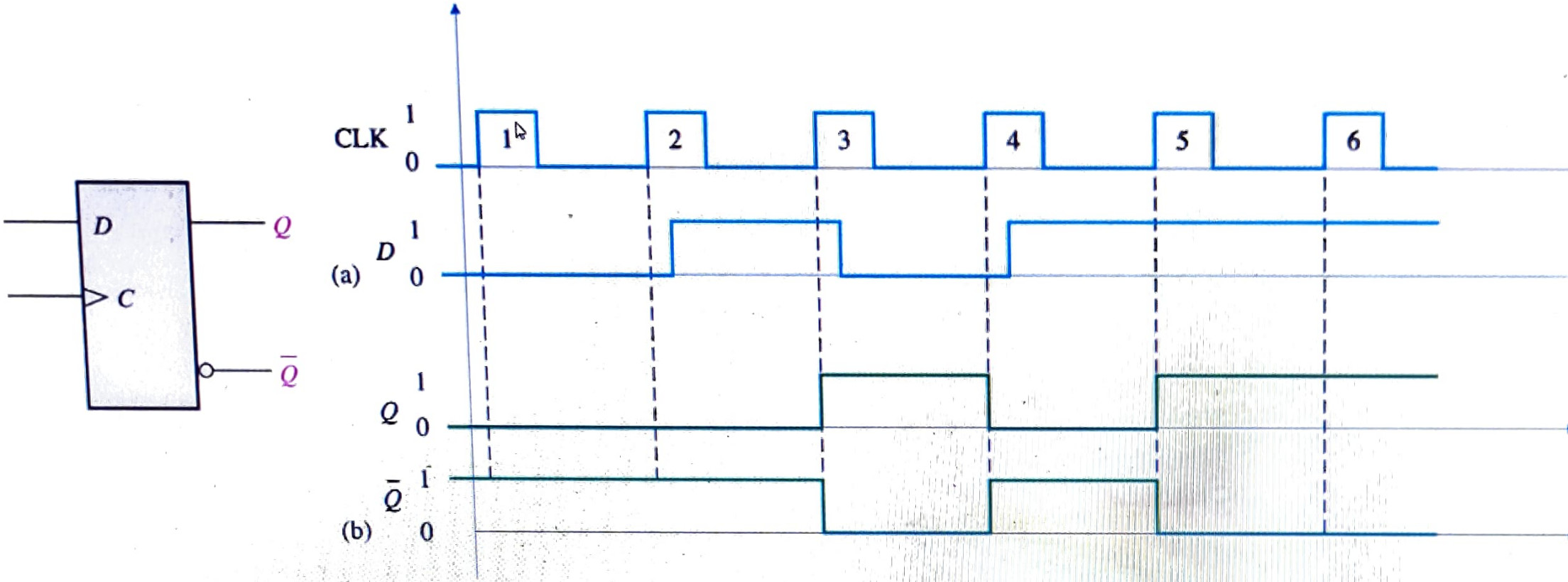


Figure 2

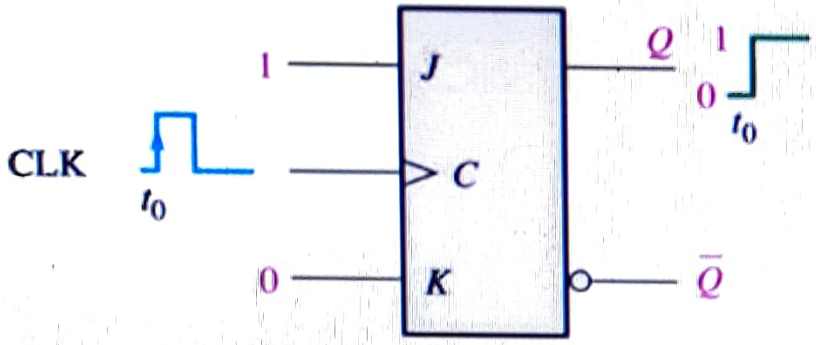
D Flip-flop



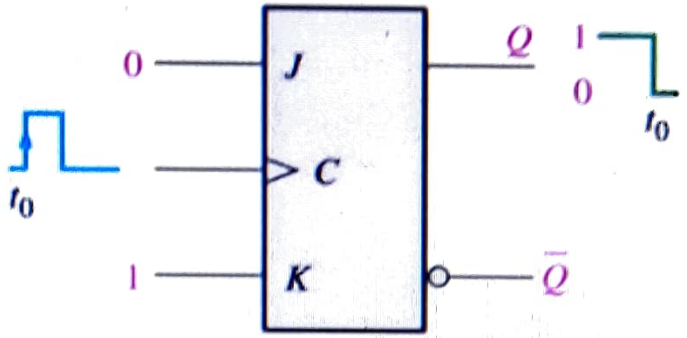
The J-K Flip-Flop

- The *J* and *K* inputs of the **J-K flip-flop** are synchronous
  - Input data are transferred to the flip-flop's output only on the triggering edge of the clock pulse
- When *J* is HIGH and *K* is LOW, the *Q* output goes HIGH on the triggering edge of the clock pulse, and the flip-flop is **SET**.
- When *J* is LOW and *K* is HIGH, the *Q* output goes LOW on the triggering edge of the clock pulse, and the flip-flop is **RESET**.
- When both *J* and *K* are LOW, the output does not change from its prior state.
- When *J* and *K* are both HIGH, the flip-flop changes state. This called the **toggle** mode.

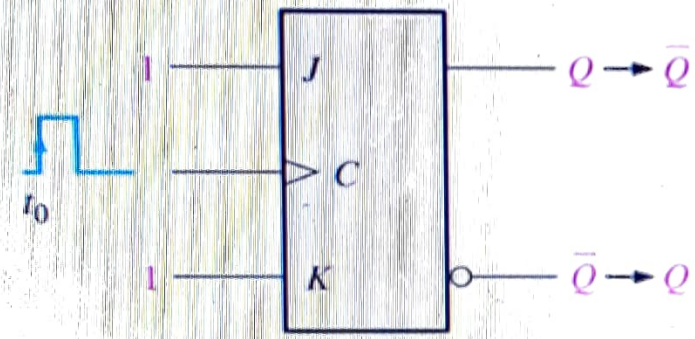
Operation of a positive edge-triggered J-K flip-flop



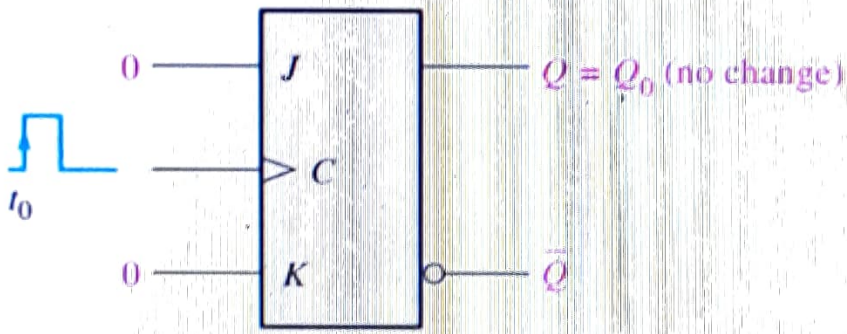
(a) $J = 1$, $K = 0$ flip-flop SETS on positive clock edge. (If already SET, it remains SET.)



(b) $J = 0$, $K = 1$ flip-flop RESETS on positive clock edge. (If already RESET, it remains RESET.)



(c) $J = 1$, $K = 1$ flip-flop changes state (toggle).



(d) $J = 0$, $K = 0$ flip-flop does not change. (If SET, it remains SET; if RESET, it remains RESET.)