

DLD LAB END EXAM

YASH GUPTA

S202000010237

Paper Code: 2

AIM: To implement 4 bit Synchronous counter with the following sequence 12-3-10-5-15 and repeats counting.

Procedure:

- ~~Truth~~ making Truth Table of 4-bit Synchronous counter for the sequence 12-3-10-5-15
- K-map for T_0, T_1, T_2, T_3 using the truth table and finding the expression for T_0, T_1, T_2, T_3
- Building circuit in logism software using expression T_0, T_1, T_2, T_3

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TRUTH TABLE

Present state				Next state				T _n flip-flop			
Q ₃	Q ₂	Q ₁	Q ₀	Q ₃ ⁺	Q ₂ ⁺	Q ₁ ⁺	Q ₀ ⁺	T ₃	T ₂	T ₁	T ₀
0	0	0	0	1	1	0	0	1	1	0	0
0	0	0	1	x	x	x	x	x	x	x	x
0	0	1	0	x	x	x	x	x	x	x	x
0	0	1	1	1	0	1	0	1	0	0	1
0	0	0	0	x	x	x	x	x	x	x	x
0	1	0	1	1	1	1	1	1	0	1	0
0	1	1	0	x	x	x	x	x	x	x	x
0	1	1	1	x	x	x	x	x	x	x	x
1	0	0	0	x	x	x	x	x	x	x	x
1	0	0	1	x	x	x	x	x	x	x	x
1	0	1	0	0	1	0	1	1	1	1	1
1	0	1	1	x	x	x	x	x	x	x	x
1	1	0	0	0	0	1	1	1	1	1	1
1	1	0	1	x	x	x	x	x	x	x	x
1	1	1	0	x	x	x	x	x	x	x	x
1	1	1	1	1	1	0	0	0	0	1	1

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K-map

1) $T_3 \rightarrow$

Q_3, Q_2	00	01	11	10
00	1	X	1	X
01	X	1	X	X
11	1	X	0	X
10	X	X	X	1

Q_3 (vertical), Q_2 (horizontal)

$$T_3 = \overline{Q_3} + \overline{Q_2}$$

2) $T_2 \rightarrow$

Q_3, Q_2	00	01	11	10
00	1	X	0	X
01	X	0	X	X
11	1	X	0	X
10	X	X	X	1

Q_3 (vertical), Q_2 (horizontal)

$$T_2 = \overline{Q_2}$$

3) $T_1 \rightarrow$

Q_3, Q_2	00	01	11	10
00	0	X	0	X
01	X	1	X	X
11	1	X	1	X
10	X	X	X	1

Q_3 (vertical), Q_2 (horizontal)

$$T_1 = Q_2 + Q_3$$

4) $T_0 \rightarrow$

Q_3, Q_2	00	01	11	10
00	0	X	1	X
01	X	0	X	X
11	1	X	1	X
10	X	X	X	1

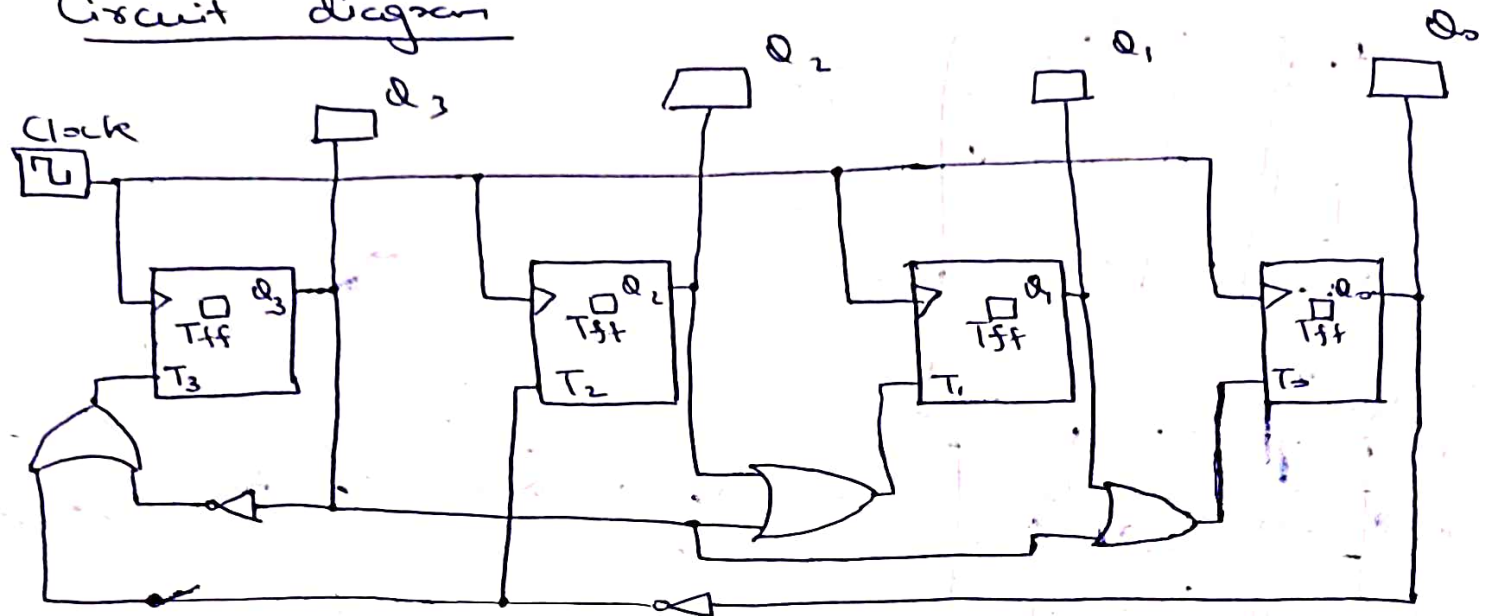
Q_3 (vertical), Q_2 (horizontal)

$$T_0 = Q_3 + Q_2$$

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YASH GUPTA
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Circuit diagram



Conclusion

The 4 bit Synchronous counter has been built and implemented using T- flip flop.