Registers and counters

- A clocked sequential circuit consists of a group of flip-flops and combinational gates
- Circuits with flip-flops and additional functionality are
  - Registers
  - Counters

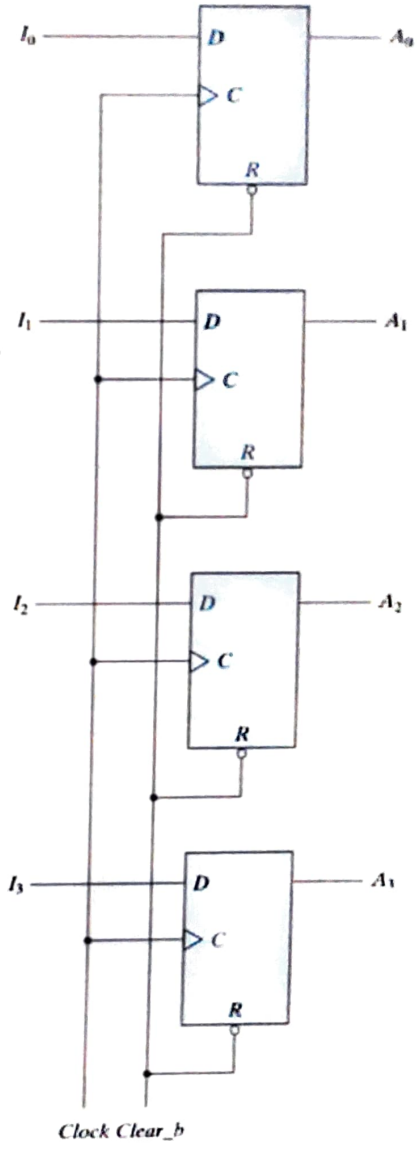
Register

- A register is a group of flip-flops
- All the FFs are connected to a common clock
  - Capable of storing one bit of information
- An n-bit register consists of a group of n flip-flops capable of storing n bits of binary information.
- FFs + Combinational logic gates (perform certain data-processing tasks)
- The flip-flops hold the binary information, and the gates determine how the information is transferred into the register

Counter

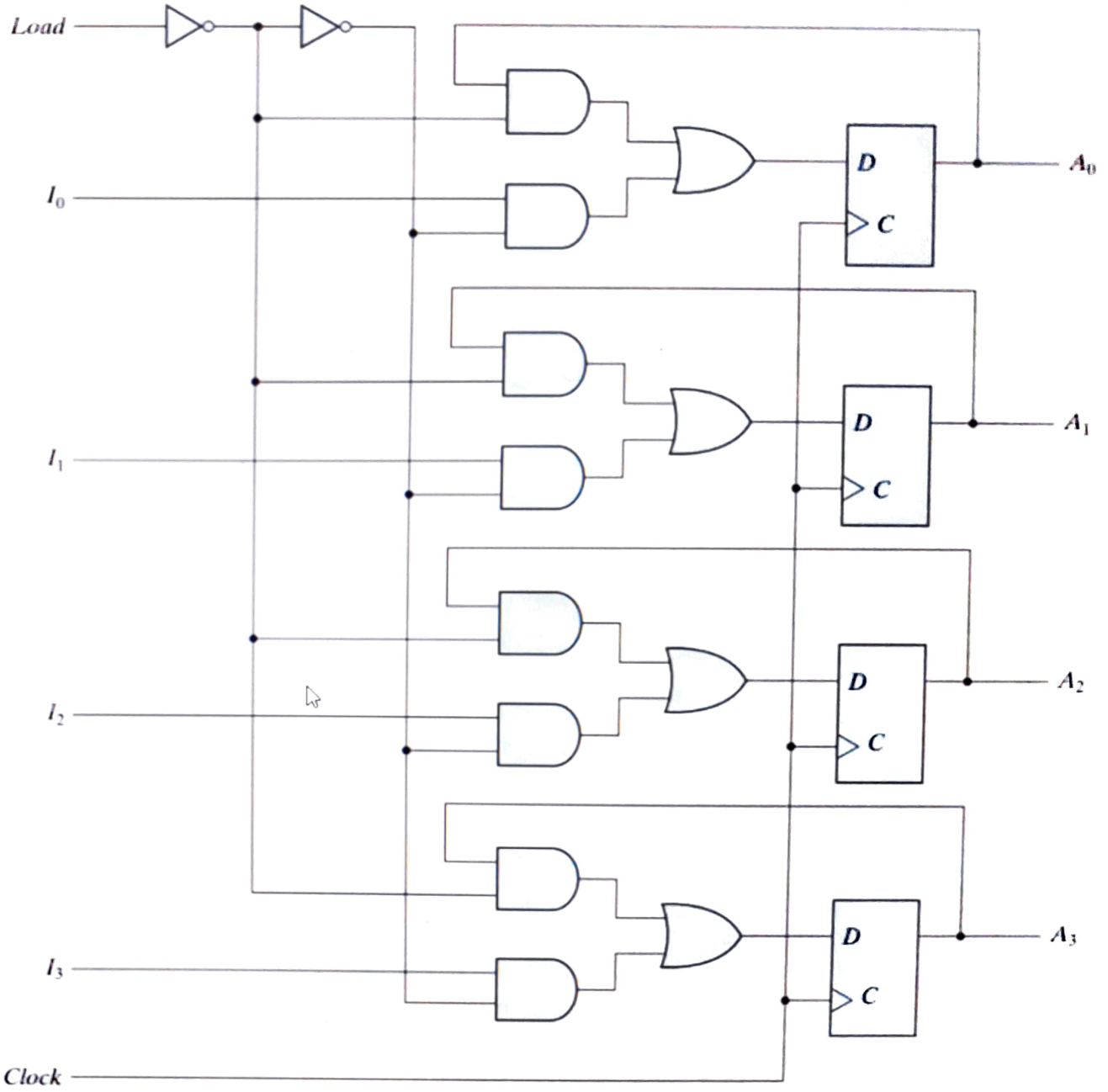
- A counter is essentially a register that goes through a predetermined sequence of binary states.
- The gates in the counter are connected in such a way as to produce the prescribed sequence of states.
- Although counters are a special type of register, it is common to differentiate them by giving them a different name.

A four-bit data storage register

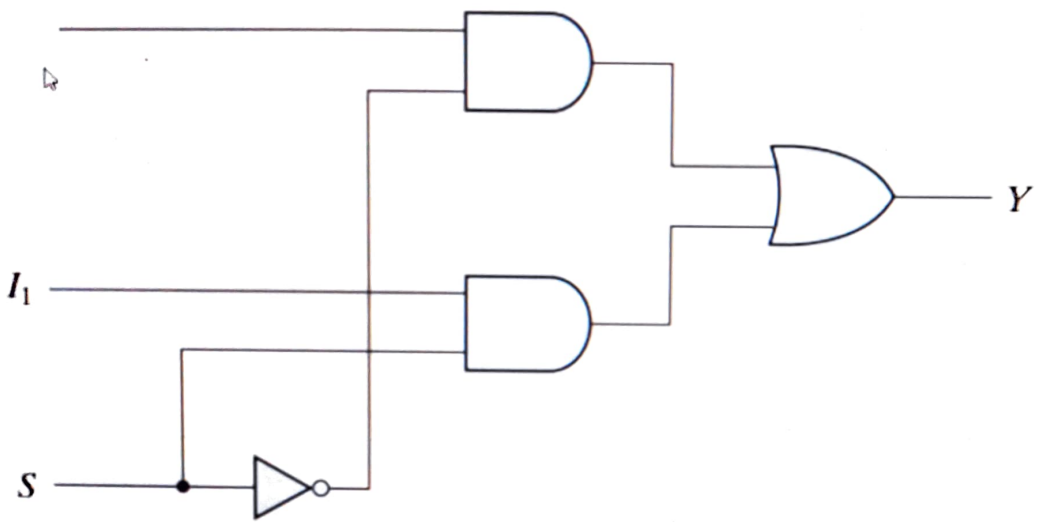


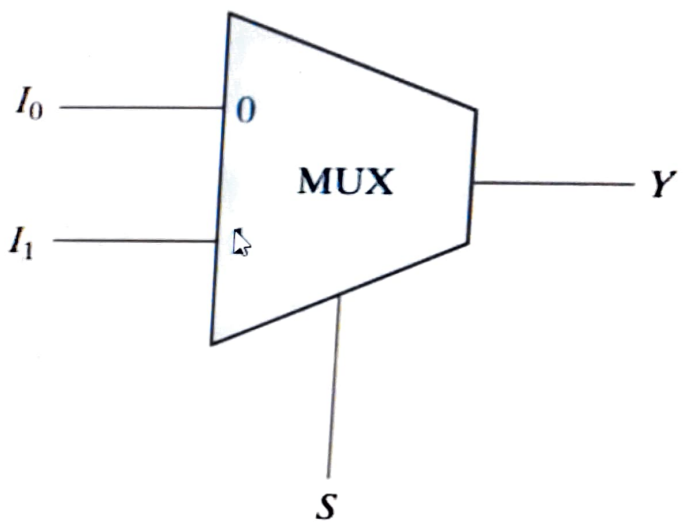
Four-bit register with parallel load

- Load control input
- The load input to the register determines the action to be taken with each clock pulse
- When the load input is 1, the data at the four external inputs are transferred into the register with the next positive edge of the clock.
- When the load input is 0, the outputs of the flip-flops are connected to their respective inputs.



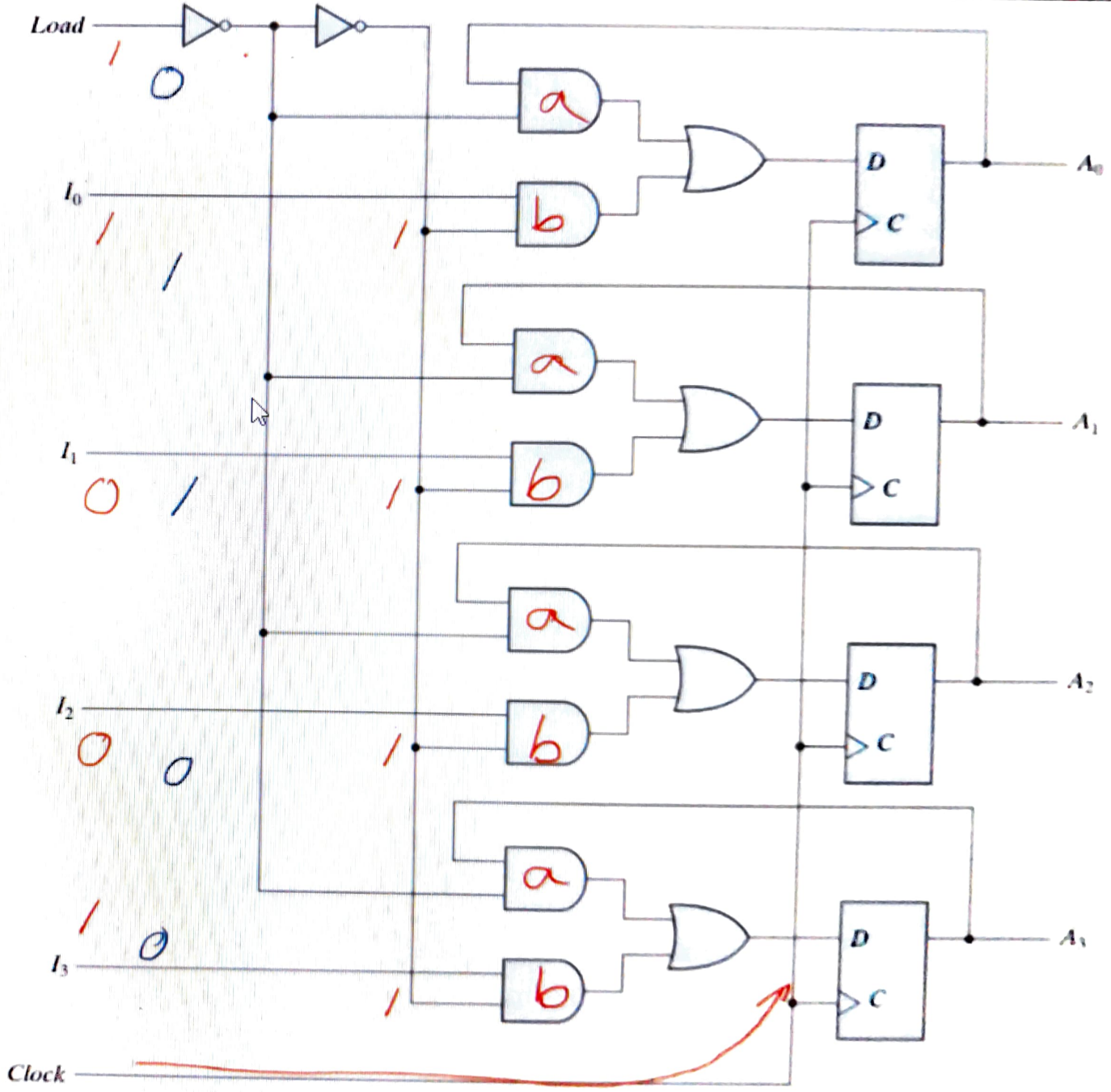
Two to one line MUX





Four-bit register with parallel load

- Load control input
- The load input to the register determines the action to be taken with each clock pulse
- When the load input is 1, the data at the four external inputs are transferred into the register with the next positive edge of the clock.
- When the load input is 0, the outputs of the flip-flops are connected to their respective inputs.



Universal Shift Register

- A clear control to clear the register to 0.
- A clock input to synchronize the operations.
- A shift-right control to enable the shift-right operation and the serial input and output lines associated with the shift right.
- A shift-left control to enable the shift-left operation and the serial input and output lines associated with the shift left.
- A parallel-load control to enable a parallel transfer and the n input lines associated with the parallel transfer.
- n parallel output lines.
- A control state that leaves the information in the register unchanged in response to the clock. Other shift registers may have only some of the preceding functions with at least one shift operation.