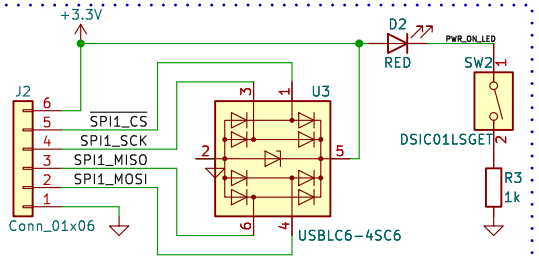
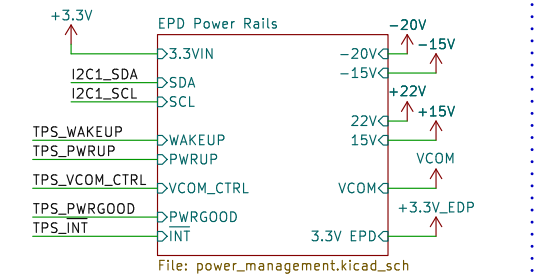
Main Power & SPI

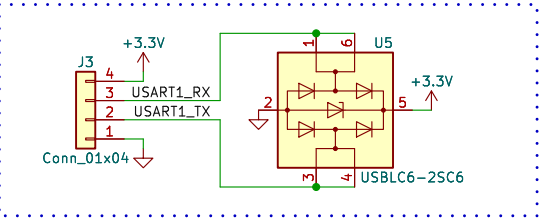


This is the interface of the driver board.
The user is expected to supply 3.3V and GND via this header.
The commands can then be send via SPI to the MCU.

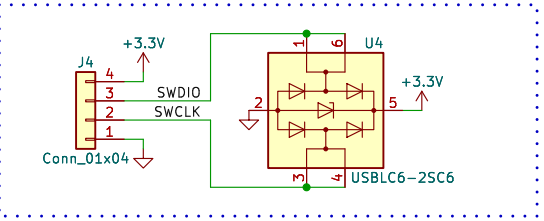
Power Rails



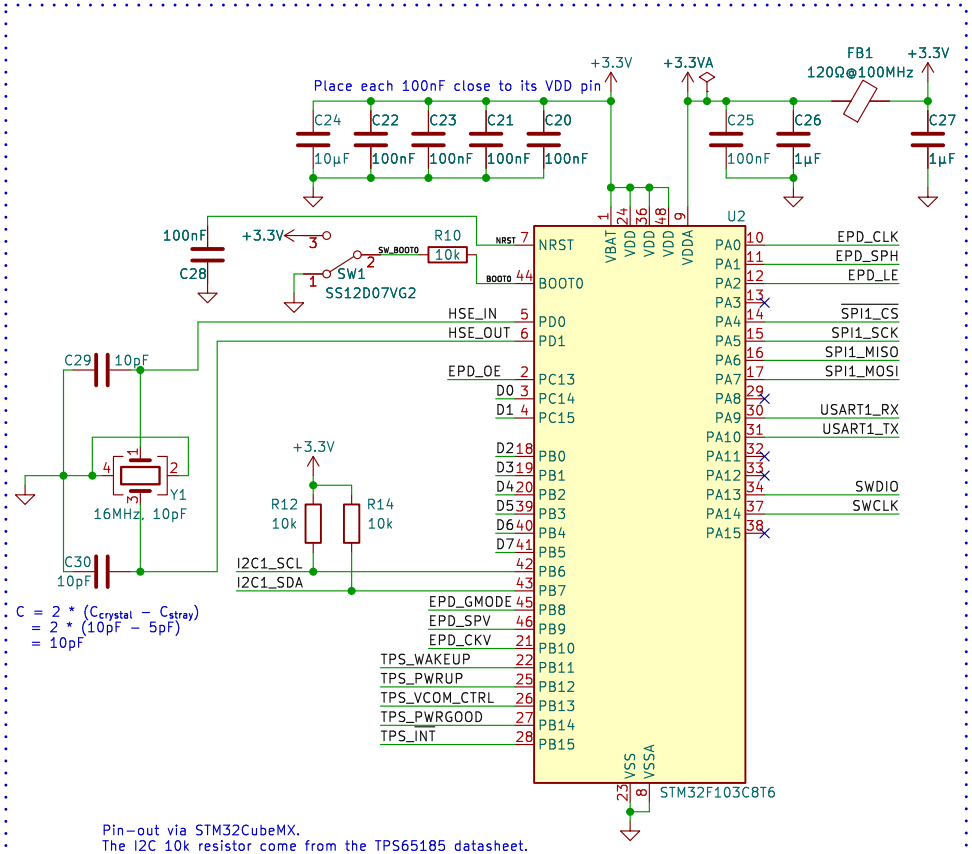
UART – Programming



Serial Wire Debug



STM32 Microcontroller



C = 2 * ($C_{crystal}$ − C_{stray})
= 2 * (10pF − 5pF)
= 10pF

Pin-out via STM32CubeMX.
The I2C 10k resistor come from the TPS65185 datasheet.
100nF capacitor used on NRST to prevent from spurious resets.

BOOT0 is not strictly needed, as the STM32 will be programmed via SWD but it doesn't hurt.

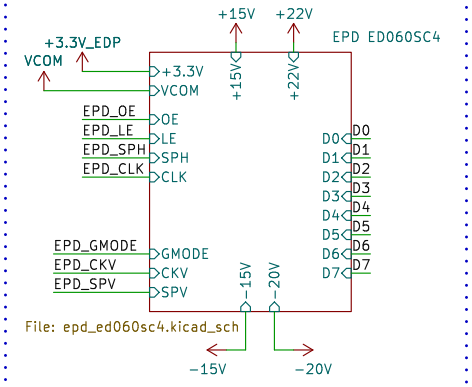
Number of pins required from the µC: 32

TPS 65185: 7 (4 min)
- SDA & SCL (I^2C)
- WAKEUP & PWRUP
- PWRGOOD (Can be iomitted)
- VCOM_CTRL (Can be omitted and connected to 3.3V)
- INT (Can be omitted and left floating)

ED060SC4: 15
- GMODE
- SPV
- CKV
- CL
- LE
- OE
- SPH
- D0 to D7 (Data Bus)

STM32F103C8 Reserved: 10
- SWD (SWCLK, SWDIO)
- USART (RX, TX)
- SPI (SCK, MOSI, MISO, CS)
- Oscillator (OSC_IN, OSC_OUT)

EPD Screen



TODO:
- Test points

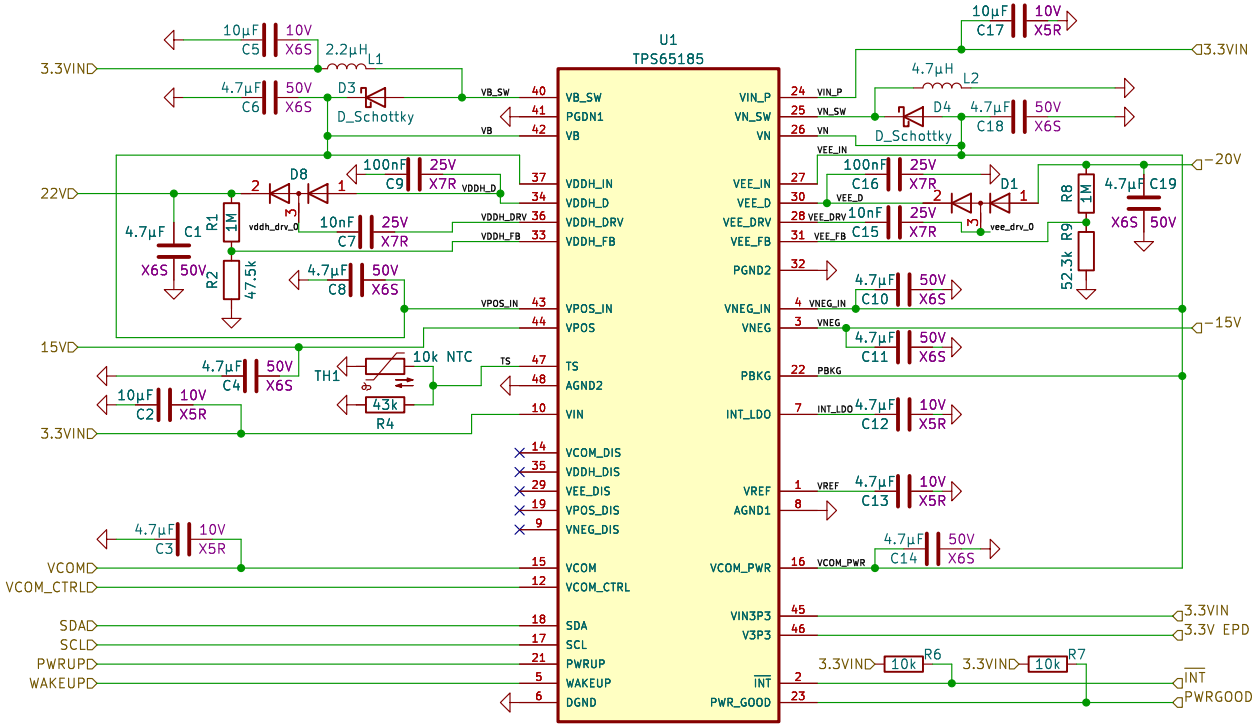
https://github.com/Mael-Le-Garrec/ED060SC4_driver_board

hatrix

Sheet: /
File: ED060SC4_SPI_driver_board.kicad_sch

Title: ED060SC4 SPI Driver Board

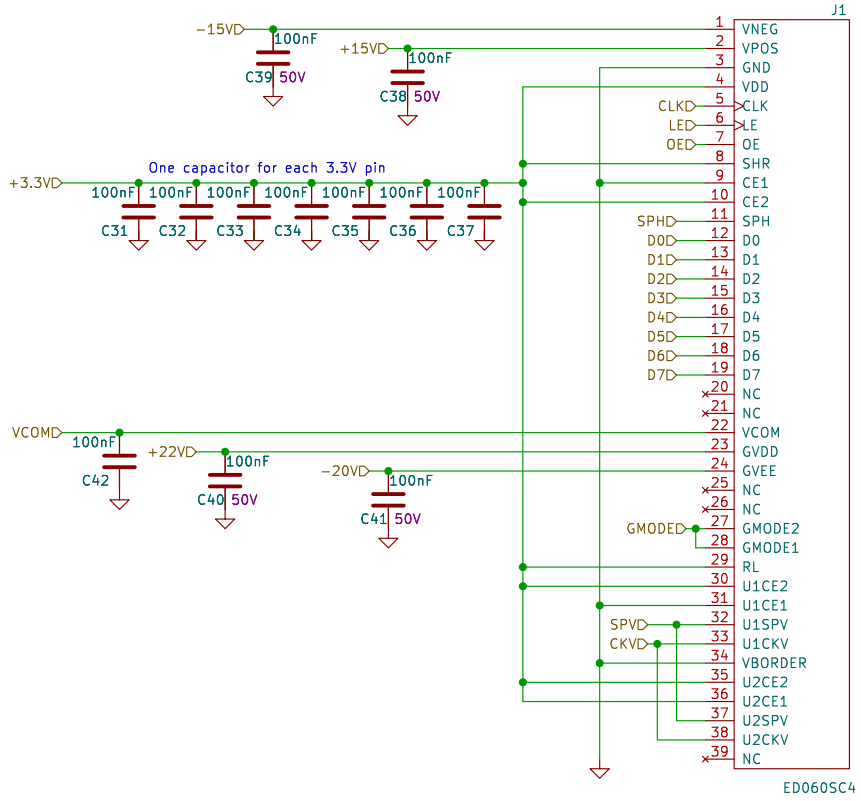
Size: A4	Date: 2023-04-12	**Rev: 0.1**
KiCad E.D.A. kicad 7.0.1		Id: 1/3



This schematic is based on one found in TI's "TPS65185 Evaluation Module" user's guide.
It is suited for the required rails −20V, −15V, 15V, 22V and 3.3V.

This schematic assumes a VIN power of 3.3V, that is also used for the pull−up resistors of $\overline{\text{INT}}$ and PWR_GOOD.

Sheet: /EPD Power Rails/		
File: power_management.kicad_sch		
Title:		
Size: A4	Date:	**Rev: 0.1**
KiCad E.D.A. kicad 7.0.1		Id: 2/3



100nF capacitors should be OK everywhere.
I got no data whatsoever to support that claim though.

Sheet: /EPD ED060SC4/		
File: epd_ed060sc4.kicad_sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 7.0.1		Id: 3/3