Honours project Proposal

Problem

A core function of the internet is the ability to switch network packets from one place to another using devices called routers and switches. These have to receive a packet, find a destination and then output to the next hop rapidly. There presently is no existing device that can evaluate the latency of simple switches to measure the lag is present in these devices. As no device exists, I want to create a one which can measure the latency for future research purposes, and evaluating future latency solutions.

Solution

To measure this packet timing, there are a few possible solutions. One is PF_RING, which is a low level linux implementation of fast packet capture, but the timing functions would have to be done by the operating system (which is slow). Another solution is also a rapid packet capture method, called DPDK, but this has the same issues as PF_RING. The proposed solution is to develop a packet timing solution on a PicoZed Xilinx Zynq FPGA development board. This board for the development of FPGA project's and incorporates gigabit ethernet phy transceivers, allowing the device to measure packets on a gigabit ethernet line at a hardware clocking level. An internal clock management system also exists called a Mixed-Mode Clock Manager which can synthesize a higher clock rate. This is vital to the timing of packets, as a higher clock rate can provide the ability to measure the packet times with greater fidelity. Another advantage of this solution is there is a ARM based linux programmable system (PS) which can interact with the FPGA (Referred to as Programmable Logic (PL)). This allows the data from each measurement to be easily transferred to another computer.

Evaluation

To measure the capabilities of the packet timing device, a commercially available switch can be used to do tests on. The method to produce the device will be engineered to ensure timing accuracy to within 1 microsecond. This will be verified through a loopback setup to get an approximation of what resolution can be measured. Data from the device would be transferred to another computer for logging to evaluate, which should produce a normal distribution to show an average packet latency.

Ethics

No human or animal testing will take place for this project.

Budget

The desired platform for this project would be a PicoZed (http://zedboard.org/product/picozed) mounted to a FMC carrier card V1 (http://zedboard.org/product/picozed-carrier-card) which will have an Ethernet FMC card attached to it (https://opsero.com/product/robust-ethernet-fmc/?attribute_supply-voltage-vadj=2.5V). This will ensure there are enough ethernet ports for both the FPGA based tester, and FPGA based network switch.

Item	**Cost (USD)**
PicoZed	265 (Already Available for Use)
FMC Carrier Card V1	425 (Already Available for Use)
Ethernet FMC Card	590 (Has been purchased by Bryan)
TOTAL	**1280 (No Further funds required)**

Risks

The equipment that I am developing on could be faulty/damaged. There are spares replacements for the PicoZed and also the FMC Carrier Card. The lead time to purchase another Ethernet FMC card would be around 2 weeks.

There is an uncertainty on the clocking rates that the FPGA fabric can clock at. This could mean that the design could work in simulation, but the physical hardware might not be able to work. Expert opinion on the subject has suggested the platform we have chosen can perform at much higher clocking rates than which we are dealing with. Also we are using the latest line of devices from Xilinx, which also ensure we have significant margins to achieve the goal.

The FPGA fabric could not be enough for the design that I produce, making the FPGA too small to fit the project. This can be mitigated by upgrading the FPGA to one which has a larger fabric space.

Requirements to be successful

I would need the FPGA hardware to have a base platform to create the device. This will be provided by Robin Dykstra. Some parts of the project require to be purchased, and this purchasing will be done by Bryan Ng. Programming the FPGA will require Vivado Software Suite, which is made by Xilinx, and installed on the ECS machines.

Timeline

	Task Mode	Task Name	Duration
1		Review Existing Literature	2 wks
2	✓	Get Custom FPGA fabric onto board and blink a LED	1 wk
3		Send and receive a data value from FPGA fabric to Linux System	1.13 mons
4		Create a program to send packet through the ethernet port	1.1 mons
5		Make LED light up when packet is sent through ethernet port, and another LED light up when the exact same packet is detected on another port.	1.1 mons
6		Construct clock structure for timing the packets. Integrate this with work previously done to start/stop a timer	1.13 mons
7		Read timer value in linux subsystem. Write these test values to a file, and then read file on another computer to visualize test data.	1.05 mons
8		Test commodity switches to get some data on how well some switches perform, compared with others	1.13 mons
9		Close up project.	1 mon