1. Description

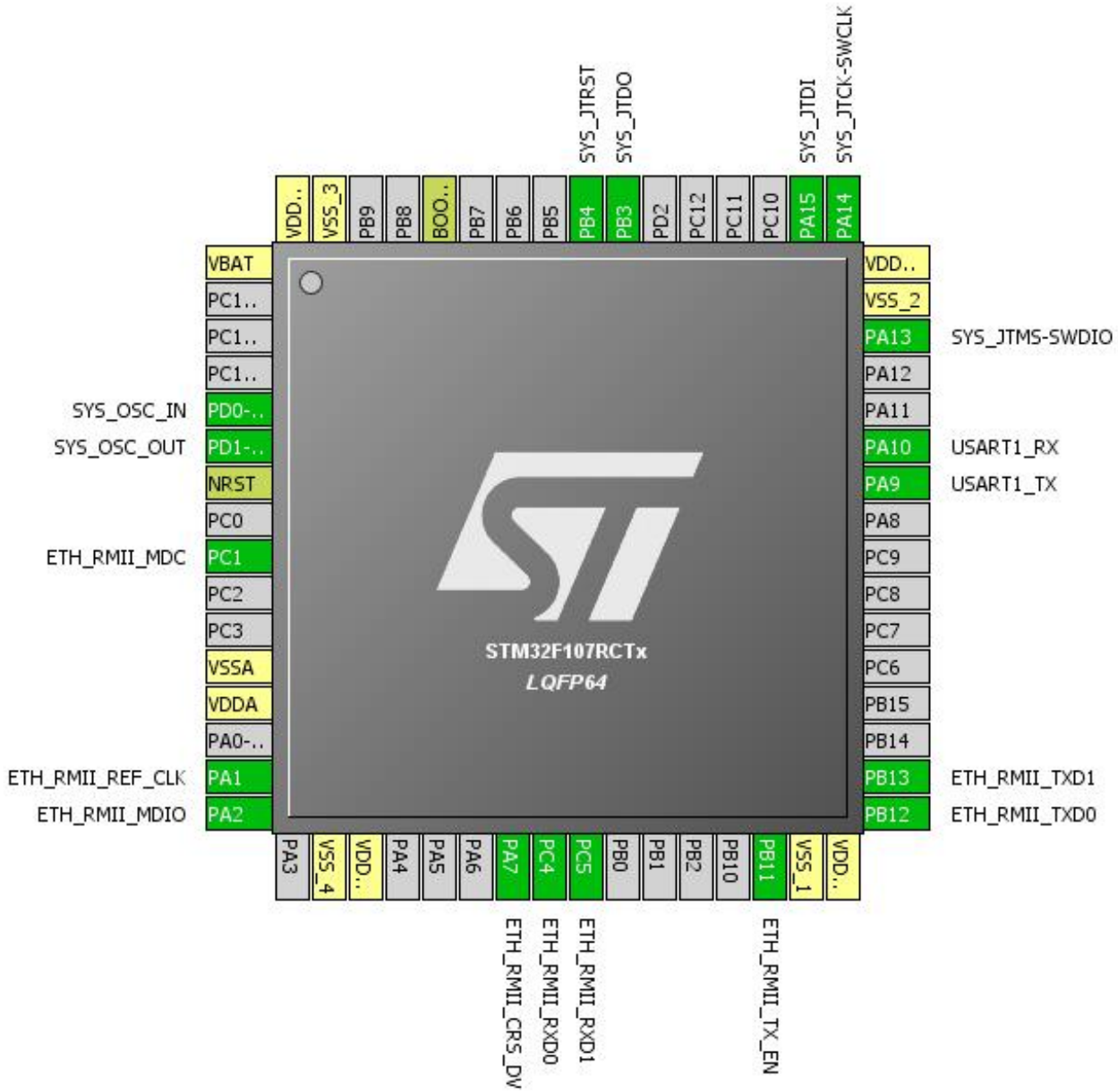
1.1. Project

Project Name	stm32f107_eth_pins
Generated with:	STM32CubeMX 4.2.0
Date	11/04/2015

1.2. MCU

MCU Serie	STM32F1
MCU Line	STM32F105/107
MCU name	STM32F107RCTx
MCU Package	LQFP64
MCU Pin number	64

2. Pinout Configuration



3. IPs and Middlewares Configuration

IP	Mode	Fonction	Pin
ETH_RMII	Mode: RMII	ETH_RMII_CRS_DV	PA7
		ETH_RMII_MDC	PC1
		ETH_RMII_MDIO	PA2
		ETH_RMII_REF_CLK	PA1
		ETH_RMII_RXD0	PC4
		ETH_RMII_RXD1	PC5
		ETH_RMII_TXD0	PB12
		ETH_RMII_TXD1	PB13
		ETH_RMII_TX_EN	PB11
SYS	Debug: JTAG(5-pins)	SYS_JTCK-SWCLK	PA14
		SYS_JTDI	PA15
		SYS_JTDO	PB3
		SYS_JTMS-SWDIO	PA13
		SYS_JTRST	PB4
	OSC: HSE-External-Clock-Source	SYS_OSC_IN	PD0-OSC_IN
		SYS_OSC_OUT	PD1-OSC_OUT
USART1	Mode: Asynchronous	USART1_RX	PA10
		USART1_TX	PA9

4. Pins Configuration

Pin	Pos	Function(s)	Label
PD0-OSC_IN	5	SYS_OSC_IN	
PD1-OSC_OUT	6	SYS_OSC_OUT	
PC1	9	ETH_RMII_MDC	
PA1	15	ETH_RMII_REF_CLK	
PA2	16	ETH_RMII_MDIO	
PA7	23	ETH_RMII_CRS_DV	
PC4	24	ETH_RMII_RXD0	
PC5	25	ETH_RMII_RXD1	
PB11	30	ETH_RMII_TX_EN	
PB12	33	ETH_RMII_TXD0	
PB13	34	ETH_RMII_TXD1	
PA9	42	USART1_TX	
PA10	43	USART1_RX	
PA13	46	SYS_JTMS-SWDIO	
PA14	49	SYS_JTCK-SWCLK	
PA15	50	SYS_JTDI	
PB3	55	SYS_JTDO	
PB4	56	SYS_JTRST	