CS 222 Computer Organization & Architecture

Lecture 21 [11.03.2019]

Introduction to Instruction Set Architecture

John Jose

Assistant Professor

Department of Computer Science & Engineering

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About Me

I hail from a small village near Kochi, Kerala.

Joined IIT Guwahati as faculty in CSE Dept in 2015

About my educational profile

Ph.D – **IIT Madras**

M.Tech – **VIT University**

VIT UNIVERSITY (Estd. u/s 3 of UGC Act 1956)
VELLORE ▪ CHENNAI
www.vit.ac.in

B.Tech – **Cochin University**

COCHIN UNIVERSITY OF SCIENCE AND TECHNOLOGY

Few Important Information

- **Instructor: John Jose**
  - **Office Room: H-201, Second Floor, CSE dept**
  - **Personal webpage: http://www.iitg.ac.in/johnjose/**
  - **email: johnjose@iitg.ac.in: Phone: 0361-2583256**
  - **MARS Research Lab: 0361-2583255**
- **Head Teaching Assistant**
  - **Sivakumar S (Ph.D Scholars, MARS Research Lab)**
- **Lecture slots**
  - **C slot (Mon 10am, Tue 11am, Fri 9am) @ 2203**
- **Course Page**
  - **http://jatinga.iitg.ernet.in/~johnjose/cs222.html**

Course Objective

- **Learn** and **appreciate** RISC instruction pipeline techniques and its capabilities.
- **Understand** the basic principles of memory hierarchy – cache memory and primary memory and **analyze** performance improvement techniques in memory systems.
- **Understand** basic I/O operations and its role in enhancing capabilities of a computer system.
- **Know** the working concepts in multi-core processors.
- **Explore** future directions in computer architecture research.

Syllabus

- RISC architectures, processor memory interaction, instruction pipeline concepts, pipeline hazards. [3 hours]
- Introduction to cache memory concepts, mapping techniques, block replacement algorithms and optimization techniques. [6 hours]
- Introduction to DRAM organization, memory controllers and scheduling. [3 hours]
- Basic I/O techniques and DMA controllers. [2 hours]
- Introduction to multicore processors, on chip interconnection systems. [3 hours]

Reference Books

- Computer Organization and Design: The Hardware/Software Interface, John L. Hennessy, David A. Patterson, Morgan Kaufman

- Computer Organization Carl V. Hamacher, Vranesic, Z.G., and Zaky, S.G. McGraw-Hill..

- Computer Organization and Architecture, William Stallings, Pearson Eduction India.

Grading

- **Grading Scheme**
  - **50% (from topics upto pre-midsem by Prof. J.K.Deka)**

  Split up of remaining 50%

  - **15% (1 Short Quiz; April second week)**
  - **35% (End semester Examination; 08.05.2019)**
- **Attendance Policy**
  - **75% attendance rule is strictly enforced.**
  - **Refrain from unethical practices.**
  - **Inform in google forms to avoid proxy disputes.**

General Policies

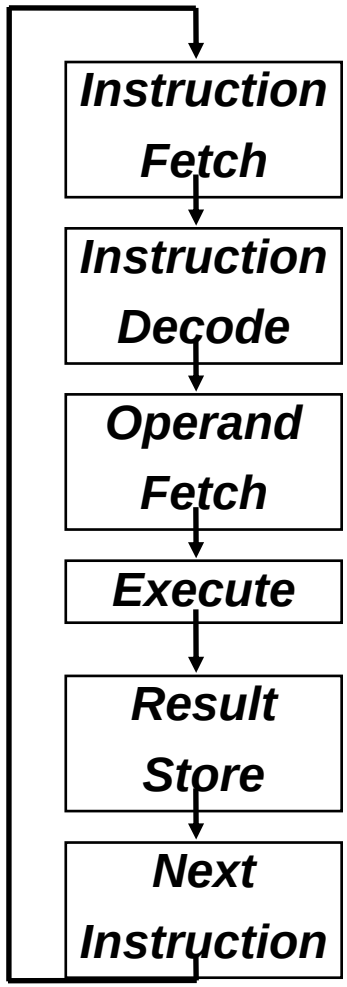
- 100% attendance is preferred. Once you miss the class you will lose the connectivity between topics
- Be on time in attending lecture class. Introductory 5 minutes is very important for the day's discussion.
- Academic dishonesty cannot be tolerated.
- I know everybody cannot score AA/AS.
  Do your best, Be sincere, Be open.
- It is not the marks but the effort that matters.
- I promise that you will enjoy this course.

Role of Computer Architects

Applications and hand held devices are part and parcel of our day to day life

What are the architectural features that will support the requirements of these applications?

Execution Cycle



Obtain instruction from program storage

Determine required actions and instruction size

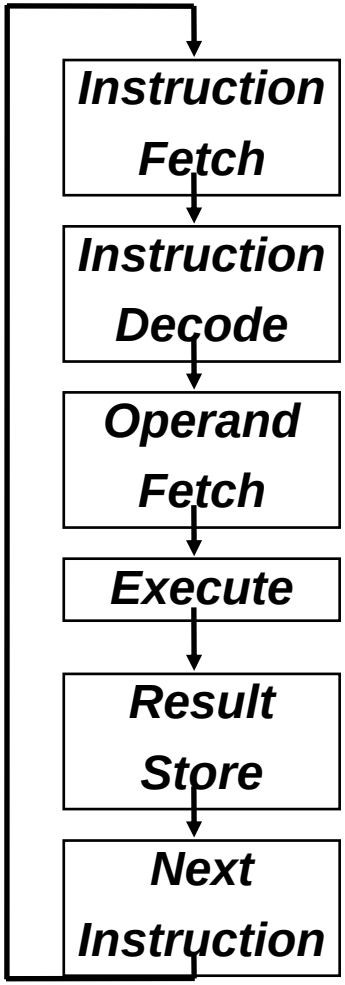
Locate and obtain operand data

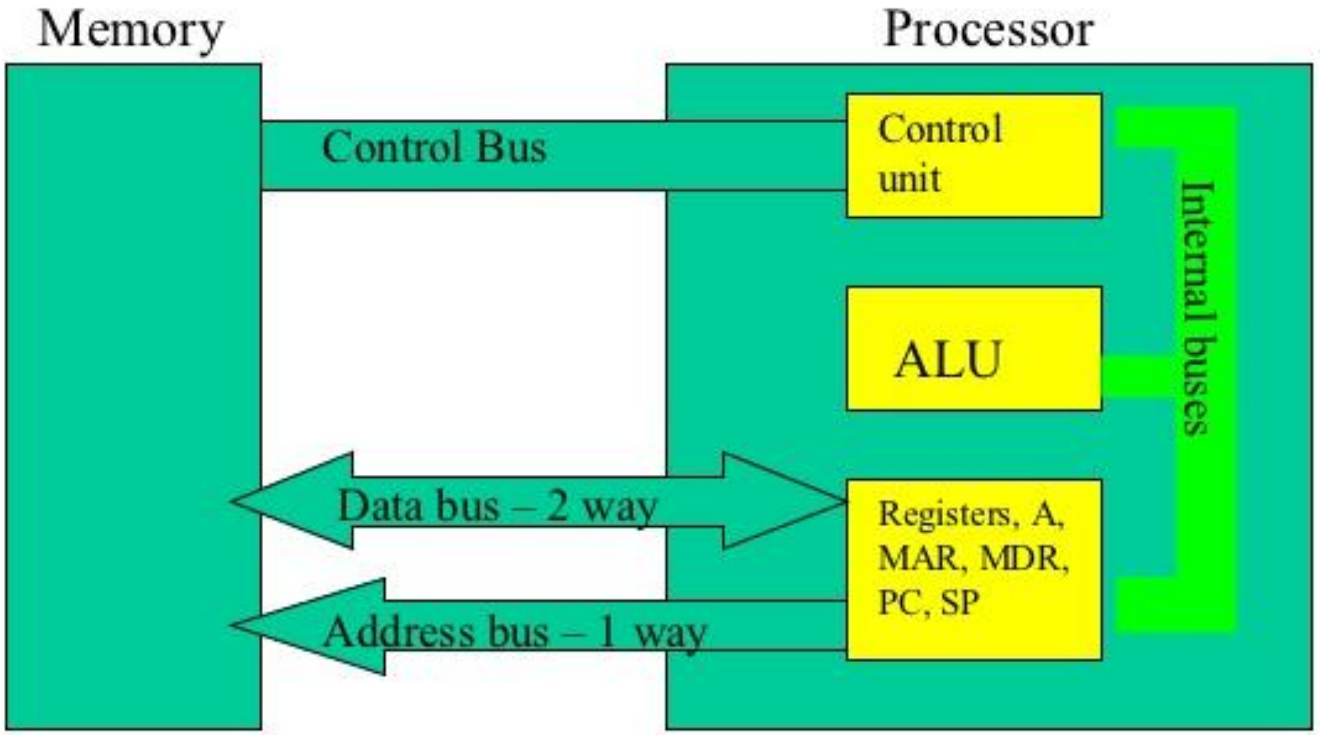
Compute result value or status

Deposit results in storage for later use

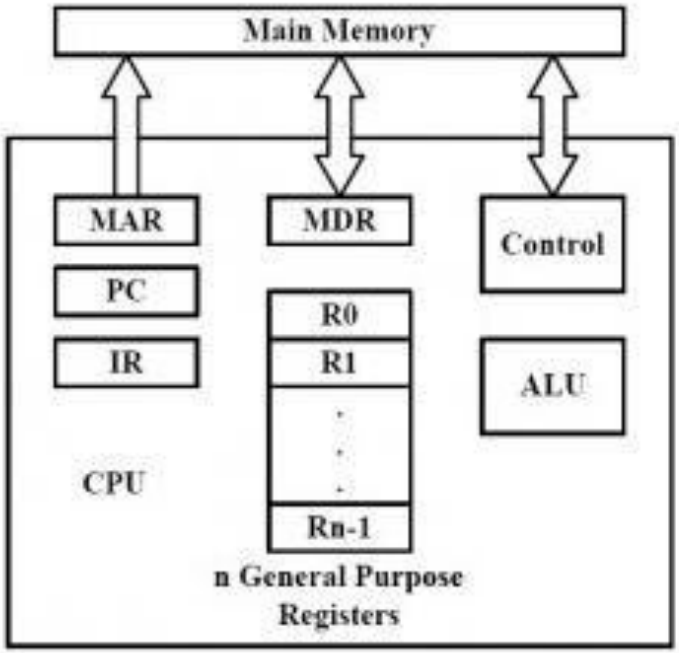
Determine successor instruction

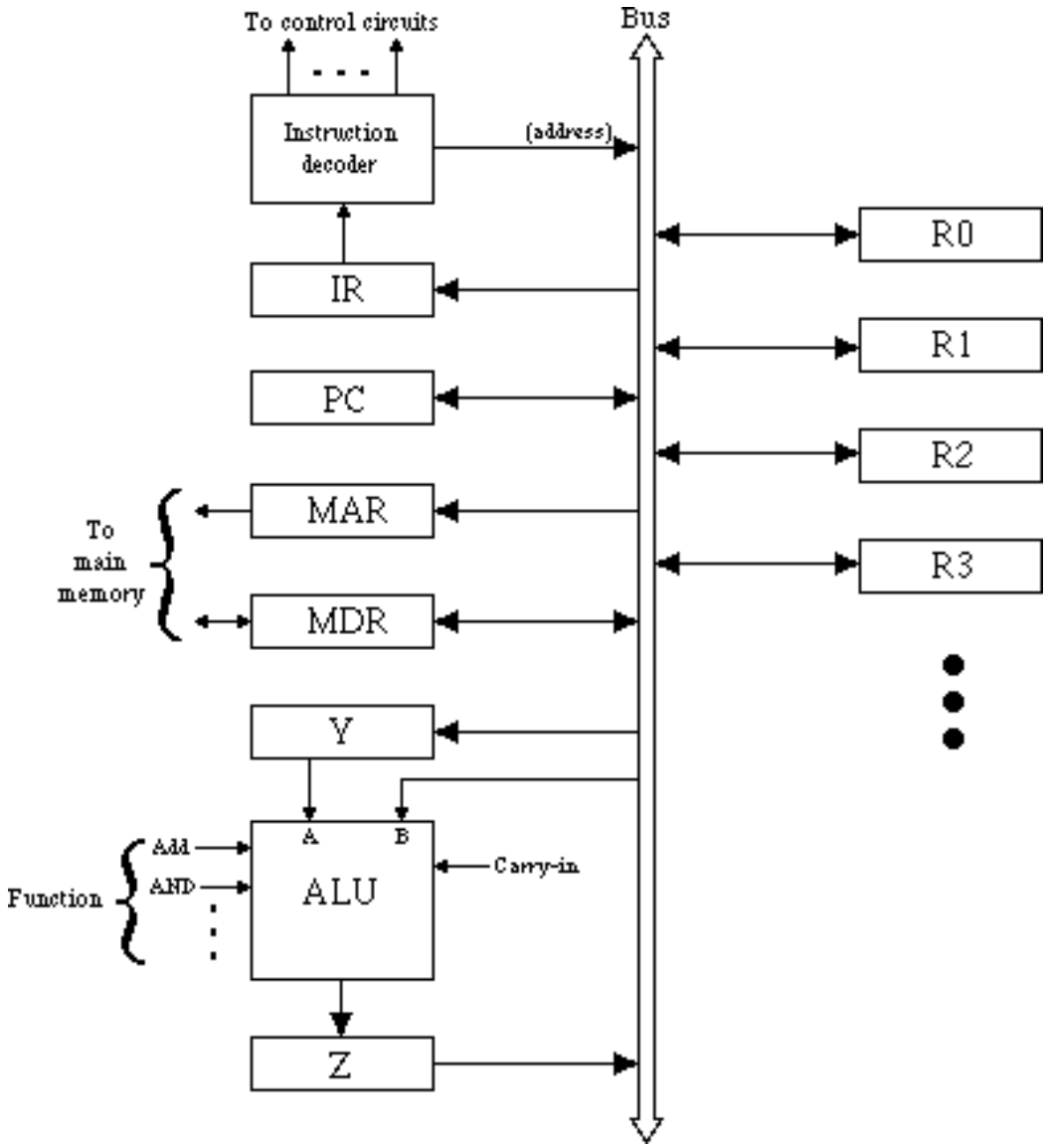
Processor Memory Interaction





Processor Memory Interaction

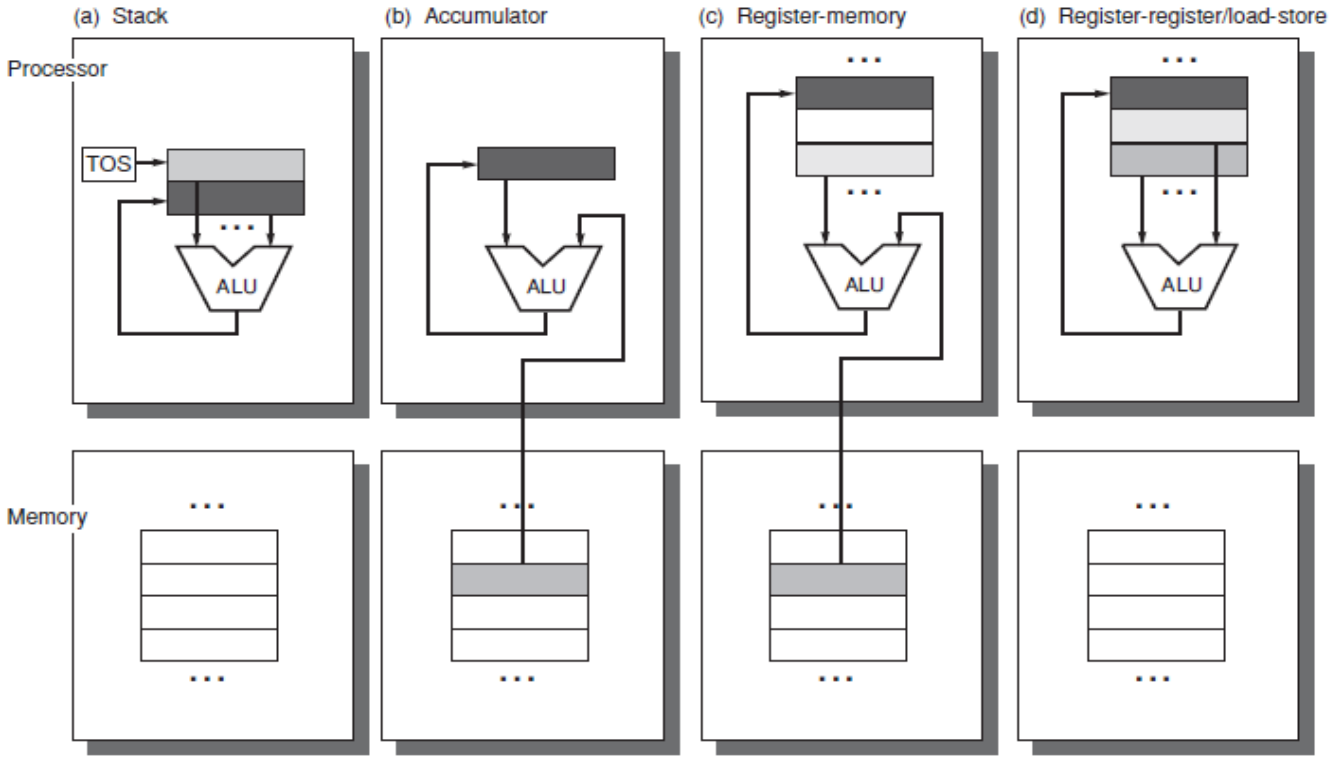




Instruction Set Architecture

- Instruction vs Program vs Software
- Opcode, Operand
- Classification of ISA
  - Stack architecture
  - Accumulator architecture
  - Register-Memory architecture
  - Register-Register/Load Store architecture

Instruction Set Architecture



Stack	Accumulator	Register (register-memory)	Register (load-store)
Push A	Load A	Load R1,A	Load R1,A
Push B	Add B	Add R3,R1,B	Load R2,B
Add	Store C	Store R3,C	Add R3,R1,R2
Pop C			Store R3,C

The code sequence for C = A + B for four classes of instruction sets.

CISC vs RISC architecture

	CISC (Complex Instruction Set Computer)	**RISC (Reduced Instruction Set Computer)**
1	Emphasis on hardware	Emphasis on software
2	Includes multi-clock complex instructions	Single-clock, reduced instruction only
3	Small code sizes	Typically larger code sizes
4	Many addressing modes	Few addressing modes.
5	An easy compiler design	A complex compiler design.
6	Pipelining does not function correctly here because of complexity in instructions.	Pipelining is not a major problem and this option speeds up the processors.

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