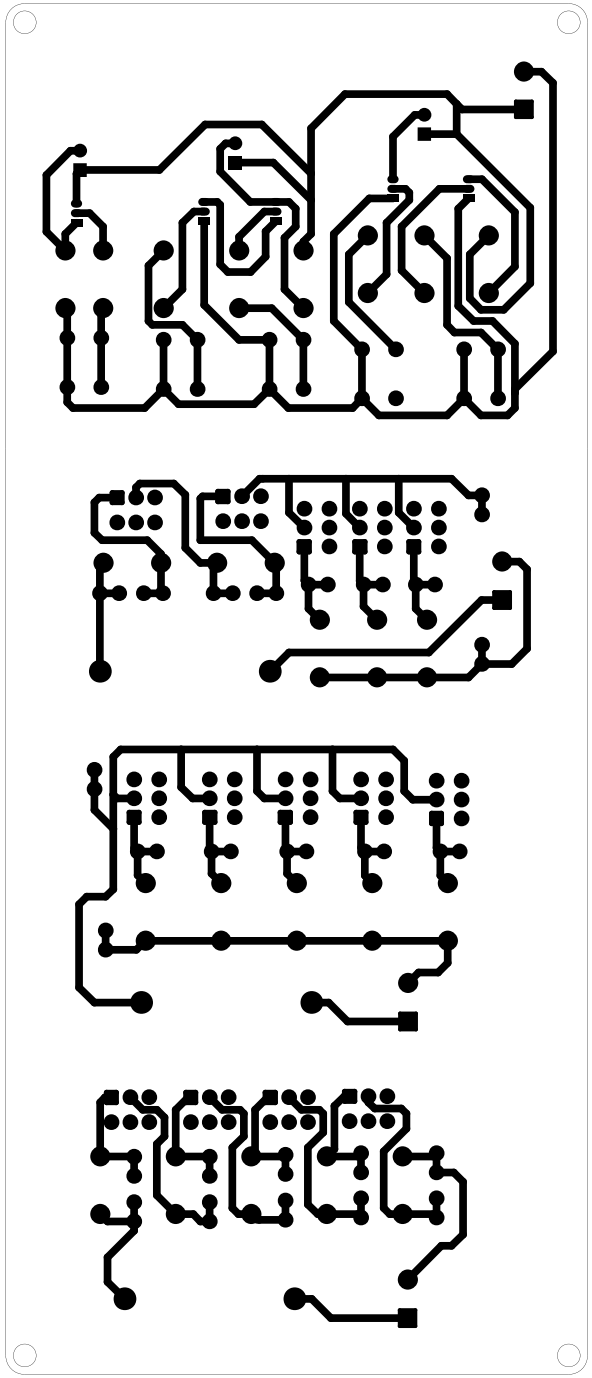

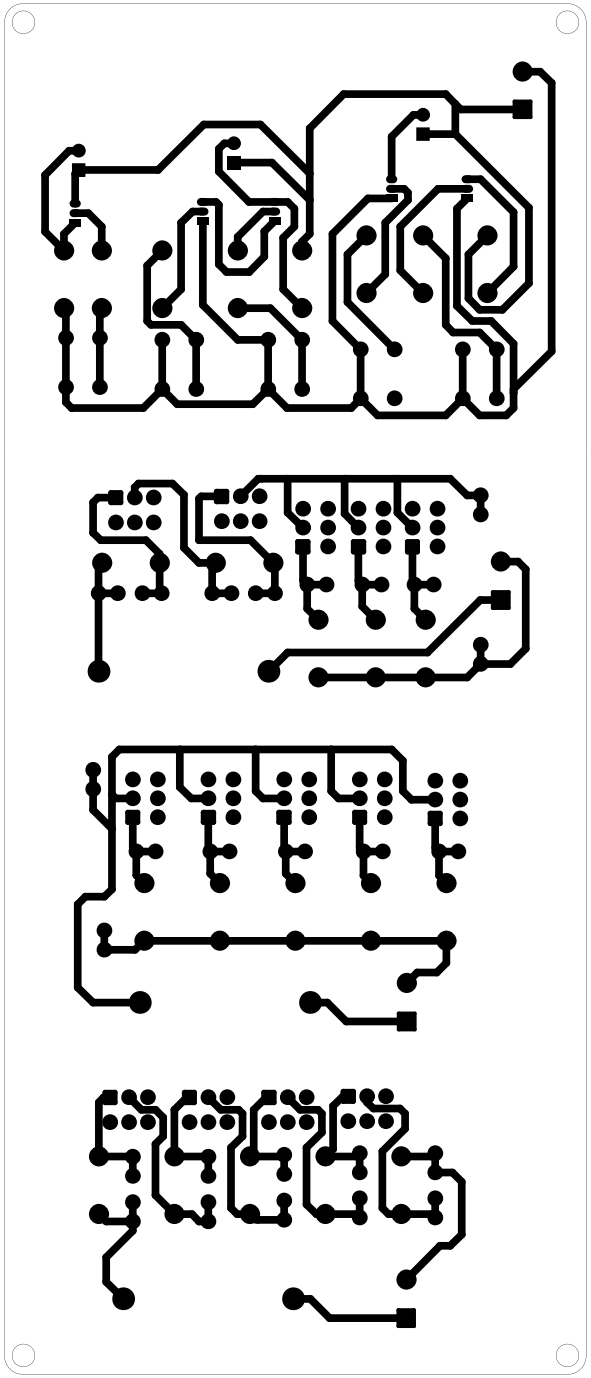

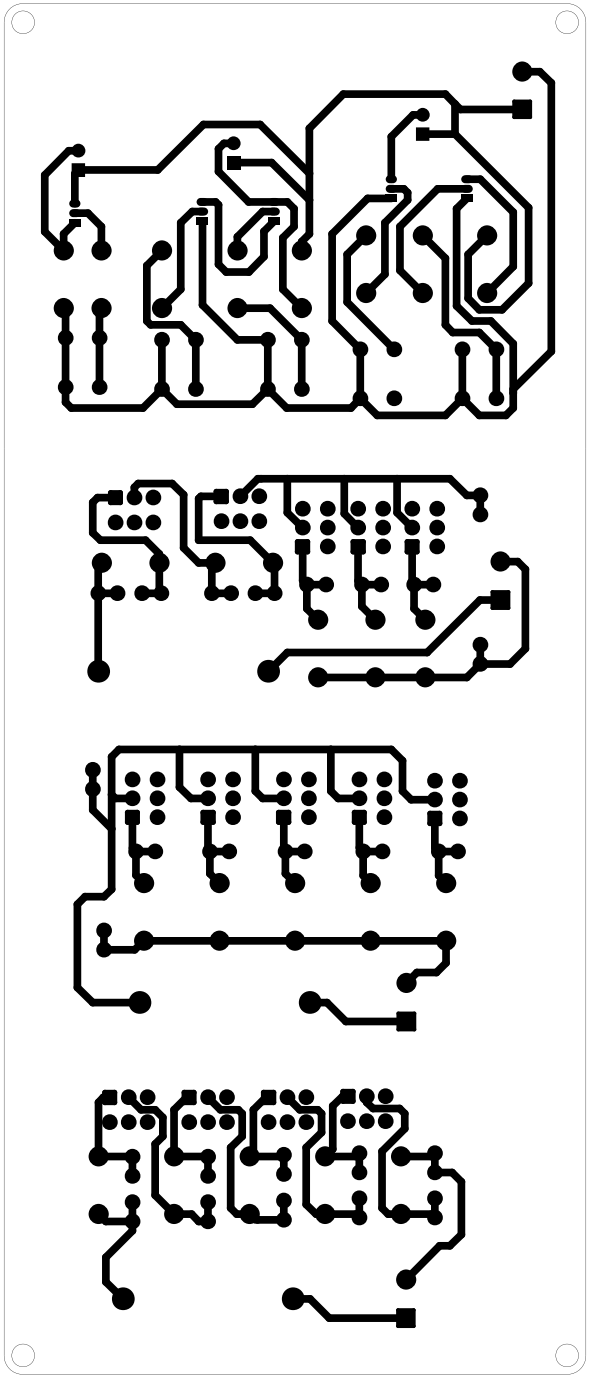

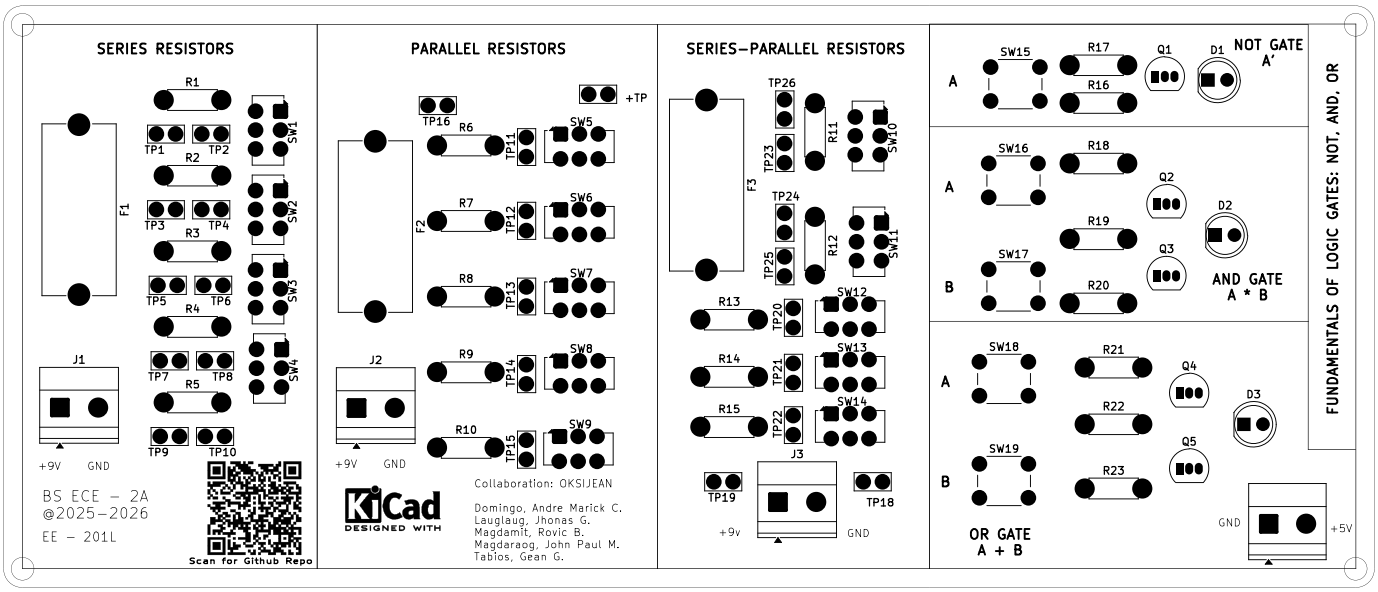
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R1
R2
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R4
R5
F1
J1
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
TP10
SW1
SW2
SW3
SW4
+9V
GND
BS ECE – 2A
@2025–2026
EE – 201L
Scan for Github Repo
PARALLEL RESISTORS
+TP
TP16
R6
R7
R8
R9
R10
F2
J2
TP11
TP12
TP13
TP14
TP15
SW5
SW6
SW7
SW8
SW9
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KiCad
DESIGNED WITH
Collaboration: OKSIJEAN
Domingo, Andre Marick C.
Lauglaug, Jhonas G.
Magdamit, Rovic B.
Magdaraog, John Paul M.
Tabios, Gean G.
SERIES–PARALLEL RESISTORS
TP26
TP23
R11
SW10
F3
TP24
TP25
R12
SW11
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TP20
SW12
R14
TP21
SW13
R15
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R16
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NOT GATE
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R18
R19
Q2
D2
B
SW17
R20
Q3
AND GATE
A * B
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SW18
R21
R22
Q4
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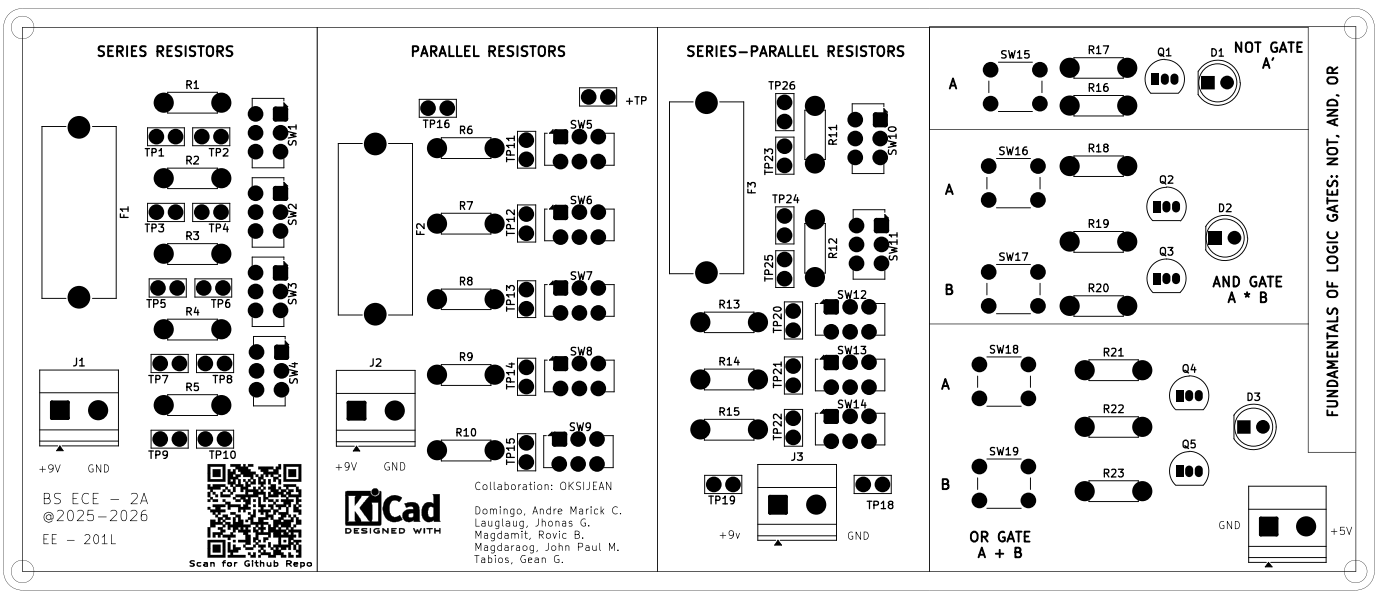
SW19
R23
Q5
OR GATE
A + B
GND
+5V
FUNDAMENTALS OF LOGIC GATES: NOT, AND, OR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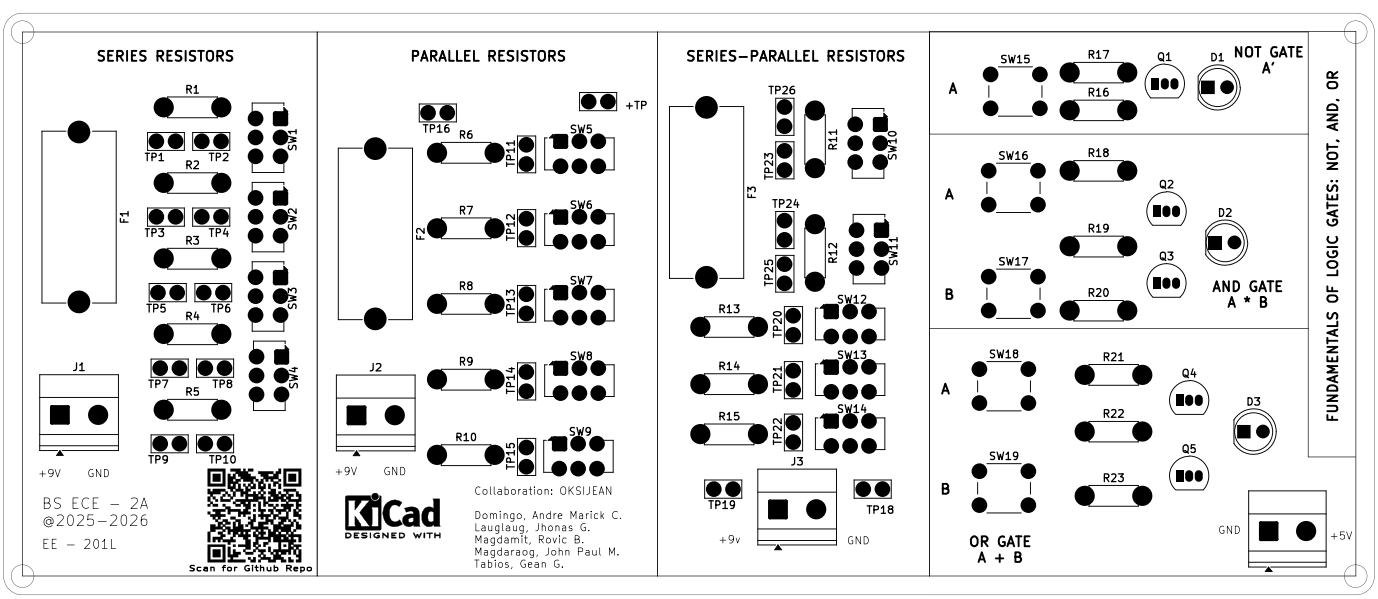
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FUNDAMENTALS OF LOGIC GATES: NOT, AND, OR