Faculty of Enigeering

Cairo University

Analog Electronics Project Documentation

PDK UMC 0.13 µm Technology

Presented for ELC 2060 Cadence Project

Presented to:

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TASK 1

MOSFETs Characteristics

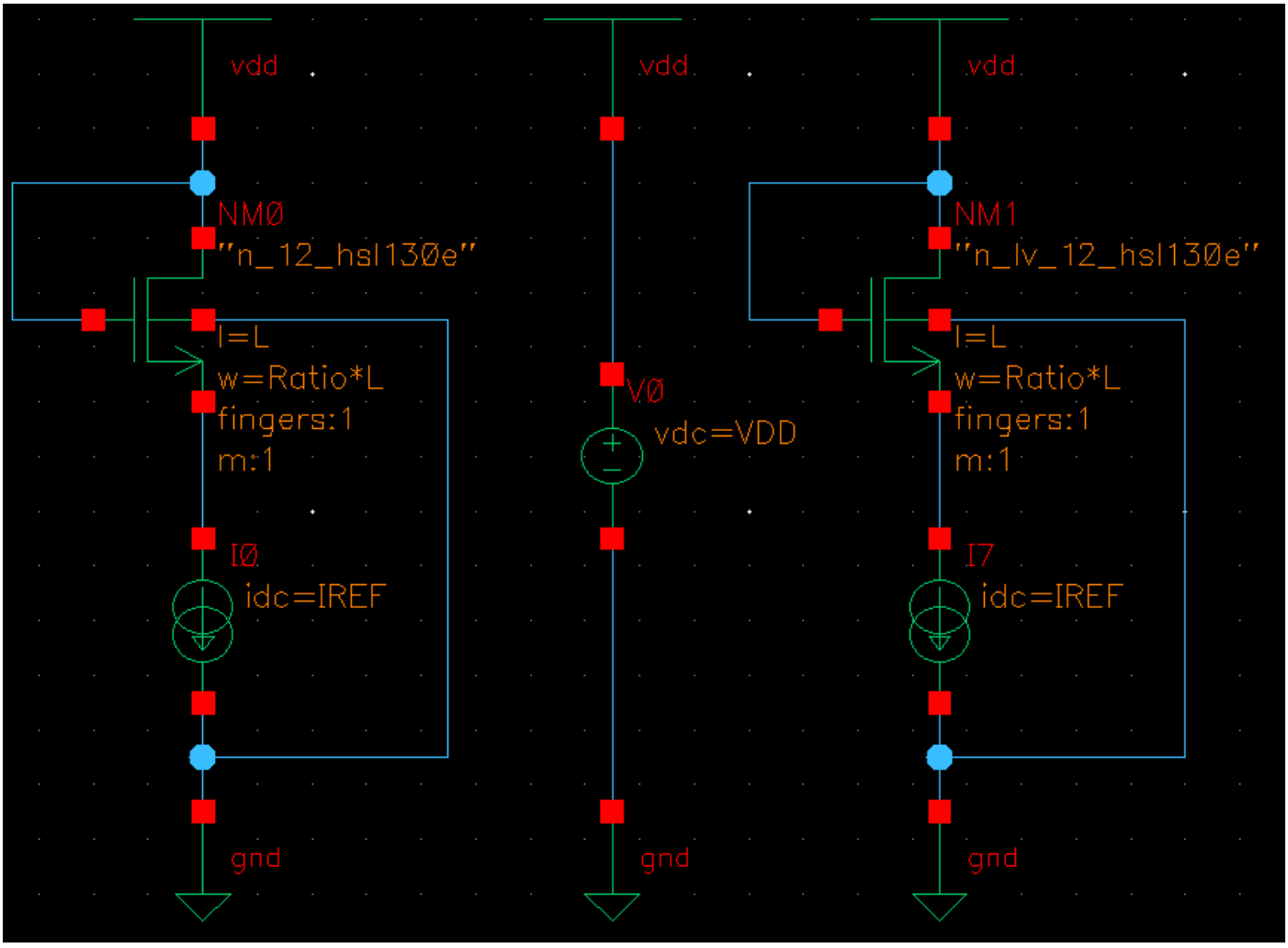
N_12_HSL130E
HIGH - SPEED NMOS

N_LV_12_HSL130E
LOW - VTH HIGH - SPEED NMOS

NM0

Circuit Schematic

NM1



Test Bench (Output Setup in ADE XL)

Note: to Know L_{min} Value Put in the Schematic L = 0 Cadence Will Delete it and write L = 120n immediately.

Global Variables

IREF	200u
L	120n,240n,480n,960n
Ratio	1
VDD	1.2

Click to add variable

task1 | adexl

Outputs Setup | Run Preview | Results | Diagnostics

Test	Name	Type	Details	EvalType	Plot	Save
ELC2060:task1:1	Vth vs W/L (NM0)	expr	v("NM0:vth" ?result "dc")	point	☑	☐
ELC2060:task1:1	Vov vs W/L (NM0)	expr	(v("NM0:vgs" ?result "dc") - v("NM0:vth" ?result "dc"))	point	☑	☐
ELC2060:task1:1	Vdsat vs W/L (NM0)	expr	v("NM0:vdsat" ?result "dc")	point	☑	☐
ELC2060:task1:1	gm.ro vs W/L (NM0)	expr	(getData("NM0:gm" ?result "dc") * getData("NM0:rout" ?result "dc"))	point	☑	☐
ELC2060:task1:1	Vth vs W/L (NM1)	expr	v("NM1:vth" ?result "dc")	point	☑	☐
ELC2060:task1:1	Vov vs W/L (NM1)	expr	(v("NM1:vgs" ?result "dc") - v("NM1:vth" ?result "dc"))	point	☑	☐
ELC2060:task1:1	Vdsat vs W/L (NM1)	expr	v("NM1:vdsat" ?result "dc")	point	☑	☐
ELC2060:task1:1	gm.ro vs W/L (NM1)	expr	(getData("NM1:gm" ?result "dc") * getData("NM1:rout" ?result "dc"))	point	☑	☐

Curves Colors For $L = L_{min}$ (Red), $2L_{min}$ (Yellow), $4L_{min}$ (Green), $8L_{min}$ (Blue)

Q1

N_12_HS_L130E (High Speed NM0)	N_LV_12_HS_L130E (Low V_{th} High Speed NM1)

NM0 V_{th} (Threshold Voltage) NM1

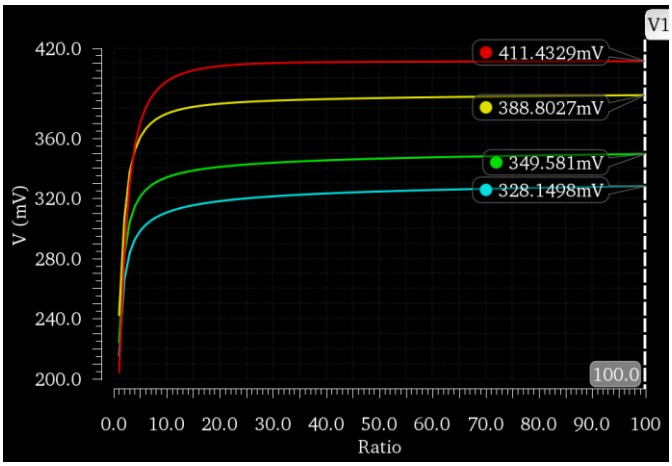


Figure (1.1)

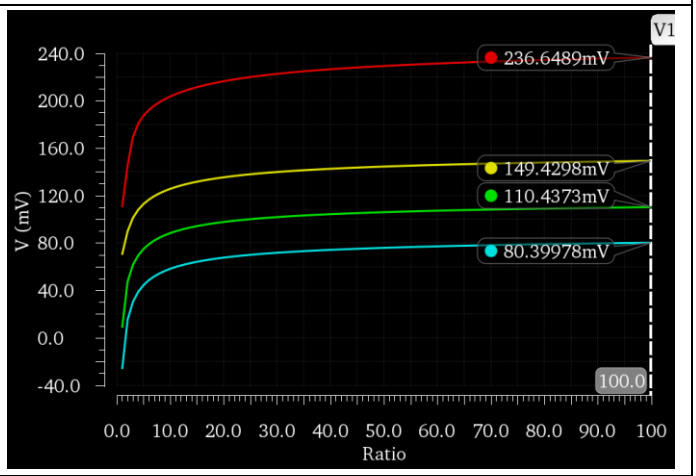


Figure (1.2)

NM0 V_{ov} (Overdrive Voltage) NM1

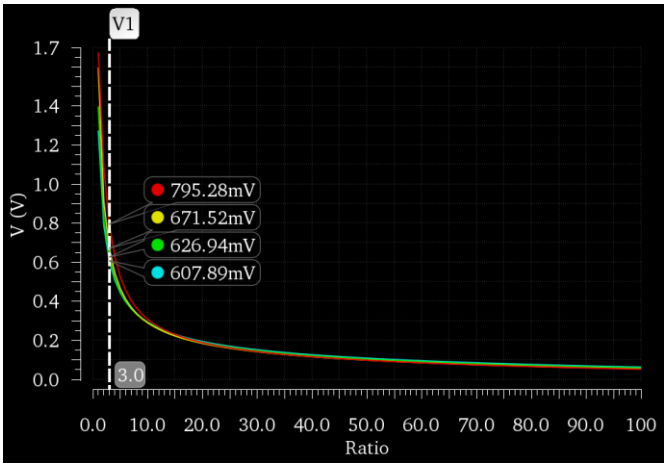


Figure (1.3)

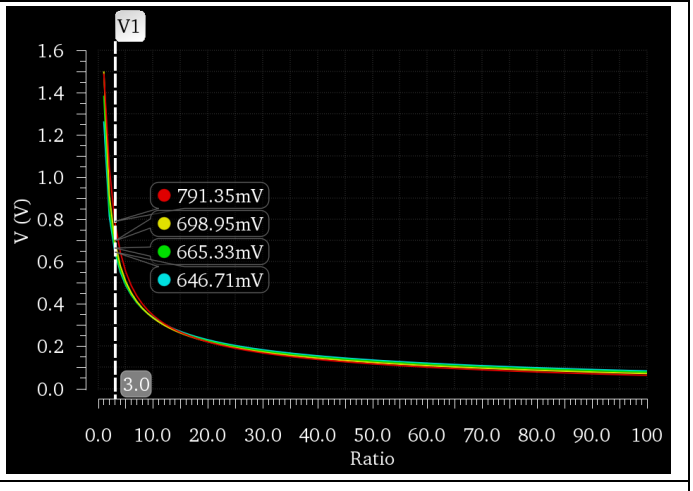


Figure (1.4)

NM0 V_{dsat} (Saturation Voltage) NM1

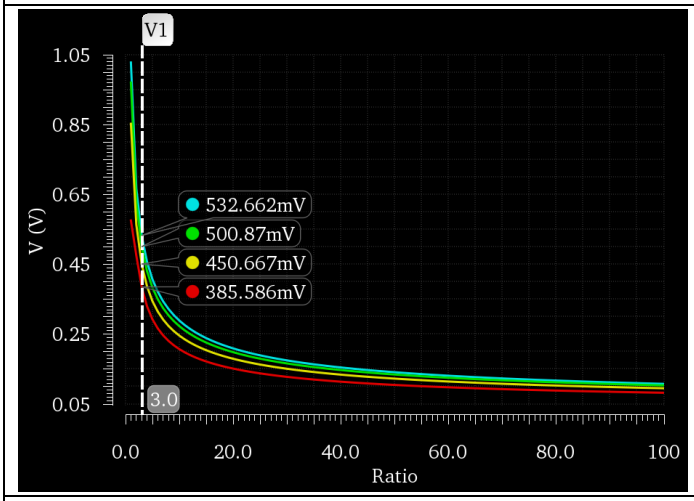


Figure (1.5)

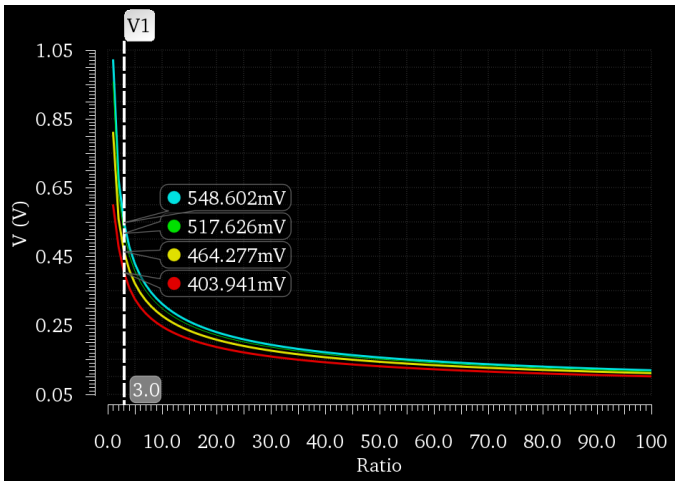


Figure (1.6)

NM0 $g_m . r_o$ (Intrinsic Gain) NM1

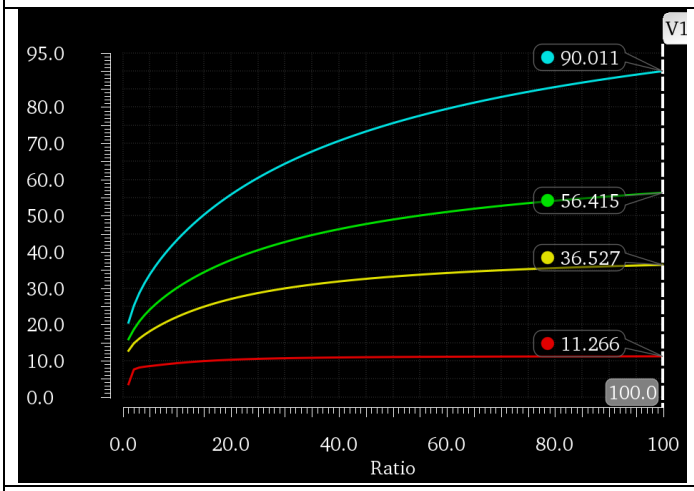


Figure (1.7)

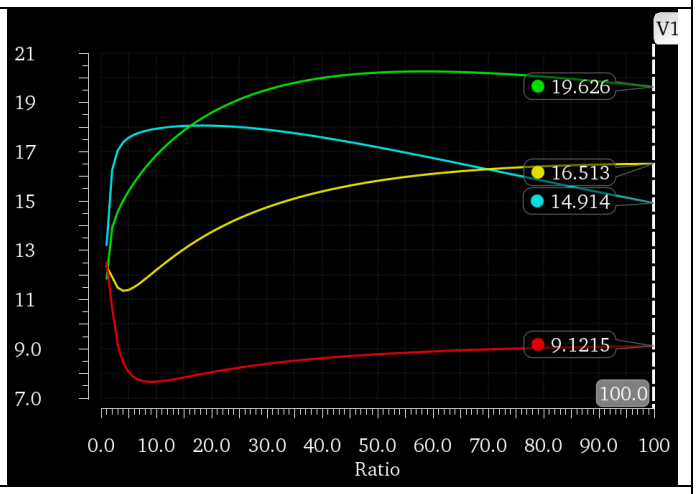


Figure (1.8)

Comments for The Parameters (Another Comments in Long Eqn. Section):

V_{th} vs W/L : in Figures (1.1) & (1.2): -

- V_{th} Decrease While L Increase and it Stay Constant With W/L Pass a Certain Value.

V_{ov} vs W/L : in Figures (1.3) & (1.4): -

- Small Variations as L increase at small W/L and V_{ov} Decreases While W/L Increase and seems to be Constant with L Increase at large W/L.

V_{dsat} vs W/L : in Figures (1.5) & (1.6): -

- Small Variations as L increase at small W/L and V_{dsat} Decrease While W/L Increase and V_{dsat} increases with L Increase.

Comparison Between V_{ov} & V_{dsat}

- $V_{ov} = V_{gs} - V_{th} = V_{dsat}$ → When Square Law is Valid @ Long Channel
- $V_{ov} \neq V_{dsat}$ at Short Channel as we see in Figures (1.3) & (1.4) & (1.5) & (1.6) Due to Square law isn't Valid due to Short Channel Effects even it can be due to Velocity Saturation, Mobility Degradation and Drain induced Barrier lowering (DIBL)

$g_m.r_o$ vs W/L : in Figures (1.7) & (1.8): -

- Intrinsic Gain ($A_o = g_m r_o$) the highest gain Can Reach for the transistors.
- In NM0 as L increase the intrinsic gain increase while it is Random at NM1, And this is the reason for that if we need high gain or stable gain, we choose NM0 (N_12_HS_L130E).

Q2

Mention the long channel equation for (V_{th} , V_{ov} , $g_m.r_o$).

Is the trend of simulations similar to the equations?

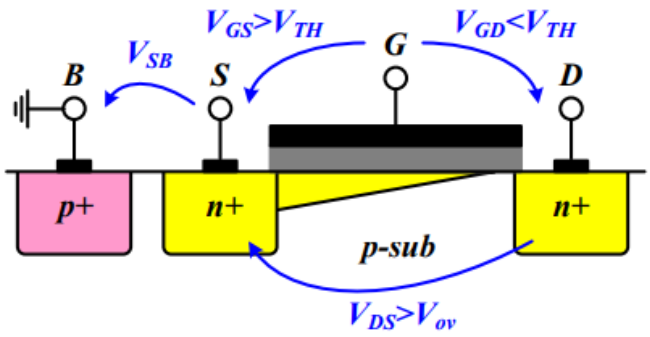
- Overview: The equations used to describe MOSFET behavior differ depending on the purpose. The square law equations are an estimation of MOSFET behavior in the saturation region, while the long channel equations provide a more comprehensive explanation of MOSFET behavior in all operational areas, such as the linear and saturation regions. The long channel equations are more precise because they consider various physical aspects, including the effect of bulk bias on the threshold voltage, the shortening of the effective channel length at high drain-to-source voltages, and the output resistance of the device. Although the square law equations serve as an excellent approximation for MOSFET behavior in the saturation region, they do not cover all possible device behaviors. As a result, the long channel equations, which are more accurate, are frequently used in device simulation tools and circuit design software, such as Cadence.

- Threshold voltage (V_{th}):

  In all our Previous Relations we assumed that the Source and the body are connected, so $V_{SB} = 0$, but What if they aren't Connected?

  - We Find that the Threshold Voltage Is Function of V_{SB} as Follows:

    $V_{TH} = V_{TH_o} + \gamma\left(\sqrt{2\varphi_F + V_{SB}} - \sqrt{|2\varphi_F|}\right)$ Where V_{t0} is the threshold voltage at zero bulk bias, γ is the body effect coefficient Depends on (C_{ox}) and Doping, and (φ_F): Surface Potential at Threshold Depends on Doping Level and Intrinsic Carrier Concentration n_i.



  - Comments on (V_{th}): -

    When W/L Increase and i_d & V_g want to be Constant when the Body is Grounded V_s Decrease and V_{SB} Increase it Make V_{th} as Shown in Figures (1.1) & (1.2),

    So, yes, the Trend of V_{th} Curve is Described by The Long Channel Equation.

- Overdrive voltage (V_{ov}):

  The Effective Voltage $V_{ov} = V_{gs} - V_{th}$, Where V_{gs} is the gate-to-source Voltage.

  - From the Square Law and Long Channel Equations.

$$i_d = \frac{K_n}{2}(V_{ov})^2 = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}V_{ov}^2 \rightarrow V_{ov} = \sqrt{\frac{2I_d}{\mu_n C_{ox}\frac{W}{L}}}$$

  - Comments on (V_{ov}): -

    Relation Between $V_{ov} \propto \frac{1}{\sqrt{W/L}}$ and this is the Trend for V_{ov} As Shown in Figures (1.3) & (1.4) As it Start at High Values Then It Decrease Gradually Till it Saturated like the Inversion of Square Root Function.
    So, yes, the Trend of V_{ov} Curve is Described by The Long Channel Equation.

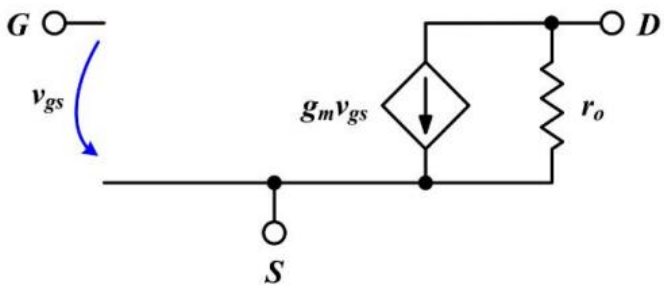
- Intrinsic Gain ($g_m . r_o$): -

  In Square Law and the Long Channel Equations Assume there is No Channel Length Modulation.

$$g_m = \frac{\triangle I_D}{\triangle V_{GS}} = \frac{\partial I_D}{\partial V_{GS}} = \frac{\partial I_D}{\partial V_{ov}} = \frac{\partial}{\partial V_{ov}}\left[\frac{1}{2}\mu_n C_{ox}\frac{W}{L}V_{ov}^2(1+\lambda V_{DS})\right]$$

$$g_m = \mu_n C_{ox}\frac{W}{L}V_{ov} = \mu_n C_{ox}\frac{W}{L}\sqrt{\frac{2I_D}{\mu_n C_{ox}\frac{W}{L}}} = \sqrt{2I_D K_n} = \sqrt{2I_D \mu_n C_{ox}\frac{W}{L}}$$

$$r_o = \frac{1}{Slope} = \frac{\triangle V_{DS}}{\triangle I_D} = \frac{1}{\frac{\partial I_D}{\partial V_{DS}}} = \frac{V_A}{I_{DS}} = \frac{1}{\lambda I_{DS}} = \frac{1}{g_{DS}} = \frac{1+\lambda V_{DS}}{\lambda I_D} = \frac{V_A\frac{L}{\Delta L} + V_{DS}}{I_D}$$



$$g_m . r_o = \frac{1+\lambda V_{DS}}{\lambda I_D}.\sqrt{2I_D\mu_n C_{ox}\frac{W}{L}} = \frac{1+\frac{\Delta L}{V_A L}V_{DS}}{\frac{\Delta L}{V_A L}I_D}.\sqrt{2I_D\mu_n C_{ox}\frac{W}{L}}$$

Where $V_A \propto L$ and $\lambda \propto \frac{1}{L} \rightarrow \lambda \approx \frac{\Delta L}{V_A L}$ (Shichman – Hodges Model)

  - Comments on ($g_m . r_o$): -

    Relation Between $g_m . r_o \propto \sqrt{W/L}$ & λ and this is the Trend for $g_m . r_o$
    As Shown in Figures (1.7) & (1.8) Like the Square Root Function.
    So, yes, the Trend of $g_m . r_o$ Curve is Described by The Long Channel Equation.

- Mention one advantage and one disadvantage for N_LV_12_HS_L130E compared to N_12_HS_L130E.
  What do you recommend being used in a High - Gain amplifier ?

P.O.C	N_LV_12_HS_L130E (NM1)	N_12_HS_L130E (NM0)
Advantage	Low - Threshold Voltage, High - Speed NMOS transistor this Lowering in Threshold Voltage, resulting in faster switching speeds which can lead to lower power consumption. The lower V_{th} allows the transistor to turn on more easily, resulting in faster rise and fall times. This makes it suitable for applications that require high - speed switching, such as digital circuits and high - frequency amplifiers.	High - Speed NMOS transistor Transistors have a higher V_{th}, resulting in lower leakage current and better immunity to process variations and noise.
Disadvantage	This Transistor Has higher leakage current and susceptibility to process variations, noise, and interference. Making the Device easily triggered by small voltage fluctuations.	This Transistor Has Slower switching speed, which can limit its use in high - speed applications and resulting in higher power consumption.

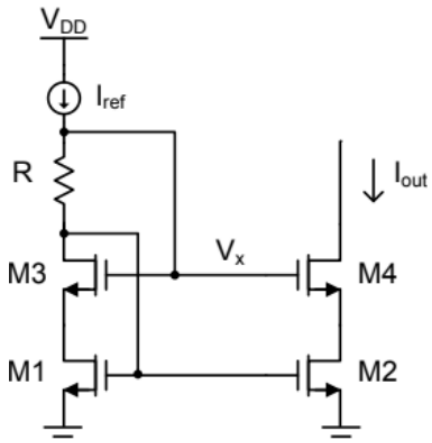
- High Gain Amplifier Choice Between N_LV_12_HS_L130E (NM1) & N_12_HS_L130E (NM0)
  - The choice between the two transistors depends on the trade-offs between speed, power consumption, and reliability. In a high-gain amplifier, the choice should be based on the specific requirements of the amplifier design, such as the input and output voltage levels, the frequency range, and the desired gain. A simulation or prototype should be created to determine the best transistor choice for the specific high-gain amplifier application.
  - The intrinsic gain characteristic charts presented are indicated in Figures (1.7) & (1.8). that the N_12_HS_L130E device has higher intrinsic gain values than the N_LV_12_HS_L130E device, despite having similar dimensions. As a result, if power consumption is not a concern, the N_12_HS_L130E (NM0) device would be a more appropriate option for meeting the requirements of high gain with noise immunity and high speed.

TASK 2

Current Mirror

USING GM/ID METHODOLOGY

- Use the NMOS core high speed HS transistor (N_12_HS_L130E) and the poly resistor. (RNPPO_MML130E) to design an accurate high - swing current mirror (according to the architecture shown) operating at $V_{DD} = 1.2$ V with the following specifications:
- $I_{out} = 2I_{REF} = 200\ \mu A$, With Error $< 1\%$ @ $V_{out} = 500$ mV.
- $V_{comp} \leq 350$ mV
  (Defined as the minimum output voltage required for all devices to operate in saturation).
- $R_{out} \geq 500\ k\Omega$ @ $V_{out} = 500$ mV.



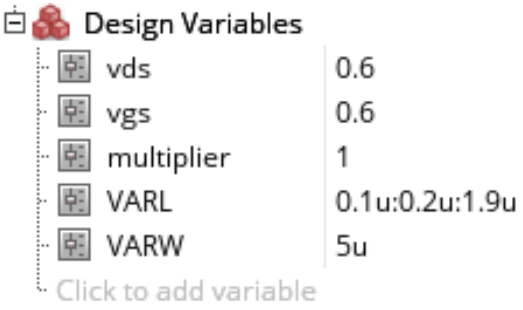
Overview For g_m/I_D Design Methodology:

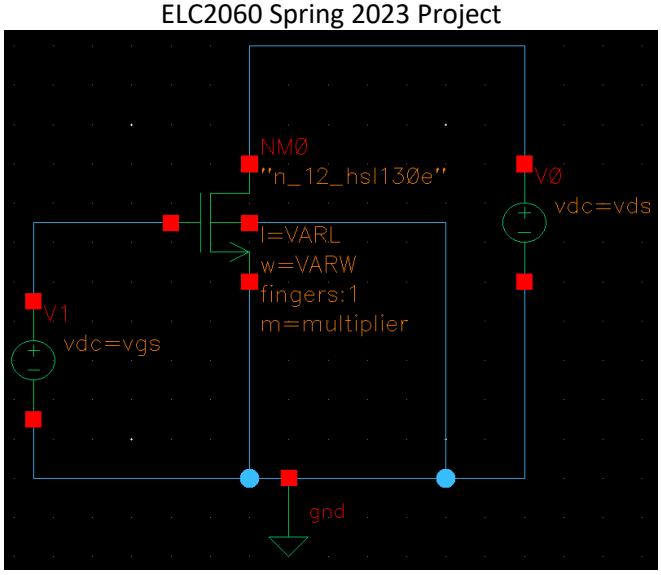
- Traditionally, square law was used in hand analysis to obtain initial design point.
- But short channel and moderate/weak inversion devices do not obey the square law.
- Square law is seldom used in nowadays designs.
- The popular approach nowadays is using g_m/I_D design methodology.
- Perform DC sweeps for both PMOS and NMOS to generate design charts vs g_m/I_D.
- g_m/I_D is a key MOSFET FoM (Figures - of - Merit)
- Use these charts (LUTs) to design your circuit to meet required specs.
- g_m/I_D captures the relation between the basic function of the transistor (the transconductance) and the most valuable resource (the power consumption).
- The range of g_m/I_D values doesn't differ much from one device to another and from one technology to another.
- g_m/I_D can be thought of as a normalized measure for the device inversion level.
- Plot Everything vs g_m/I_D !!

Test Bench (Output Setup in ADE Explorer)

g_m/I_D Charts Using Cadence Virtuoso:

$g_m.r_o$ Chart (Gain), I/W Chart (Current Density)
V_{dsat} Chart (To Adjust V_{comp}),
$W_{for\ M_4\ \&\ M_2}$ @ $I_D = 200\ \mu A$ Chart Function from I/W.



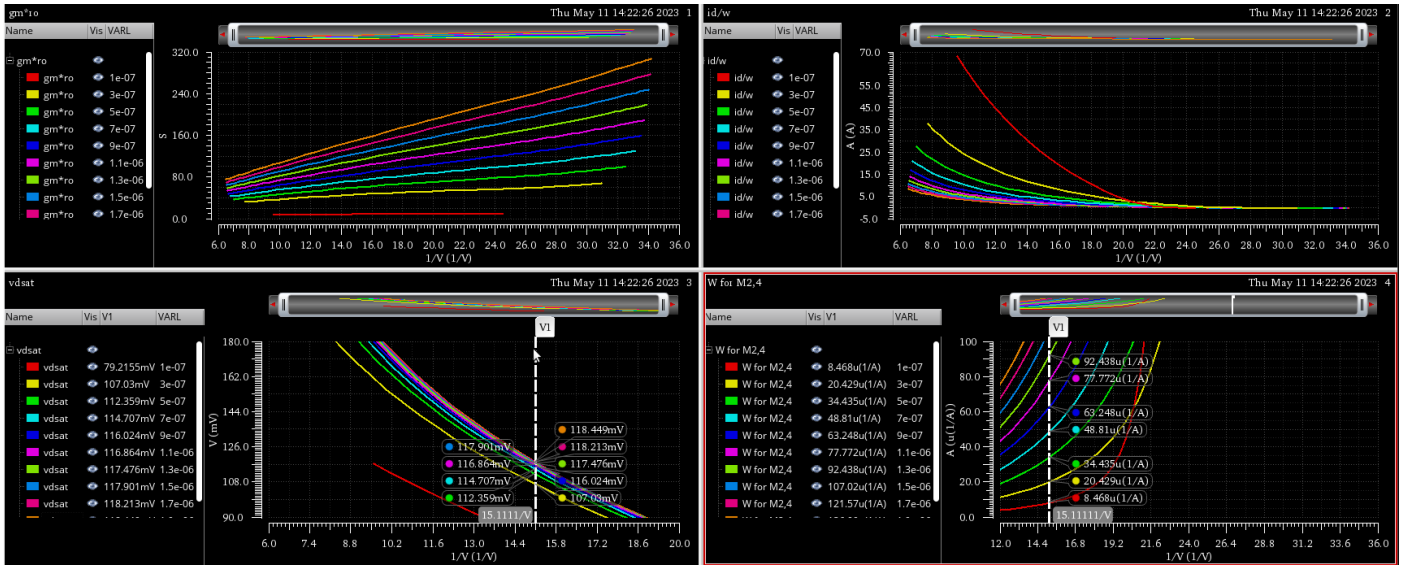


Schematic Used for g_m/I_D Charts.

gm_id_charts | maestro

Outputs Setup | Run Preview | Results | Diagnostics

Test	Name	Type	Details	EvalType	Plot	Save
ElectronicsProject:gm_id_charts:1		expr	OS("/NM0" "gmoverid")	point	☐	☐
ElectronicsProject:gm_id_charts:1		expr	(OS("/NM0" "id") / VAR("VARW"))	point	☐	☐
ElectronicsProject:gm_id_charts:1		expr	(OS("/NM0" "gm") / OS("/NM0" "gds"))	point	☐	☐
ElectronicsProject:gm_id_charts:1	/NM0	oppoint	/NM0 vdsat gds gm id gmoverid	point	☐	☑
ElectronicsProject:gm_id_charts:1		expr	OS("/NM0" "vdsat")	point	☐	☐
ElectronicsProject:gm_id_charts:1	gm*ro	expr	waveVsWave(?x OS("/NM0" "gmoverid") ?y (OS("/NM0" "gm") / OS("/NM0" "gds")))	point	☑	☐
ElectronicsProject:gm_id_charts:1	id/w	expr	waveVsWave(?x OS("/NM0" "gmoverid") ?y (OS("/NM0" "id") / VAR("VARW")))	point	☑	☐
ElectronicsProject:gm_id_charts:1	vdsat	expr	waveVsWave(?x OS("/NM0" "gmoverid") ?y OS("/NM0" "vdsat"))	point	☑	☐
ElectronicsProject:gm_id_charts:1	W for M2,4	expr	(0.0002 / waveVsWave(?x OS("/NM0" "gmoverid") ?y (OS("/NM0" "id") / VAR("VARW"))))	point	☑	☐



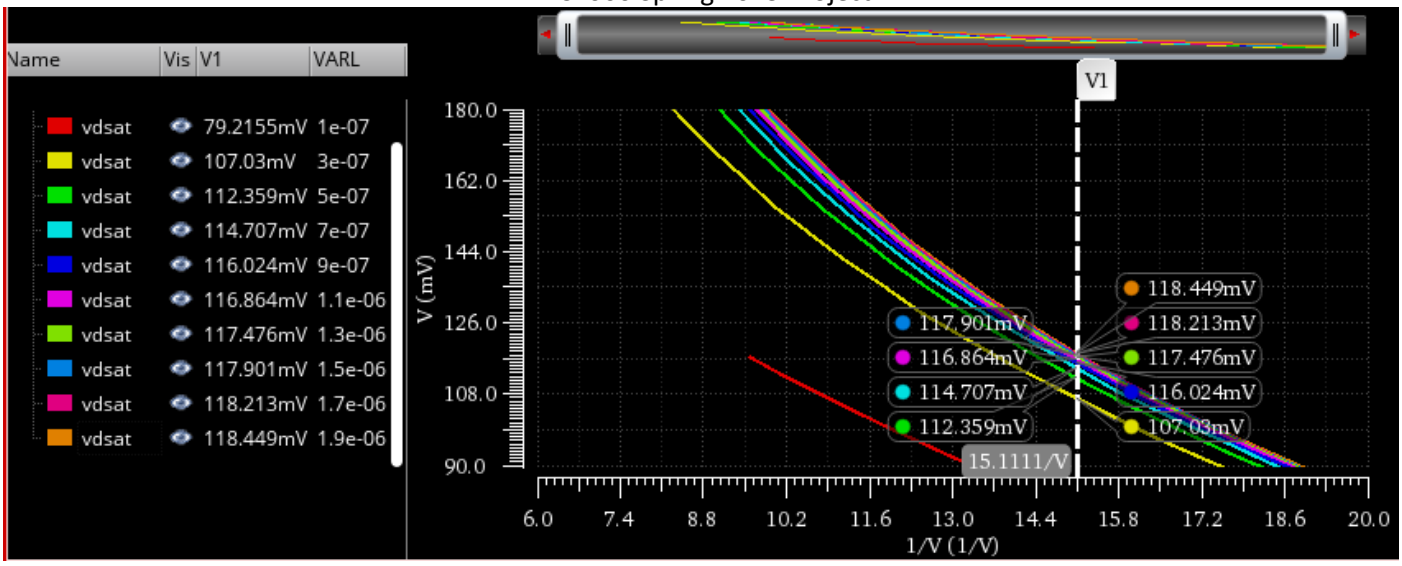
g_m/I_D Charts: gm. ro, I/W, V_{dsat} , and W for 200uA

Design Steps: -

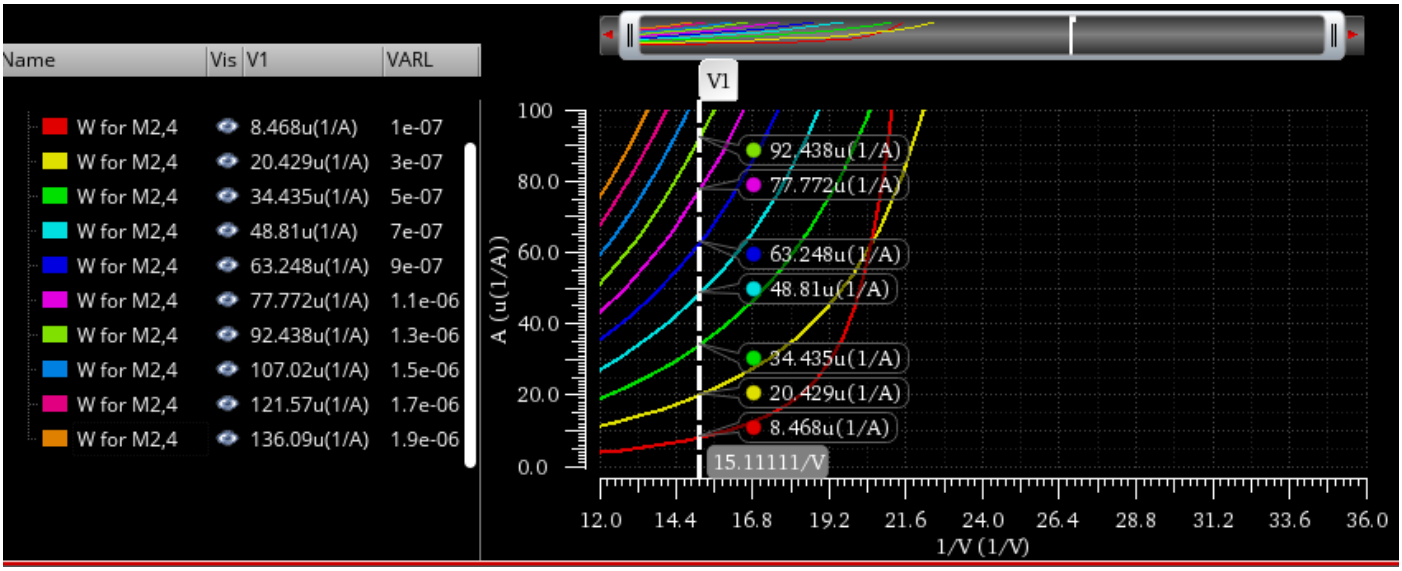
① From V_{dsat} Charts Choose a Value for V_{dsat} to Adjust $V_{comp} = 2V_{ov}$

Where choose $V_{dsat} < \frac{V_{comp}}{2} \rightarrow V_{dsat} < \frac{350\ mV}{2} \rightarrow V_{dsat} < 175\ mV.$

We choose $V_{dsat} = 114.707\ mV$, the Sky Color Curve as Shown in the Figure Below @ $g_m/I_D \approx 15\ V^{-1}$ & @ $L = 700\ nm$ go with this Values to $W_{for\ M_4\ \&\ M_2}$ to get W.



② From $g_m/I_D \approx 15\ V^{-1}$ and $L = 700$ nm that We Choose From V_{dsat} Charts And then go to $W_{\text{for } M_4 \,\&\, M_2}$ to get W, As Shown in the Figure Below from the required Curve.



③ Get The Value of the poly resistor. (RNPPO_MML130E) (R),
First we get the maximum & Minimum: -

To Keep M_3 in SAT: $\rightarrow V_{GD_3} < V_{th}, \therefore I_{REF}R < V_{th}, \ \therefore R < \frac{V_{th}}{I_{REF}} \rightarrow R < 4\ k\Omega$

To Keep M_1 in SAT: $\rightarrow V_{GD_1} < V_{th}, \therefore -I_{REF}R + V_{GS_3} < V_{th}, \therefore R > \frac{V_{ov}}{I_{REF}} \rightarrow R > 1.75\ k\Omega$

We Choose Average Value $R = 2.2\ k\Omega$.

Design Parameters	Value	Notes
W	48.8 µm	$W_{M_4 \,\&\, M_2} = 2 * W_{M_1 \,\&\, M_3}$
L	700 nm	L is the Same for all Transistors
R	2.2 kΩ	Make all Transistors in SAT Region and Adjust Value of R_{out} & V_{comp} with W/L Ratio.
# Fingers for M_1 & M_3	4	Should $\#Fingers_{M_2 \,\&\, M_4} = Double * \#Fingers_{M_1 \,\&\, M_3}$ to Adjust Error to be < 1%
# Fingers for M_2 & M_4	8	

Test Bench (Output Setup in ADE XL)

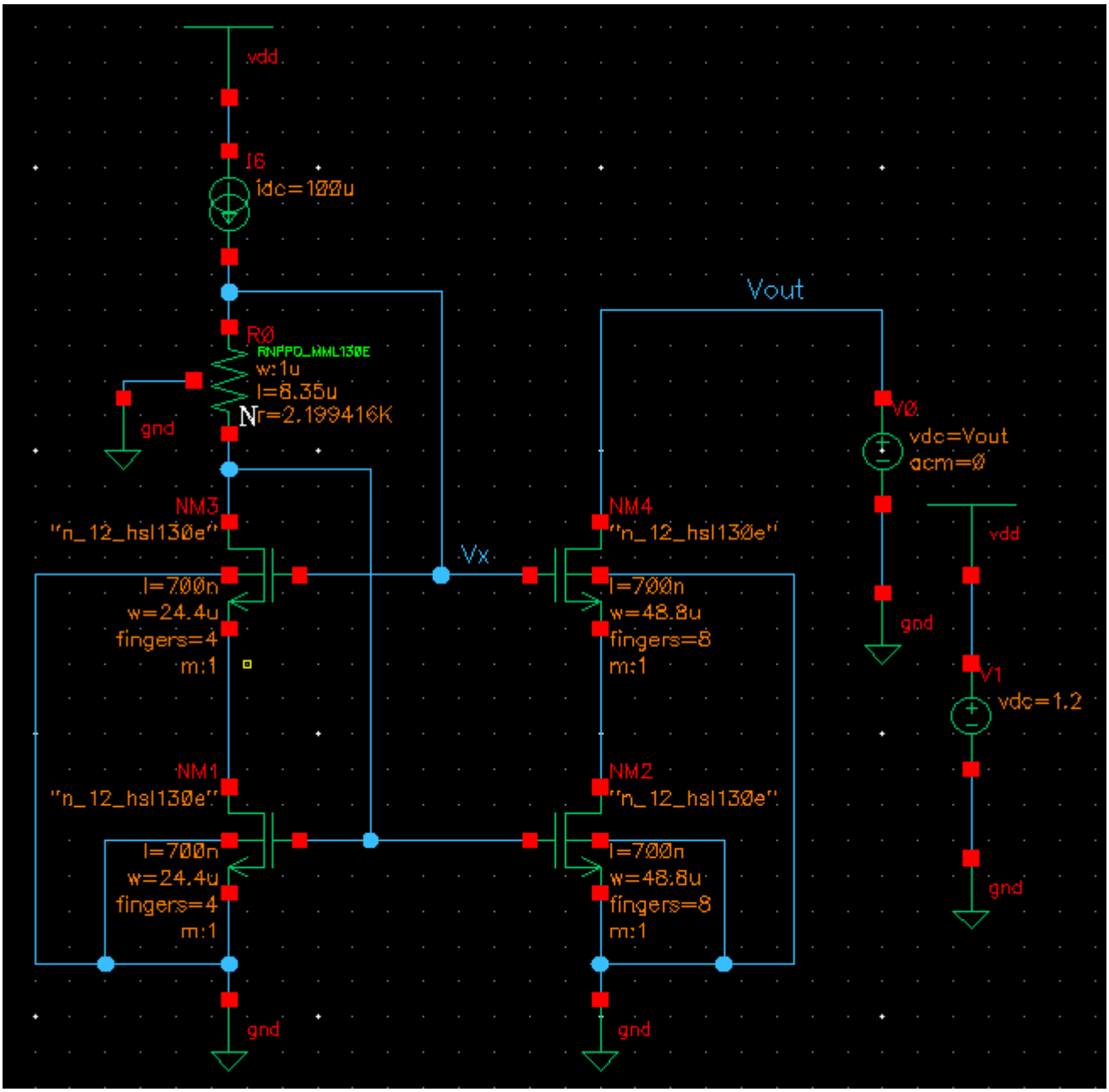
task2 × adexl ×

Outputs Setup | Run Preview | Results | Diagnostics

Test	Name	Type	Details
ELC2060:task2:1	Rout	expr	(1 / deriv(getData("NM4:ids" ?result "dc")))
ELC2060:task2:1	Rout (Formula)	expr	(getData("NM2:rout" ?result "dc") + getData("NM4:rout" ?result "dc") + (getData("NM2:rout" ?result "dc") * getData("NM4:rout" ?result "dc") * getData("NM4:gm" ?result "dc")))
ELC2060:task2:1	Region M1	expr	getData("NM1:region" ?result "dc")
ELC2060:task2:1	Region M2	expr	getData("NM2:region" ?result "dc")
ELC2060:task2:1	Region M3	expr	getData("NM3:region" ?result "dc")
ELC2060:task2:1	Region M4	expr	getData("NM4:region" ?result "dc")
ELC2060:task2:1	Error	expr	(((getData("NM4:ids" ?result "dc") - (2 * getData("NM3:ids" ?result "dc"))) * 100) / (2 * getData("NM3:ids" ?result "dc")))
ELC2060:task2:1	Iout	expr	getData("NM4:ids" ?result "dc")
ELC2060:task2:1		signal	/NM4/D
ELC2060:task2:1	Rout AC	expr	(VF("/Vout") / IF("/NM4/D"))

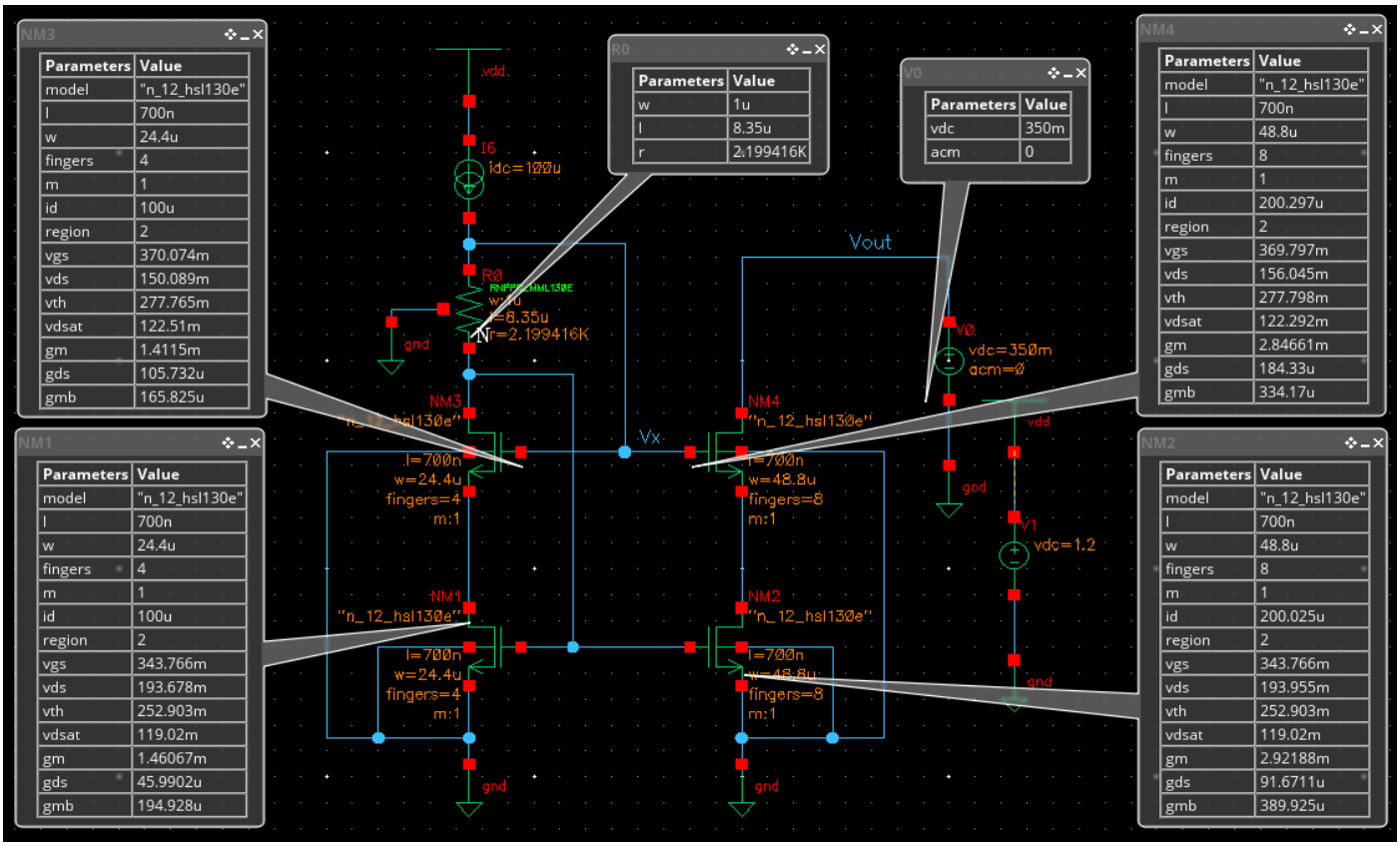
① Schematic diagram with dimensions and component values annotated.

Q1



Q2

② Schematic diagram with DC operating point annotated at $V_{out} = 350$ mV to verify the V_{comp} specification (Using BALLONS).



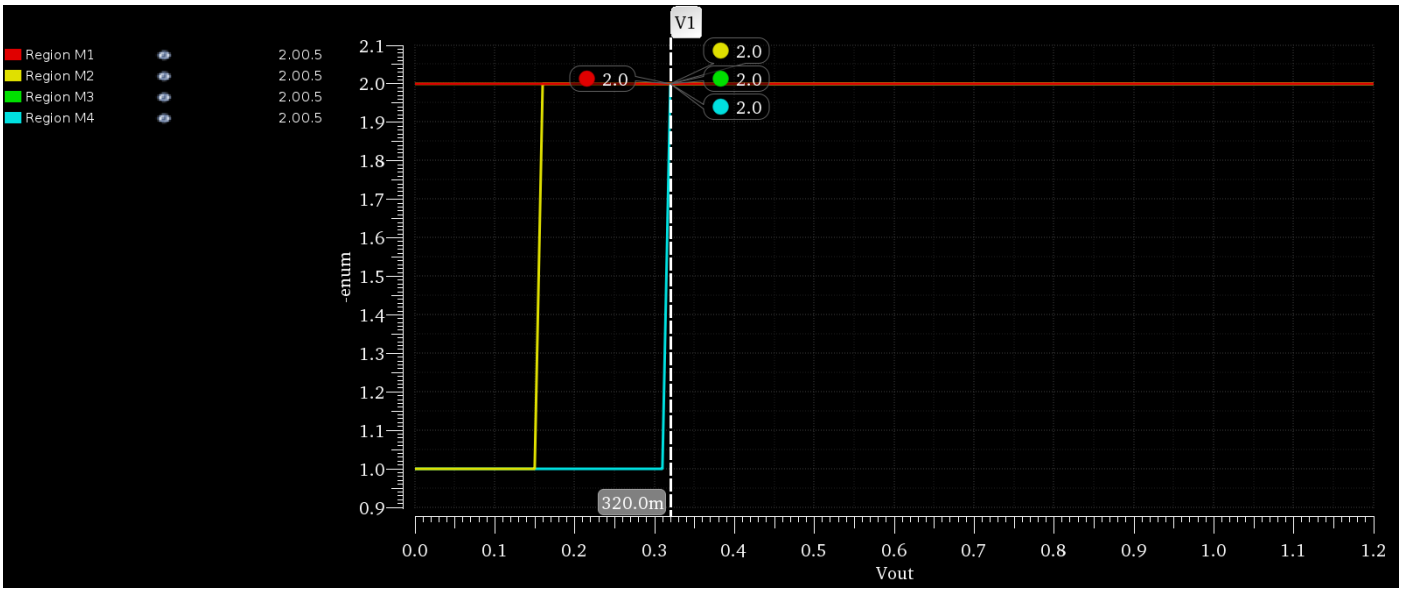
Note: In Cadence Region Parameters: -

(Cut off → 0 , Triode → 1 , Saturation → 2 , Subthreshold → 3 , Breakdown → 4)

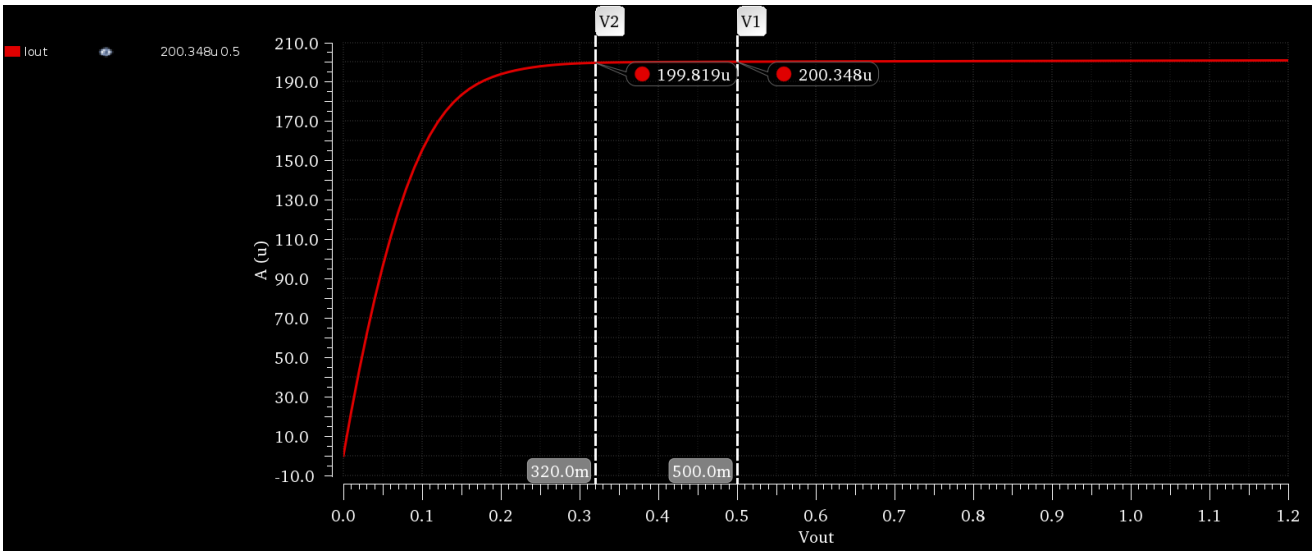
③ Simulation results to verify I_{out} and R_{out} specifications.

Q3

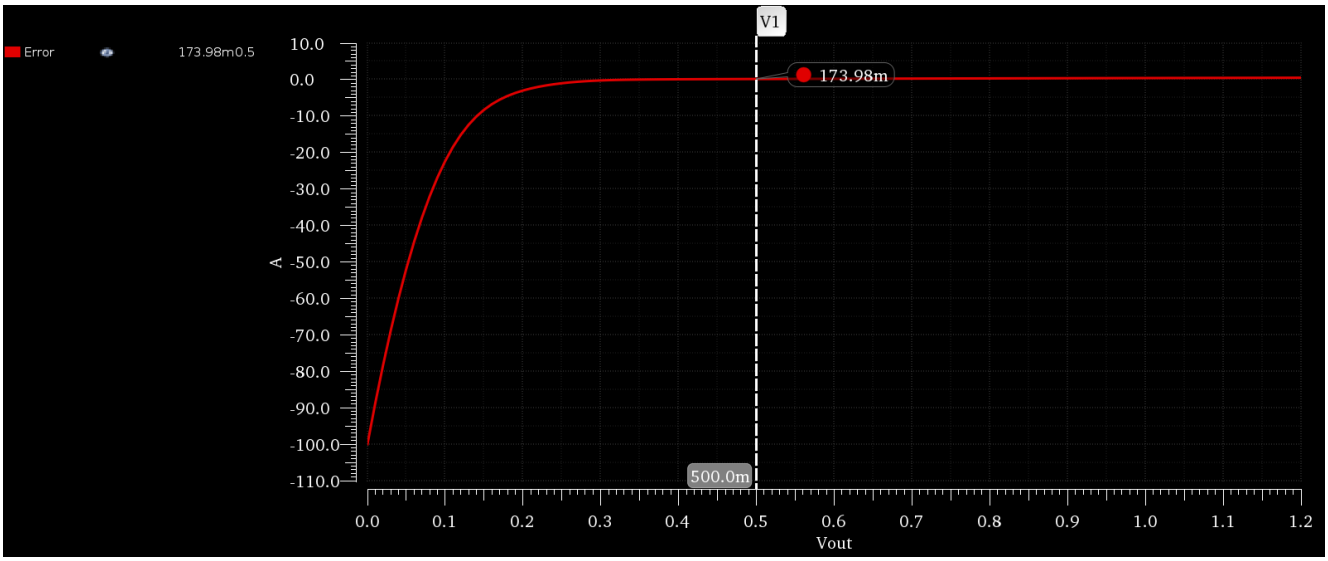
- V_{Comp} (Compliance Voltage): 320 mV.



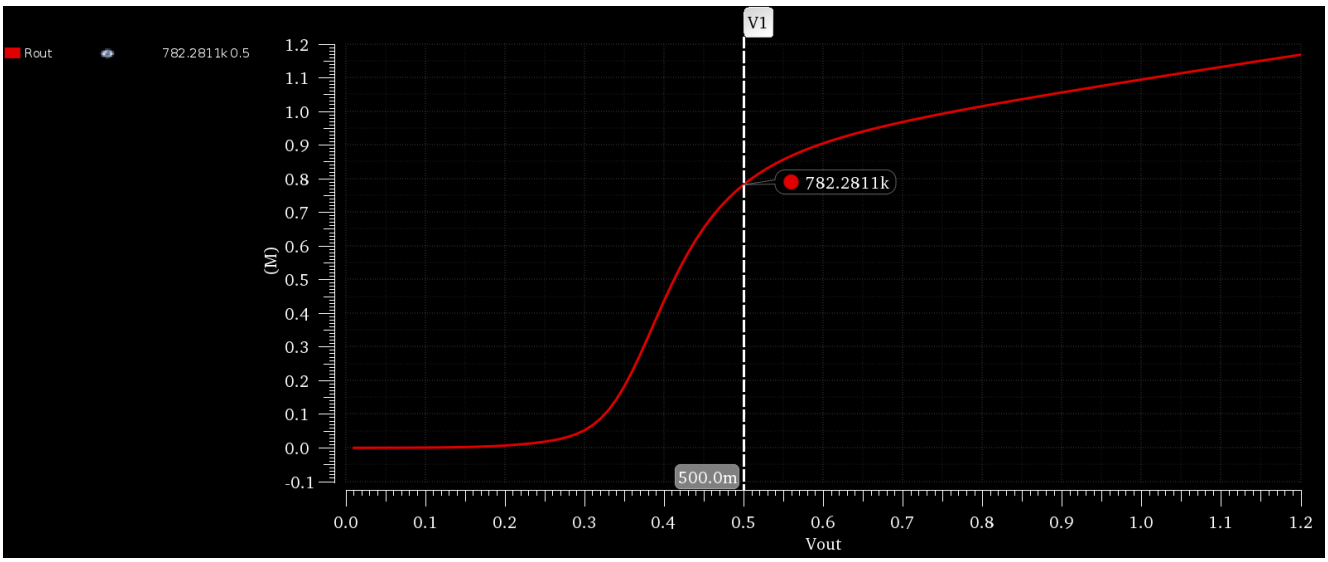
- I_{out} (Output Current): 200.297 µA.



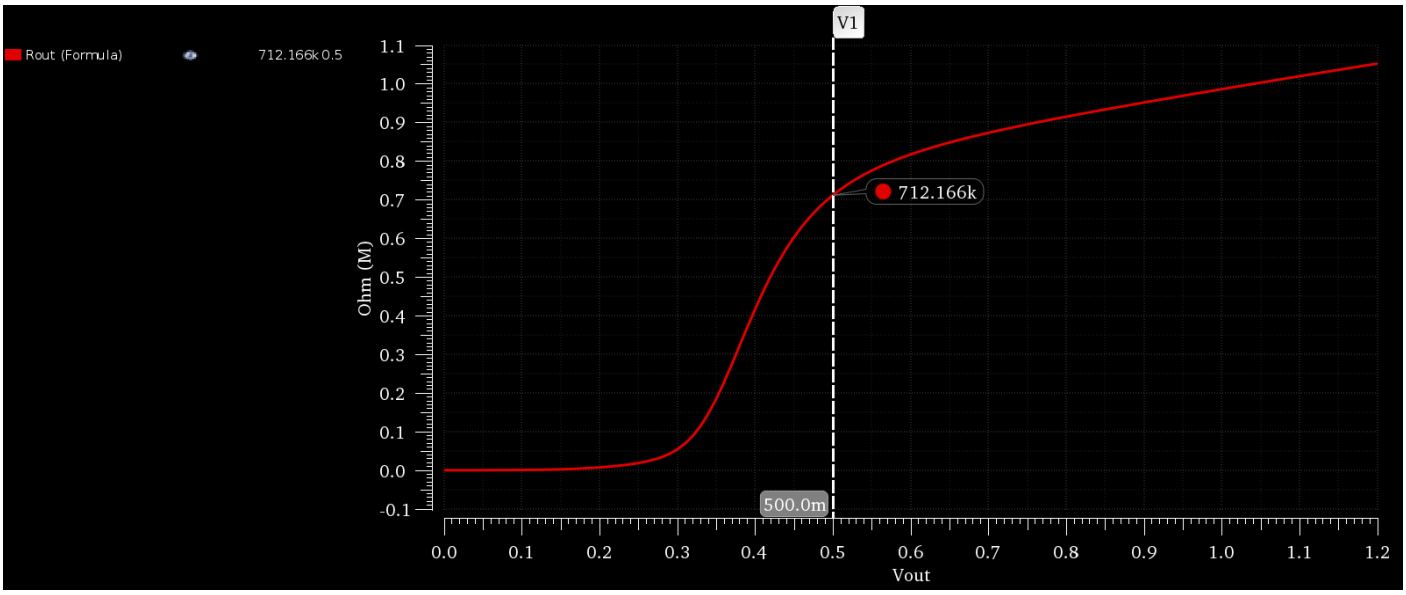
- $\text{Error} = \frac{I_{out}-2I_{ref}}{2I_{ref}} * 100\ \% = 0.173\ \%$ @ $V_{out} = 500$ mV.



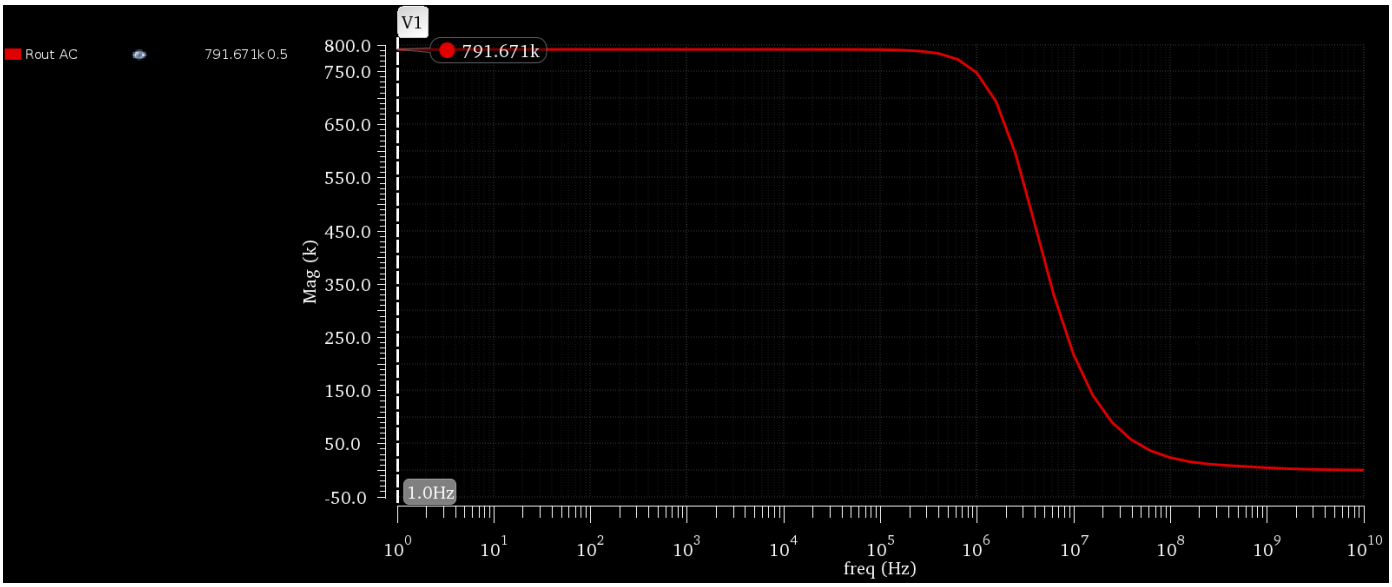
- $R_{out} = 1/\text{slope} = 1/\text{deriv}(I_D \text{ for } M_4)$ for Sweep on $V_{out} = 782.28$ kΩ.



- $R_{out} = r_{o_4} + r_{o_2} + g_{m_4}.r_{o_2}.r_{o_4} = 712.166\ k\Omega.$



- R_{out} From AC Analysis $= VF('V_{out}')/IF('I_{out}') = 791.67\ k\Omega.$

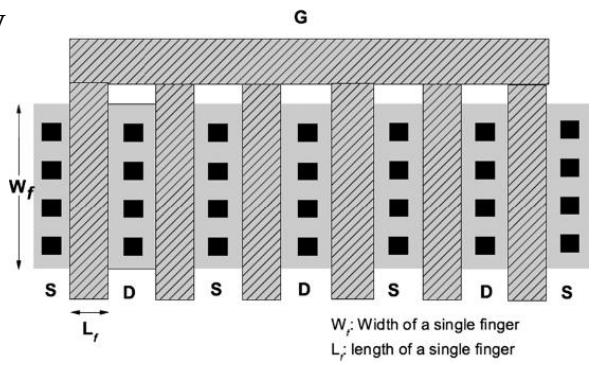


Specs. @ $V_{out} = 500$ mV	Required	Achieved
V_{comp}	≤ 350 mV.	320 mV.
Error	< 1 %	0.173 %
R_{out}	$\geq 500\ k\Omega$	$782.28\ k\Omega$

Q4

④ An estimate of this mirror's area.

- Total Area $= (\sum_{i=1}^{4} W_i * L_i)_{\text{for Transistors}} + (W * L)_{\text{for poly resistor}}$
  Area $= 2 * 48.8\mu * 700n + 2 * 24.4\mu * 700n + 1\mu * 8.35\mu = 110.83\ (\mu m)^2$
- This Area is Not Accurate but Changed Slightly as W & L used for Transistors are the Effective Lengths not the Real Values Got from the Real Layout but it Approach to it.
- $A_{effictive_{simulation}} < A_{Layout}$
  Hint: I am not going to get into the layout design since it is not the required design scope.



Q5

⑤ If your manager told you the area you ended up with is too large and you need to sacrifice one of the specs to have reasonable area, suggest a modification and comment on what you'll gain and lose from it. (g_m/I_D Methodology Charts point of View Look at Page 10).

- As Shown in the Table Below got From Simulations by Preserving the V_{Comp} Value & $R_{poly\ Resistor} = 2.2\ k\Omega + R_{size}$, R_{out} Will Decrease, and All Transistors are in SAT Region.
- Sacrifice: I Scarify with R_{out} As When Decreasing L & W Area will Decrease and R_{out} will Decrease Preserving the same Current Density (I/W), g_m/I_D Value & V_{comp}.
- Gain: Area Reduced to max 75 % From its initial Value, Preserve $V_{comp} \geq 350$ mV,
  And also Gain High Swing Accurate Current Mirror as R_{out} Decrease.
- Lose: R_{out} Value Decrease and Stability for the Circuit Decrease as R_{out} Decrease.
- Note: From Task 1 Figure (1.1) As L Decrease V_{th} Increase which can provide better noise margin and immunity (Gain).
- Reason for Sacrifice: The decreasing output resistance (Rout) is due to the channel-length modulation effect, the Big Drop in Size (W/L) Ratio of Transistors, parasitic capacitances, and threshold voltage variations.

From g_m/I_D Methodology We Choose Values for L & W From $W_{for\ M_4\ \&\ M_2}$ Charts in Page 10							
# iteration	L (m)	W (m)	R_{out} (kΩ)	V_{comp} (mV)	Error %	$Area_{total}$	% Area Decreasing
1	700n	48.8 µ	782.28	320	0.173	110.83	My Design
2	500n	34.4 µ	560.205	320	0.185	59.95	45.908
3	300n	20.4 µ	332.586	320	0.203	26.71	75.9
Result	Decrease	Decrease	Decrease	No Change	Small Variation	Decrease	Increase
Sacrify	–	–	Yes	No	No	Gain	Gain

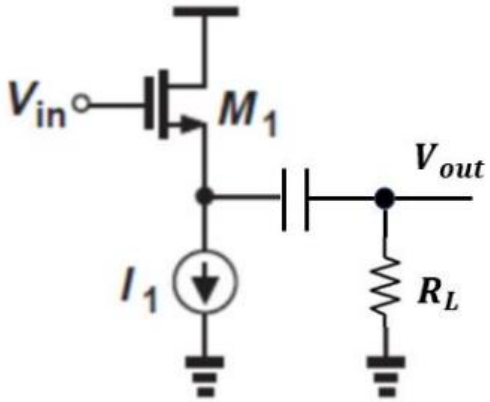
Task 3

TASK 3

Power Amplifier

USING TUNING METHODOLOGY

- Use the NMOS core high voltage RF transistor (N_33_RF) , an ideal current source, and an ideal DC blocking cap of 1µF to design a class A Power Amplifier (according to the architecture shown) operating at $V_{DD} = 3.3V$ with the following specifications:
- $V_{in,DC} = 2.3$ V.
- $V_{in,AC} = A\sin(2\pi ft)$, $f = 50$ MHZ, $A = 1$ V.
- $R_L = 50\ \Omega$, $|V_{out,peak}| > 650$ mV.
- Output Signal Linearity is Characterized as $\frac{|V_{out,max}| - |V_{out,min}|}{V_{out,max}} < 5\ \%$



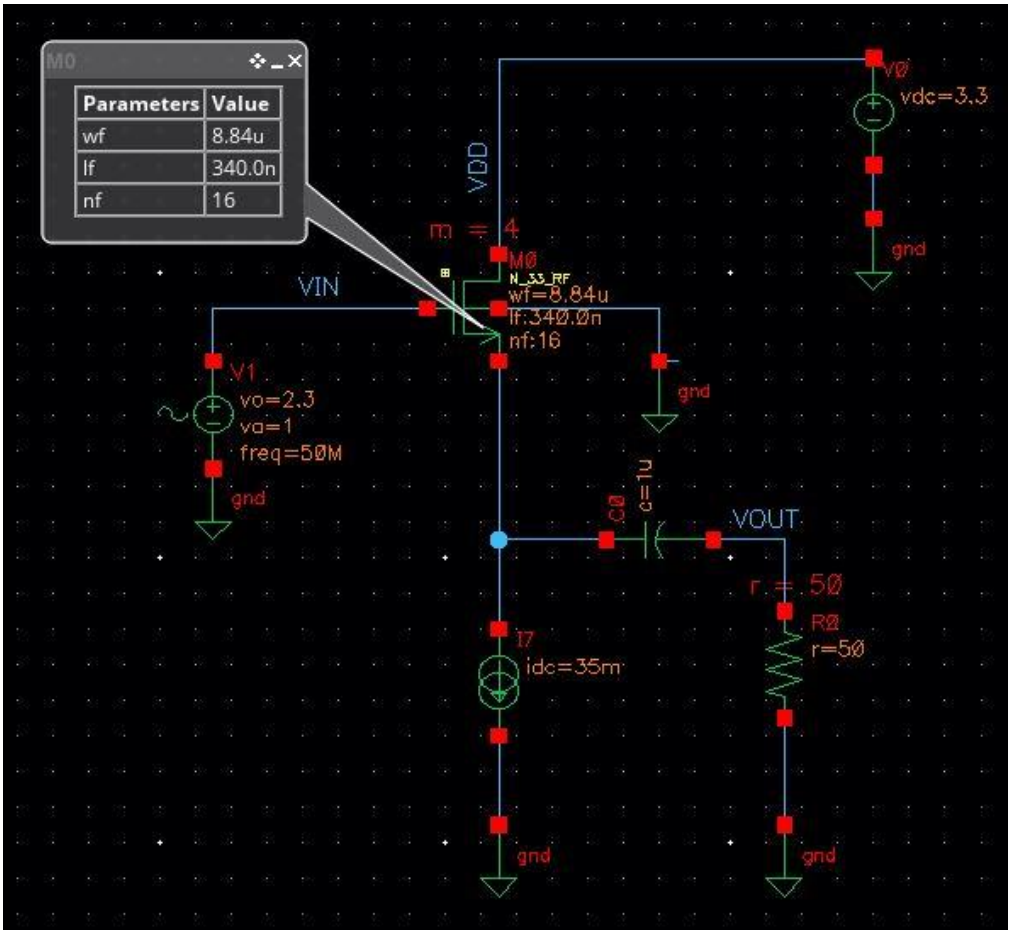
Design Steps: -

- Doing Transient Analysis by Sweeping on the Ratio (W/L)
- Sweep on DC Current From it Get Point that Achieve All the Specs.

Test	Name	Type	Details	EvalType	Plot	Save	Spec
First...	VoutMin	expr	ymin(VT("/VOUT"))	point	☑	☐	
First...	VoutPeak	expr	ymax(VT("/VOUT"))	point	☑	☐	
First...	Vout	expr	VT("/VOUT")	point	☑	☐	
First...	Vs	expr	VT("/net04")	point	☑	☐	
First...	VDS	expr	v("M0:vds" ?result "tran")	point	☑	☐	
First...	IL	expr	IT("/R0/PLUS")	point	☑	☐	
First...		expr	IT("/M2/D")	point	☑	☐	
First...	Id	expr	getData("M0:id" ?result "tran")	point	☑	☐	
First...	gm	expr	getData("M0:gm" ?result "tran")	point	☑	☐	
First...		signal	/R0/PLUS	point	☐	☑	
First...		signal	/M2/D	point	☐	☑	
First...	PLoad	expr	(rms(IL) * rms(IL) * 50)	point	☑	☐	
First...	Pdc	expr	(average(Id) * 3.3)	point	☑	☐	
First...	Efficiency	expr	((PLoad / Pdc) * 100)	point	☑	☐	
First...	Linearity	expr	(((VoutPeak + VoutMin) / VoutPeak) * 100)	point	☑	☐	

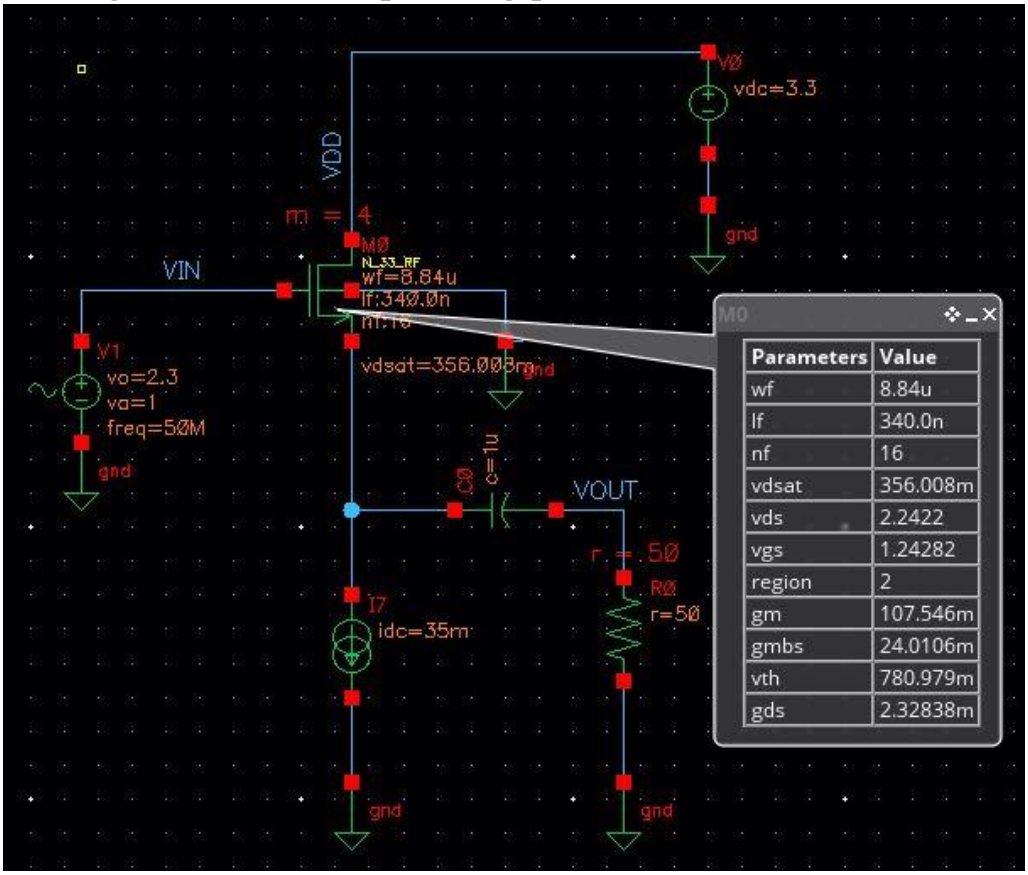
① Schematic diagram with dimensions and component values annotated.

Q1



② Schematic diagram with DC operating point annotated.

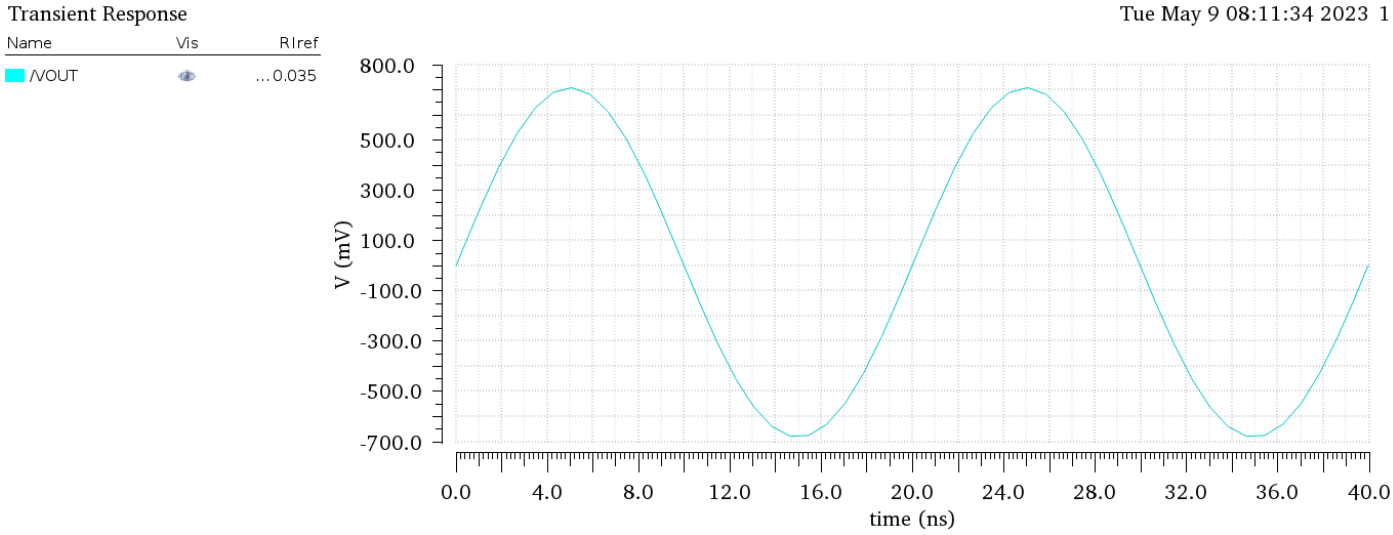
Q2

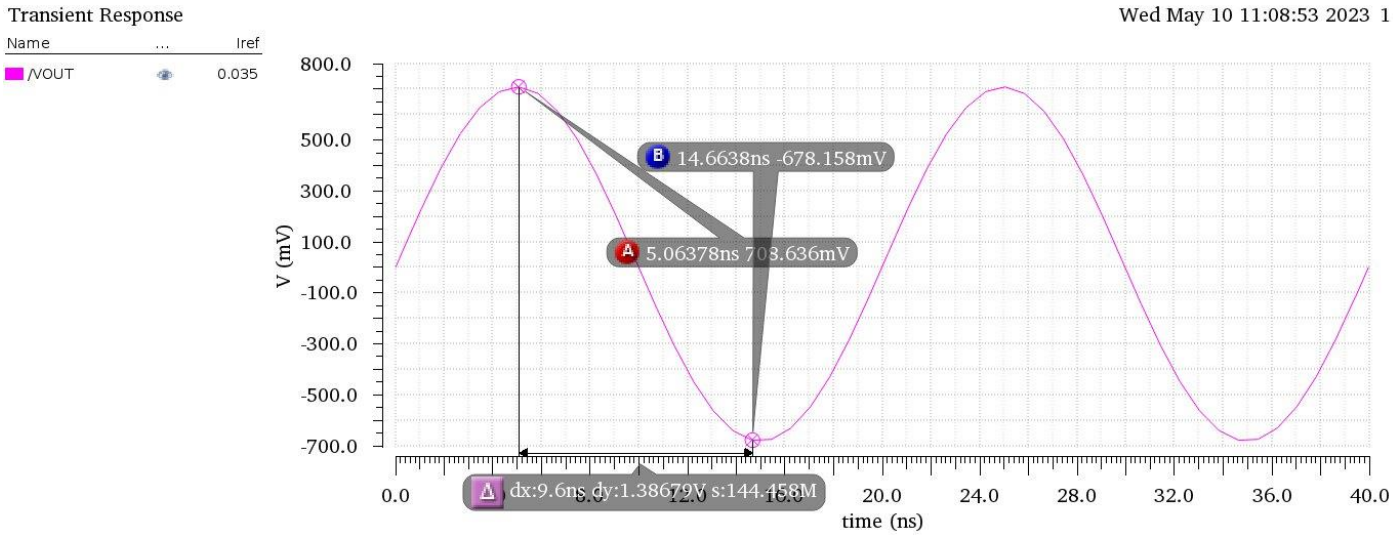


③ Transient simulation results to verify the required specifications:

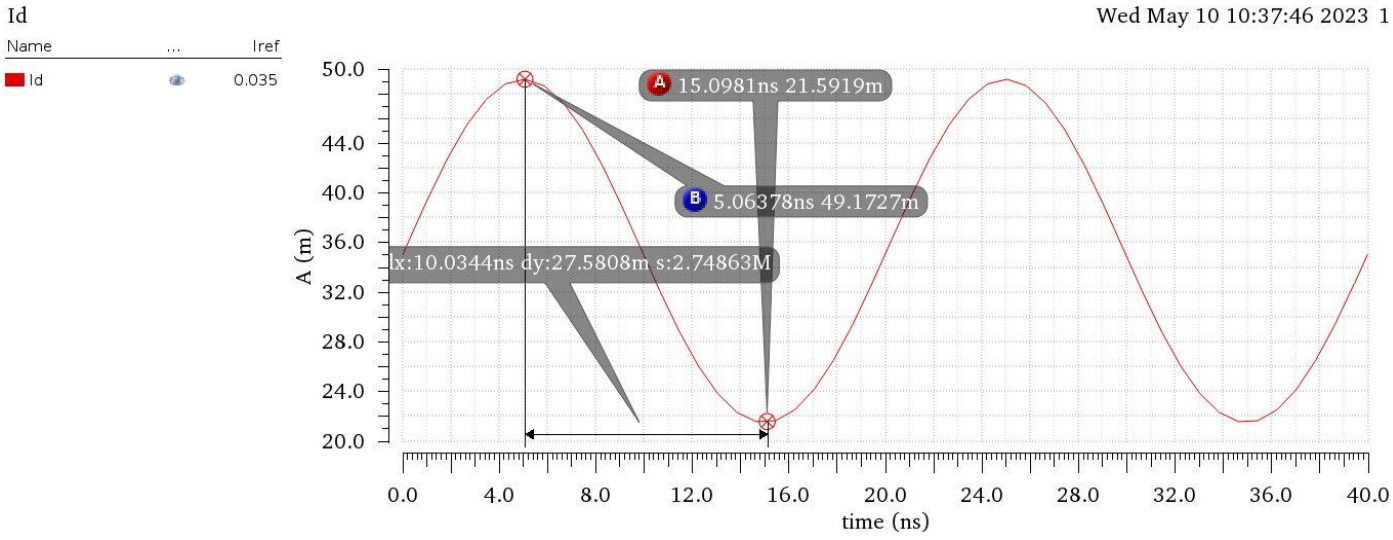
Q3

a) Plot a complete period of V_{out} vs time at the given frequency.





b) Plot a complete period of the current flowing in the main device to make sure the device doesn't turn off as (The Total Current in +ve Part).



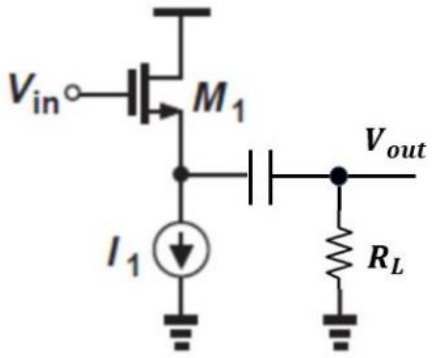
Parameters: R=26, Iref=35m						
16	First_PROJECT:Power_Amplifier2:1	Vout				
16	First_PROJECT:Power_Amplifier2:1	VoutPeak	708.6m			
16	First_PROJECT:Power_Amplifier2:1	VoutMin	-678.2m			
16	First_PROJECT:Power_Amplifier2:1	Linearity	4.301			
16	First_PROJECT:Power_Amplifier2:1	Efficiency	4.174			
16	First_PROJECT:Power_Amplifier2:1	gm				
16	First_PROJECT:Power_Amplifier2:1	VDS				
16	First_PROJECT:Power_Amplifier2:1	Id				
16	First_PROJECT:Power_Amplifier2:1	IL				
16	First_PROJECT:Power_Amplifier2:1	Pdc	116.1m			
16	First_PROJECT:Power_Amplifier2:1	PLoad	4.845m			
16	First_PROJECT:Power_Amplifier2:1	Vs				
16	First_PROJECT:Power_Amplifier2:1	/R0/PLUS				

Specs.	Required	Achieved
$\lvert V_{out,max} \rvert$	$\geq$ 650 mV.	708.6 mV.
$\lvert V_{out,min} \rvert$	$\geq$ 650 mV.	678.2 mV.
Linearity Error	$\leq$ 5 %	4.301

Q4

④ Calculation of the efficiency using simulations and compare it with the theoretical equation.

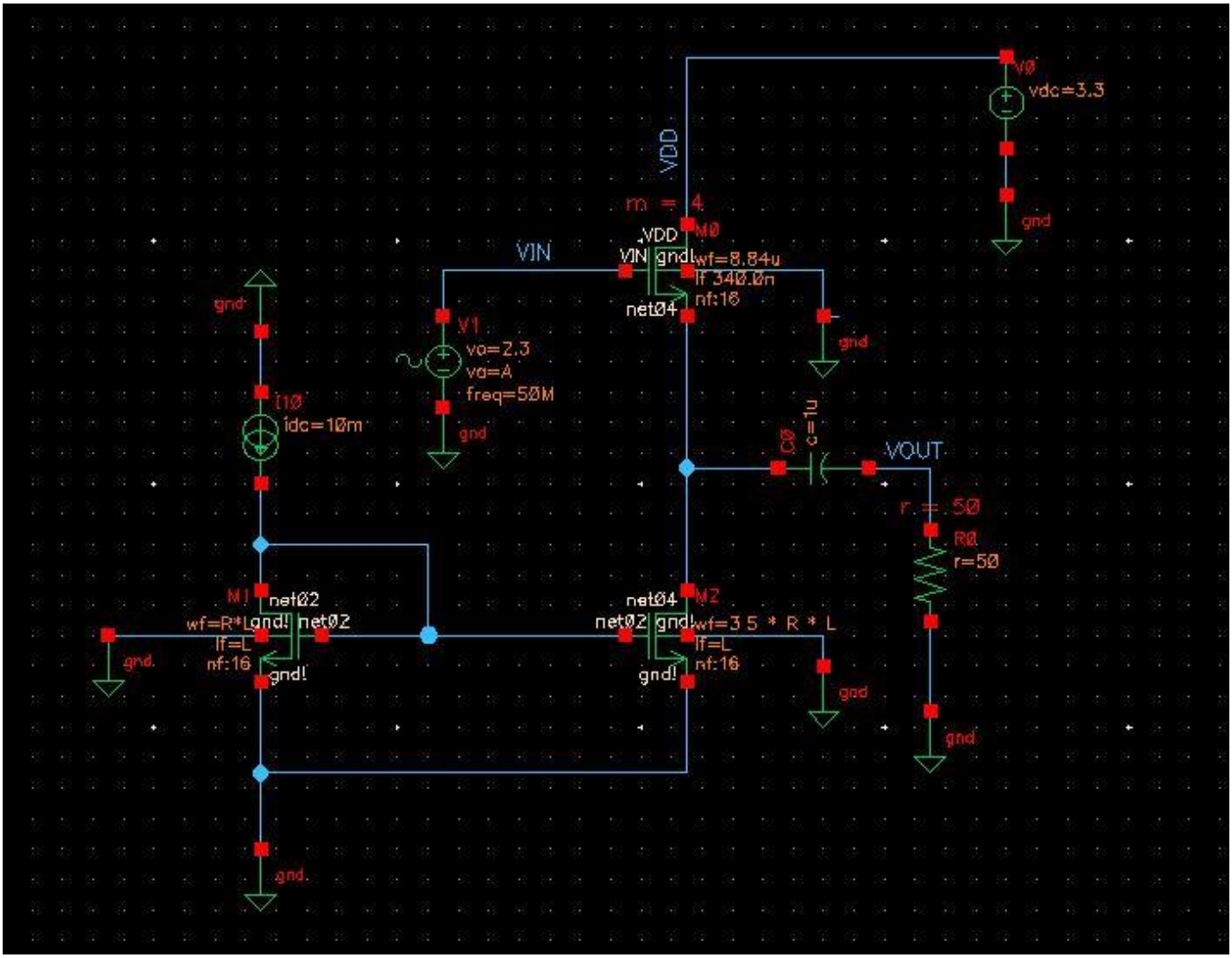
- Efficiency $(\eta)_{Simulations} = 4.174$
- Hand Analysis:
- $V_{in}(t) = 2.3 + \sin(2\pi ft)$, $f = 50$ MHZ.
  $\because R_l = 50\ \Omega$, $I_D = 35$ mV , $V_{CC} = 3.3$ V
  $V_{out,Peak} = 708.6$ mV
- It's a Class A power Amplifier.
- $(\eta)_{Theoretical} = \frac{(V_{out,peak})^2}{2\, R_L . V_{CC} . I_D} * 100\ \% = 4.3473\ \%$



⑤ Replace the ideal current source with a current mirror with $I_{REF} = 10$ mA using N_33_RF device, design the mirror using a suitable topology of your choice, and plot V_{out} and $I_{main\ device}$. Did the linearity degrade? Why/why not?

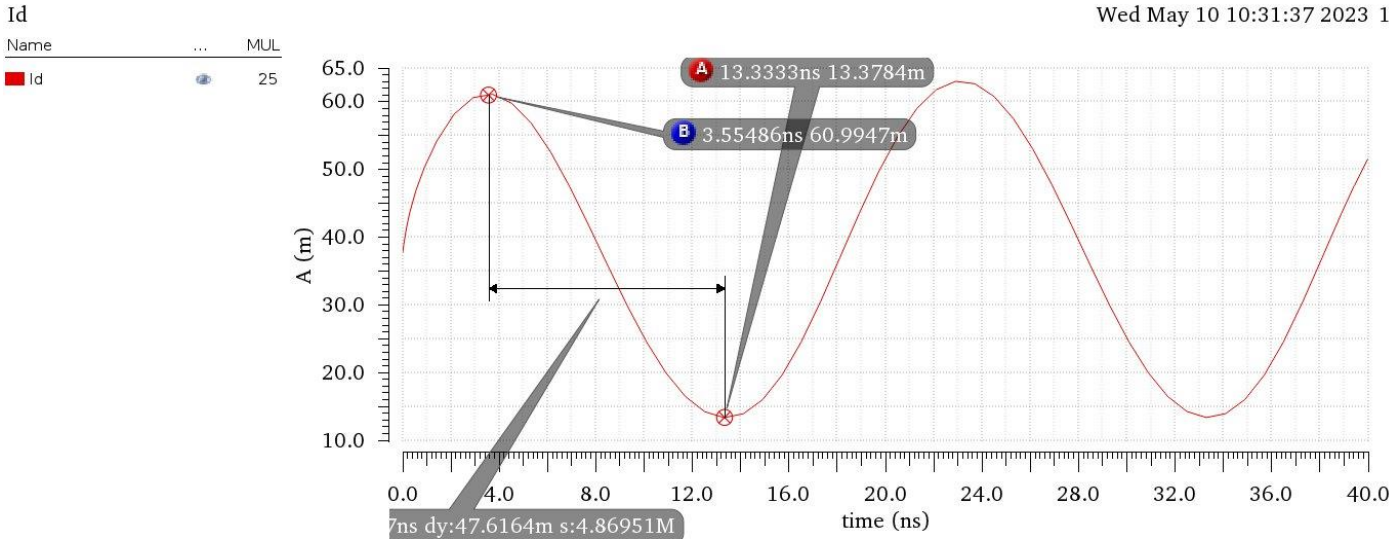
Q5

→ Regarding the replacement of the ideal current source with mirroring circuit, we have simply used the simplest mirroring circuit topology to mirror a current of value I = 35 mA, so the design of mirroring circuit was as following: A diode connected transistor with a V_{DD} connected to its drain and another transistor with a size equal to 3.5 the size of the diode connected transistor with a ground connected to the source of both the transistors, And both transistors are connected through their gates.

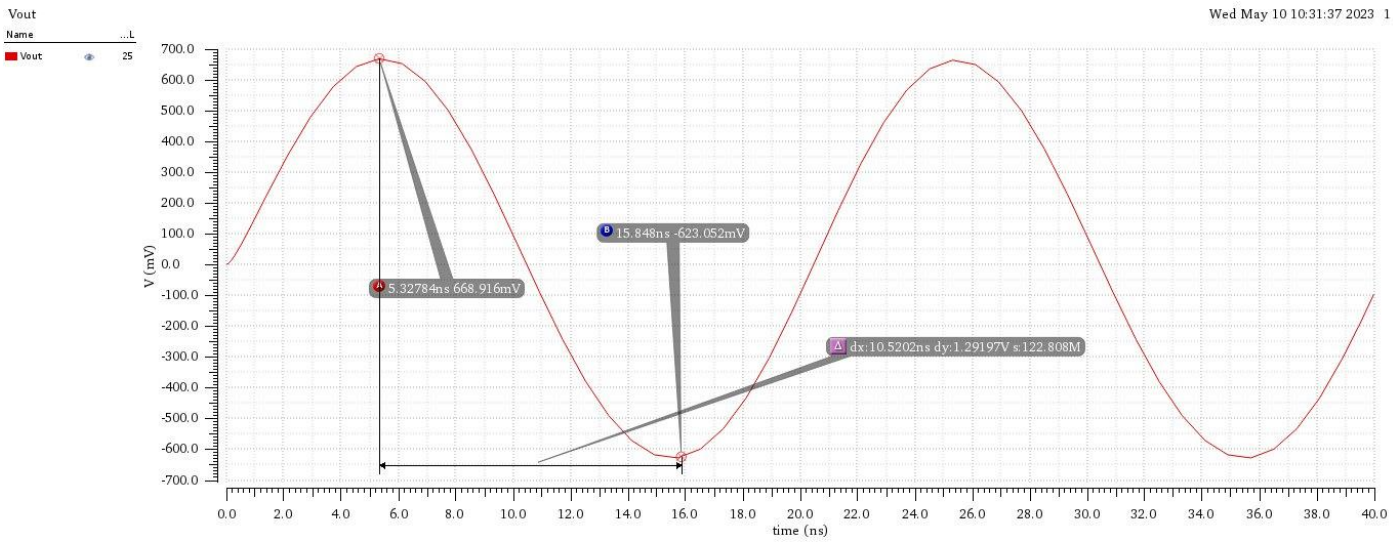


First_PROJECT:With_CS_Final:1	Vout				
First_PROJECT:With_CS_Final:1	VoutPeak	668.9m			
First_PROJECT:With_CS_Final:1	VoutMin	-626.6m			
First_PROJECT:With_CS_Final:1	Linearity	6.319			
First_PROJECT:With_CS_Final:1	Efficiency	3.408			
First_PROJECT:With_CS_Final:1	gm				
First_PROJECT:With_CS_Final:1	VDS				
First_PROJECT:With_CS_Final:1	Id				
First_PROJECT:With_CS_Final:1	IL				
First_PROJECT:With_CS_Final:1	Pdc	123.8m			
First_PROJECT:With_CS_Final:1	PLoad	4.219m			
First_PROJECT:With_CS_Final:1	Vs				
First_PROJECT:With_CS_Final:1	/R0/PLUS				
First_PROJECT:With_CS_Final:1	IT("/M2/D")				
First_PROJECT:With_CS_Final:1	/M2/D				

Plot $I_{main\ device}$



Plot V_{out}



⑥ Did the linearity degrade? Why/why not?

Q6

- Yes, linearity has degraded.
- Because after replacing the ideal current source with a non-ideal mirroring circuit, V_{out} became variable with the current coming out from the mirroring circuit in addition $V_{out,min}$ decreased and g_m will change then the error increased as Error $= \frac{|V_{out,max}|-|V_{out,min}|}{V_{out,max}}$, So Linearity is Degraded.

  $Error_{Before\ CM} = 4.301\ \%$, $Error_{After\ CM} = 6.319\ \%$

Specs.	V_{out}	$I_{main\ Device}$
$\lvert V_{out,max}\rvert$	668.916 mV.	60.9947 mA.
$\lvert V_{out,min}\rvert$	623.052 mV.	13.3784 mA.

The END Thank You