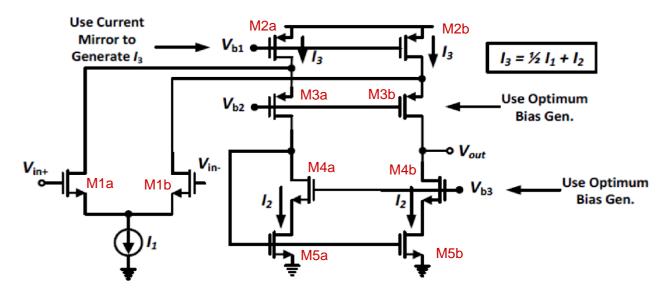


Third Year 2023/2024 Electronics Project ELC3060

# **CMOS Operational Amplifier Design**

#### I. Design

The purpose of this project is to design and simulate a folded-cascode operational amplifier used as a buffer.



## II. Specifications

You are required to design the single-ended single-stage op-amp shown such that:

- $V_{DD}$  = 3.3V (use **HG devices** with thick oxide and thus will not breakdown for high voltage)
- $V_{\text{inCM}} = V_{\text{DD}}/2$  (input common-mode voltage = 1.65V)
- $A_{DC} > 55$  dB (DC differential gain)
- GBW > 100 MHz for a load capacitance of  $C_L$ =2pF
- Slew Rate  $> 100 \text{ V/}\mu\text{sec}$
- Output Swing  $> 1.5 V_{pp}$  (Definition of swing is when the DC-gain drops by 10dB)
- Input referred thermal noise density  $< 10nV/\sqrt{Hz}$  (Ignore 1/f noise)
- $PM > 60^{\circ}$
- Minimize power consumption
- Do not use ideal current sources (assume that you have only one ideal current source of  $25\mu A$  coming from  $V_{DD}$ ). Use biasing circuit to generate  $I_1$  and optimum bias for  $V_{b1}$ ,  $V_{b2}$ , and  $V_{b3}$ .
- Design all current mirrors to provide close to optimum compliance voltage (to obtain maximum output swing). BUT Adjust  $V_{DS}$  of any transistor in the current mirror (or current source) to  $(V_{\text{eff}} + 100 \text{mV})$  in order to improve  $r_o$  of this transistor.

### III. Simulations

- Simulate the circuit (DC analysis save operating point, AC analysis)
  - Print all transistor operating point information (DC)
  - Plot the gain and phase versus frequency (AC). Show open-loop gain and PM
  - Plot the common-mode rejection ratio (CMRR)
  - Plot the power supply rejection ratio (PSRR)
- Place the op-amp in a unity feedback (**Buffer**) configuration:
  - Simulate stability using STB analysis and IPROBE
  - Plot STB gain and phase versus frequency (AC) and calculate open-loop gain and PM What is the difference between those results and previous open-loop AC results?
  - Plot the DC-gain versus  $V_{\text{out}}$  (report when DC-gain drops by 10dB to verify specifications) Plot closed-loop (CL) frequency response. What is the  $A_{\text{CL}}$  and  $BW_{\text{CL}}$  (comment)?
  - Simulate input-referred noise and tabulate top 4 contributors @10MHz (comment).
  - Simulate the slew rate and verify the specifications.
  - Apply a sine input signal of  $1V_{pp}$  @  $10 \, MHz$  and plot  $V_{out}$  (Add proper input DC value). Plot DFT (in dB) and calculate harmonic distortion (HD2, HD3, and THD) in dB.
  - Plot V<sub>out</sub> for a small step input of 100mV (Add proper input DC value). Calculate the fractional gain error (FGE) and 1% settling time (compare with hand analysis).

### IV. Assessment

#### This project should be done by groups of $\underline{5}$ students

You are required to deliver a report that contains:

- 1- **Schematic diagrams** (snapshots from Cadence showing dimensions and values)
- 2- **Design procedure** (hand calculations)
- 3- **Simulation results** (snapshots from Cadence)
- 4- **Discussion** of your results and conclusions

Any missing item from the **4 items above will be penalized in the report grading.** Please be aware that 'bad' presentation (report document, figures...etc.) of your work is going to affect your grade.

- You should provide the required simulations using **CADENCE**.
- Deadline to submit the project report is Sunday (5 May 2024) 11:59 pm
- Any copied reports will be given Zero.
- All the equations derivations should be written in **WORD**.
- Project submission will be by submitting a **PDF file** uploaded to google classroom
- The cover page must contain the group names in **Arabic** and their **ID's**.
- All graphs and figures should be clear with readable axes and traces.
- If the students participating in the project ID's are: 9202293, 9202162, 9202038, 9202125 & 9202136 then the report name should be "9202293\_9202162\_9202038\_9202125\_9202136".