Cadence Virtuoso LAB (3) Report

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Analog IC Design

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- ## Part 1: Sizing Chart

  - ✓ **Specifications Achievement: (10 Points)**
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    - P2: Specs Declaration (L, V^*, Current and Supply Voltage).
    - P3: The Last variable in the design is to calculate $W = 10\ \mu m$.
    - P4: Sweeping V_{GS} and set $V_{DS} = \frac{V_{DD}}{2}$
    - P5: $V^* = \frac{2I_D}{g_m}$ & $V_{ov} = V_{GS} - V_{TH}$ on Calculator.
    - P6: Plot V^* and V_{ov} Overlaid Vs V_{GS}.
    - P7: On the V^* & V_{ov} Chart Locate V_Q^* Find V_{ov_Q} and V_{GS_Q}.
    - P8: Plot $I_D, g_m,$ and g_{ds} Vs V_{GS} Find I_{D_X}, g_{m_X} & g_{ds_X} @ V_{GS_Q}.
    - P9: Cross Multiplication Technique to get the required value of W.
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- ## Part 2: Cascode Amplifier For Gain

  - ✓ **Op Analysis (10 Questions)**
    - Q1: Create a new cell and schematic
      $I_B = 20\ \mu A,\ L = 0.5\ \mu m,\ C_L = 1\ pF, W_{part\ 1}$.
    - Q2: Choose V_B @ $V_{DS} \approx V^* + 100\ mV$.
    - Q3: feedback loop and resistors with different resistances DC/AC.
    - Q4: Simulate the DC OP point of CS and cascode amplifiers.
    - Q5: Check that all transistors operate in saturation.
    - Q6: Do all transistors have the same V_{th}? Why?
    - Q7: What is the relation ($\ll, <, =, >, \gg$) between g_m and g_{ds}?
    - Q8: What is the relation ($\ll, <, =, >, \gg$) between g_m and g_{mb}?
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  - ✓ **AC Analysis (6 Questions)**
    - Q1: Create a new simulation configuration.
    - Q2: Use calculator to create parameters (DC gain, BW, GBW, UGF).
    - Q3: Report the Bode plot (magnitude) of CS and cascode.
    - Q4: hand analysis to calculate (DC gain, BW, GBW, UGF).
    - Q5: Report a table comparing the (DC gain, BW, GBW, UGF).
    - Q6: Comment on the results.

Cascode Amplifier

Part 1

Sizing Chart

P1: Intrinsic Gain of a MOSFET.

→ Square Law.

$$\left|A_{v_o}\right| \approx g_m r_o = \frac{2I_D}{V_{ov}} \times \frac{V_A}{I_D} = \frac{2V_A}{V_{ov}} \rightarrow \text{We used } g_m = \frac{2I_D}{V_{ov}}, V_{ov} = \frac{2I_D}{g_m}$$

$$V^* = V_{ov}$$

→ For Real MOSFET.

$$V_{ov} \neq \frac{2I_D}{g_m} \rightarrow \text{Define } V^* = \frac{2I_D}{g_m} \Leftrightarrow g_m = \frac{2I_D}{V^*}, \left|A_{v_o}\right| \approx \frac{2V_A}{V^*}$$

P2: **Specs (Specifications)**

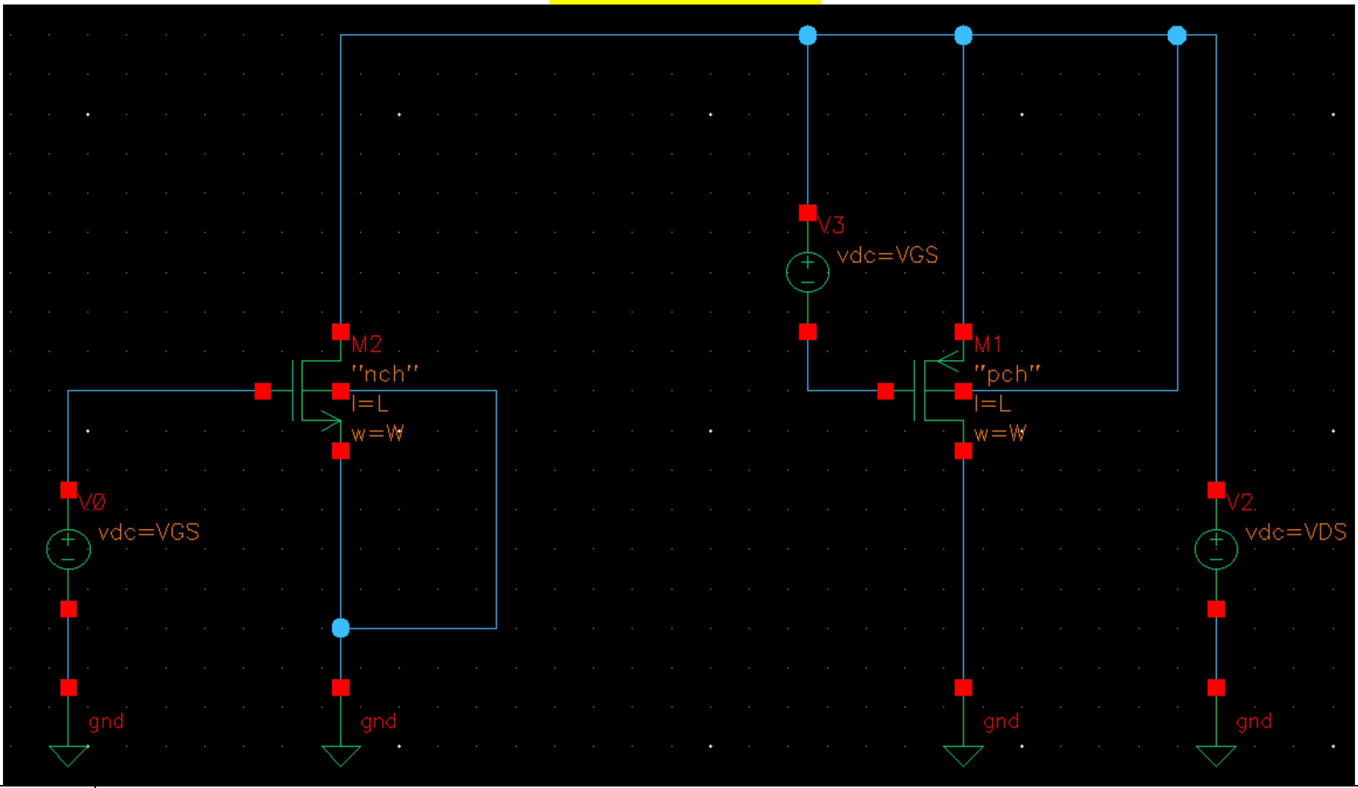
We want to design CS and cascode amplifiers with the parameters below.

Parameters	$0.18\ \mu m$ CMOS
L	$0.5\ \mu m$
V^*	$160\ mV$
Supply (V_{DD})	$1.8\ V$
Current Consumption (I_D)	$15\ \mu A.$

P3:

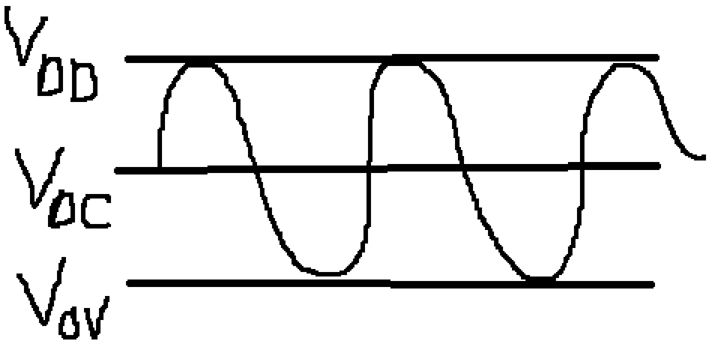
The remaining variable in the design is to calculate W.
Since the square-law is not accurate, we cannot use it to determine the sizing. Instead, we will use a sizing chart generated from simulation.
Create a testbench for NMOS transistor as shown below
(we will use NMOS only in this lab). Use $W = 10\ \mu m$
(we will understand why shortly) and $L = 0.5\ \mu m$
(the same L selected before).

Schematic

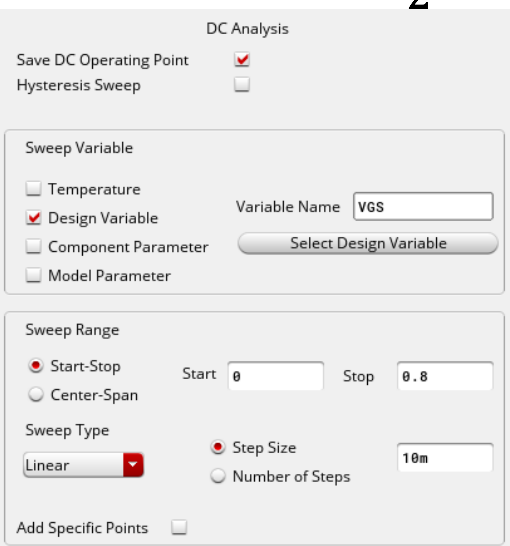


P4

Sweep V_{GS} from 0 to $\approx V_{TH} + 0.4V = 0.8$ with 10 mV step. Set $V_{DS} = \frac{V_{DD}}{2}$.



$$V_{DC} = \frac{V_{DD}}{2} = V_{CM_O} = V_{DS}$$



P5

We want to compare $V^* = \frac{2I_D}{g_m}$ and $V_{ov} = V_{GS} - V_{TH}$ by plotting them overlaid. Use the calculator to create expressions for V^* and Vov .

$$V_{ov} = V_{GS} - V_{th}$$

```
v("M2:vgs" ?result "dc")-v("M2:vth" ?result "dc")
```

$$V^* = \frac{2I_D}{g_m}$$

```
2*getData("M2:id" ?result "dc")/getData("M2:gm" ?result "dc")
```

Output Setup

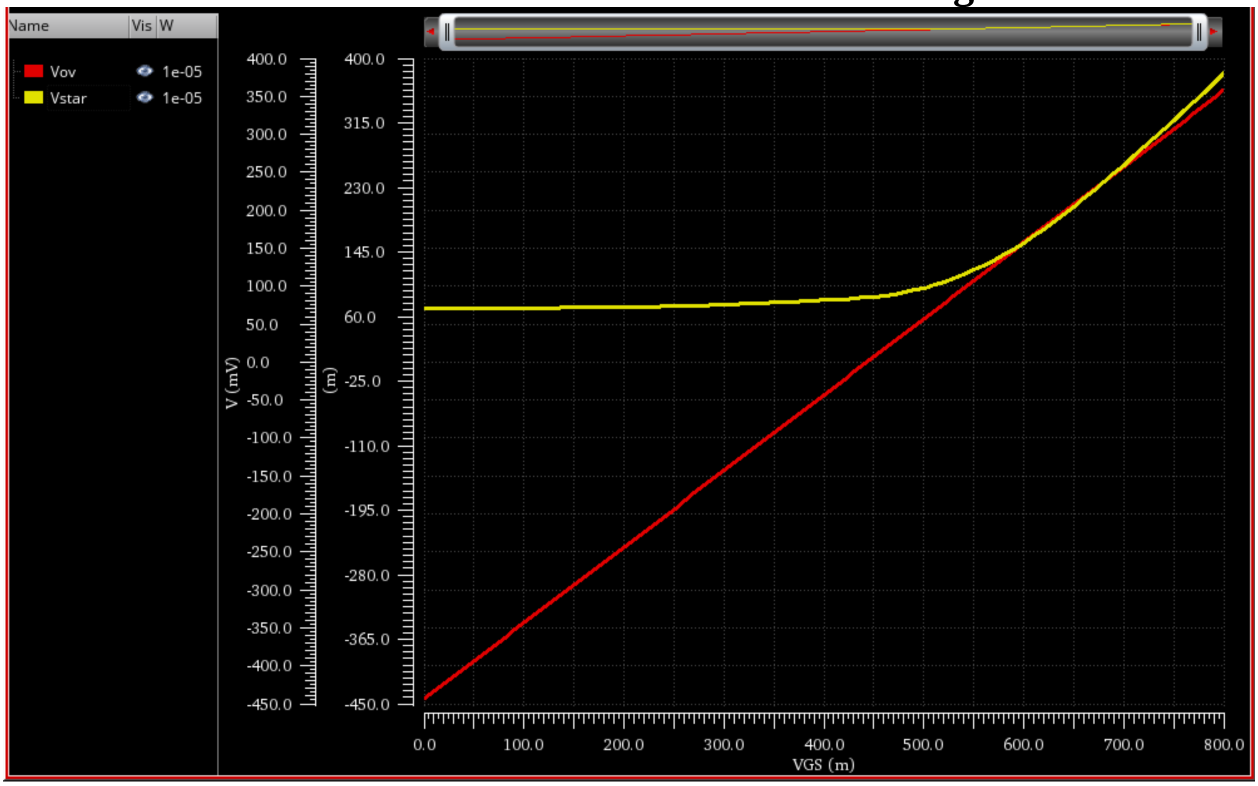
LAB_3_PART_1 × | adexl ×

Outputs Setup | Run Preview | Results | Diagnostics

Test	Name	Type	Details	EvalType	Plot	Save
IEEE_Workshop:LAB_3_PART_1:1	Vov	expr	(v("M2:vgs" ?result "dc") - v("M2:vth" ?result "dc"))	point	✓	
IEEE_Workshop:LAB_3_PART_1:1	Vstar	expr	((2 * getData("M2:id" ?result "dc")) / getData("M2:gm" ?result "dc"))	point	✓	
IEEE_Workshop:LAB_3_PART_1:1	id	expr	getData("M2:id" ?result "dc")	point	✓	
IEEE_Workshop:LAB_3_PART_1:1	gm	expr	getData("M2:gm" ?result "dc")	point	✓	
IEEE_Workshop:LAB_3_PART_1:1	gds	expr	getData("M2:gds" ?result "dc")	point	✓	

P6

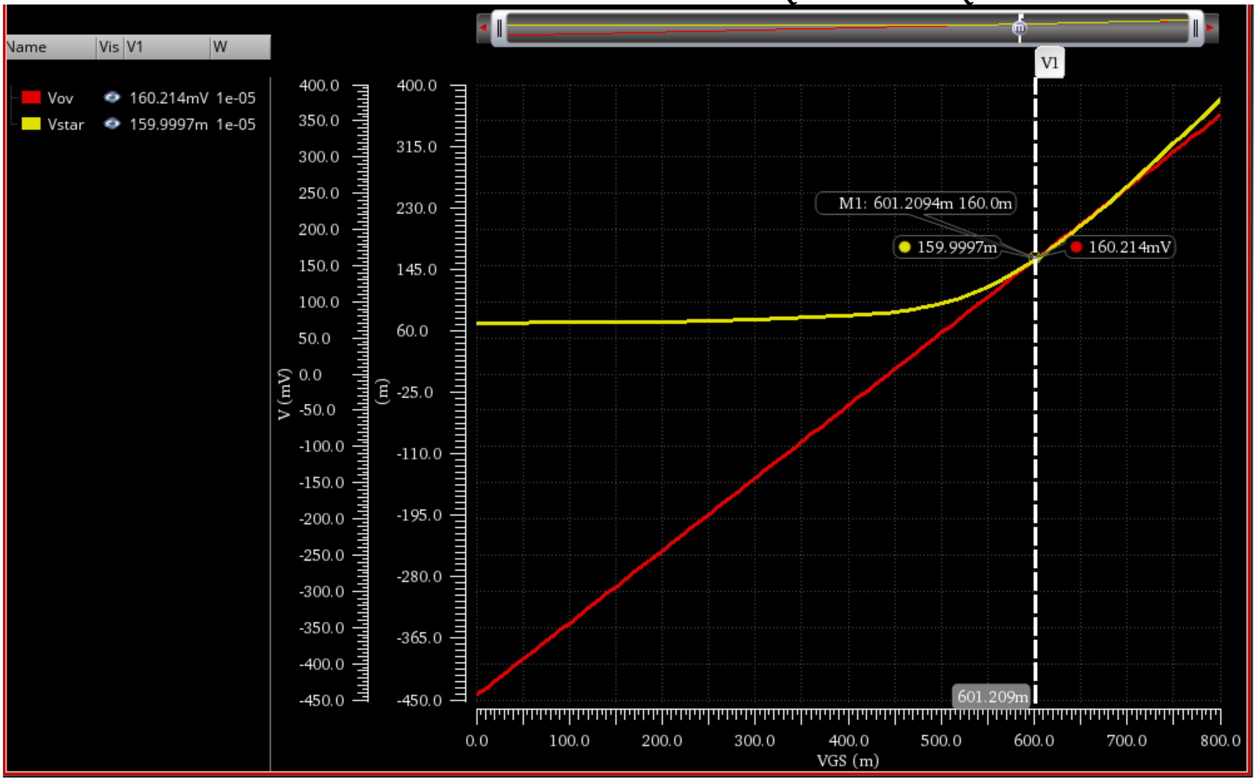
Plot V^* and V_{ov} Overlaid vs V_{GS}
Y-axis of Both Curves Has Same Range



We will notice that at the beginning of the strong inversion region, V^* and V_{ov} are relatively close to each other (i.e., square law is relatively valid). For deep strong inversion (large V_{ov}: velocity saturation and mobility degradation) or weak inversion (near-threshold and subthreshold operation) the behavior is quite far from the square law.

P7

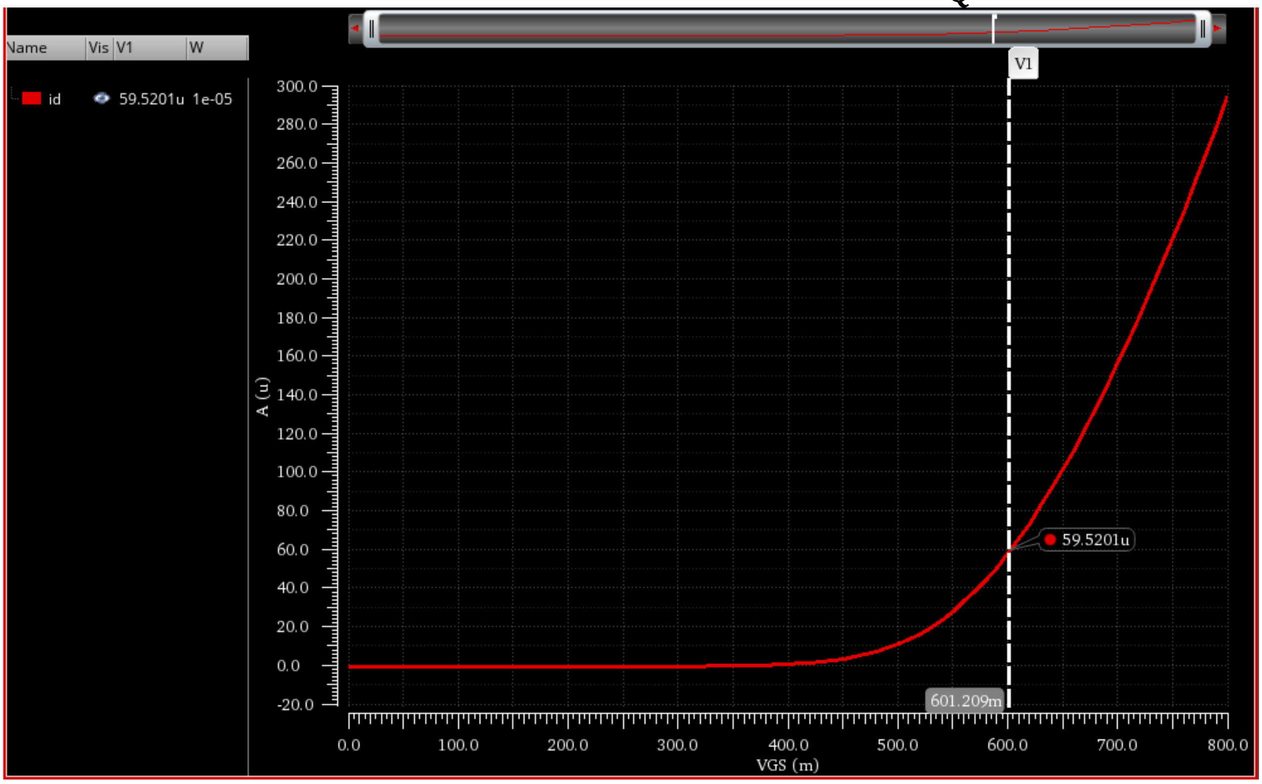
On the V^* and V_{ov} Chart Locate the Point at Which $V^* = V^*_Q$ Find the Corresponding V_{ov_Q} and V_{GS_Q}.



$$@\ V^*_Q = 160\ \text{mV} \rightarrow V_{ov_Q} = 160.214\ \text{mV}.$$
$$\rightarrow V^* = 159.9997\ \text{mV} \rightarrow V_{GS_Q} = 601.209\ \text{mV}.$$

P8

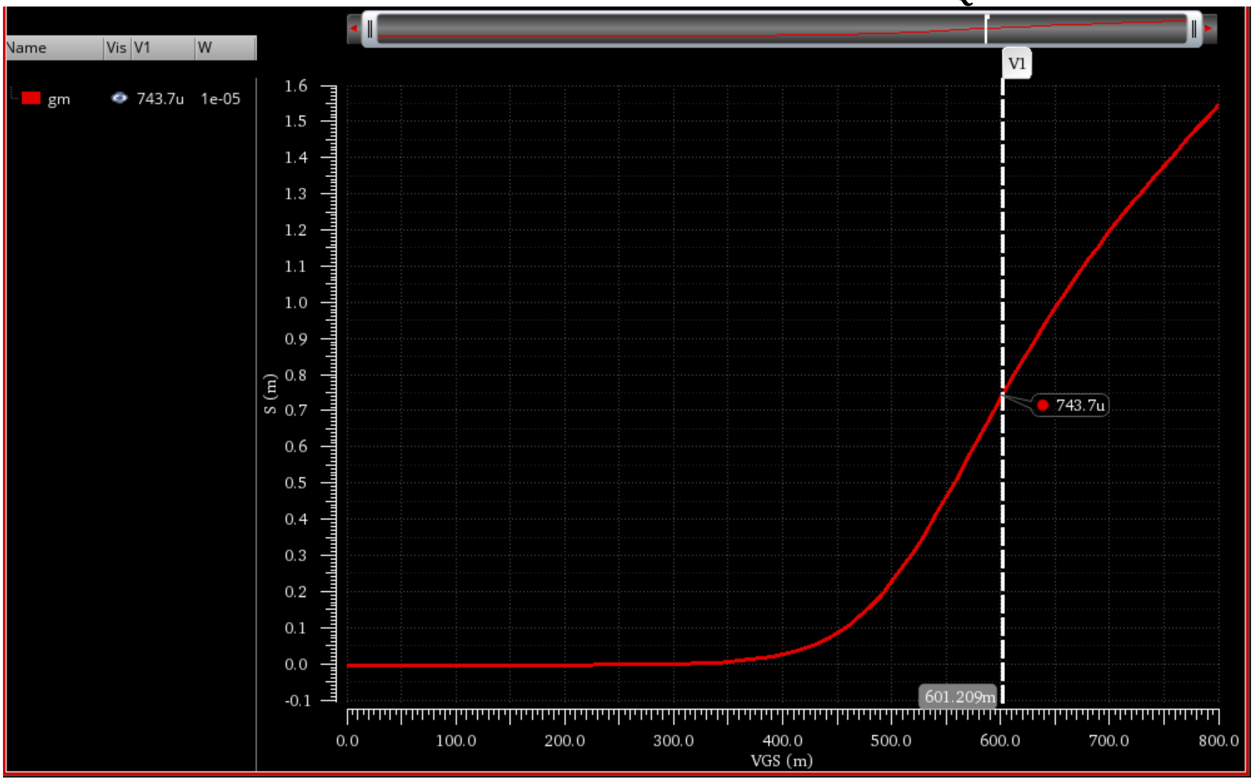
Plot I_D vs V_{GS}. Find its Values at V_{GS_Q}



$$@V_{GS_Q} = 601.209\ \text{mV} \rightarrow I_{D_X} = 59.5201\ \mu\text{A}.$$

P8

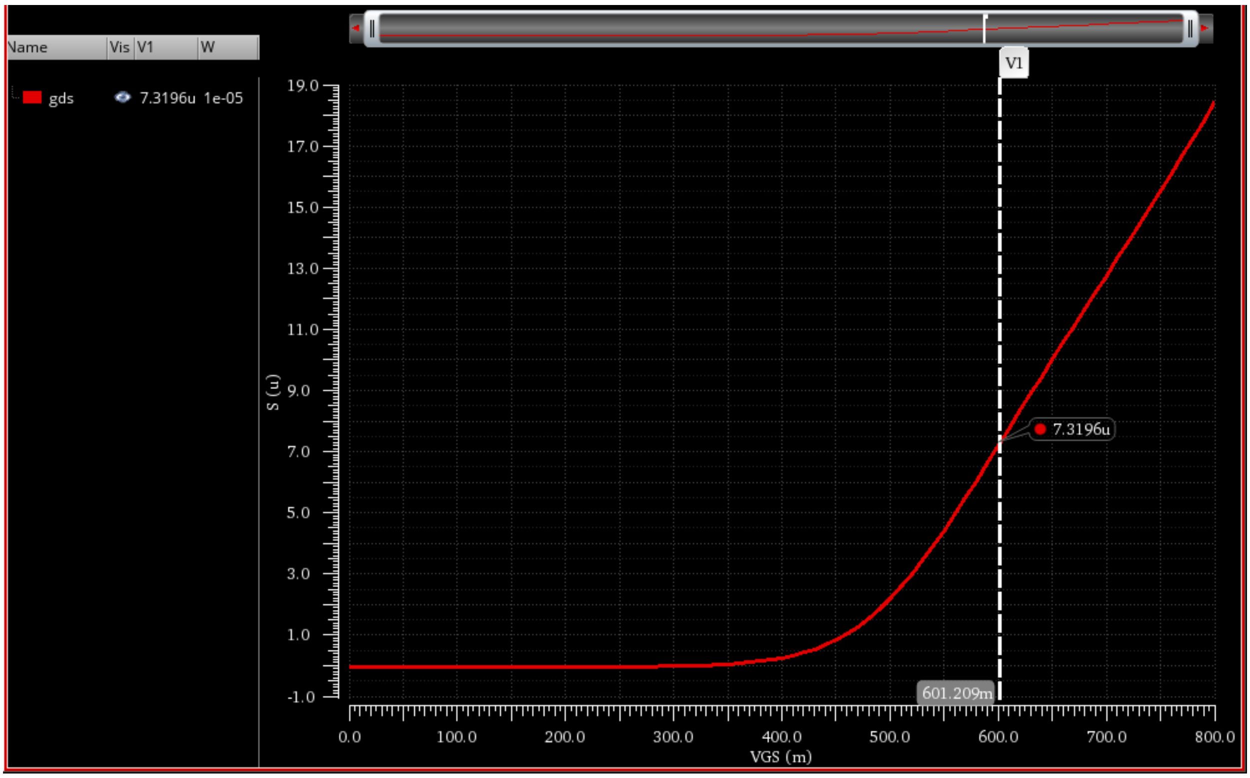
Plot g_m vs V_{GS}. Find its Values at V_{GS_Q}



$$@V_{GS_Q} = 601.209\ \mathrm{mV} \rightarrow g_{m_X} = 743.7\ \mu S.$$

P8

Plot g_{ds} vs V_{GS}. Find its Values at V_{GS_Q}



$$@V_{GS_Q} = 601.209\ \mathrm{mV} \rightarrow g_{ds_X} = 7.3196\ \mu S \rightarrow r_o = \frac{1}{g_{ds_X}} = 136.62\ k\Omega$$

P9	**Now back to the assumption that we made that $W = 10\mu m$.** **This is not the actual value that we will use for our design.** **But the good news is that I_D is always proportional to W irrespective of the operating region and the model of the MOSFET (regardless square – law is valid or not). Thus, we can use ratio and proportion (cross-multiplication) to determine the correct width at which the current will be $I_{D_Q} = 15\ \mu A$ as given in the specs.** **Calculate W as shown below.**

$\mathbf{W}$	$\mathbf{I_D}$
$W_{assumed} = 10\ \mu m$	I_{D_X} @ V_Q^* (From The Chart)
$W_{required} = ?$	$I_{D_Q} = 15\ \mu A$ (From The Specs)

$\mathbf{W}$	$\mathbf{I_D}$
$W_{assumed} = 10\ \mu m$	I_{D_X} @ V_Q^* (From The Chart) $= 59.5201\ \mu A$
$W_{required} = ?$	$I_{D_Q} = 15\ \mu A$ (From The Specs)

$$W_{required} = 2.52\ \mu m.$$

P10	**Now we are almost done with the design of the amplifier.** **Note that g_m is also proportional to W as long as V_{ov} is constant.** **On the other hand, $r_o = \frac{1}{g_{ds}}$ is inversely proportional to W (I_D) as long as L is constant. Before leaving this part, calculate g_{m_Q} and g_{ds_Q} using ratio and proportion (cross-multiplication).**

$\mathbf{g_m}$	$\mathbf{W}$
$g_{m_X} = 743.7\ \mu S$	$W_{assumed} = 10\ \mu m$
$g_{m_{required}} = ?$	$W_{required} = 2.52\ \mu m$

$$g_{m_{required}} = 187.412\ \mu S.$$

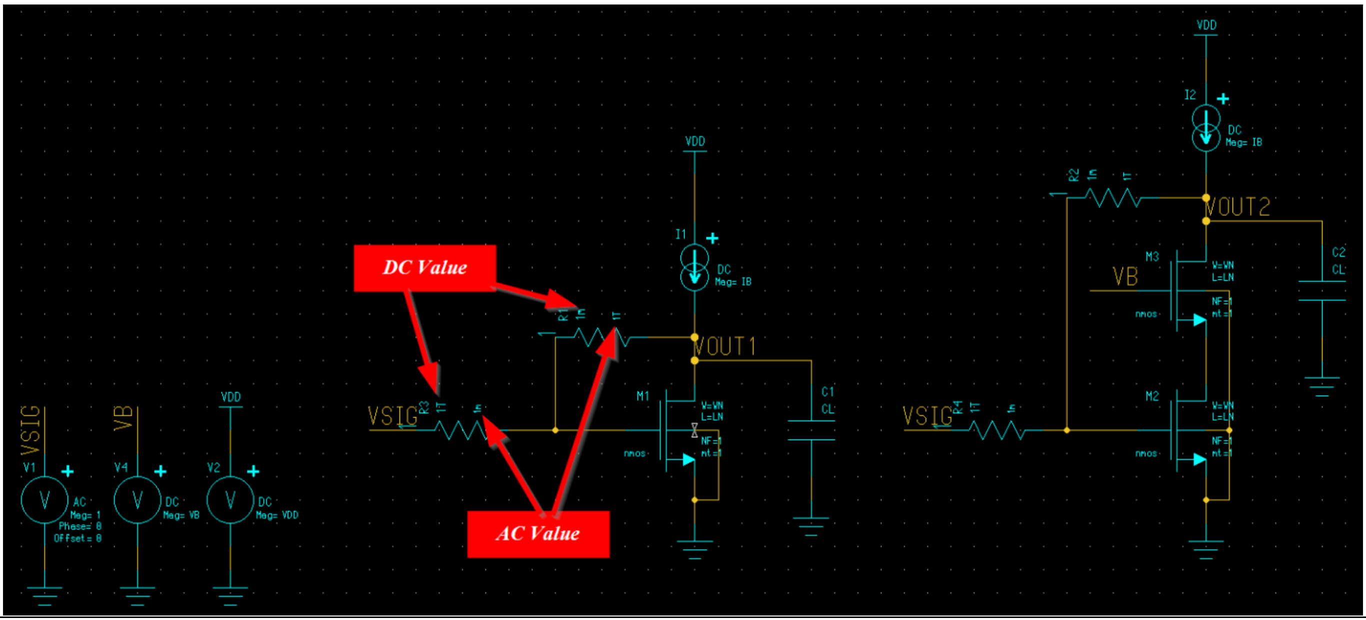
$\mathbf{g_{ds}}$	$\mathbf{W}$
$g_{ds_X} = 7.3196\ \mu S$	$W_{assumed} = 10\ \mu m$
$g_{ds_{required}} = ?$	$W_{required} = 2.52\ \mu m$

$$g_{ds_{required}} = 1.845\ \mu S \rightarrow r_o = 542.141\ k\Omega.$$

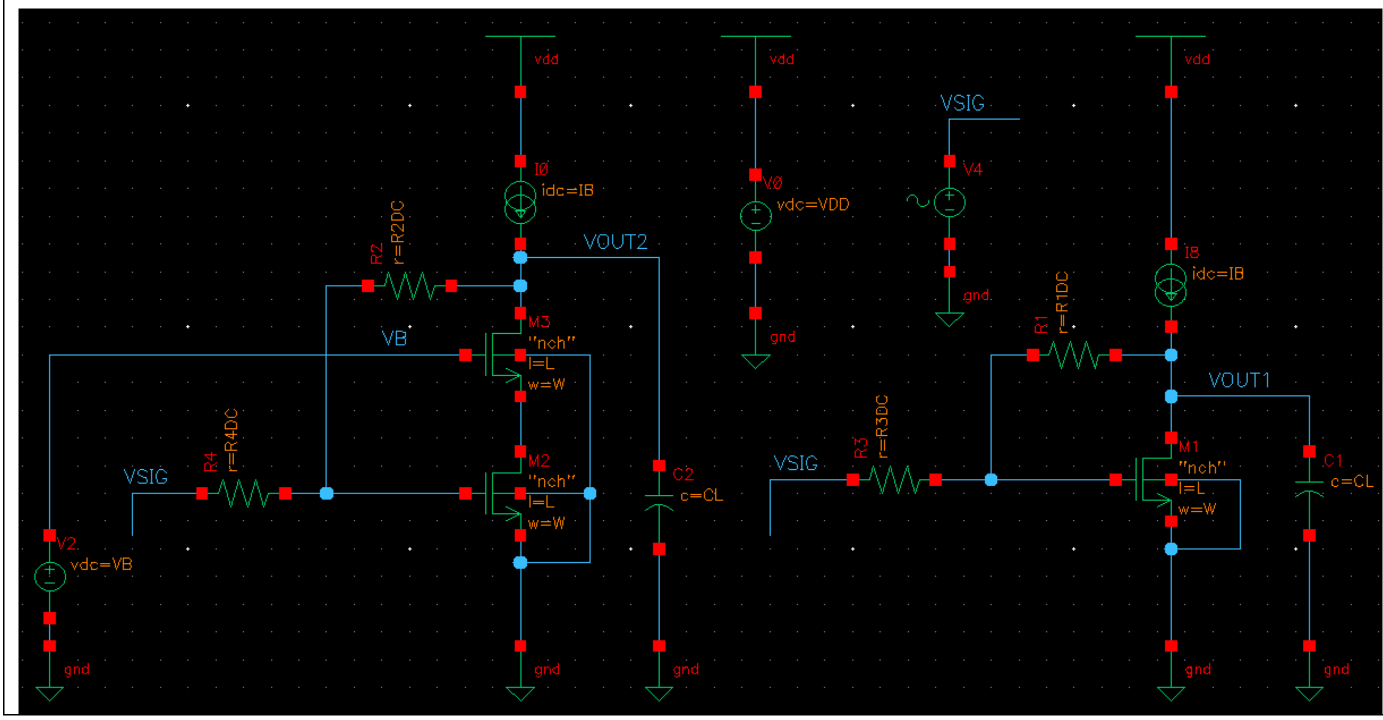
Part 2

Cascode For Gain

Circuit



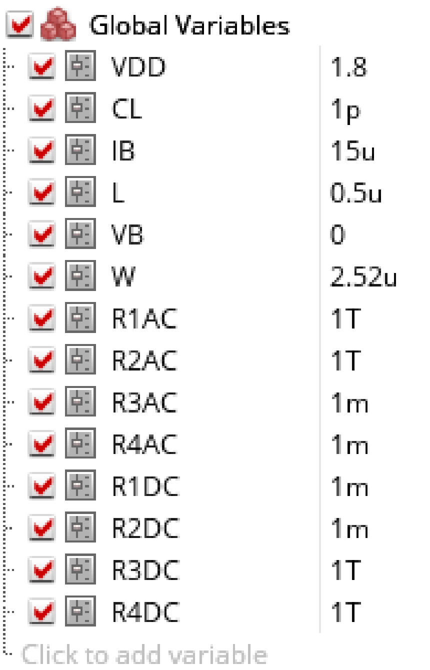
Schematic

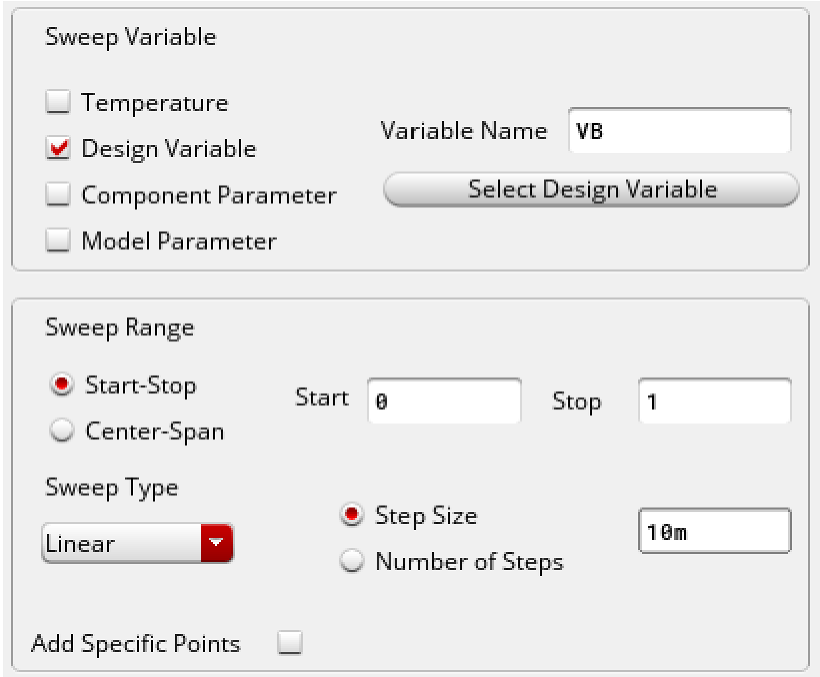


OP Analysis

Q1

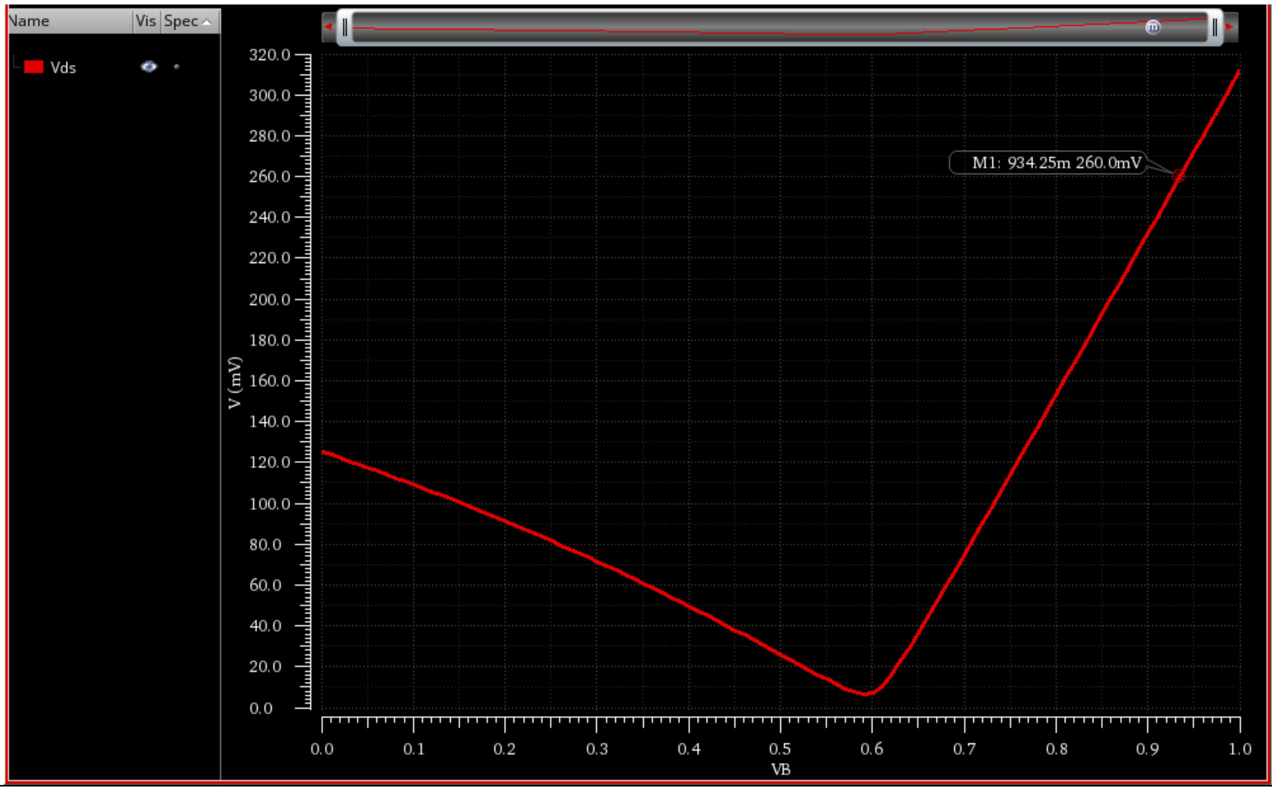
Create a new cell and schematic. Construct the circuit shown below. Use $I_B = 15\ \mu A$, $L = 0.5\ \mu m$, W as selected in Part 1, and $C_L = 1\ pF$.





Q2

Choose V_B (the cascode device bias voltage) such that M_2 has $V_{DS} \approx V^* + 100\ mV$ (you may sweep V_B and plot V_{DS} vs V_B to help you choose a good value for V_B). $\rightarrow V_B = 934.25\ mV$. @ $V_{DS} = 260\ mV$.

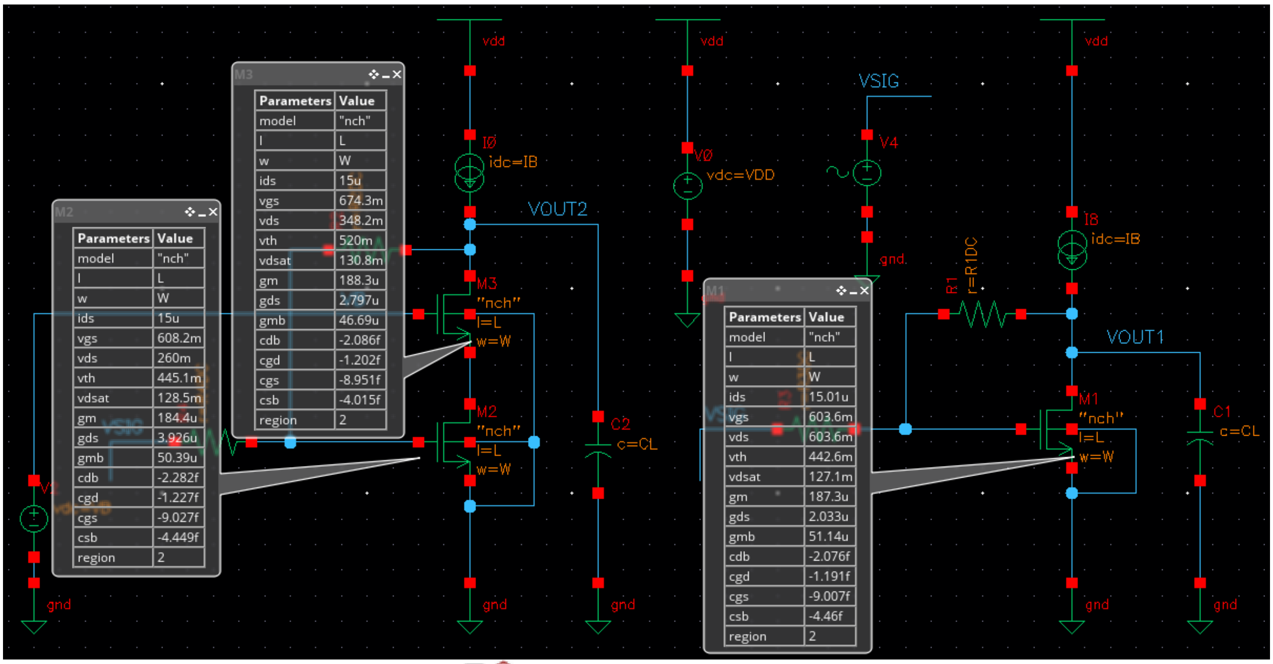


Q3	**We need to bias transistors in saturation; however, the output node is a high impedance node; thus, it is difficult to control its DC voltage. As a workaround in simulation, we use a feedback loop and resistors with different resistances in DC/AC to change the circuit connections in DC/AC simulations (use the AC property in ideal resistor). The input transistor is diode connected for DC simulation. (Always in saturation), while in AC simulation the feedback is disconnected, and the AC input source is connected. Set the feedback resistance 1 mΩ DC and 1 TΩ AC and set the source resistance oppositely.**

Q4

Simulate the DC OP point of the above CS and cascode amplifiers. Report a snapshot showing the following parameters for M_1, M_2 and M_3 in addition to DC node voltages clearly annotated.

$$@\ V_B = 934.25\ mV.$$



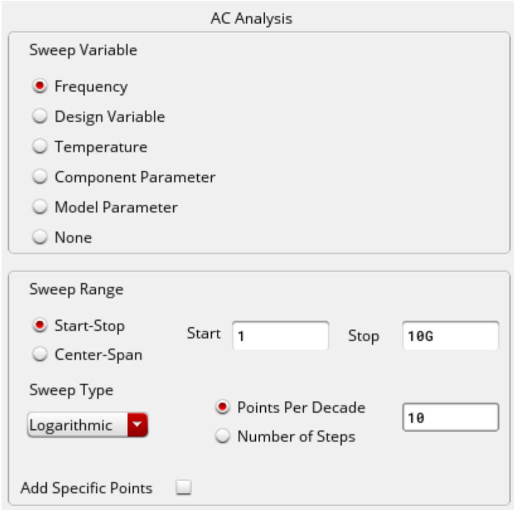
Global Variables	
VDD	1.8
CL	1p
IB	15u
L	0.5u
VB	934.25m
W	2.52u
R1AC	1T
R2AC	1T
R3AC	1m
R4AC	1m
R1DC	1m
R2DC	1m
R3DC	1T
R4DC	1T
Click to add variable	

Q5	**Check that all transistors operate in saturation.** ○ As we see in Q4 the Ballons annotate that region = 2 in all transistors (M_1 , M_2 , M_3) that represents all transistors operate in Saturation.
Q6	**Do all transistors have the same V_{TH}? Why?** ○ $V_{th_1} \approx V_{th_2}$ as $V_{SB} = 0$ as V_{th} depend on V_{SB} and not equal V_{th_3} due to the body effect of $M_3 \rightarrow V_{SB} \neq 0$. So, $V_{th_1} \approx V_{th_2} \neq V_{th_3}$
Q7	**What is the relation (≪, <, =, >, ≫) between g_m and g_{ds}?** ○ $g_m \gg g_{ds}$ for all transistors (M_1 , M_2 , M_3).
Q8	**What is the relation (≪, <, =, >, ≫) between g_m and g_{mb}?** ○ $g_m > g_{mb}$ for all transistors (M_1 , M_2 , M_3).
Q9	**What is the relation (≪, <, =, >, ≫) between C_{GS} and C_{GD}?** ○ $C_{GS} < C_{GD}$ (−ve Sign) or $\lvert C_{GS} \rvert > \lvert C_{GD} \rvert$ (Magnitude Value) for all transistors (M_1 , M_2 , M_3).
Q10	**What is the relation (≪, <, =, >, ≫) between C_{SB} and C_{DB}?** ○ $C_{SB} < C_{DB}$ (−ve Sign) or $\lvert C_{SB} \rvert > \lvert C_{DB} \rvert$ (Magnitude Value) for all transistors (M_1 , M_2 , M_3).

AC Analysis

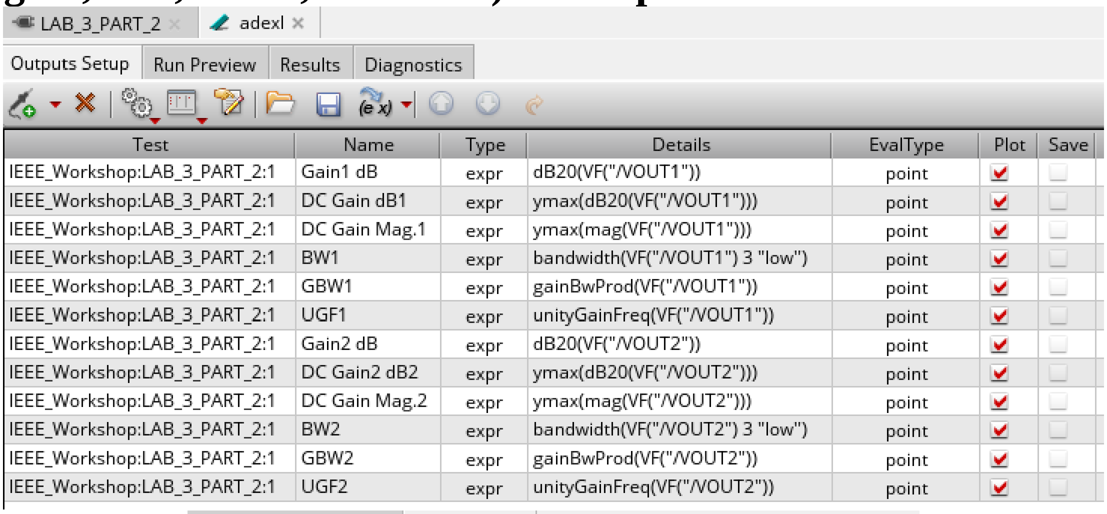
Q1

Create a new simulation configuration. Perform AC analysis. (1Hz: 10GHz, logarithmic, 10 points / decade) to simulate gain and bandwidth.

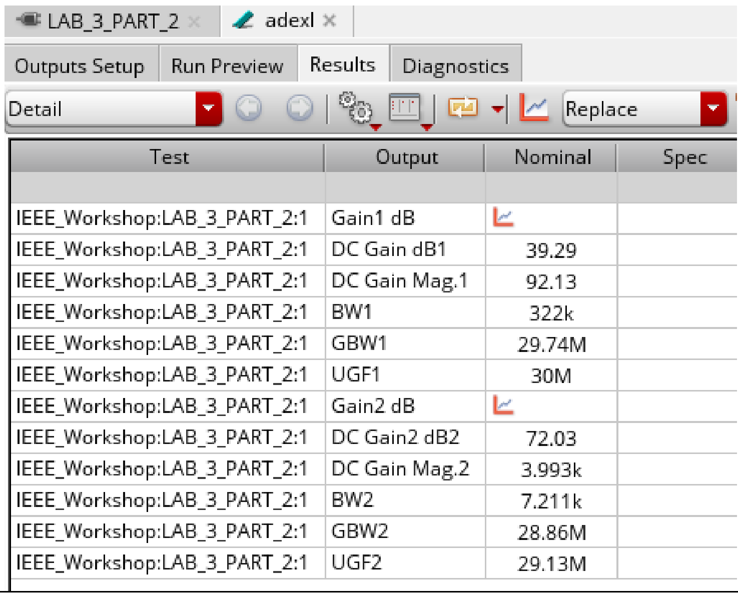


Q2

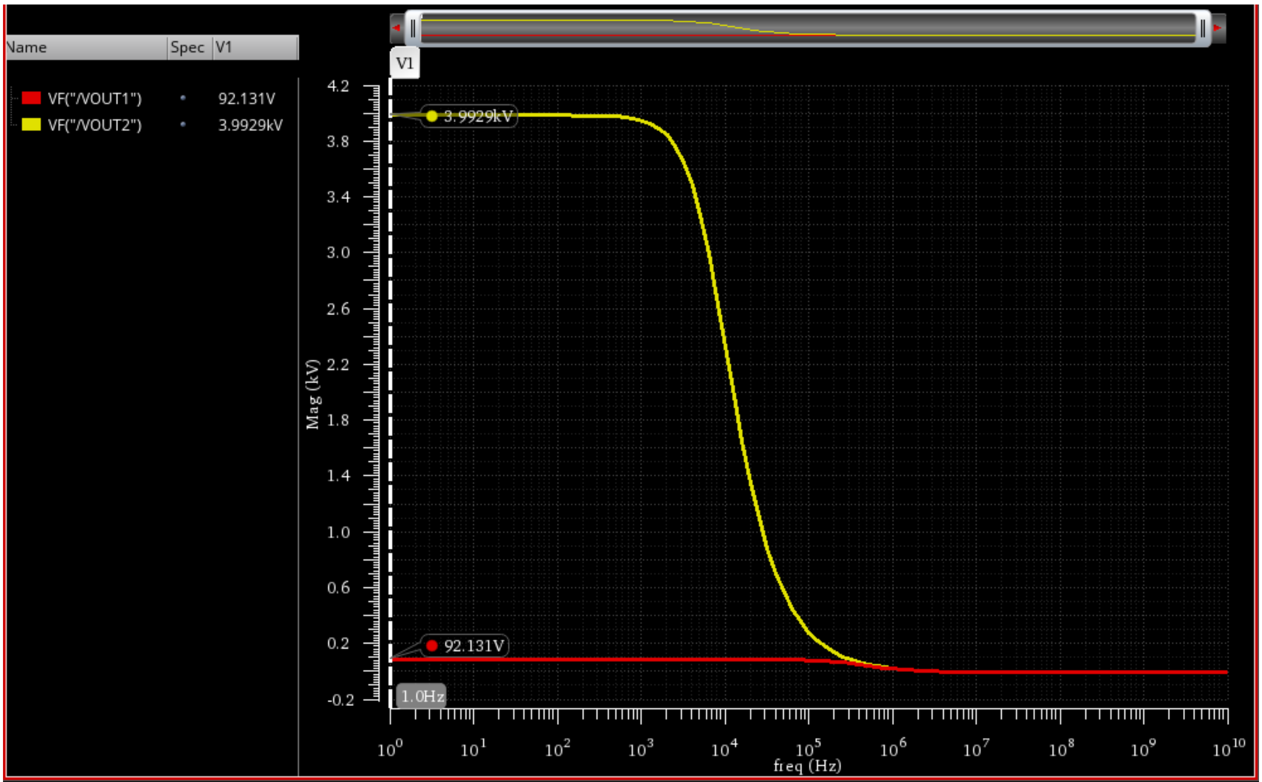
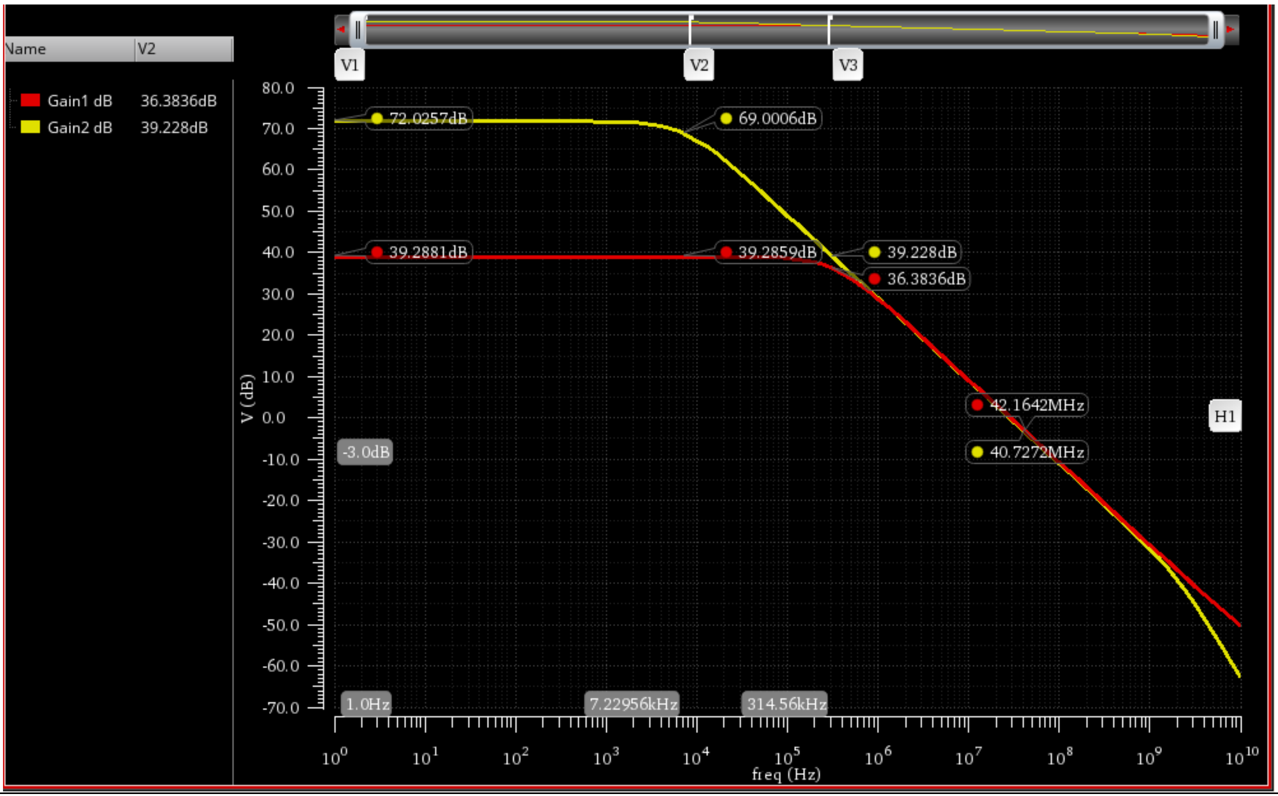
Use calculator to create expressions for circuit parameters (DC gain, BW, GBW, and UGF) and export them to adexl.



Test	Name	Type	Details	EvalType	Plot	Save
IEEE_Workshop:LAB_3_PART_2:1	Gain1 dB	expr	dB20(VF("/VOUT1"))	point	✓	
IEEE_Workshop:LAB_3_PART_2:1	DC Gain dB1	expr	ymax(dB20(VF("/VOUT1")))	point	✓	
IEEE_Workshop:LAB_3_PART_2:1	DC Gain Mag.1	expr	ymax(mag(VF("/VOUT1")))	point	✓	
IEEE_Workshop:LAB_3_PART_2:1	BW1	expr	bandwidth(VF("/VOUT1") 3 "low")	point	✓	
IEEE_Workshop:LAB_3_PART_2:1	GBW1	expr	gainBwProd(VF("/VOUT1"))	point	✓	
IEEE_Workshop:LAB_3_PART_2:1	UGF1	expr	unityGainFreq(VF("/VOUT1"))	point	✓	
IEEE_Workshop:LAB_3_PART_2:1	Gain2 dB	expr	dB20(VF("/VOUT2"))	point	✓	
IEEE_Workshop:LAB_3_PART_2:1	DC Gain2 dB2	expr	ymax(dB20(VF("/VOUT2")))	point	✓	
IEEE_Workshop:LAB_3_PART_2:1	DC Gain Mag.2	expr	ymax(mag(VF("/VOUT2")))	point	✓	
IEEE_Workshop:LAB_3_PART_2:1	BW2	expr	bandwidth(VF("/VOUT2") 3 "low")	point	✓	
IEEE_Workshop:LAB_3_PART_2:1	GBW2	expr	gainBwProd(VF("/VOUT2"))	point	✓	
IEEE_Workshop:LAB_3_PART_2:1	UGF2	expr	unityGainFreq(VF("/VOUT2"))	point	✓	



Test	Output	Nominal	Spec
IEEE_Workshop:LAB_3_PART_2:1	Gain1 dB		
IEEE_Workshop:LAB_3_PART_2:1	DC Gain dB1	39.29	
IEEE_Workshop:LAB_3_PART_2:1	DC Gain Mag.1	92.13	
IEEE_Workshop:LAB_3_PART_2:1	BW1	322k	
IEEE_Workshop:LAB_3_PART_2:1	GBW1	29.74M	
IEEE_Workshop:LAB_3_PART_2:1	UGF1	30M	
IEEE_Workshop:LAB_3_PART_2:1	Gain2 dB		
IEEE_Workshop:LAB_3_PART_2:1	DC Gain2 dB2	72.03	
IEEE_Workshop:LAB_3_PART_2:1	DC Gain Mag.2	3.993k	
IEEE_Workshop:LAB_3_PART_2:1	BW2	7.211k	
IEEE_Workshop:LAB_3_PART_2:1	GBW2	28.86M	
IEEE_Workshop:LAB_3_PART_2:1	UGF2	29.13M	

Q3	**Report the Bode plot (magnitude) of CS and cascode appended on the same plot.** **RED Curve = V_{out_1} (CS) , Yellow Curve = V_{out_2} (Cascode)**  **Bode plot (dB) of CS and cascode appended on the plot.** 

Q4

Using small signal parameters from OP simulation, perform hand analysis to calculate DC gain, BW, and GBW of both circuits.

CS Amplifier.

- $r_o = \frac{1}{g_{ds}} = \frac{1}{2.033\ \mu} = 491.9\ k\Omega$
- $A_o = g_{m_1} r_o = 187.3\ \mu \times 491.9\ k = 92.13 = 39.3\ dB$
- $BW = \frac{1}{2\pi \times r_o \times \left(C_L + C_{DB} + C_{GD}\left(1 + \frac{1}{A_o}\right)\right)} = 322.5\ kHZ$
- $GBW = A_o \times BW = 29.71\ MHZ$

Cascode Amplifier.

- $A_o = g_{m_2}\left(r_{o_3}\left(1 + g_{m_3} r_{o_2}\right) + r_{o_2}\right), r_{o_3} = \frac{1}{g_{ds_3}}\ ,\ r_{o_2} = \frac{1}{g_{ds_2}}$

  $A_o = 184.4\ \mu\ \left(\frac{1}{2.797\mu} \times \left(1 + 188.3\mu \times \frac{1}{3.926\mu}\right) + \frac{1}{3.926\mu}\right)$

  $A_o = 3.275\ k = 70.3\ dB$
- $r_{out} = \left(r_{o_3}\left(1 + g_{m_3} r_{o_2}\right) + r_{o_2}\right) = 17.76\ M\Omega$
- $BW = \frac{1}{2\pi \times r_{out} \times \left(C_L + C_{DB3} + C_{GD3}\left(1 + \frac{1}{A_o}\right)\right)} = 8.932\ kHZ$
- $GBW = A_o \times BW = 29.25\ MHZ$

Q5

Report a table comparing the DC gain, BW, UGF, and GBW of both circuits from simulation and hand analysis.

Analysis	Hand Analysis Results		Simulation Results	
Metrics	CS Amplifier	Cascode Amplifier	CS Amplifier	Cascode Amplifier
A_o	92.13	3.275 k	92.13	3.993 k
BW	322.5 k	8.932 k	322 k	7.211 k
GBW ≈ UGF	29.71 M	29.25 M	29.74 M	28.86 M

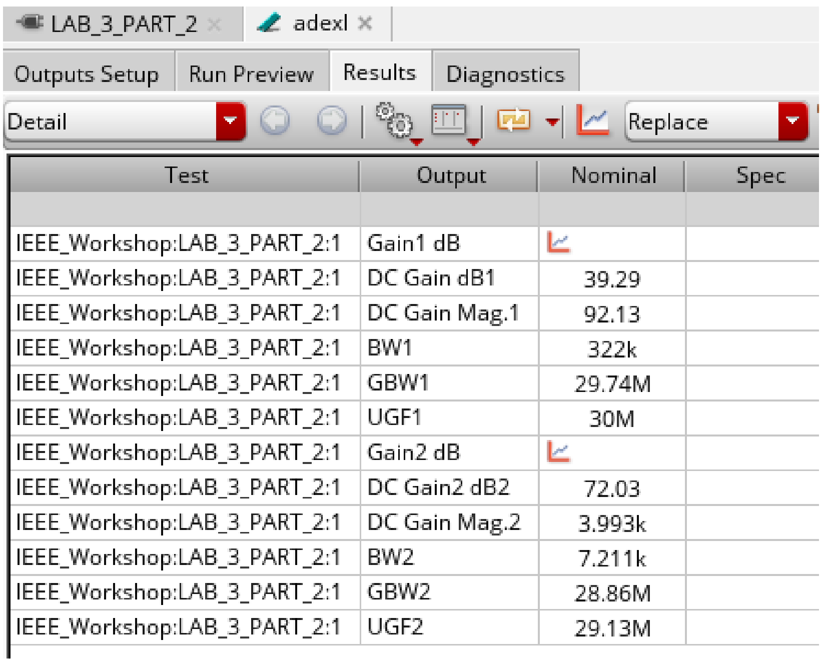
Q6

Comment on the results.

- As we see in Q5 Hand Analysis Results are not accurate enough Due to Miller's effects Approximations.
- $(GBW_{CS} = UGF_{CS}) \approx (GBW_{Cascode} = UGF_{Cascode})$
- $BW_{CS} > BW_{Cascode}$
- $A_{o_{Cascode}} > A_{o_{CS}}$
- Cascode for Gain: BW is Limited By output Pole as when R_D Increased R_{SIG} Decreased.
- Gain is Increased in Cascode But BW is Decreased (Limited) Because in Cascode:

$$A_v \approx g_{m_2} r_{o_2} g_{m_3} r_{o_3} \rightarrow g_{m_3} r_{o_3} \qquad \rightarrow \text{(Increased)}$$

$$\omega_{p_{out}} = \frac{\omega_{p_{CS}}}{g_{m_3} r_{o_3}} \quad \text{(Decreased)} \rightarrow \text{ BW} \rightarrow \text{(Decreased)}$$



Test	Output	Nominal	Spec
IEEE_Workshop:LAB_3_PART_2:1	Gain1 dB		
IEEE_Workshop:LAB_3_PART_2:1	DC Gain dB1	39.29	
IEEE_Workshop:LAB_3_PART_2:1	DC Gain Mag.1	92.13	
IEEE_Workshop:LAB_3_PART_2:1	BW1	322k	
IEEE_Workshop:LAB_3_PART_2:1	GBW1	29.74M	
IEEE_Workshop:LAB_3_PART_2:1	UGF1	30M	
IEEE_Workshop:LAB_3_PART_2:1	Gain2 dB		
IEEE_Workshop:LAB_3_PART_2:1	DC Gain2 dB2	72.03	
IEEE_Workshop:LAB_3_PART_2:1	DC Gain Mag.2	3.993k	
IEEE_Workshop:LAB_3_PART_2:1	BW2	7.211k	
IEEE_Workshop:LAB_3_PART_2:1	GBW2	28.86M	
IEEE_Workshop:LAB_3_PART_2:1	UGF2	29.13M	