وَمَا أُوتِيتُمْ مِنَ الْعِلْمِ إِلَّا قَلِيلًا

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Analog IC Design
Lab 05
Simple vs Low Compliance Cascode Current Mirror

Intended Learning Objectives

In this lab you will:

- Design and simulate low-voltage and simple current mirrors.
- Compare low-voltage and simple current mirrors.
- Learn how to use hierarchical design.

Part 1: Sizing Chart

1) We can show that

$$g_m = \frac{2I_D}{V_{ov}}$$

which is based on the square-law. For a real MOSFET, if we compute V_{ov} and $\frac{2I_D}{g_m}$ they will not be equal. Let's define a new parameter called V-star (V^*) which is calculated from actual simulation data using the formula

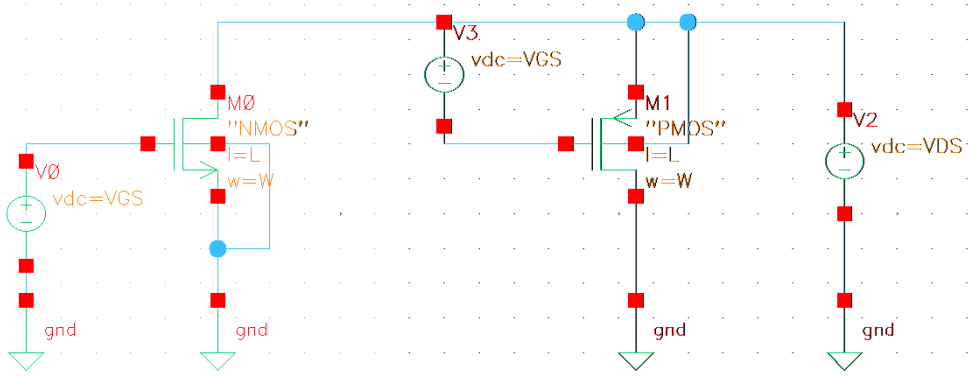
$$V^* = \frac{2I_D}{g_m} \leftrightarrow g_m = \frac{2I_D}{V^*}$$

For a square-law device, $V^* = V_{ov}$, however, for a real MOSFET they are not equal. An often used sweet-spot that provides good compromise between different trade-offs is $V^* = 200mV$.

2) We want to design current mirrors with the parameters below.

Parameter	0.13um CMOS	0.18um CMOS
L	$1\mu m$	$1\mu m$
V^*	$125mV$	$200mV$
Supply	$1.2V$	$1.8V$
Reference current	$20\mu A$	$20\mu A$

3) The remaining variable in the design is to calculate W. Since the square-law is not accurate, we cannot use it to determine the sizing. Instead, we will use a sizing chart generated from simulation. Create a testbench for NMOS transistor as shown below (**we will use both NMOS and PMOS in this lab**). Use $W = 10\mu m$ (we will understand why shortly).



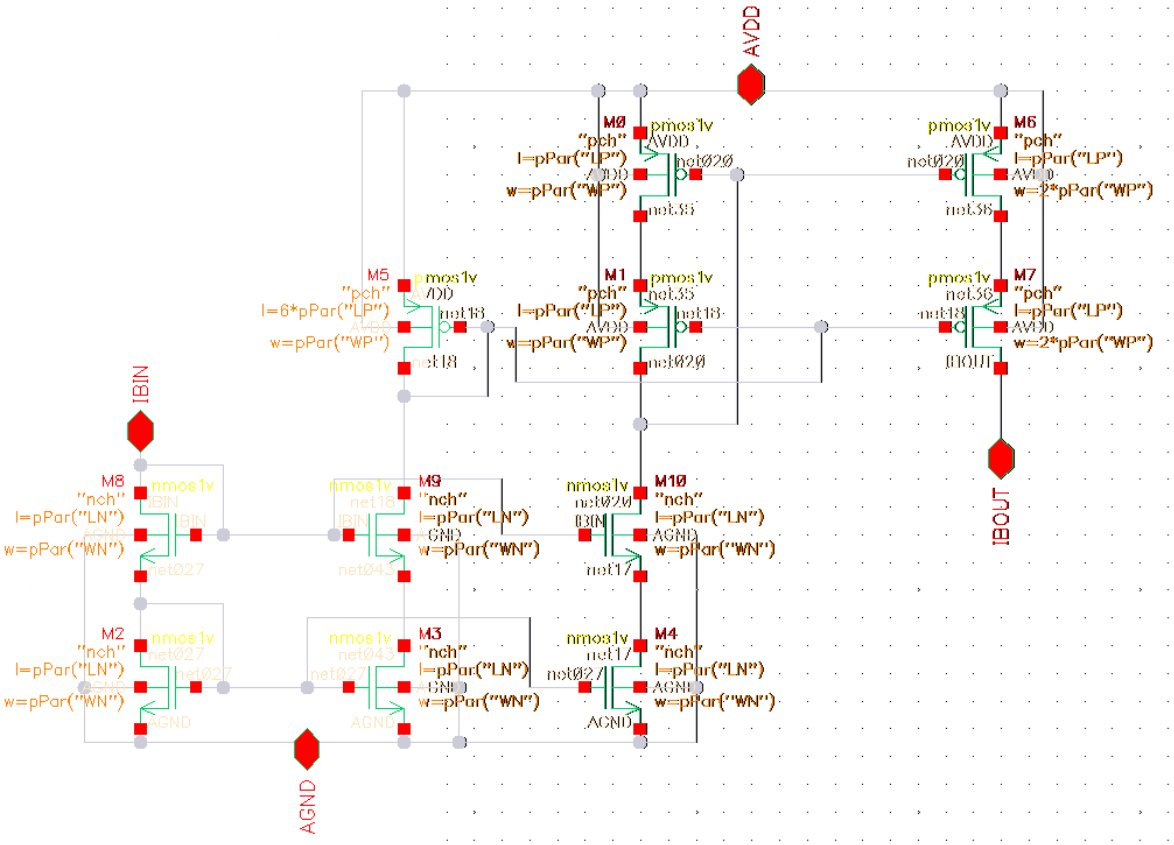
4) Sweep VGS from 0 to $\approx V_{TH} + 0.4V$ with 10mV step. Set $V_{DS} = V_{DD}/2$.
5) We want to compare $V^* = 2I_D/g_m$ and $V_{ov} = V_{GS} - V_{TH}$ by plotting them overlaid. Use the calculator to create expressions for V^* and V_{ov}. You can save the expressions to reuse them later.
6) Plot V^* and V_{ov} overlaid vs VGS. Make sure the y-axis of both curves has the same range. You will notice that at the beginning of the strong inversion region, V^* and V_{ov} are relatively close to each other (i.e., square-law is relatively valid). For deep strong inversion (large V_{ov}: velocity saturation and mobility degradation) or weak inversion (near-threshold and subthreshold operation) the behavior is quite far from the square-law.
7) An often used sweet-spot that provides good compromise between different trade-offs is $V^* = 200mV$. On the V^* and V_{ov} chart locate the point at which $V^* = 200mV$. Find the corresponding V_{ovQ} and V_{GSQ}.
8) Plot I_D, g_m, and g_{ds} vs V_{GS}. Find their values at V_{GSQ}. Let's name these values I_{DX}, g_{mX}, and g_{dsX}.
9) Now back to the assumption that we made that $W = 10\mu m$. This is not the actual value that we will use for our design. But the good news is that I_D is always proportional to W irrespective of the operating region and the model of the MOSFET (regardless square-law is valid or no). Thus, we can use ratio and proportion (cross-multiplication) to determine the correct width at which the current will be I_{DQ} as given in the specs. Calculate W as shown below.

W	I_D
$\mathbf{10\mu m}$	I_{DX} @V_Q^* (from the chart)
?	$I_{DQ} = 20\mu A$ (from the specs)

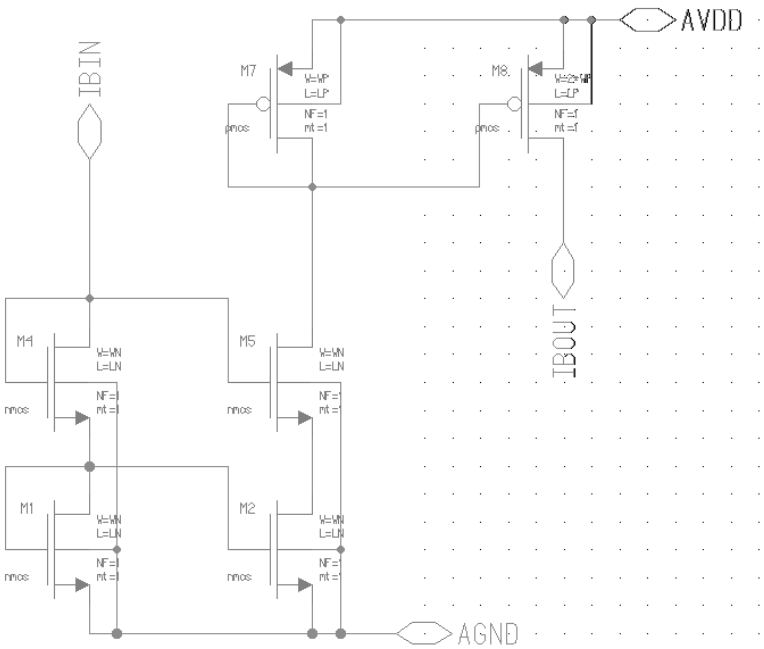
10) Now we are almost done with the design of the amplifier. Note that g_m is also proportional to W as long as V_{ov} is constant. On the other hand, $r_o = 1/g_{ds}$ is **inversely** proportional to W (I_D) as long as L is constant. Before leaving this part, calculate g_{mQ} and g_{dsQ} using ratio and proportion (cross-multiplication).

PART 2: Current Mirror

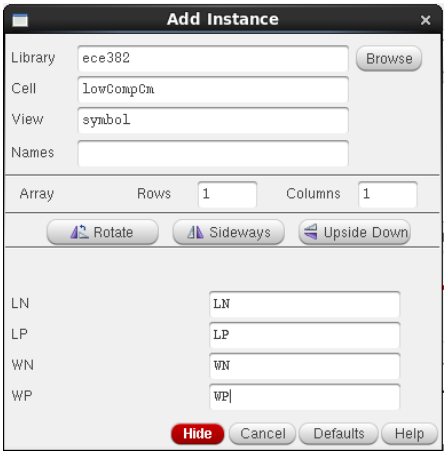
1) Create a new schematic and name it "lab_05_ws_cm". Construct the low compliance current mirror circuit shown below.
2) Construct the circuit shown below. Add labels (IBIN, IBOUT, AGND, AVDD) to nets (wires) using the hotkey "l", then create ports using the hotkey "p" or using the toolbar.
   ➔ Cadence Hint: For W and L we use pPar("VariableName"), which passes the variable to the upper level of hierarchy. The variables will appear when you instantiate the cell as explained below.
3) For the wide-swing bias transistor (the magic battery) note that we use longer length $(6 * L)$ as shown below.



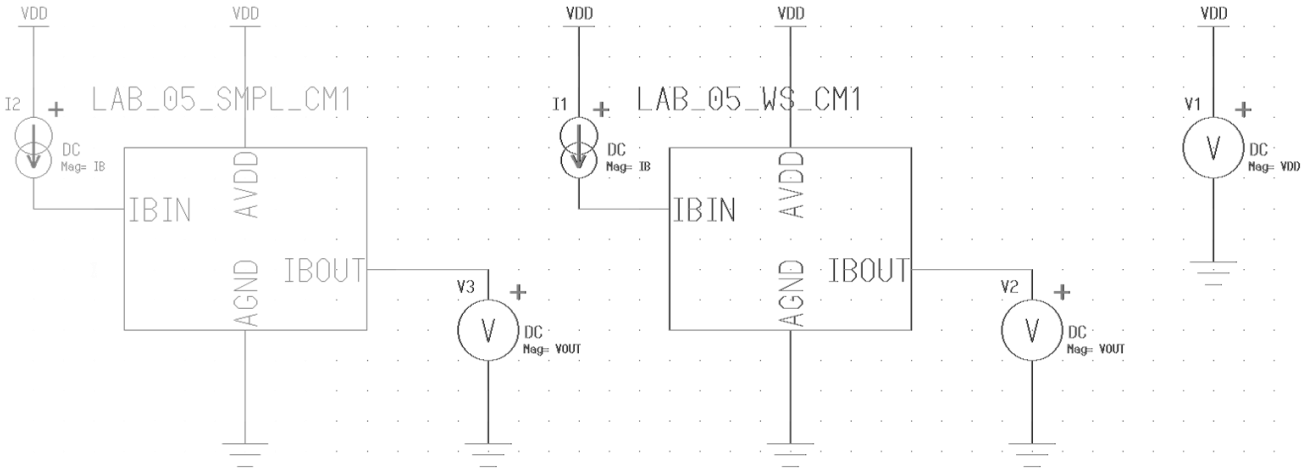
4) The current mirror takes input current IBIN and generates output current IBOUT = 2*IBIN (note the sizing of transistors in IBOUT branch).
5) Create a symbol for the CM (From the menu bar: Add -> Generate Symbol)
6) Create a testbench in a higher level of hierarchy as shown below to test the current mirror.
7) In the library manager copy the “lab_05_ws_cm” cell and name the new cell “lab_05_simple_cm”. Edit the new cell to design another simple current mirror using two PMOS transistors only as shown below. Create a symbol for the simple current mirror. We will compare this simple mirror with the wide swing cascode you have just designed.



8) Create a new cell for the testbench schematic “lab_05_cm_tb” to test the two current mirrors.
9) When you instantiate the cells, you can set the pPar parameters as shown below.



10) Use IB = 20uA and set the sizing as in Part 1.



Report the following:

1) Schematic of the two CMs with DC node voltages clearly annotated at VOUT = VDD/2 (double click the symbol to go to lower level of hierarchy and show the schematic).
2) Snapshots showing the following parameters for all transistors at VOUT = VDD/2. You may summarize the results in a table.

ID
VGS
VDS
VTH
VDSAT
GM
GDS
GMB
Region

3) Check that all transistors have V_{GS}, g_m and g_{ds} as designed in Part 1.
4) Are all transistors operating in saturation?
5) Perform DC sweep (not parametric sweep) using VOUT = 0:10m:VDD. Report IBOUT vs VOUT for the two CMs overlaid in the same plot.
    - Comment on the difference between the two circuits.
    - IBOUT of the simple CM is exactly equal to IBIN*2 at a specific value of VOUT. Why?
6) Percent of error in IBOUT vs VOUT (ideal IBOUT should be IBIN*2) for the two CMs in the current mirror operating region (VOUT = 0 to VDD – V^*) overlaid in the same plot.
    - Comment on the difference between the two circuits.

7) Rout vs VOUT (take the inverse of the derivative of IBOUT plot) for the two CMs in the current mirror operating region (VOUT = 0 to VDD – V^*) overlaid in the same plot. Use log scale on the y-axis. Add a cursor at VOUT = VDD/2.
    - Comment on the difference between the two circuits.
    - Does Rout change with VOUT? Why?
8) Analytically calculate Rout of both circuits at VOUT = VDD/2. Compare with simulation results in a table.

Lab Summary

In Part 1 you learned:

- How to generate and use design charts for NMOS and PMOS transistors.
- How to design a simple current mirror.
- How to design a low-voltage current mirror.

In Part 2 you learned:

- How to do a hierarchical design in Mentor tools.
- How the output resistance of a simple current mirror changes with the output voltage.
- How the output resistance of a low-voltage current mirror changes with the output voltage.

Acknowledgements

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