ADT &
Cadence Virtuoso
LAB (7) Report

By: Magdy Ahmed Abbas Abdelhamid

IEEE

CAIRO UNIVERSITY STUDENT BRANCH

Analog Electronics Workshop

GM/ID DESIGN METHODOLOGY

Part 1

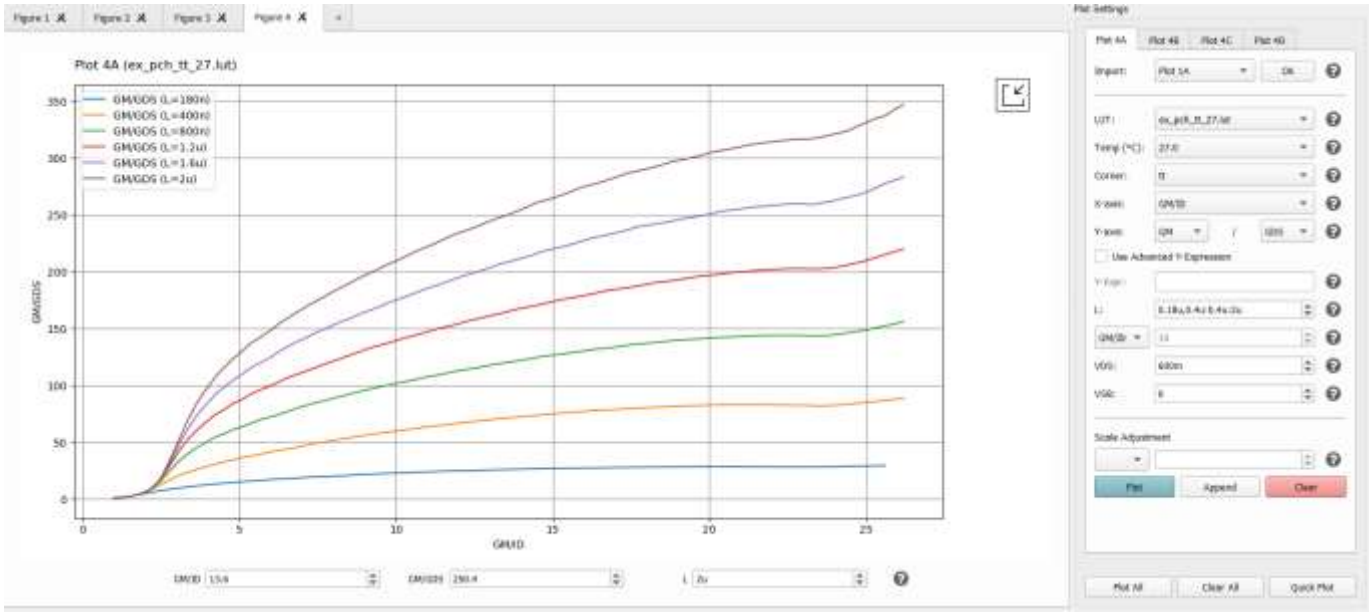
GM/ID DESIGN CHART

5T - OTA Required Specifications

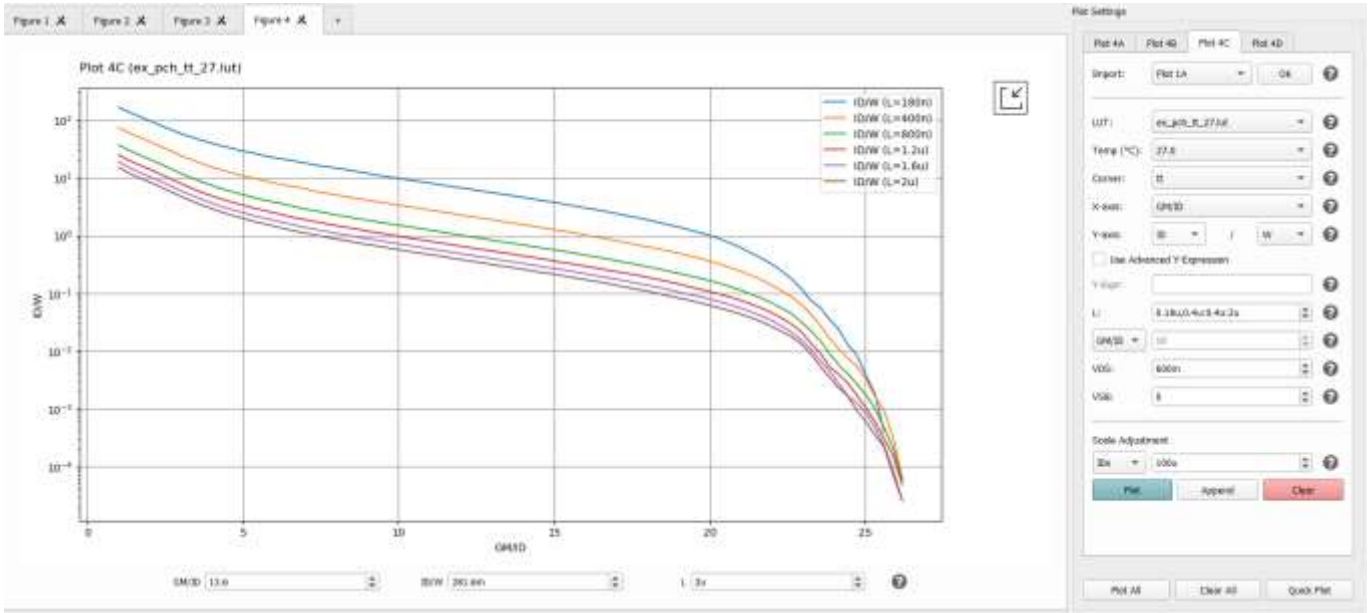
DC Current (I_{REF})	10 µA.
Supply (V_{DD})	1.8 V.
$V_{DS} = \frac{V_{DD}}{3}$	0.6 V.
Length (L)	0.18 µm, 0.4µm: 0.4µm: 2µm.
Load	5 pF.
Open loop DC Voltage gain	≥ 34 dB.
CMRR @ DC	≥ 74 dB.
Phase Margin	≥ 70°
OTA Current Consumption	≤ 20 µA.
CM Input Range – Low	≤ 0.8 V.
CM Input Range – High	≥ 1.5 V.
GBW	≥ 5 MHZ.

Using ADT Device Xplore, plot the following design charts vs gm/ID for PMOS.

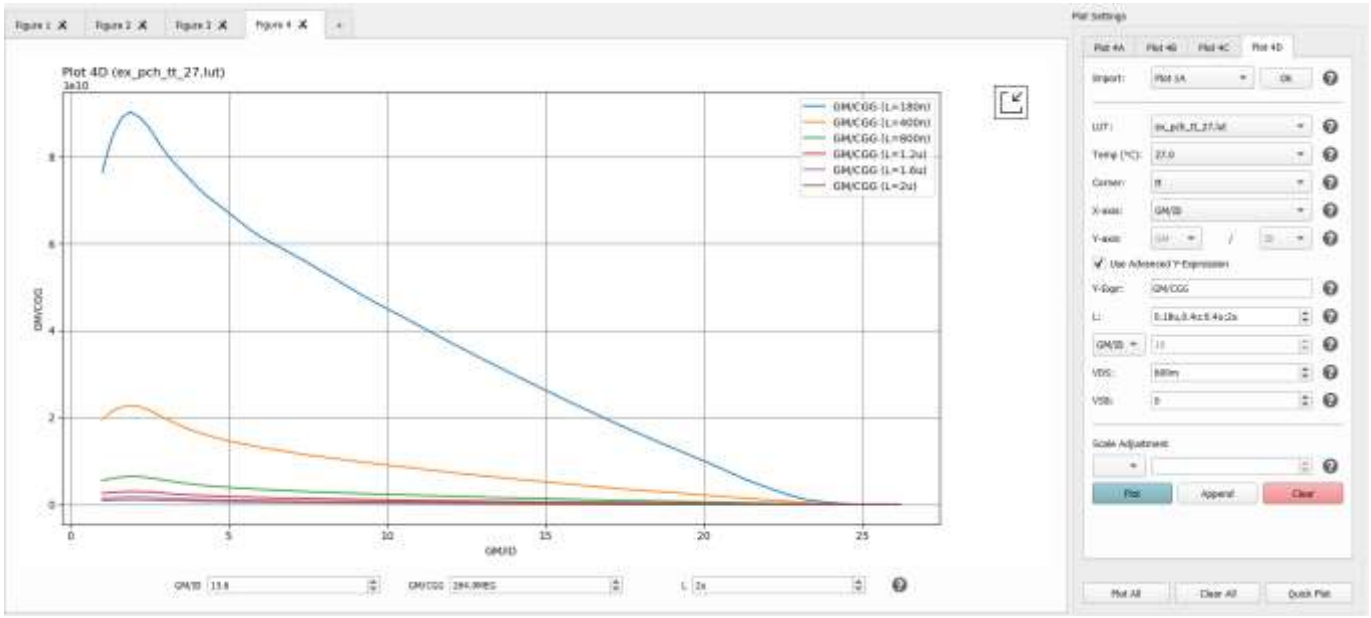
(1) g_m/g_{ds}



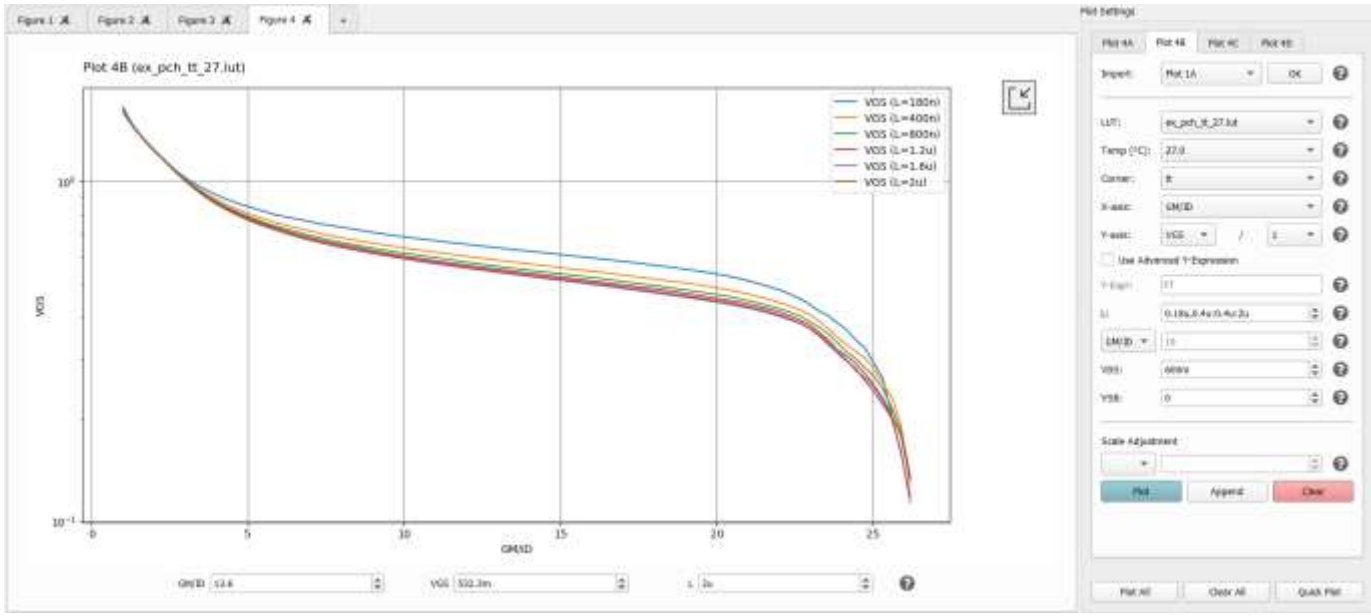
(2) I_D/W



(3) g_m/C_{gg} (Use Advanced Y Expression)

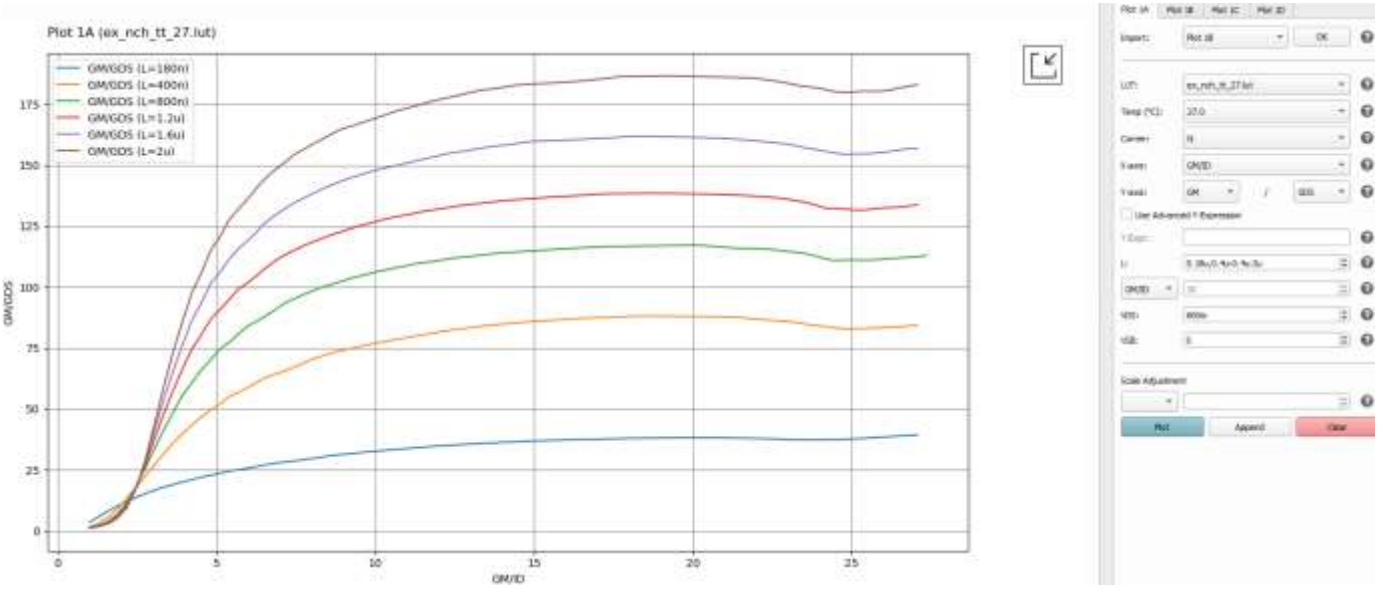


(4) V_{GS}

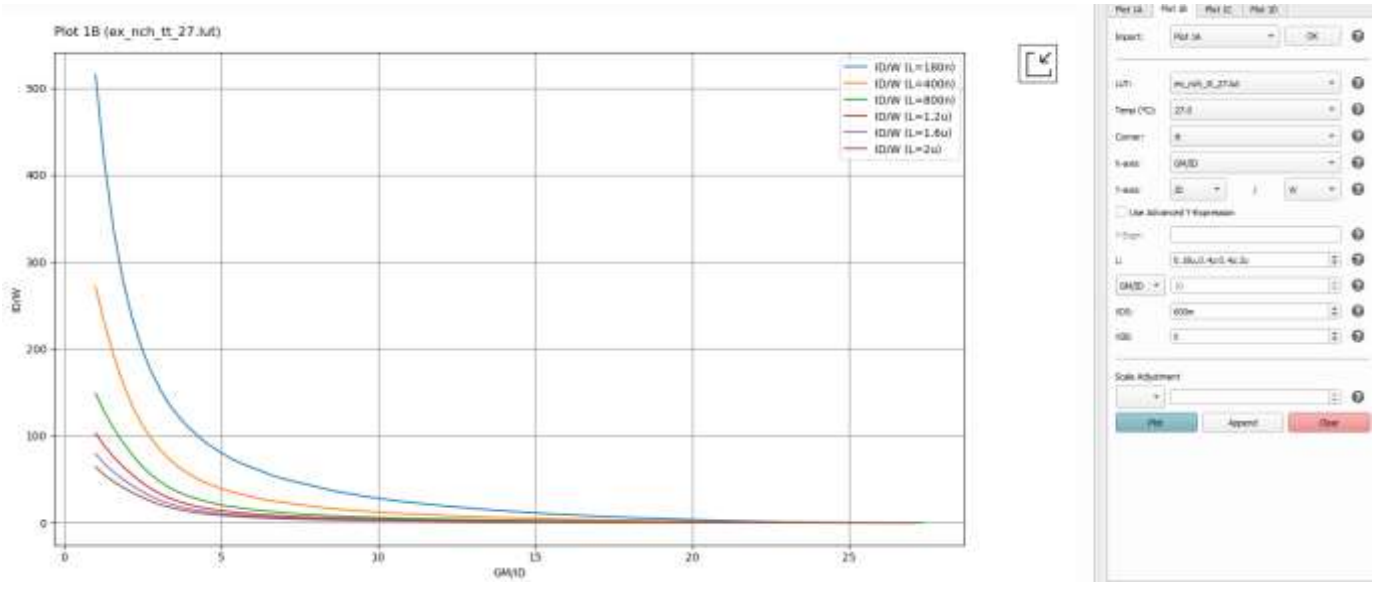


Using ADT Device Xplore, plot the following design charts vs gm/ID for NMOS.

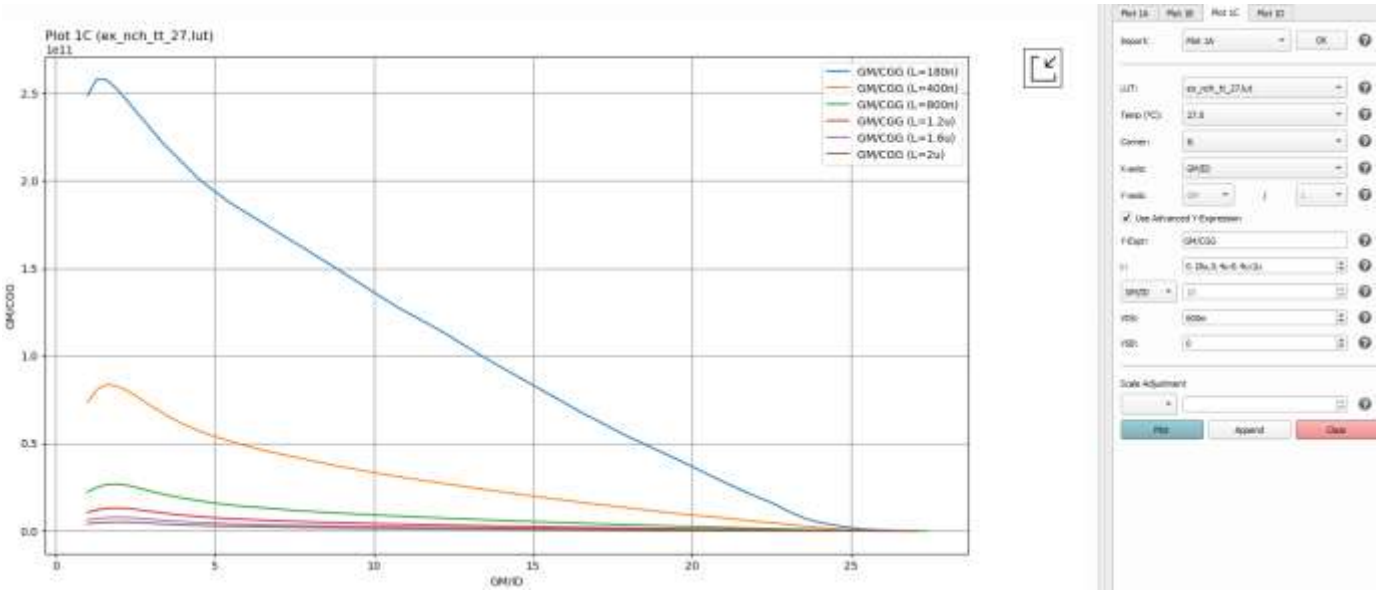
(5) g_m/g_{ds}



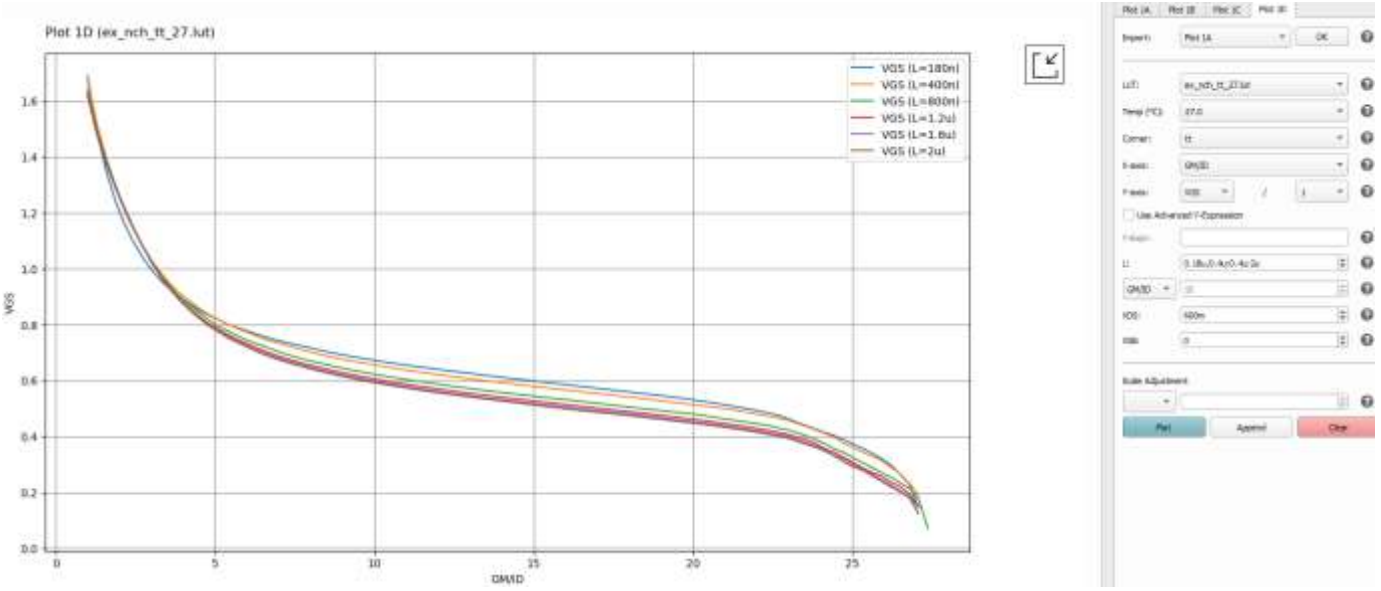
(6) I_D/W



(7) g_m/C_{gg} (Use Advanced Y Expression)



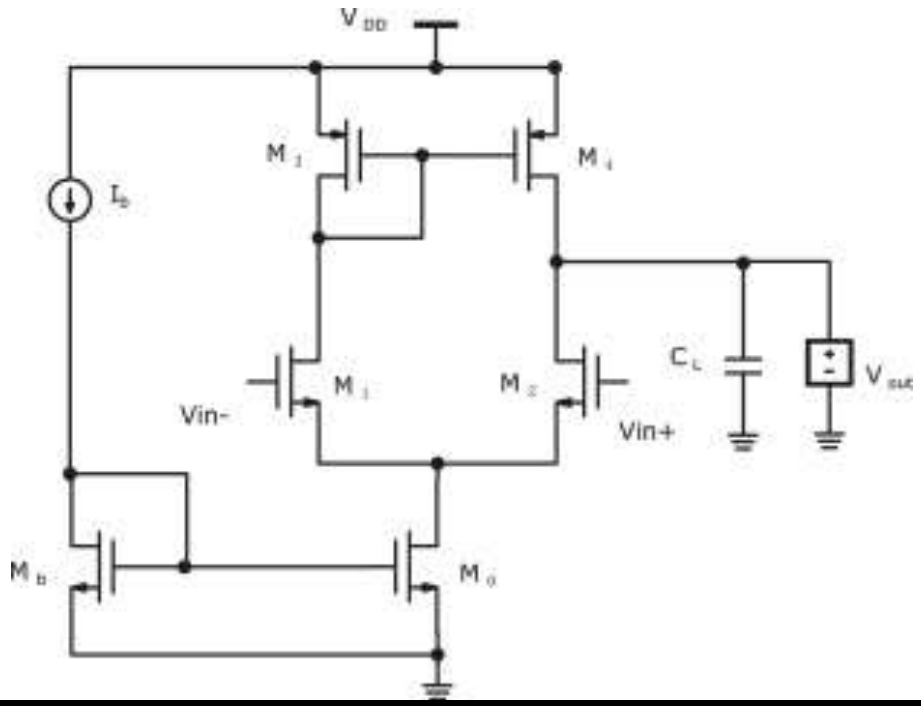
(8) V_{GS}

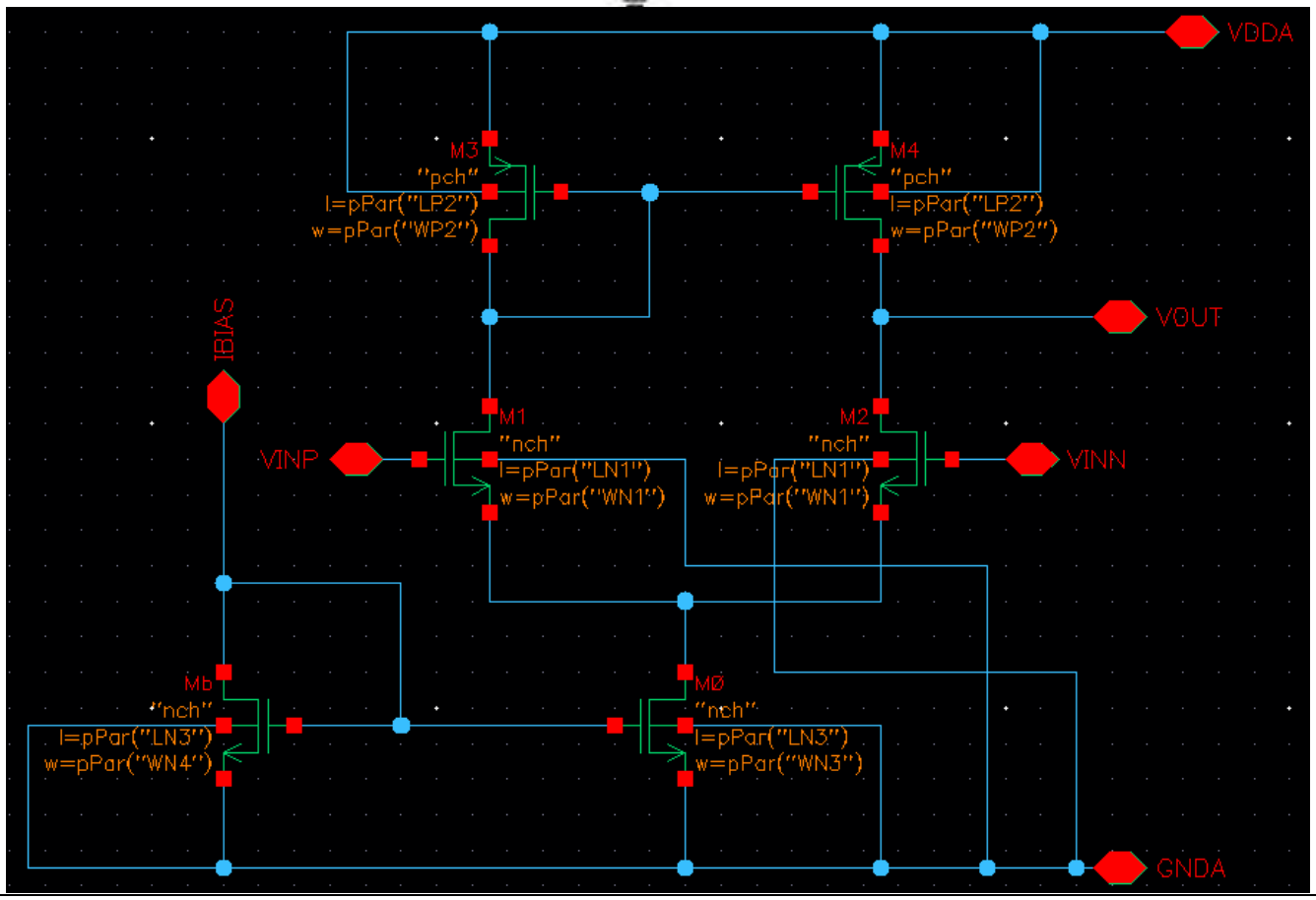


Part 2

OTA Design

5T – OTA Design.





Report the following:

❖ **Detailed design procedure and hand analysis. You need to explain why you chose the architecture that you implemented (Topology Selection).**

- **The Required gain is not High $(\mathbf{only\ 34\ dB\ =\ 50})$ So it Can be Achieved by a Simple Single Stage OTA.**
  - **If The Gain is High, We Must use $\mathbf{Cascode}$ or Two Stage OTA.**
- **Since The Required CMIR is Close to $\mathbf{V_{DD}}$, we need to use a NMOS input Stage $(\mathbf{CMIR\ \rightarrow\ V_{in} = 0.8 - 1.5})$.**
- **NMOS input Stage has Other Advantages as Well**
  - **NMOS has Low input bias current, and High input impedance.**
  - **NMOS has Lower input voltage noise, and Faster response time.**
- **Single Stage OTA has a Single Dominant Pole, so we Don't need to Worry about Phase Margin.**
  - **For two – Stage you Must use Compensation Network.**
- **Use Simple Current Mirror for Biasing.**
  - **The Reference Current is $\mathbf{10\ \mu A}$.**
  - **Doubled by Mirror Such That $\mathbf{20\ \mu A}$ goes to Diff. Pair $\mathbf{(10\ \mu A)}$ for Each Branch.**

❖hand analysis:

❖Design of Input Pair.

- $\mathbf{GBW = \frac{g_{m_{1,2}}}{2\pi C_L}}$, $\mathbf{g_{m_{1,2}} = 2\pi \times 5p \times 5M \approx 160\ \mu S.}$

  $\mathbf{I_D = \frac{20\mu}{2} = 10\ \mu A}$, $\mathbf{\frac{g_m}{I_D} = 16\ S/A,\ r_o = \frac{2A_v}{g_m}, g_{ds} = \frac{1}{r_o}}$
- **Next, we need to Find the Channel Length to get the Required Gain.**
- **We Assume PMOS and NMOS have Same $\mathbf{g_{ds}}$**
  - $\mathbf{g_{ds_{1,2}} = g_{ds_{3,4}} = 2\ \mu S, A_v = \frac{g_m r_o}{2} \rightarrow \frac{g_m}{g_{ds}} > 80}$
  - $\mathbf{\frac{g_m}{g_{ds}} = 2A_v = g_m r_o}$, $\mathbf{\frac{g_m}{I_D} = 16}$, $\mathbf{L = 570nm}$ **(From Design Chart).**
- **Going to the $\mathbf{\frac{I_D}{W}}$ Chart $\rightarrow$ $\mathbf{W = 3.8\ \mu m, r_o = \frac{2A_v}{g_m}, g_{ds} = \frac{1}{r_o}}$**

❖Design of Current Mirror Load. (Using ADT PMOS Charts)

- **From the DC gain Spec Select the Length of the Current Mirror Load.**
- $\mathbf{\lambda = \frac{g_{ds}}{I_D} = \frac{g_m/I_D}{g_m/g_{ds}}}$ **Slightly Increase With $\mathbf{\frac{g_m}{I_D}}$ (Weak Dependence).**
- **Assume an Arbitrary but Large $\mathbf{\frac{g_m}{I_D}}$, e.g., $\mathbf{\frac{g_m}{I_D} = 10 \rightarrow get\ g_m = 100\ \mu S.}$**
- **Then then from $\mathbf{\frac{g_m}{g_{ds}}}$ Chart $\rightarrow$ get L.**
- **The Design of the Current Mirror Load is Determined by CMIR, noise, and Output Swing Specs.**
  - $\mathbf{CMIR_{HIGH} = V_{DD} - |V_{GS_3}| + V_{GS_1} - V_{dsat_1} < 1.5\ V.}$
- **Get $\mathbf{V_{GS_1}}$ and $\mathbf{V_{dsat_1}}$ (or Use $\mathbf{V_1^*}$)**
  - $\mathbf{1.5 = V_{DD} - |V_{GS_3}| + V_{GS_1} - V_{dsat_1}}$
- **Go to $\mathbf{\frac{I_D}{W}}$ Chart $\rightarrow$ Get W**

❖Design of Tail Current Source. (Using ADT NMOS Charts)

- $\mathbf{A_{vCM} = \frac{V_{out}}{V_{ICM}} \approx -\frac{1}{2g_{m_{3,4}}R_{SS}}}$, $\mathbf{R_{ss} = r_o > 500\ k\Omega, g_{ds} < 2\ \mu S.}$
- $\mathbf{CMRR = \frac{A_v}{A_{vCM}} \approx g_{m_{1,2}}(r_{o_1} // r_{o_2}).2g_{m_{3,4}}R_{SS}}$
- $\mathbf{\lambda = \frac{g_{ds}}{I_D}}$ **Slightly Increase With $\mathbf{\frac{g_m}{I_D}}$ (Weak Dependence).**
- **Assume an Arbitrary but Large $\mathbf{\frac{g_m}{I_D} \rightarrow get\ L}$**
- $\mathbf{CMIR_{LOW} = V_{GS_b} + V_{dsat_0} = 0.8\ V.}$
- **The Tail Current Source Has Double the Current.**
- **Going to the $\mathbf{\frac{I_D}{W}}$ Chart $\rightarrow$ get W.**

Table Showing $W, L, g_m, I_D, \frac{g_m}{I_D}, V_{dsat}, V_{ov} = V_{GS} - V_{th}, V^* = \frac{2I_D}{g_m}$ For All Transistors $\left(\text{As Calculated From } \frac{g_m}{I_D} \text{ Curves}\right)$

- **From the Design Charts:**

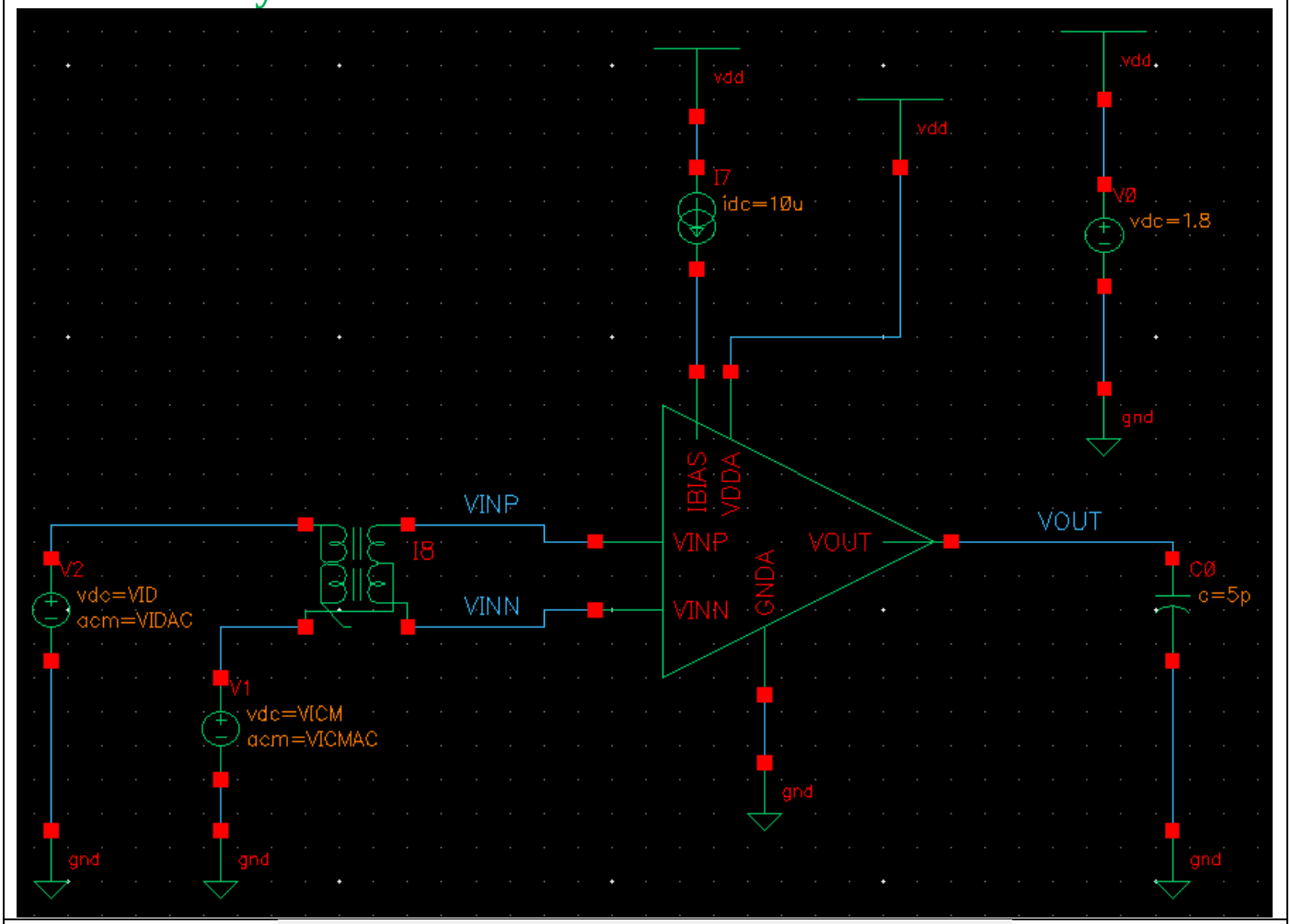
Transistors	Input Pair M1 & M2	Current Mirror Loads M3 & M4	Tail Current Source	
			M0	Mb
W	$3.8\ \mu m.$	$4.2\ \mu m.$	$6.3\ \mu m.$	$3.14\ \mu m.$
L	$570\ nm.$	$535\ nm.$	$1.4\ \mu m.$	$1.4\ \mu m.$
g_m	$160\ \mu S.$	$100\ \mu S.$	$200\ \mu S.$	$100\ \mu S.$
I_D	$10\ \mu A.$	$10\ \mu A.$	$20\ \mu A.$	$10\ \mu A.$
$\frac{g_m}{I_D}$	16	10	10	10
V_{dsat}	$98\ mV.$	$167\ mV.$	$158\ mV.$	$158\ mV.$
$V_{ov} = V_{GS} - V_{th}$	$114\ mV.$	$195\ mV.$	$165\ mV.$	$165\ mV.$
$V^* = \frac{2I_D}{g_m}$	$125\ mV.$	$200\ mV.$	$200\ mV.$	$200\ mV.$

Part 3

Open Loop OTA Simulation

Schematic

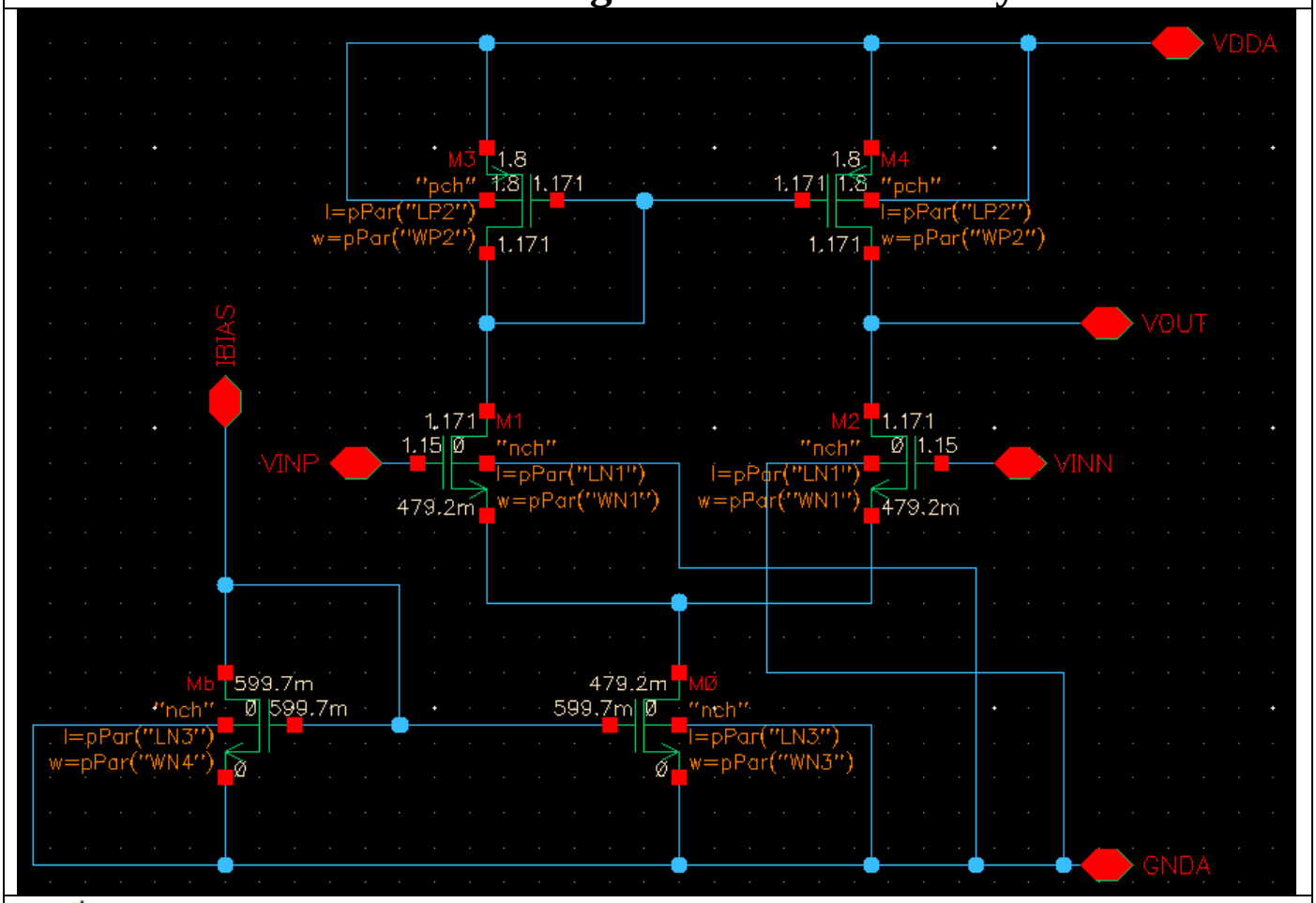
(1) Schematic of the OTA with DC node voltages clearly annotated.



LN1	570n
LN3	1.4u
LP2	535n
WN1	3.8u
WN3	6.3u
WN4	3.14u
WP2	4.2u

Hide | Cancel | Defaults | Help

DC Node Voltages Annotated Clearly



DC Analysis

Global Variables	
VICM	1.15
VICMAC	0
VID	0
VIDAC	0

Is the current (and g_m) in the input pair exactly equal? (YES).

- **Yes, Currents and g_m are the Same.**

IEEE_Workshop:LAB_7_PART_3_tb:1	gm_M1	163.6u
IEEE_Workshop:LAB_7_PART_3_tb:1	gm_M2	163.6u
IEEE_Workshop:LAB_7_PART_3_tb:1	ID_M1	9.956u
IEEE_Workshop:LAB_7_PART_3_tb:1	ID_M2	9.956u

$$g_{m_1} = g_{m_2} = 163.6\ \mu S.$$
$$I_{D_1} = I_{D_2} = 9.956\ \mu A.$$

- **What is DC voltage at VOUT? Why?**

VOUT

	VIDAC	VOUT (V)
1	0.000	1.171

- **Simulation: VOUT $= 1.171$ V its Constant Value for VOUT as We Run DC Analysis With VICM $= 1.15$ V Approximatly Equals VOUT As it's following the diode connected node.**

- **Hand Analysis: $\mathbf{VOUT_{DC} = V_{DD} - V_{GS_{3,4}} = 1.8 - 0.629 = 1.171\ V}$.**

(2) Diff. Small Signal CCS: -

- **AC Analyis**

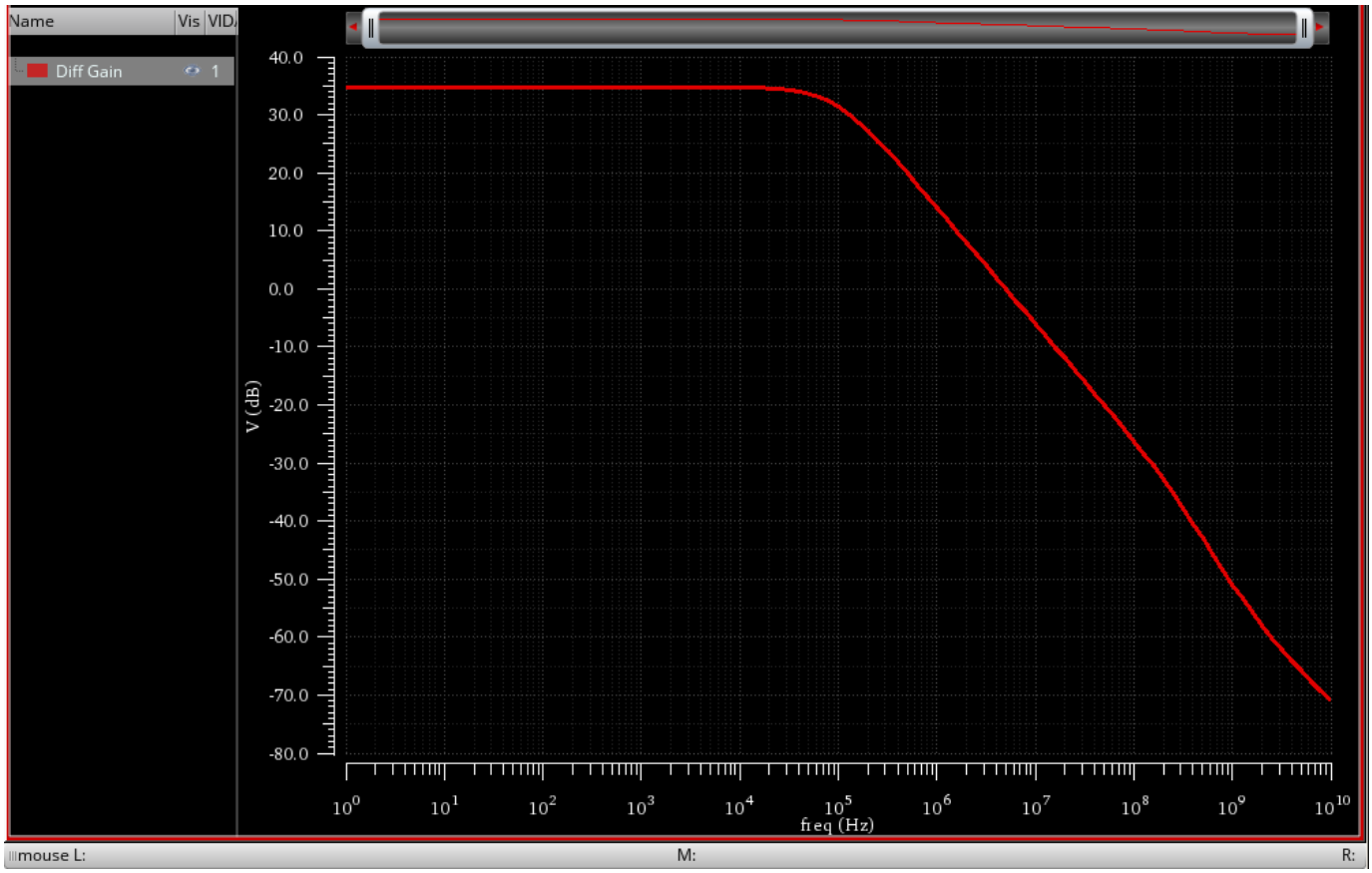
Global Variables

VICM	1.15
VICMAC	0
VID	0
VIDAC	1

Test	Name	Type	Details	EvalType	Plot	Save
IEEE...	Ao	expr	ymax(mag(v("/VOUT" ?result "ac")))	point	☑	☐
IEEE...	Ao_dB	expr	dB20(ymax(mag(v("/VOUT" ?result "...	point	☑	☐
IEEE...	BW	expr	bandwidth(mag(v("/VOUT" ?result "a...	point	☑	☐
IEEE...	fu	expr	unityGainFreq(mag(v("/VOUT" ?resu...	point	☑	☐
IEEE...	GBW	expr	(Ao * BW)	point	☑	☐

Test	Output	Nominal
IEEE_Workshop:LAB_7_PART_3_tb:1	Ao	56.35
IEEE_Workshop:LAB_7_PART_3_tb:1	Ao_dB	35.02
IEEE_Workshop:LAB_7_PART_3_tb:1	BW	90.92k
IEEE_Workshop:LAB_7_PART_3_tb:1	fu	5.143M
IEEE_Workshop:LAB_7_PART_3_tb:1	GBW	5.123M

Plot diff gain (in dB) vs frequency.



Compare simulation results with hand calculations in a table.

Specs.	Simulation	Hand Analysis
A_o	56.35	$g_{m_{1.2}} * \frac{r_o}{2} = 55.64$
$A_{o_{dB}}$	35.02 dB	34.01 dB.
BW	90.92 KHZ	$\frac{1}{2\pi R C_L} = 95.5$ KHZ
fu	5.143 MHZ	$\frac{g_m}{2\pi C_L} = 5.21$ MHZ
GBW	5.123 MHZ	$A_v * BW = 5.31$ MHZ

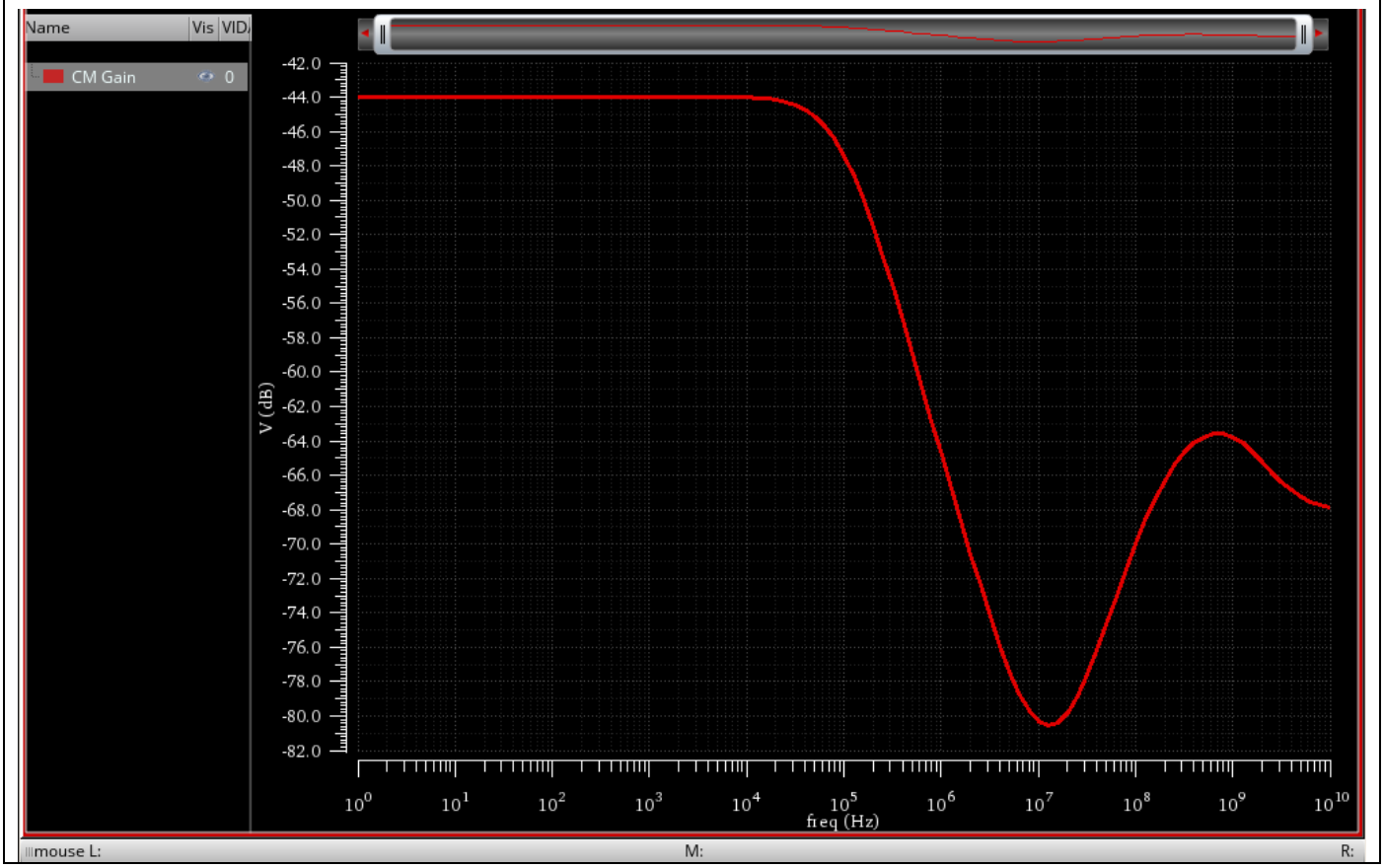
(3) CM Small CCS: -

AC Analysis

Global Variables

VICM	1.15
VICMAC	1
VID	0
VIDAC	0

Plot CM gain in dB vs frequency.

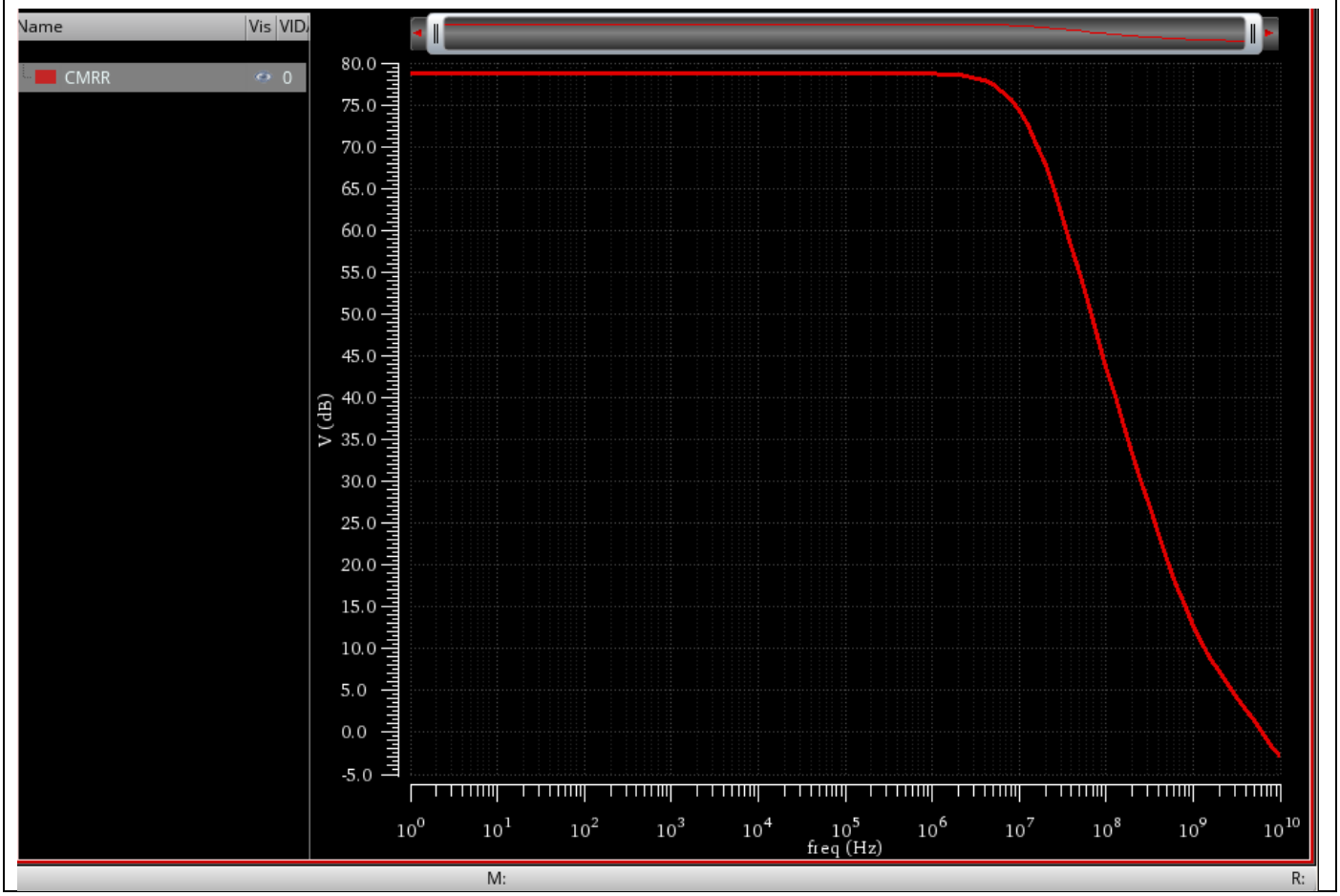


Compare simulation results with hand calculations in a table.

Test	Output	Nominal
IEEE_Workshop:LAB_7_PART_3_tb:1	Ao	6.382m
IEEE_Workshop:LAB_7_PART_3_tb:1	Ao_dB	-43.9
IEEE_Workshop:LAB_7_PART_3_tb:1	BW	90.93k
IEEE_Workshop:LAB_7_PART_3_tb:1	GBW	580.3
IEEE_Workshop:LAB_7_PART_3_tb:1	CM Gain	

Specs.	Simulation	Hand Analysis
$\mathbf{A_o}$	$\mathbf{6.382m}$	$\mathbf{\frac{1}{2g_{m_{3,4}}R_{ss}} = 6.11m}$
$\mathbf{A_{o_{dB}}}$	$\mathbf{-43.9\ dB}$	$\mathbf{-44.1\ dB}$

(4) CMRR

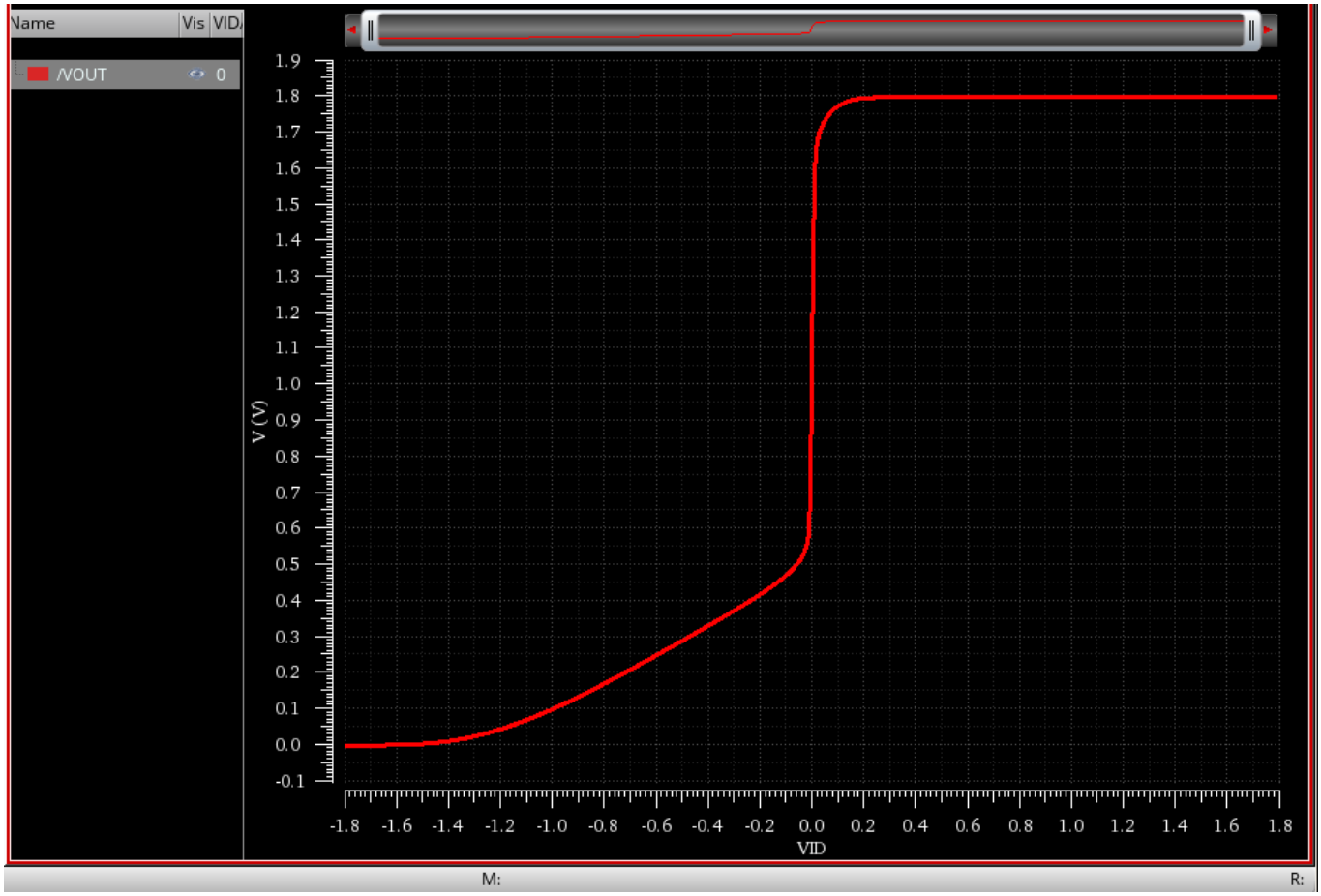


- **Compare simulation results with hand calculations in a table.**

Specs.	Simulation	Hand Analysis
CMRR	$78.919\ \text{dB}$	$2g_{m_{3,4}}R_{ss}g_{m_{1,2}} * \frac{r_o}{2} = 78.172\ \text{dB}$

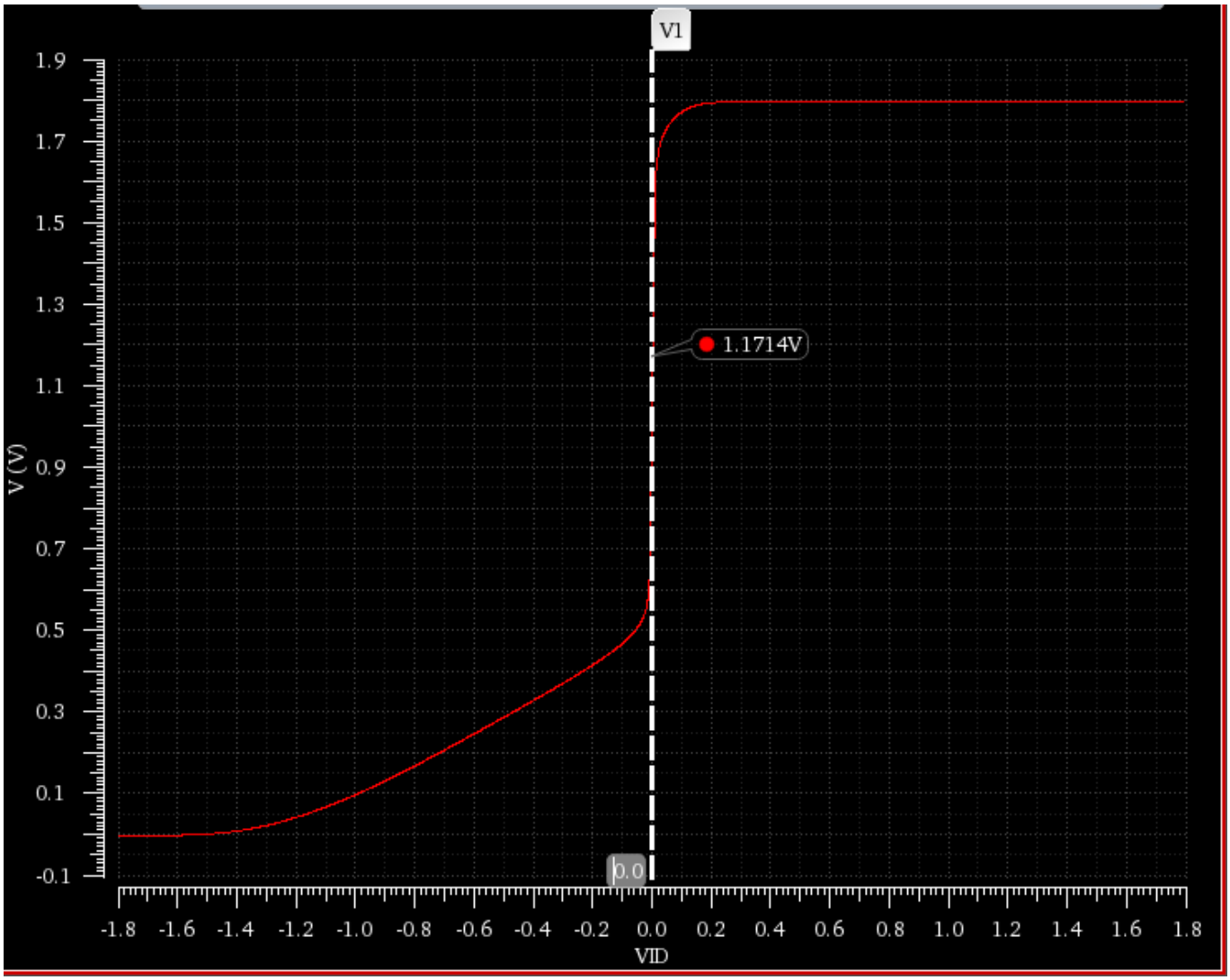
(5) Diff large signal ccs: -

- **Plot VOUT vs VID.**

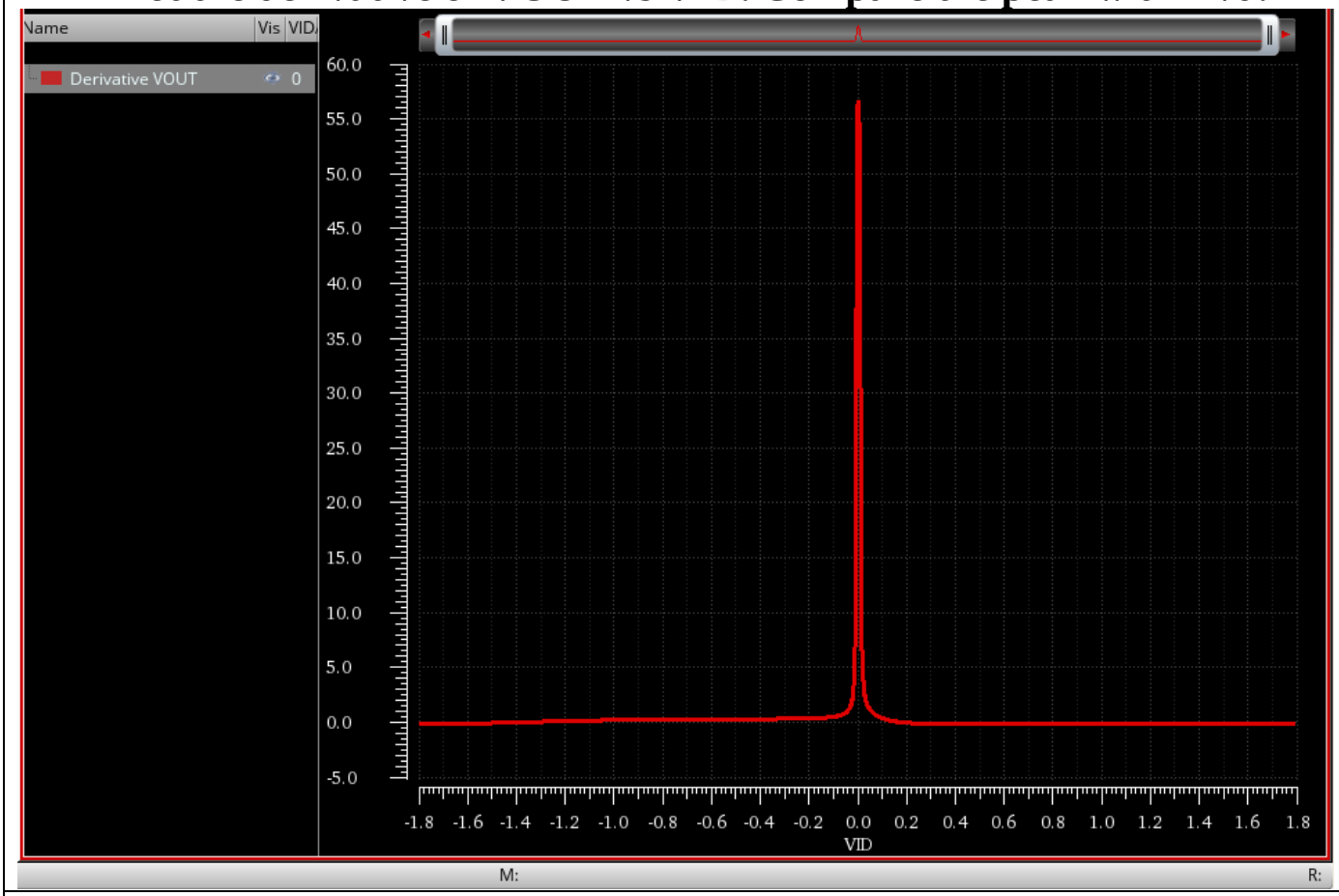


From the plot, what is the value of Vout at VID = 0? Why?

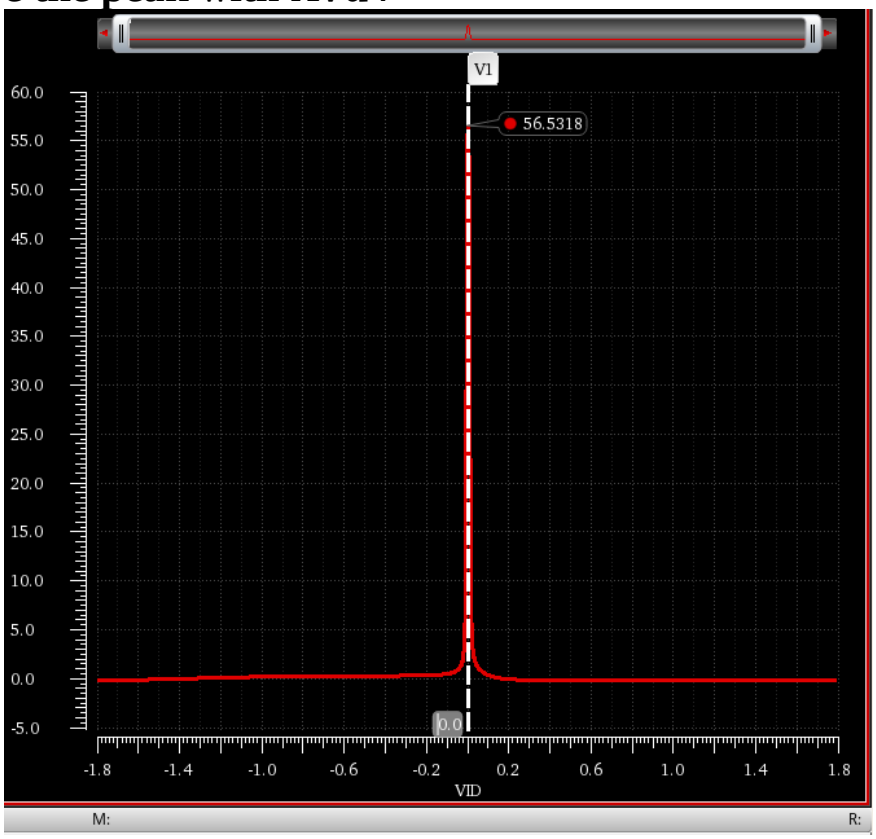
- **This Value is the Same like that we Get Before (DC Value). And its Following the Diode Connection.**
  $VOUT_{DC} = V_{DD} - V_{GS_{3,4}} = 1.8 - 0.629 = 1.171\ V.$



Plot the derivative of VOUT vs VID. Compare the peak with Avd.



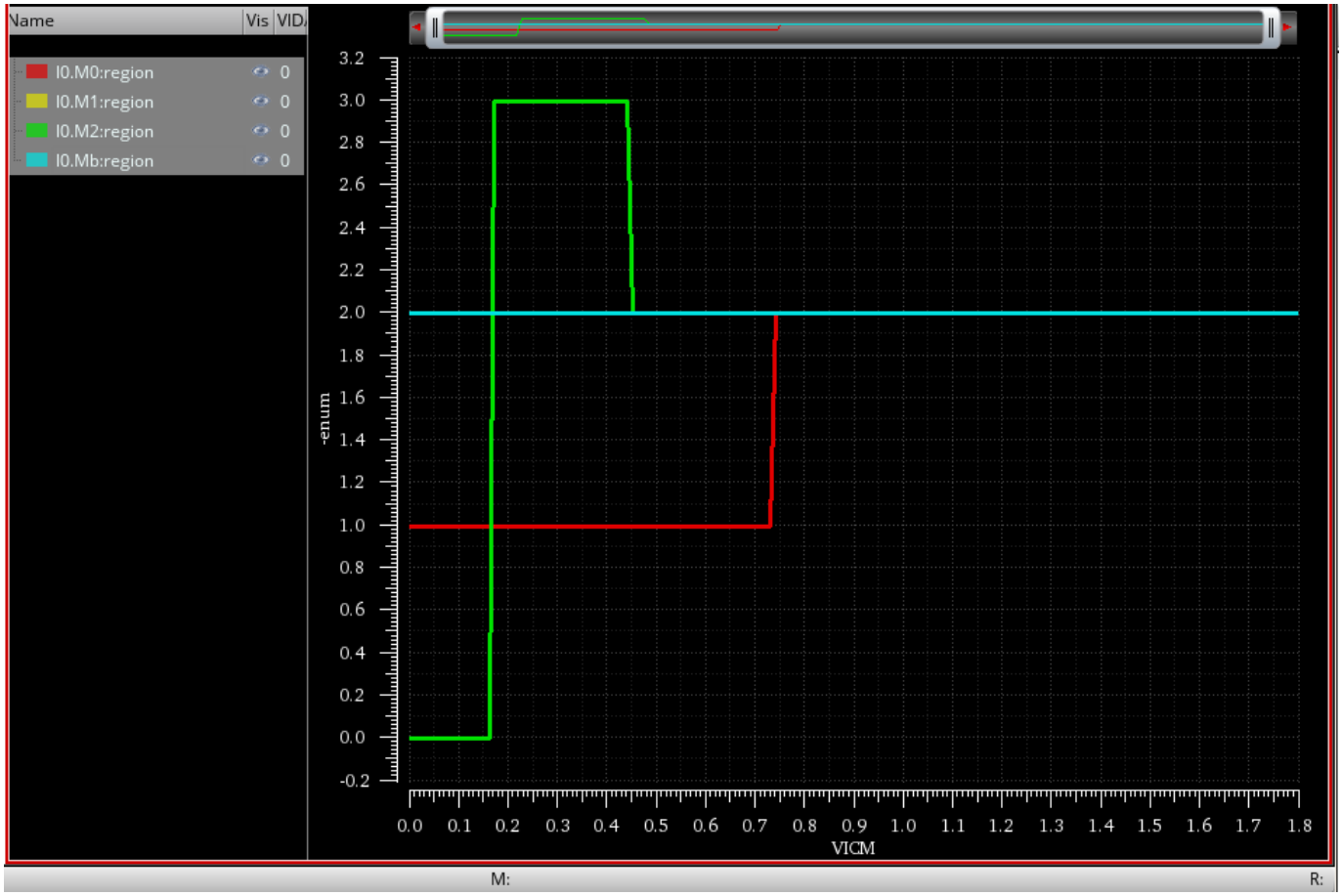
Compare the peak with Avd .



The Peak = 56.5318 Approximately equals to Avd = 56.35

(6) CM large signal ccs (region vs VICM): -

- **Plot "region" OP parameter vs VICM for the input pair and the tail current source (0 cut-off, 1 triode, 2 sat, 3 subth, and 4 breakdown).**

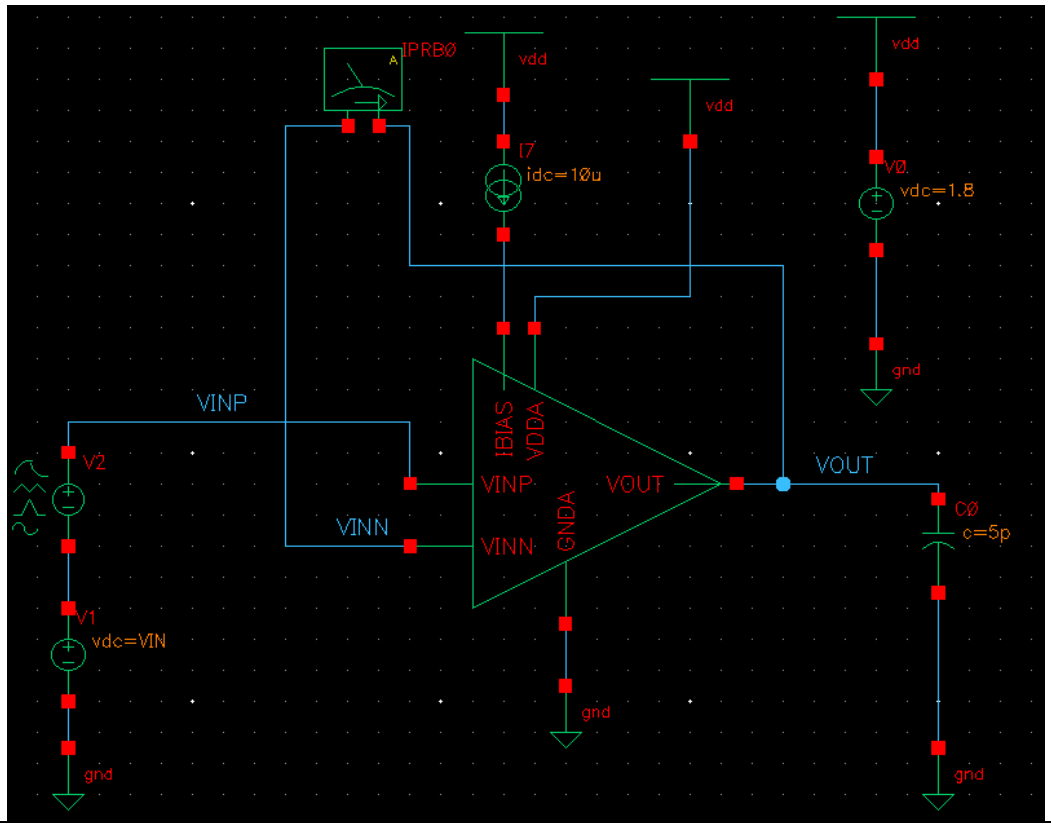


- **As We See input pair and the tail current source Transistors All in Saturation Region in VICM Range from $0.8\ V$ to V_{DD}.**

Part 4

Closed Loop OTA Simulation

Schematic



(1) Closed Loop

- **Is the current (and gm) in the input pair exactly equal? Why?**

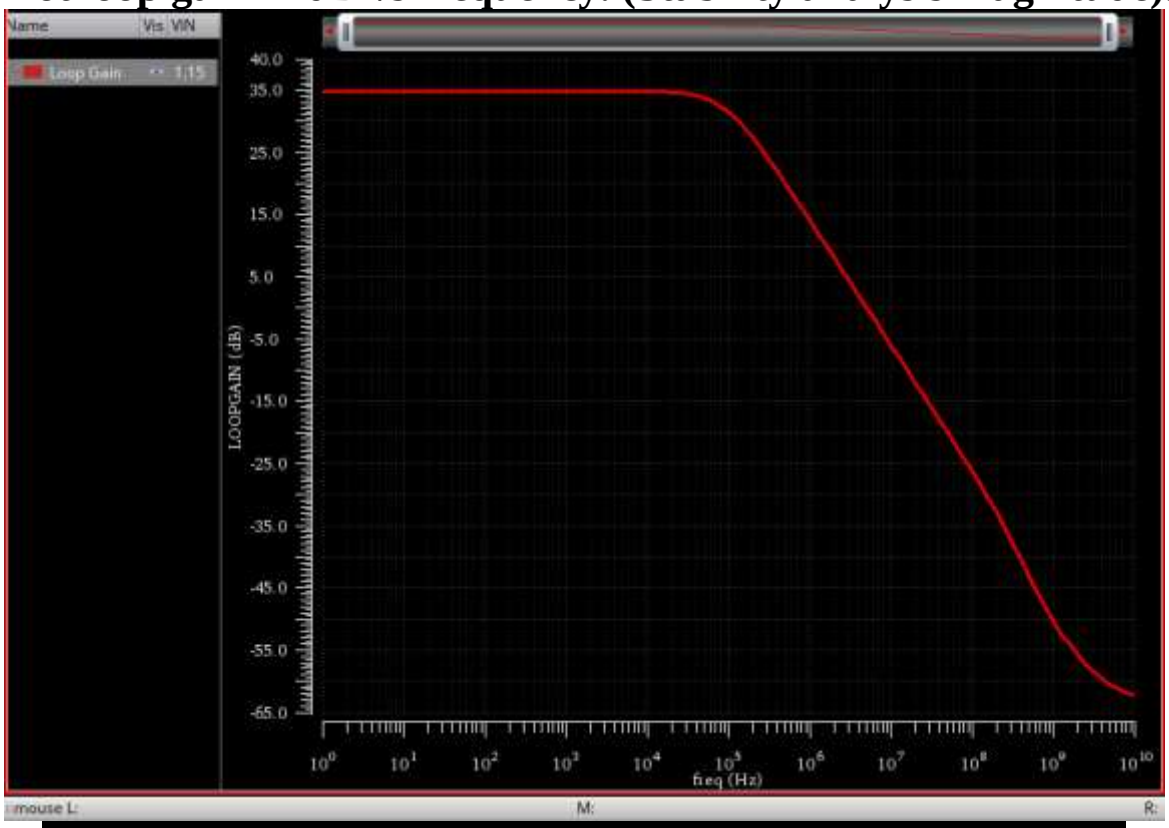
Test	Output	Nominal
IEEE_Workshop:LAB_7_PART_4_tb:1	ID_M1	9.498u
IEEE_Workshop:LAB_7_PART_4_tb:1	gm_M1	156.8u
IEEE_Workshop:LAB_7_PART_4_tb:1	ID_M2	9.877u
IEEE_Workshop:LAB_7_PART_4_tb:1	gm_M2	160.9u

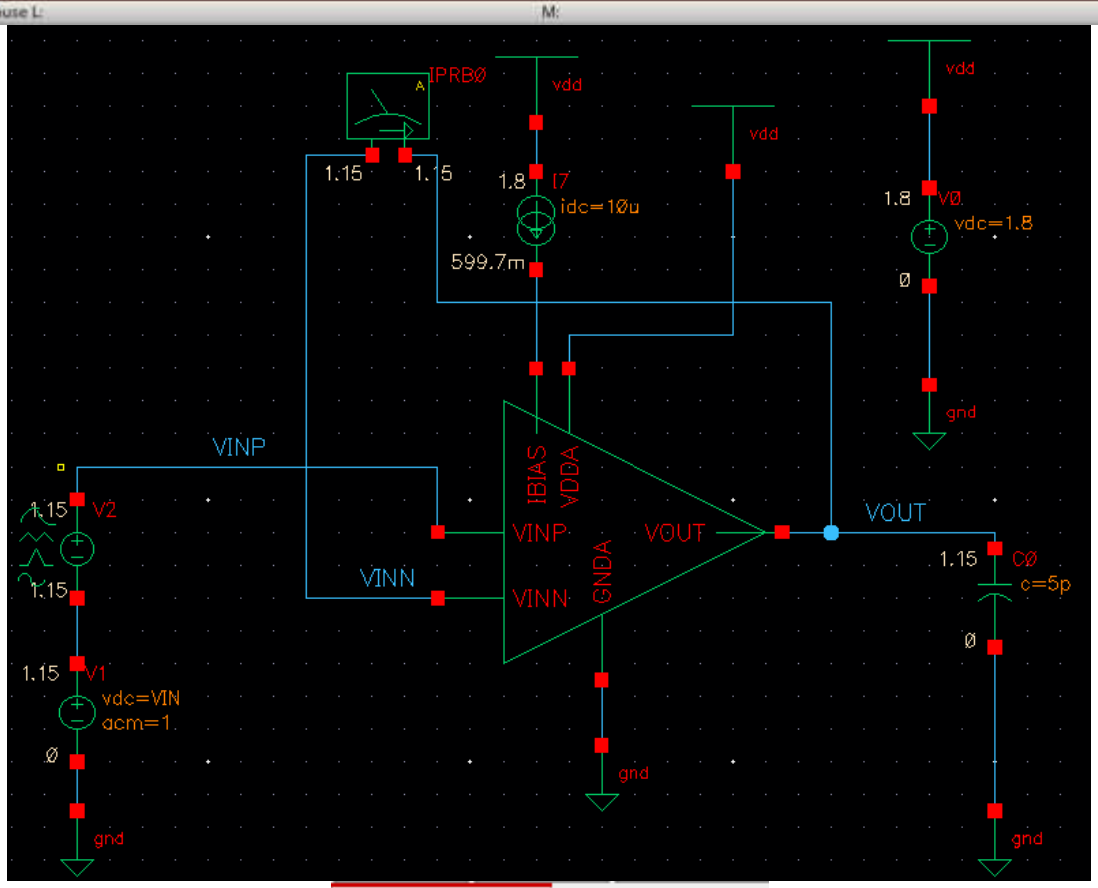
Not Equal, As the Feedback Loop Connected to Output Node Return to one of the Inputs, so V_{in} in two Inputs Not Equal.
therefore $I_1 \neq I_2$, $g_{m_1} \neq g_{m_2}$

- **Calculate the Mismatch in *ID* and gm.**
  - **Mismatch $(I_D) = 0.379\ \mu A = 379\ nA$.**
  - **Mismatch $(g_m) = 4.1\ \mu S$.**

(2) Loop Gain

- **Plot loop gain in dB vs frequency. (Stability analysis magnitude).**

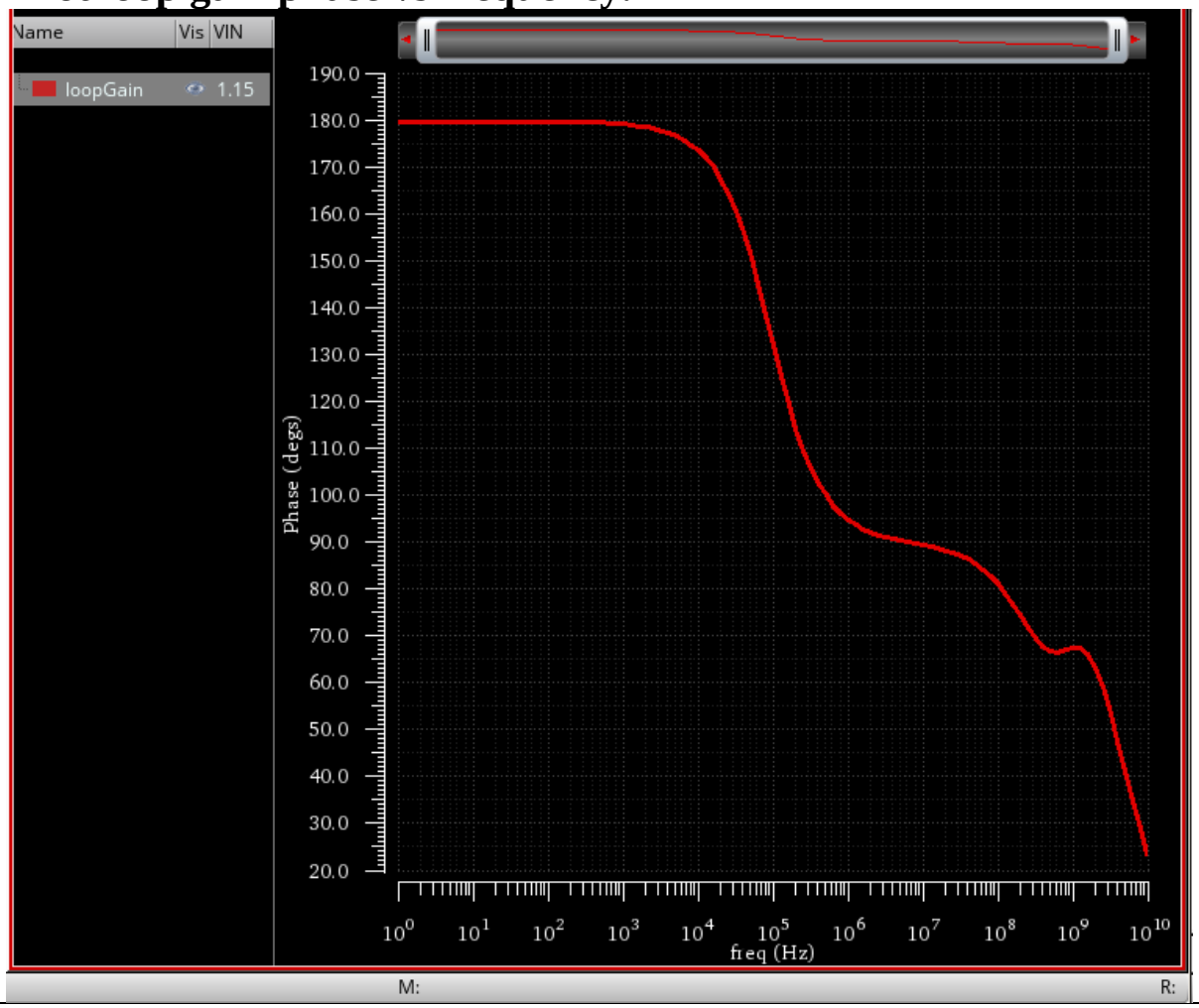




/phaseMargin

	VIN	/phase... (Deg)
1	1.150	90.55

- **Plot loop gain phase vs frequency.**



- **Compare DC gain and GBW with those obtained from open-loop simulation. Comment.**

GBW	5.117M
Phase Margin	90.55
DC Gain	56.5

Gain is the same of the open loop gain because the feedback is unity gain (Beta = 1).

- **Compare simulation results with hand calculations in a table.**

P.O.C	Simulation	Hand
DC Gain	56.5	$A_v * \beta = 56.35$
GBW	5.117 MHZ	$\frac{g_m}{2\pi C_L} = 5.1216$ MHZ

Specs. Achieved

Specs	Required	Achieved
DC Current (I_{REF})	10 µA.	
Supply (V_{DD})	1.8 V.	
Load	5 pF.	
Open loop DC Voltage gain	≥ 34 dB.	35.02 dB.
CMRR @ DC	≥ 74 dB.	78.92 dB.
Phase Margin	≥ 70°	90.55°
OTA Current Consumption	≤ 20 µA.	20 µA.
CM Input Range – Low	≤ 0.8 V.	0.75 V.
CM Input Range – High	≥ 1.5 V.	1.8 V.
GBW	≥ 5 MHZ.	5.117 MHZ.