Project (Deadline: Thursday May 11th, 2023)

For the 3 tasks, use the PDK of a UMC 0.13µm technology:

Task #1 (10 marks):

For an NMOS with Drain and Gate connected to $V_{DD} = 1.2V$ and Source connected to a current source $I_{REF} = 200\mu A$ to GND and Bulk connected to GND. Sweep W from W=L to W=100L.

1. For the parameters:
   - V_{th}
   - V_{ov}
   - V_{DSAT}
   - $g_m r_o$

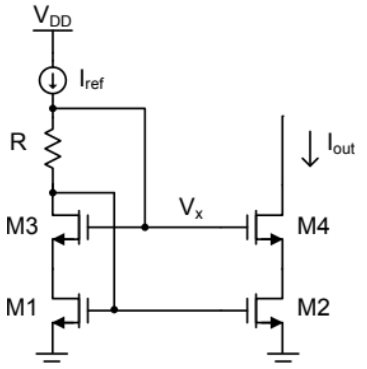
   Plot each of these parameters vs W/L at L=L_{min}, L=2L_{min}, L=4L_{min}, and L=8L_{min} for the following devices:
   - **N_12_HS_L130E** (high-speed NMOS)
   - **N_LV_12_HS_L130E** (Low-Vth high-speed NMOS)

   (For each parameter, insert 2 figures next to each other, each having the 4 parametric curves for one of the 2 devices) (8 marks)
2. **Mention** the long-channel equation for V_{th}, V_{ov}, & $g_m r_o$. Is the trend of the simulations similar to the equations? (1 mark)
3. **Mention one** advantage and **one** disadvantage for **N_LV_12_HS_L130E** compared to **N_12_HS_L130E**. What do you recommend to be used in a **high-gain amplifier**? (1 mark)

Task #2 (10 marks):

Use the NMOS core high speed HS transistor (**N_12_HS_L130E**) and the poly resistor (**RNPPO_MML130E**) to design an accurate high-swing current mirror (according to the architecture shown) operating at $V_{DD} = 1.2V$ with the following specifications:

- $I_{out} = 2I_{REF} = 200\mu A$, with error $< 1\%$ @V_{out}=500mV
- $V_{comp} \leq 350mV$ (defined as the minimum output voltage required for all devices to operate in saturation)
- $R_{out} \geq 500k\Omega$ @ $V_{out} = 500mV$



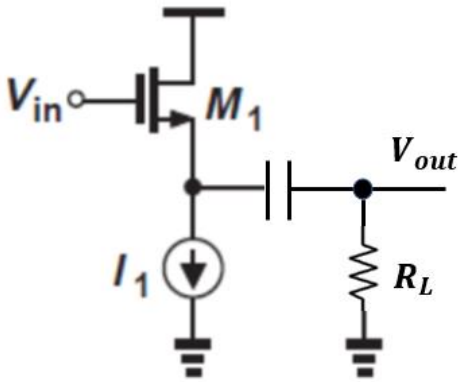
The documentation of your design must include the following:

1. Schematic diagram with dimensions and component values annotated. (1 mark)
2. Schematic diagram with DC operating point annotated at V_{out}=350mV to verify the V_{comp} specification. (2 marks)
3. Simulation results to verify I_{out} and R_{out} specifications (4 marks)
4. An estimate of this mirror's area. (1 mark)
5. If your manager told you the area you ended up with is too large and you need to sacrifice one of the specs to have reasonable area, suggest a modification and comment on what you'll gain and lose from it. (2 marks)

Task #3 (10 marks):

Use the NMOS core high voltage RF transistor (**N_33_RF**), an ideal current source, and an ideal DC blocking cap of 1µF to design a class A Power Amplifier (according to the architecture shown) operating at $V_{DD} = 3.3V$ with the following specifications:

- $V_{in,DC} = 2.3V$
- $V_{in,AC} = \mathrm{A}\sin(2\pi ft)\,, f = 50MHz, A = 1V$
- $R_L = 50\Omega$
- $\left|V_{out,peak}\right| > 650mV$
- Output signal linearity is characterized as $\frac{|V_{out,max}|-|V_{out,min}|}{V_{out,max}} < 5\%$



The documentation of your design must include the following:

1. Schematic diagram with dimensions and component values annotated. (1 mark)
2. Schematic diagram with DC operating point annotated. (1 mark)
3. Transient simulation results to verify the required specifications:
   a. Plot a complete period of V_{out} vs time at the given frequency. (1 mark)
   b. Plot a complete period of the current flowing in the main device to make sure the device doesn't turn off. (1 mark)
4. Calculation of the efficiency using simulations and compare it with the theoretical equation. (2 marks)
5. Replace the ideal current source with a current mirror with $I_{REF} = 10mA$ using **N_33_RF** device, design the mirror using a suitable topology of your choice, and plot V_{out} and $I_{main\ device}$. Did the linearity degrade? Why/why not? (4 marks)

Assessment:

- The total grade of this project is 30 points.
- Maximum number of students per group is 3.
- You are required to deliver a pdf report that clearly describes your work, including all the required items.
- Report size should not exceed 20 pages.