Cadence Virtuoso
LAB (1) Report

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Analog IC Design

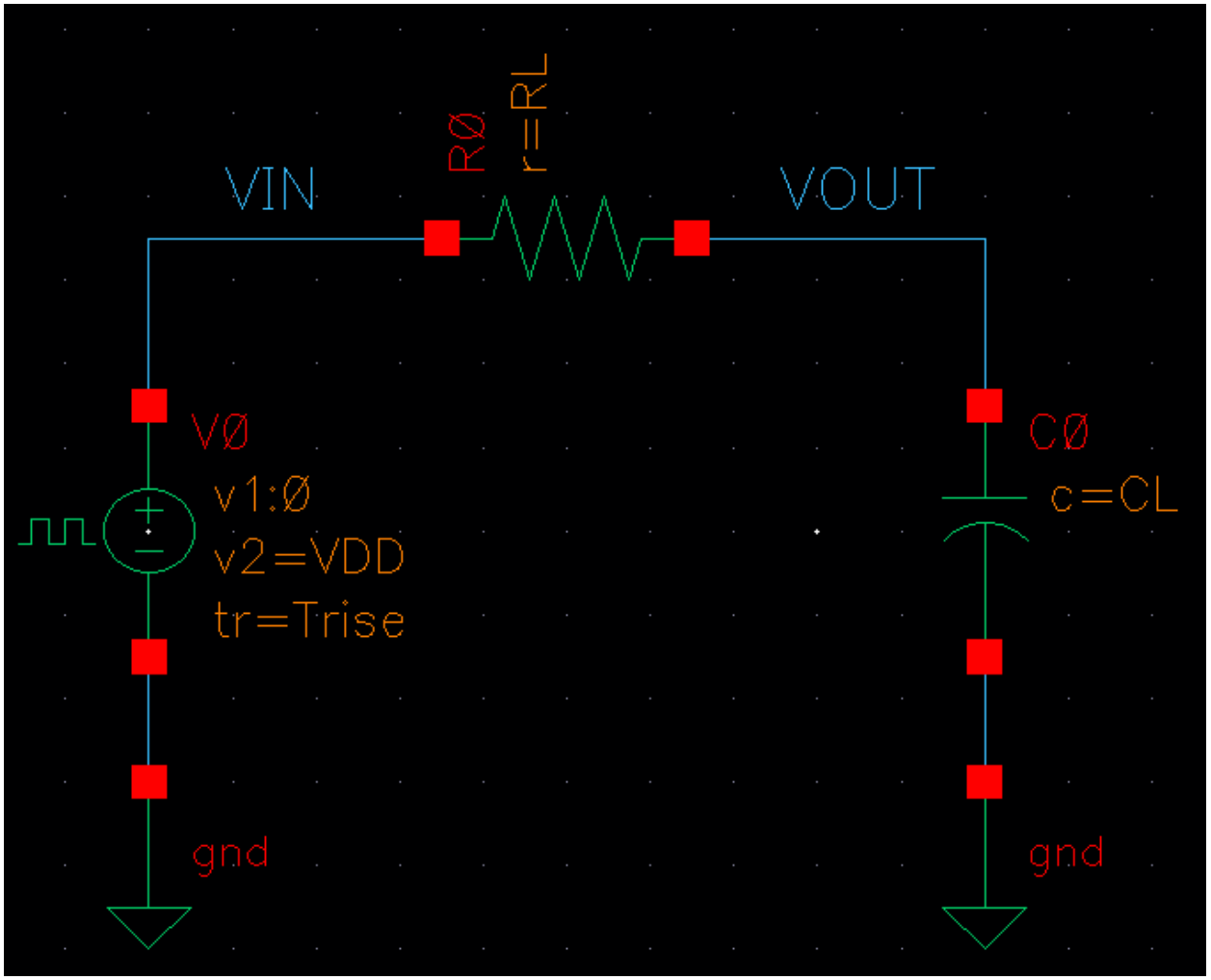
Contents: -

Part 1

Low Pass Filter Simulations

Transient Analysis for Two Periods

Q1



This is The Schematic of LPF With V_{pulse}

Q2

Voltage Pulse

Voltage 1	0 V
Voltage 2	VDD V
Period	TCLK s
Delay time	TDEL s
Rise time	Trise s
Fall time	Tfall s
Pulse width	TCLK/2 s

Capacitor $C_L = \frac{\tau}{R_L}$

Capacitance	CL F

Resistor R_L

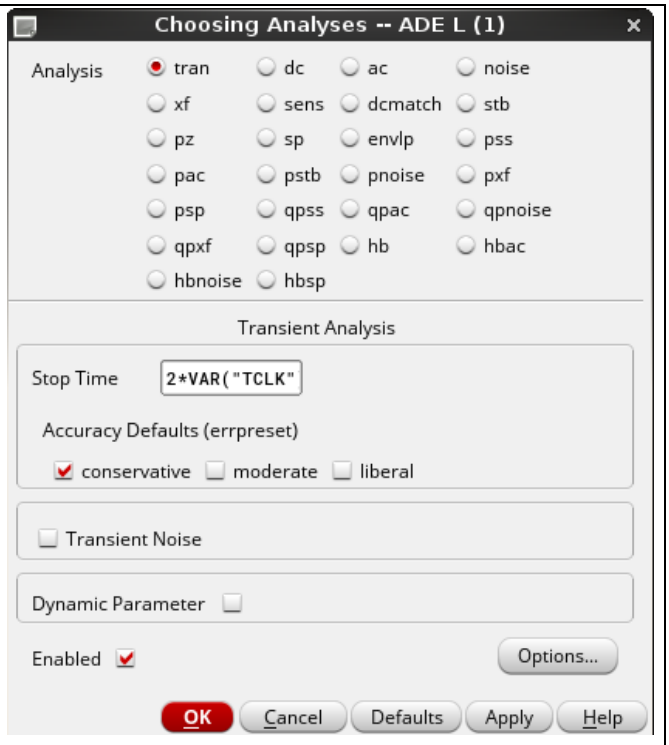
Resistance	RL Ohms

Variables Values

Global Variables	
CL	0.3p
RL	1k
TCLK	20n
TDEL	5n
Tfall	100p
Trise	100p
VDD	1
Click to add variable	

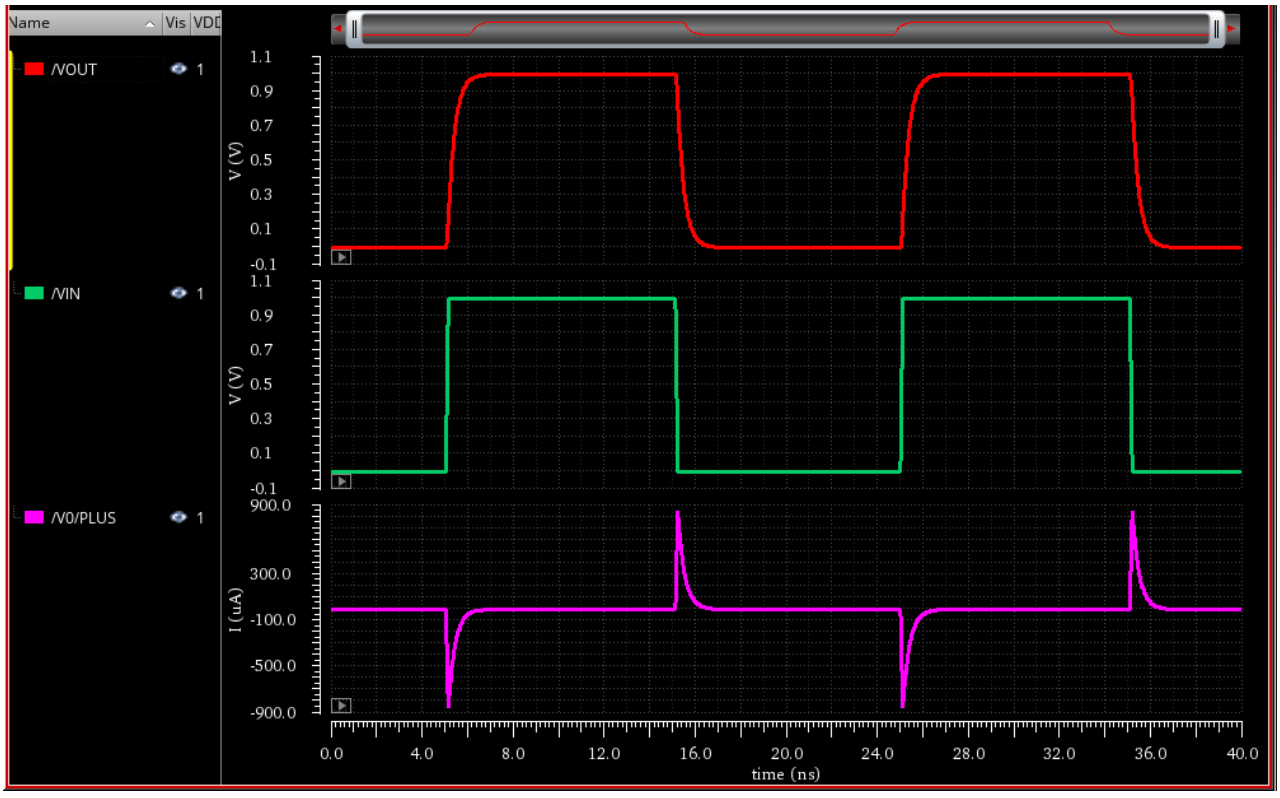
$$T_{clock} = 20n\ ,\ T_{delay} = 5n\ ,\ T_{rise} = T_{fall} = 100p\ ,\ \text{Pulse width} = 10n$$

$T_{max}steps = 0.2n$



$T_{stop} = 2 * T_{clock} = 40n$

Q3



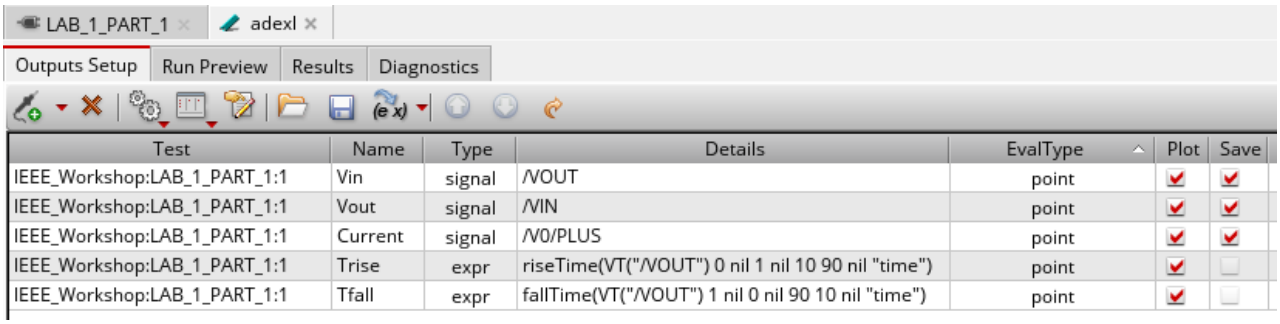
Red Curve = V_{out} , Green Curve = V_{in} , Pink Curve = Current

Q4

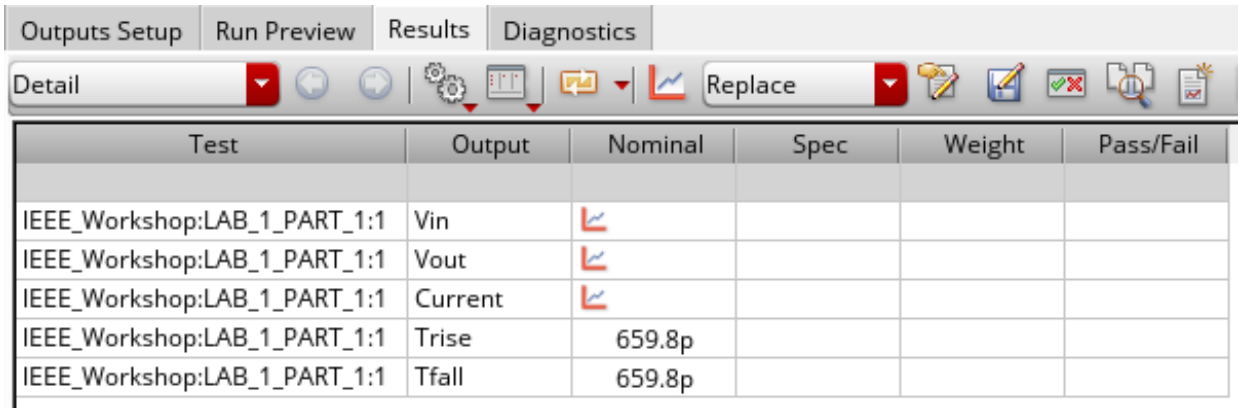
```
riseTime(VT("/VOUT") 0 nil 1 nil 10 90 nil "time" )
```

```
fallTime(VT("/VOUT") 1 nil 0 nil 90 10 nil "time" )
```

Transient Analysis Output Setup:



Test	Name	Type	Details	EvalType	Plot	Save
IEEE_Workshop:LAB_1_PART_1:1	Vin	signal	/VOUT	point	☑	☑
IEEE_Workshop:LAB_1_PART_1:1	Vout	signal	/VIN	point	☑	☑
IEEE_Workshop:LAB_1_PART_1:1	Current	signal	/V0/PLUS	point	☑	☑
IEEE_Workshop:LAB_1_PART_1:1	Trise	expr	riseTime(VT("/VOUT") 0 nil 1 nil 10 90 nil "time")	point	☑	☐
IEEE_Workshop:LAB_1_PART_1:1	Tfall	expr	fallTime(VT("/VOUT") 1 nil 0 nil 90 10 nil "time")	point	☑	☐



Test	Output	Nominal	Spec	Weight	Pass/Fail
IEEE_Workshop:LAB_1_PART_1:1	Vin				
IEEE_Workshop:LAB_1_PART_1:1	Vout				
IEEE_Workshop:LAB_1_PART_1:1	Current				
IEEE_Workshop:LAB_1_PART_1:1	Trise	659.8p			
IEEE_Workshop:LAB_1_PART_1:1	Tfall	659.8p			

Q5

Q5: Comments:

According to the charts, during the transient stage of the square pulse's rise, the capacitor charges slowly. However, in the steady state, the capacitor behaves like an ideal open circuit, producing an output voltage that matches the input voltage. Likewise, during the transient phase, current flows through the circuit, but during steady state, the current decreases to almost zero because the capacitor functions as an open circuit.

Simulation Results: **We Find That rise Time = Fall Time = 659.8 pS**

Q5: Analytical Results: -

∵ In Capacitor to Get Rising Time (Cap. Charging).

$$V_{out} = V_o\left(1 - e^{-\frac{t}{\tau}}\right), \tau_{time\ Constant} = RC = 0.3\ nS, V_o = V_{DD} = 1\ V.$$

$$e^{-t/\tau} = 1 - \frac{V_{out}}{V_o} \quad , \quad t = -\tau \ln\left(1 - \frac{V_{out}}{V_o}\right).$$

- **For 90% @ $V_{out} = 0.9V_o$.**

$$V_{out} = 0.9V_o = V_o\left(1 - e^{-\frac{t_2}{\tau}}\right) \rightarrow 0.9 = \left(1 - e^{-\frac{t_2}{\tau}}\right)$$

$$t_2 = -\tau \ln(0.1) \quad \rightarrow \quad (i)$$

- **For 10% @ $V_{out} = 0.1V_o$**

$$V_{out} = 0.1V_o = V_o\left(1 - e^{-\frac{t_1}{\tau}}\right) \rightarrow 0.1 = \left(1 - e^{-\frac{t_1}{\tau}}\right)$$

$$t_1 = -\tau \ln(0.9) \quad \rightarrow \quad (ii)$$

From (i) & (ii)

$$\therefore t_{rise} = t_2 - t_1 = -\tau \ln(0.1) + \tau \ln(0.9) = 659.17\ p\ sec.$$

∵ In Capacitor to Get Falling Time (Cap. Discharging)

$$V_{out} = V_o\left(e^{-\frac{t}{\tau}}\right), \tau_{time\ Constant} = RC = 0.3\ nS, V_o = V_{DD} = 1\ V.$$

$$e^{-\frac{t}{\tau}} = \frac{V_{out}}{V_o} \quad , \quad t = -\tau \ln\left(\frac{V_{out}}{V_o}\right)$$

- **For 10% @ $V_{out} = 0.1V_o$.**

$$V_{out} = 0.1V_o = V_o\left(e^{-\frac{t_2}{\tau}}\right) \rightarrow 0.1 = \left(e^{-\frac{t_2}{\tau}}\right)$$

$$t_2 = -\tau \ln(0.1) \quad \rightarrow \quad (iii)$$

- **For 90% @ $V_{out} = 0.9V_o$**

$$V_{out} = 0.9V_o = V_o\left(e^{-\frac{t_1}{\tau}}\right) \rightarrow 0.9 = \left(e^{-\frac{t_1}{\tau}}\right)$$

$$t_1 = -\tau \ln(0.9) \quad \rightarrow \quad (iv)$$

From (iii) & (iv)

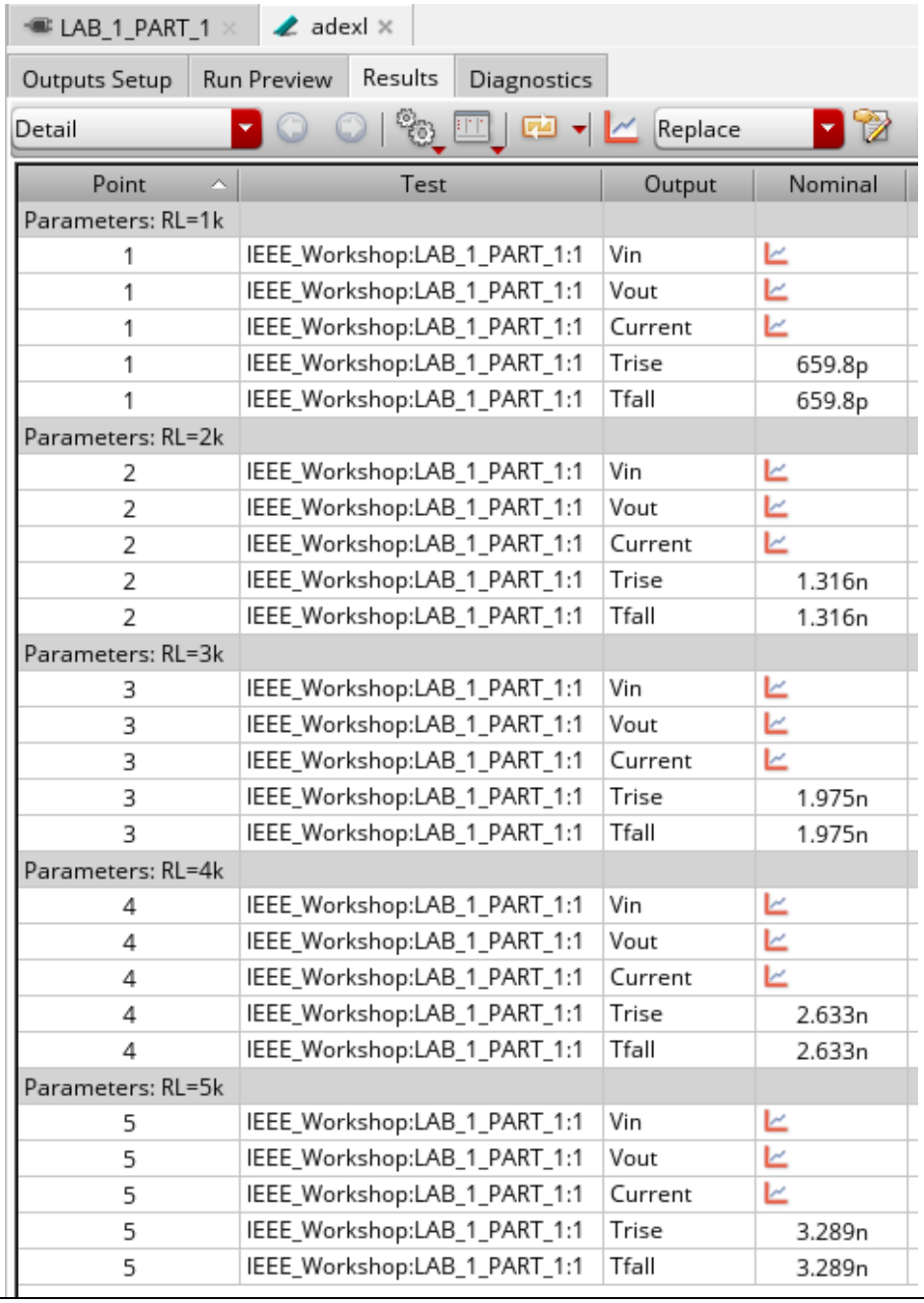
$$\therefore t_{fall} = t_2 - t_1 = -\tau \ln(0.1) + \tau \ln(0.9) = 659.17\ p\ sec.$$

$$t_{rise} = t_{fall}$$

P.O.C	Analytically	Simulation	Error
t_{rise}	659.17 p sec.	659.8 p sec.	0.1 %
t_{fall}	659.17 p sec.	659.8 p sec.	0.1 %

Q6

Parametric Sweep For R = 1: 1: 5 kΩ = Start : Step : Stop



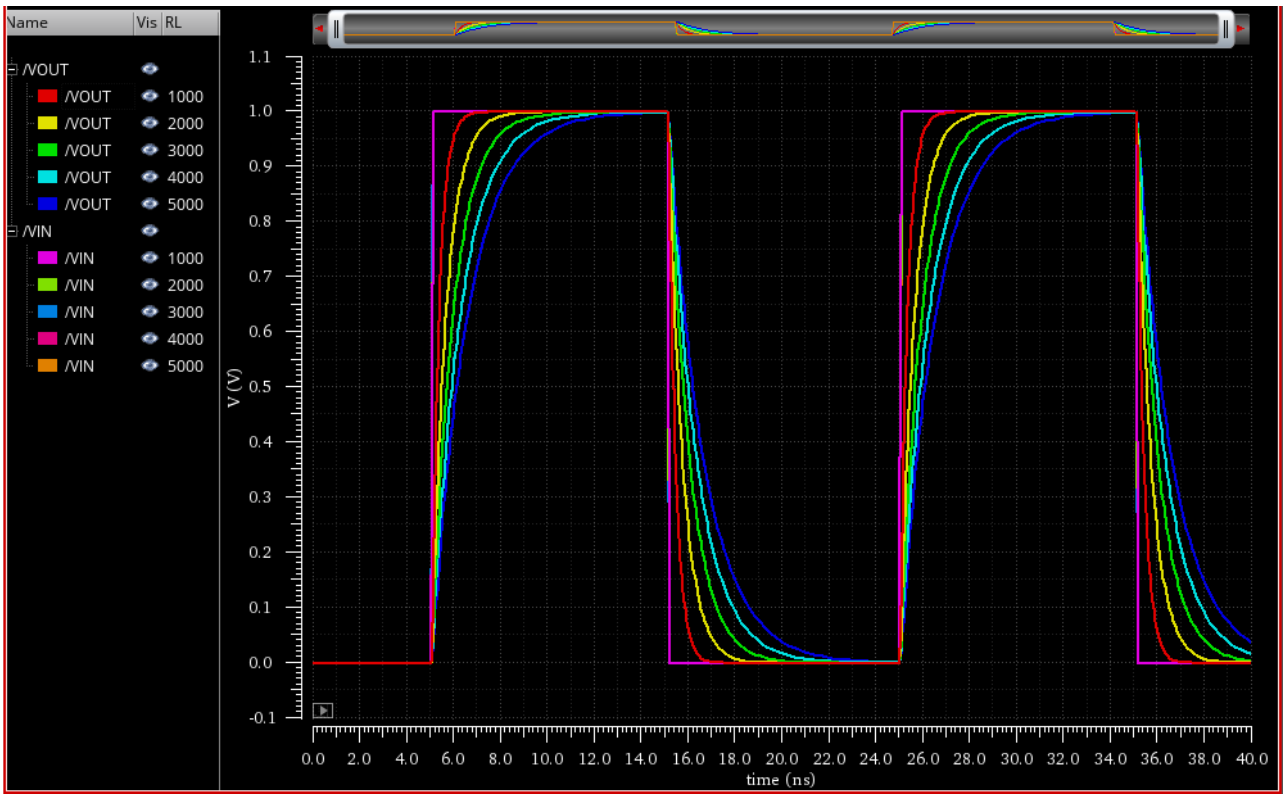
Point	Test	Output	Nominal
Parameters: RL=1k			
1	IEEE_Workshop:LAB_1_PART_1:1	Vin	
1	IEEE_Workshop:LAB_1_PART_1:1	Vout	
1	IEEE_Workshop:LAB_1_PART_1:1	Current	
1	IEEE_Workshop:LAB_1_PART_1:1	Trise	659.8p
1	IEEE_Workshop:LAB_1_PART_1:1	Tfall	659.8p
Parameters: RL=2k			
2	IEEE_Workshop:LAB_1_PART_1:1	Vin	
2	IEEE_Workshop:LAB_1_PART_1:1	Vout	
2	IEEE_Workshop:LAB_1_PART_1:1	Current	
2	IEEE_Workshop:LAB_1_PART_1:1	Trise	1.316n
2	IEEE_Workshop:LAB_1_PART_1:1	Tfall	1.316n
Parameters: RL=3k			
3	IEEE_Workshop:LAB_1_PART_1:1	Vin	
3	IEEE_Workshop:LAB_1_PART_1:1	Vout	
3	IEEE_Workshop:LAB_1_PART_1:1	Current	
3	IEEE_Workshop:LAB_1_PART_1:1	Trise	1.975n
3	IEEE_Workshop:LAB_1_PART_1:1	Tfall	1.975n
Parameters: RL=4k			
4	IEEE_Workshop:LAB_1_PART_1:1	Vin	
4	IEEE_Workshop:LAB_1_PART_1:1	Vout	
4	IEEE_Workshop:LAB_1_PART_1:1	Current	
4	IEEE_Workshop:LAB_1_PART_1:1	Trise	2.633n
4	IEEE_Workshop:LAB_1_PART_1:1	Tfall	2.633n
Parameters: RL=5k			
5	IEEE_Workshop:LAB_1_PART_1:1	Vin	
5	IEEE_Workshop:LAB_1_PART_1:1	Vout	
5	IEEE_Workshop:LAB_1_PART_1:1	Current	
5	IEEE_Workshop:LAB_1_PART_1:1	Trise	3.289n
5	IEEE_Workshop:LAB_1_PART_1:1	Tfall	3.289n

Q6: Comments: -

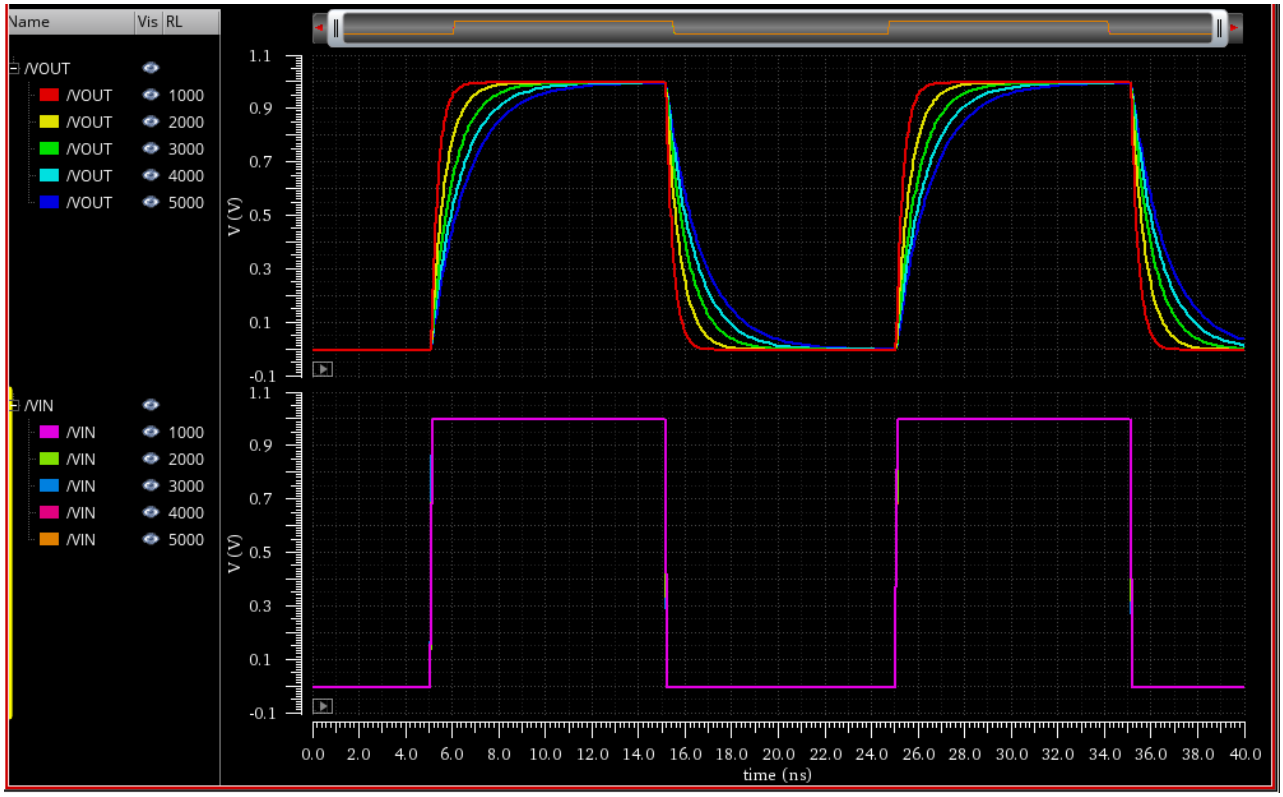
The rise and fall times increase as the resistance value increases, which aligns with our initial expectations. The analytical formulas indicate that the rise and fall times are directly related to the RC constant. Thus, as the resistance or capacitance values increase, the rise and fall times will also increase.

R	1 kΩ	2 kΩ	3 kΩ	4 kΩ	5 kΩ
T_{rise}	659.8p	1.316n	1.975n	2.633n	3.289n
T_{fall}	659.8p	1.316n	1.975n	2.633n	3.289n

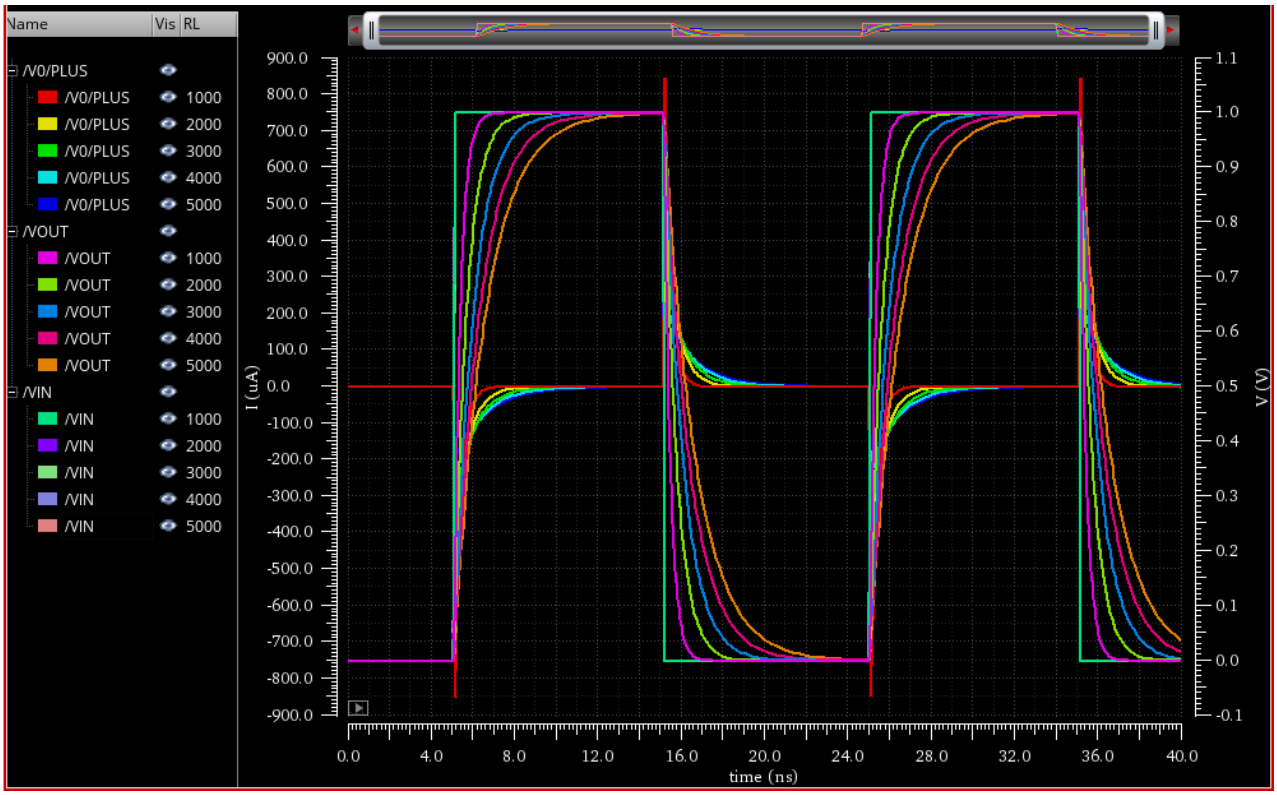
Overlaid Plotting V_{out} & V_{in}



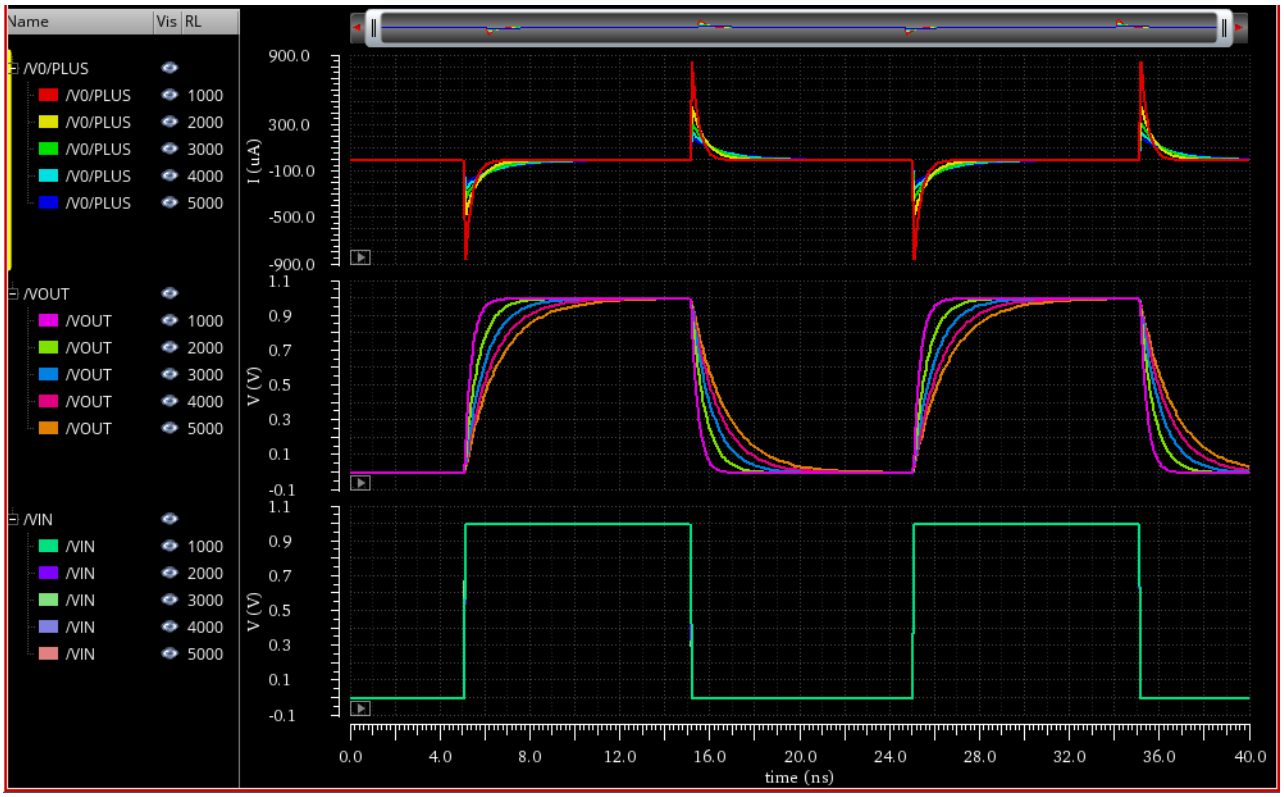
Q6



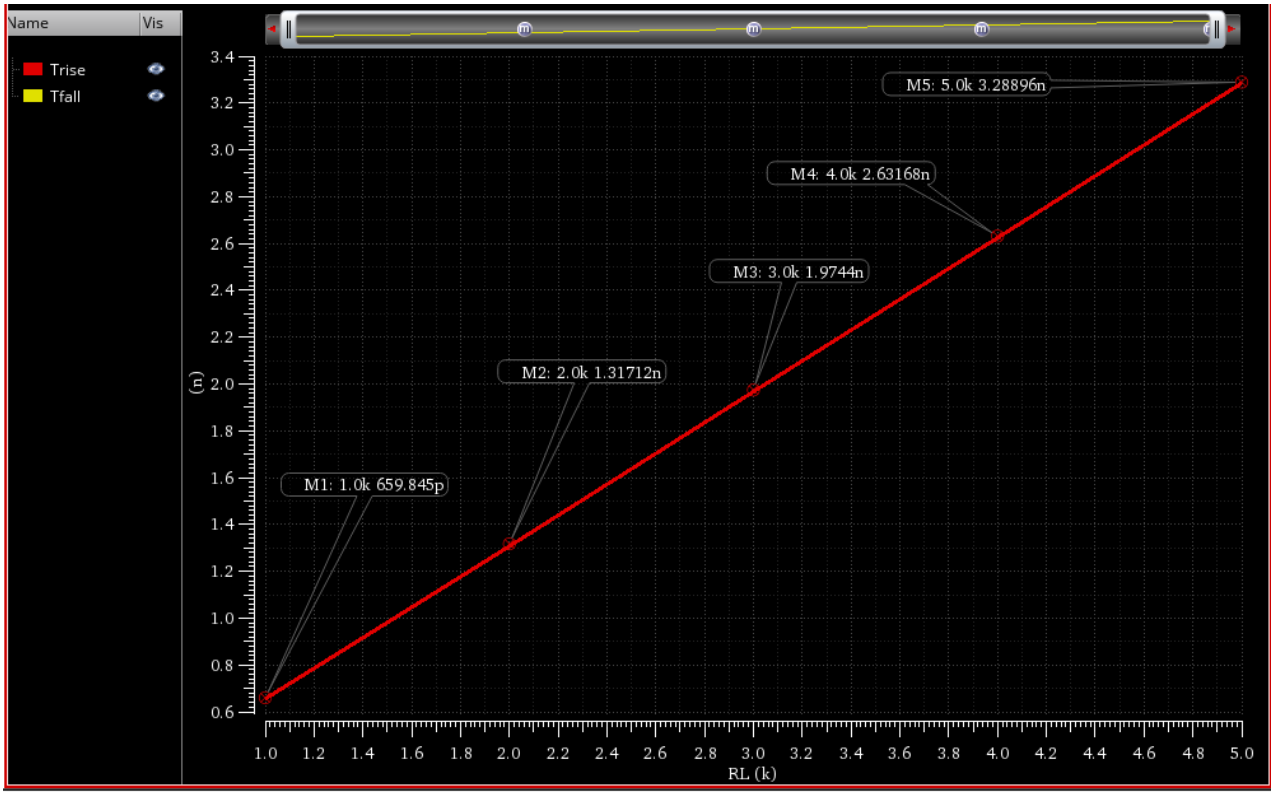
Overlaid Plotting V_{out} , V_{in} & Current



Q6

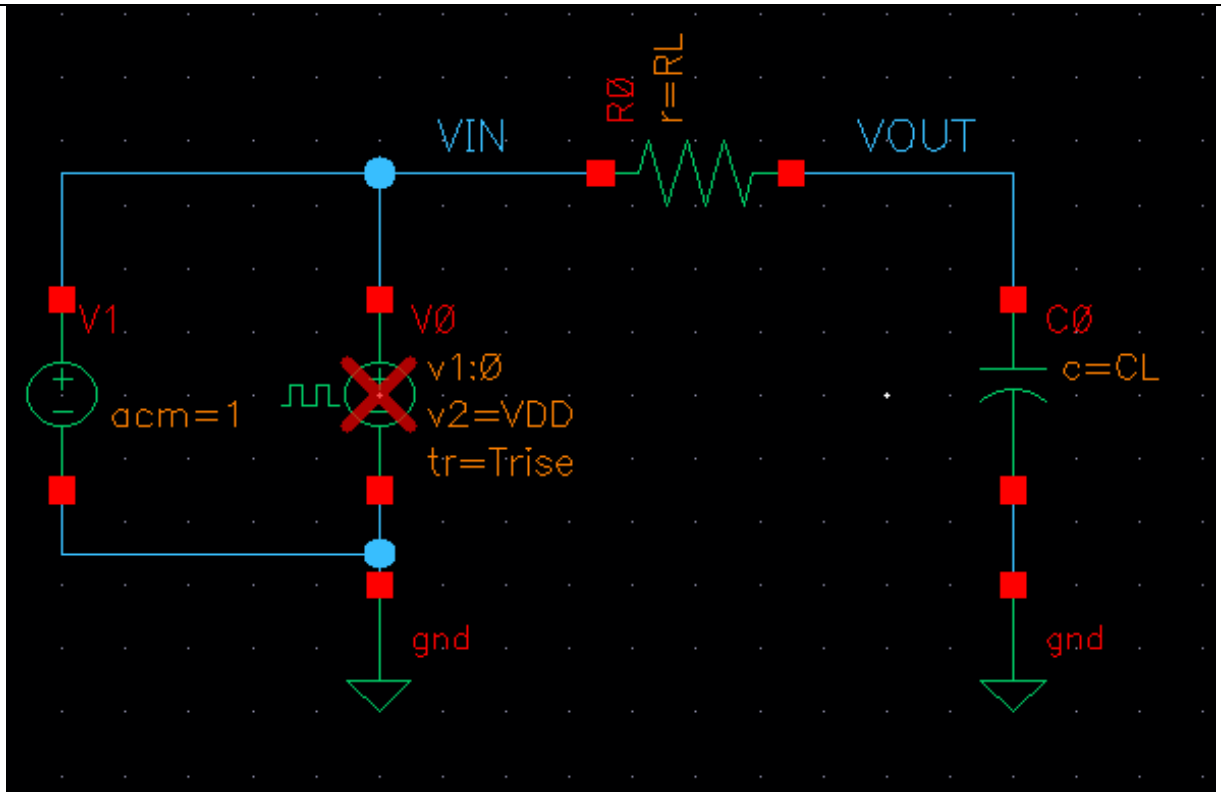


Rise and Fall time Plot vs R_L (kΩ)

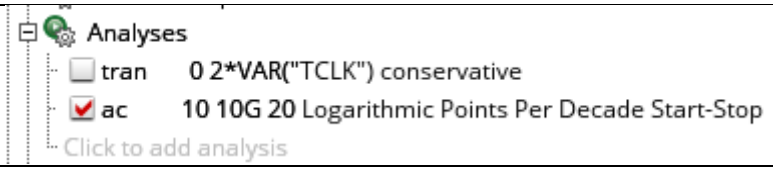


AC Analysis

Q1

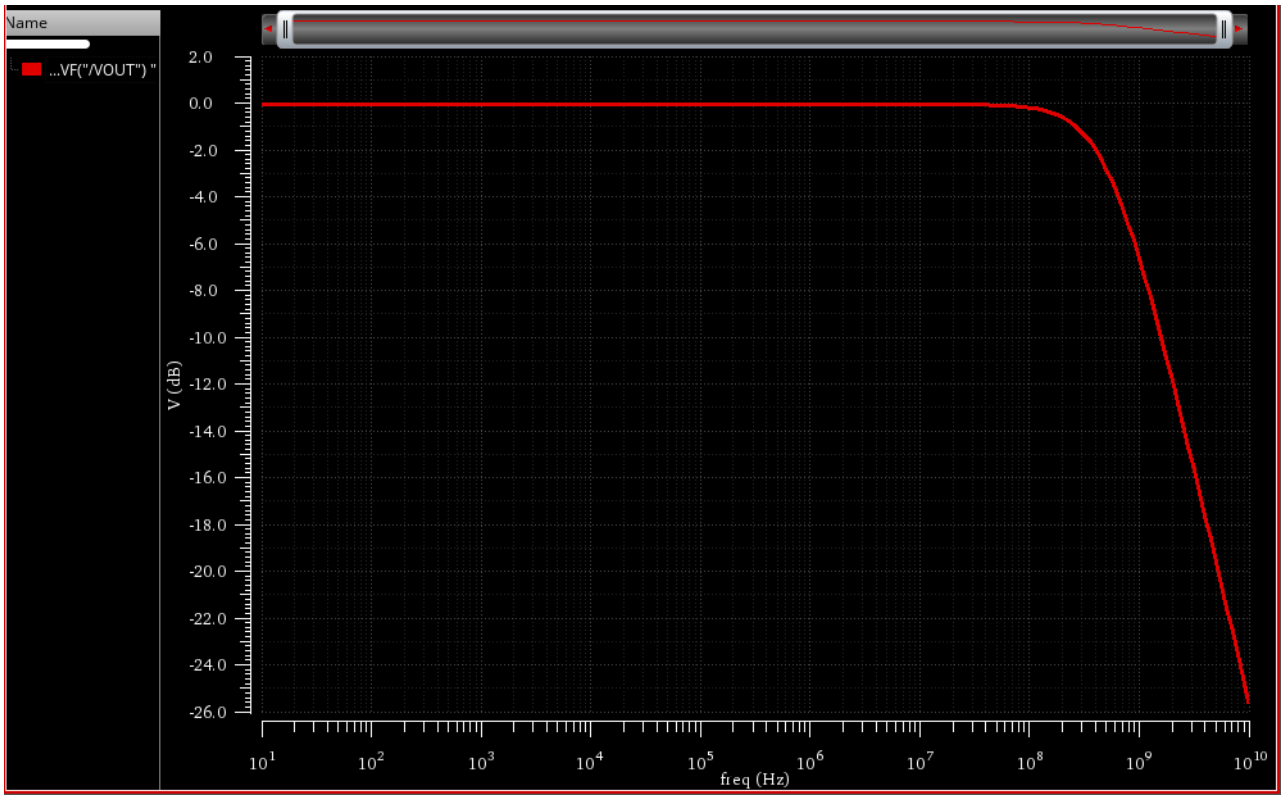


This is The Schematic of LPF With $V_{dc} \rightarrow V_{AC} = 1$



Q1

Bode Plot (Magnitude) (Log Scale) $V_{out}(dB)$



Bode Plot (Phase)

Q2

LAB_1_PART_1 | adexl

Outputs Setup | Run Preview | Results | Diagnostics

Detail | Replace

Test	Output	Nominal	Spec
IEEE_Workshop:LAB_1_PART_1:1	Vout		
IEEE_Workshop:LAB_1_PART_1:1	Vin		
IEEE_Workshop:LAB_1_PART_1:1	Current		
IEEE_Workshop:LAB_1_PART_1:1	BW	529.7M	
IEEE_Workshop:LAB_1_PART_1:1	Ao	1	

LAB_1_PART_1 | adexl

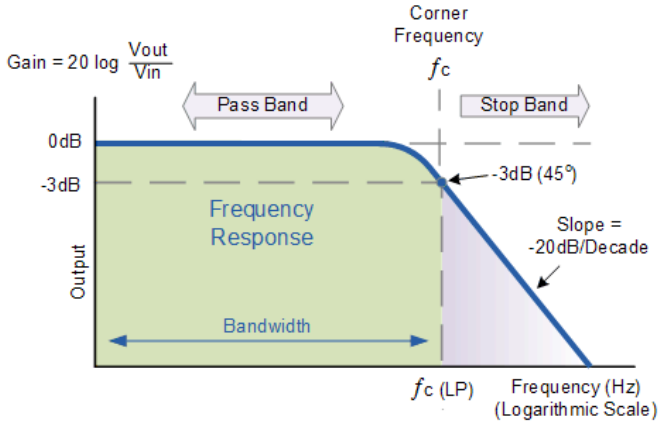
Outputs Setup | Run Preview | Results | Diagnostics

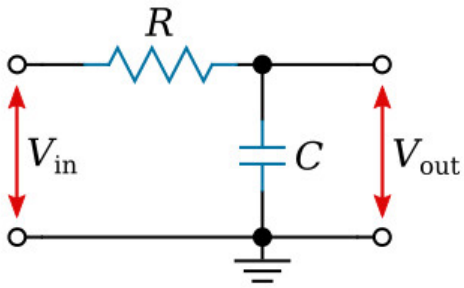
Test	Name	Type	Details	EvalType	Plot	Save
IEEE_Workshop:LAB_1_PART_1:1	Vout	signal	/VOUT	point	☑	☑
IEEE_Workshop:LAB_1_PART_1:1	Vin	signal	/VIN	point	☑	☑
IEEE_Workshop:LAB_1_PART_1:1	Current	signal	/V0/PLUS	point	☑	☑
IEEE_Workshop:LAB_1_PART_1:1	Trise	expr	riseTime(VT("/VOUT") 0 nil 1 nil 10 90 nil "time")	point	☐	☐
IEEE_Workshop:LAB_1_PART_1:1	Tfall	expr	fallTime(VT("/VOUT") 1 nil 0 nil 90 10 nil "time")	point	☐	☐
IEEE_Workshop:LAB_1_PART_1:1	BW	expr	bandwidth(mag(v("/VOUT" ?result "ac")) 3 "low")	point	☑	☐
IEEE_Workshop:LAB_1_PART_1:1	Ao	expr	ymax(mag(v("/VOUT" ?result "ac")))	point	☑	☐

Q2: Simulation Results: BW = 529.7 M HZ & DC Gain $A_o = 1$

Q3

Q3: Analytical Results: -





BW = f_c (Cut off Frequency)

$$\text{From Voltage Divider, DC Gain } A_o = \frac{V_{out}}{V_{in}} = \lim_{X_c \to \infty} \frac{X_c}{R + X_c} = 1$$

@ DC Analysis $\omega \to 0$, $X_c = \frac{1}{j\omega C} \to \infty$ (Open Circuit)

$$f_c = \frac{1}{2\pi RC} = \frac{1}{2\pi \times 1\,k \times 0.3p} \approx 530.52\ M\ Hz.$$

BW = 530.52 M Hz.

P.O.C	Analytically	Simulation	Error
DC Gain A_o	1	1	0 %
BW	530.52 M Hz.	529.7 M HZ.	0.15 %

Q4

Parametric Sweep For R = 1, 10, 100, 1000 kΩ

RL {From/To}Logarithmic:1k:4:1M{From/To}

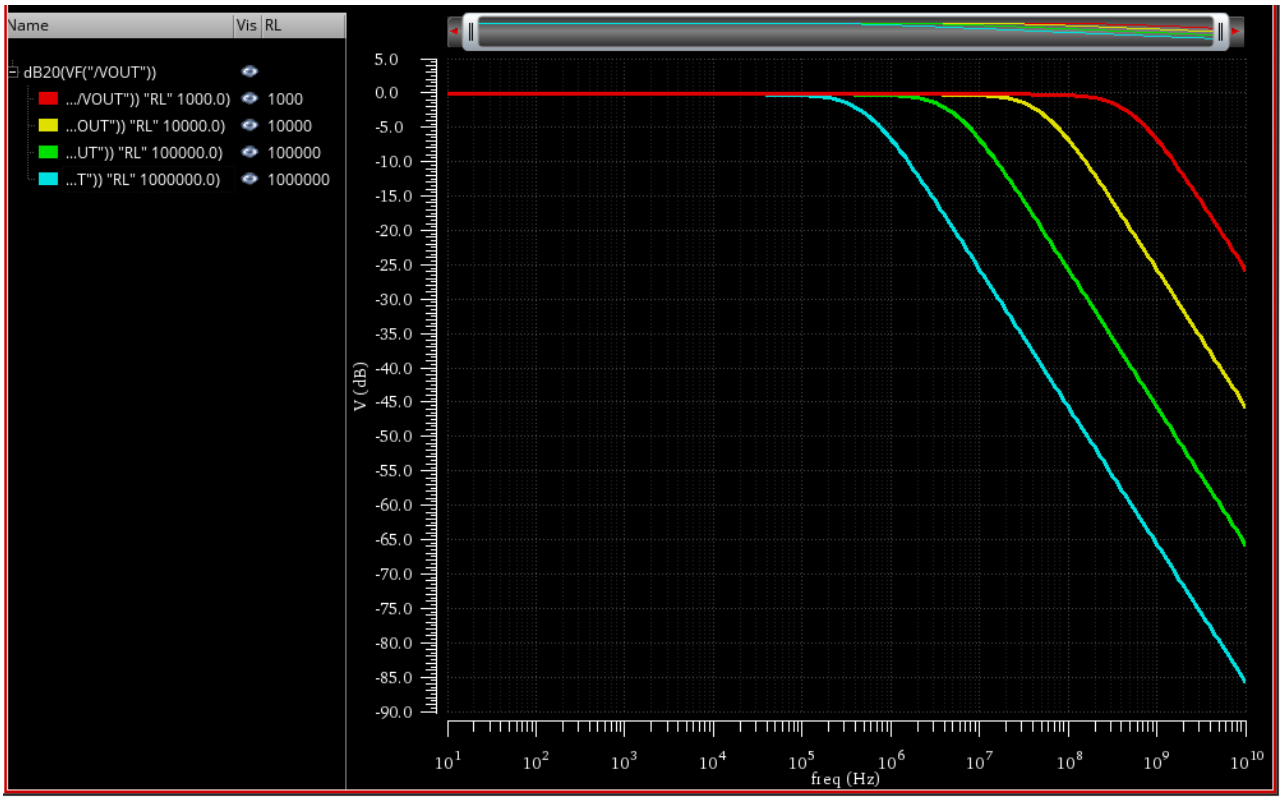
LAB_1_PART_1 | adexl

Outputs Setup | Run Preview | Results | Diagnostics

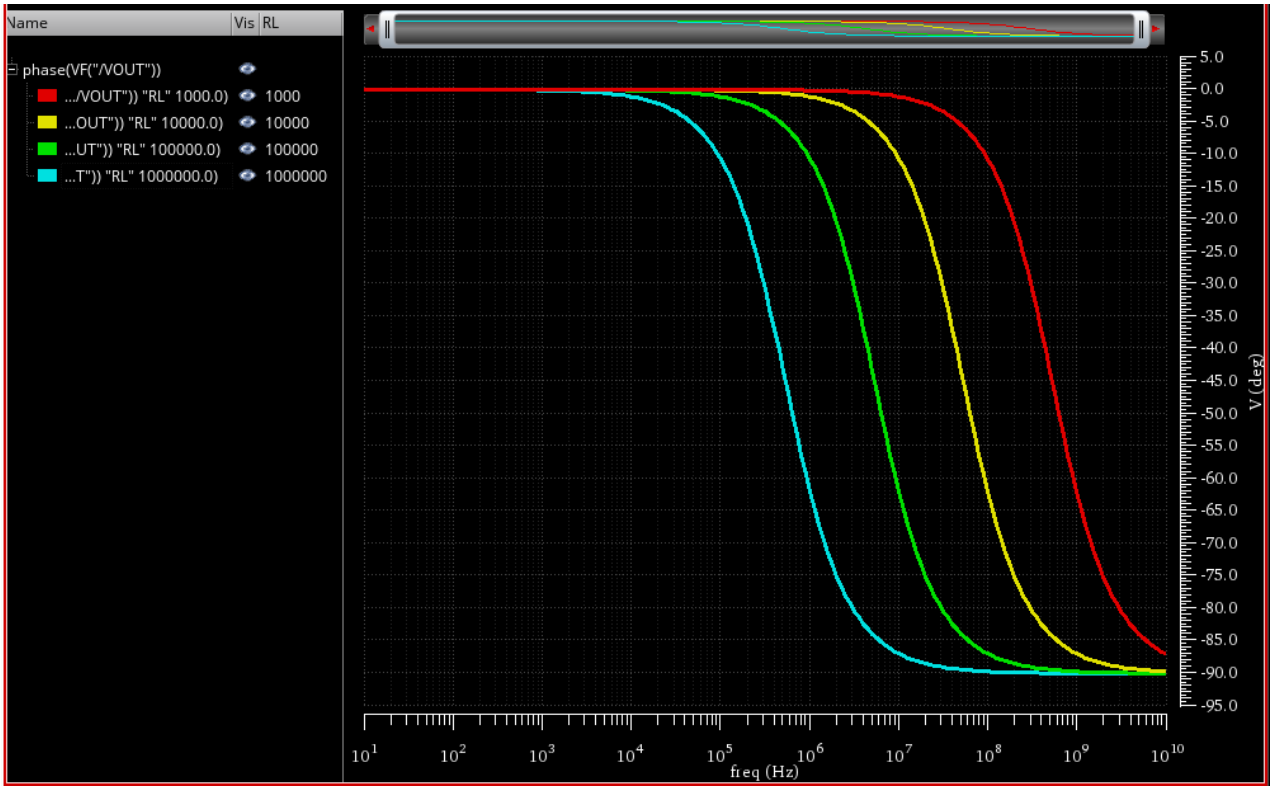
Detail | Replace

Point	Test	Output	Nominal
Parameters: RL=1k			
1	IEEE_Workshop:LAB_1_PART_1:1	Vout	
1	IEEE_Workshop:LAB_1_PART_1:1	Vin	
1	IEEE_Workshop:LAB_1_PART_1:1	Current	
1	IEEE_Workshop:LAB_1_PART_1:1	BW	529.7M
1	IEEE_Workshop:LAB_1_PART_1:1	Ao	1
Parameters: RL=10k			
2	IEEE_Workshop:LAB_1_PART_1:1	Vout	
2	IEEE_Workshop:LAB_1_PART_1:1	Vin	
2	IEEE_Workshop:LAB_1_PART_1:1	Current	
2	IEEE_Workshop:LAB_1_PART_1:1	BW	52.97M
2	IEEE_Workshop:LAB_1_PART_1:1	Ao	1
Parameters: RL=100k			
3	IEEE_Workshop:LAB_1_PART_1:1	Vout	
3	IEEE_Workshop:LAB_1_PART_1:1	Vin	
3	IEEE_Workshop:LAB_1_PART_1:1	Current	
3	IEEE_Workshop:LAB_1_PART_1:1	BW	5.297M
3	IEEE_Workshop:LAB_1_PART_1:1	Ao	1
Parameters: RL=1M			
4	IEEE_Workshop:LAB_1_PART_1:1	Vout	
4	IEEE_Workshop:LAB_1_PART_1:1	Vin	
4	IEEE_Workshop:LAB_1_PART_1:1	Current	
4	IEEE_Workshop:LAB_1_PART_1:1	BW	529.7k
4	IEEE_Workshop:LAB_1_PART_1:1	Ao	1

Overlaid Bode Plot (Magnitude) (Log Scale) V_{out} (dB)



Overlaid Bode Plot (Phase) V_{out} (in Degrees)



Q4: Comments: -

R_L	1k	10k	100k	1M
BW	529.7 M	52.97 M	5.297 M	529.7 k
A_o	1	1	1	1

We Find That as When $R_L \times 10$, BW $\div 10$ As The Relation is

$BW = f_c = \frac{1}{2\pi RC}$, And DC Gain is Constant $\rightarrow A_o = 1$

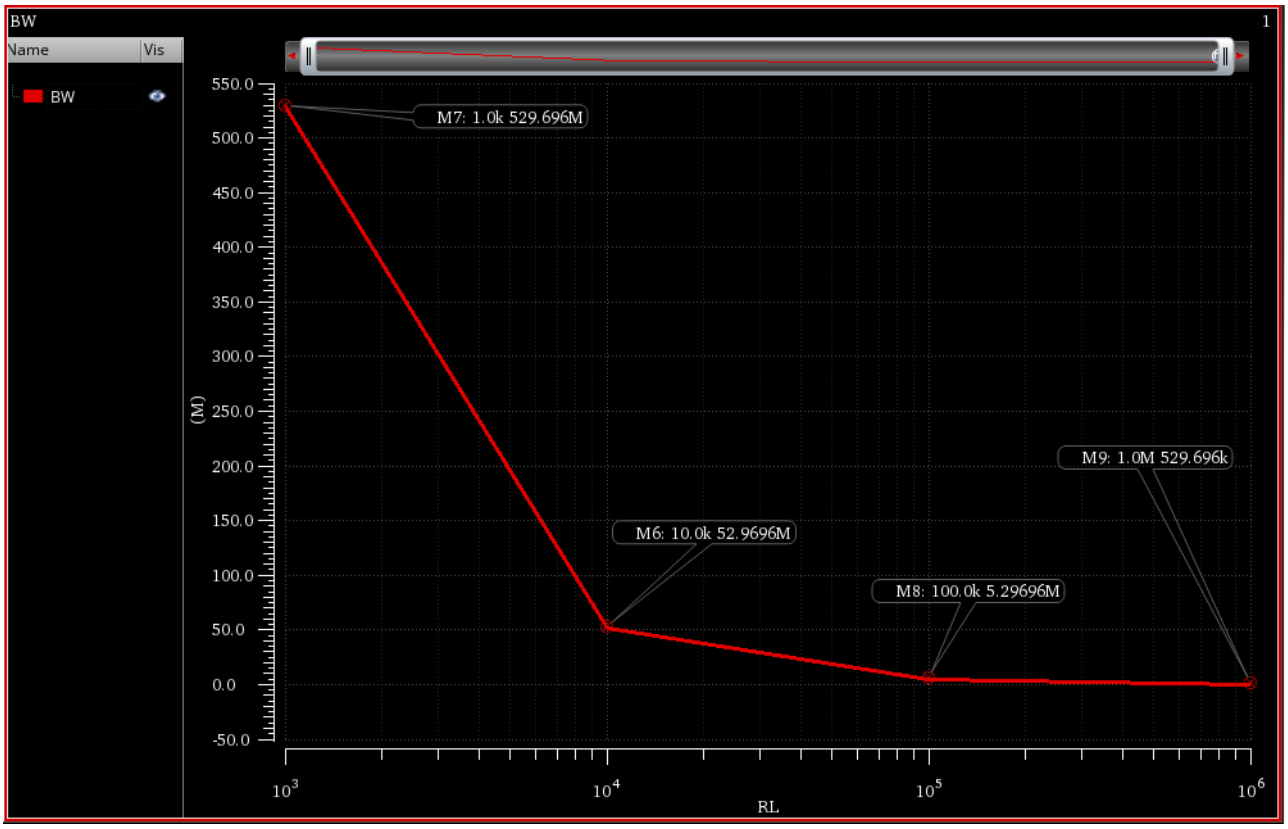
As R Increases , BW Decreases By the same factor From this Relation

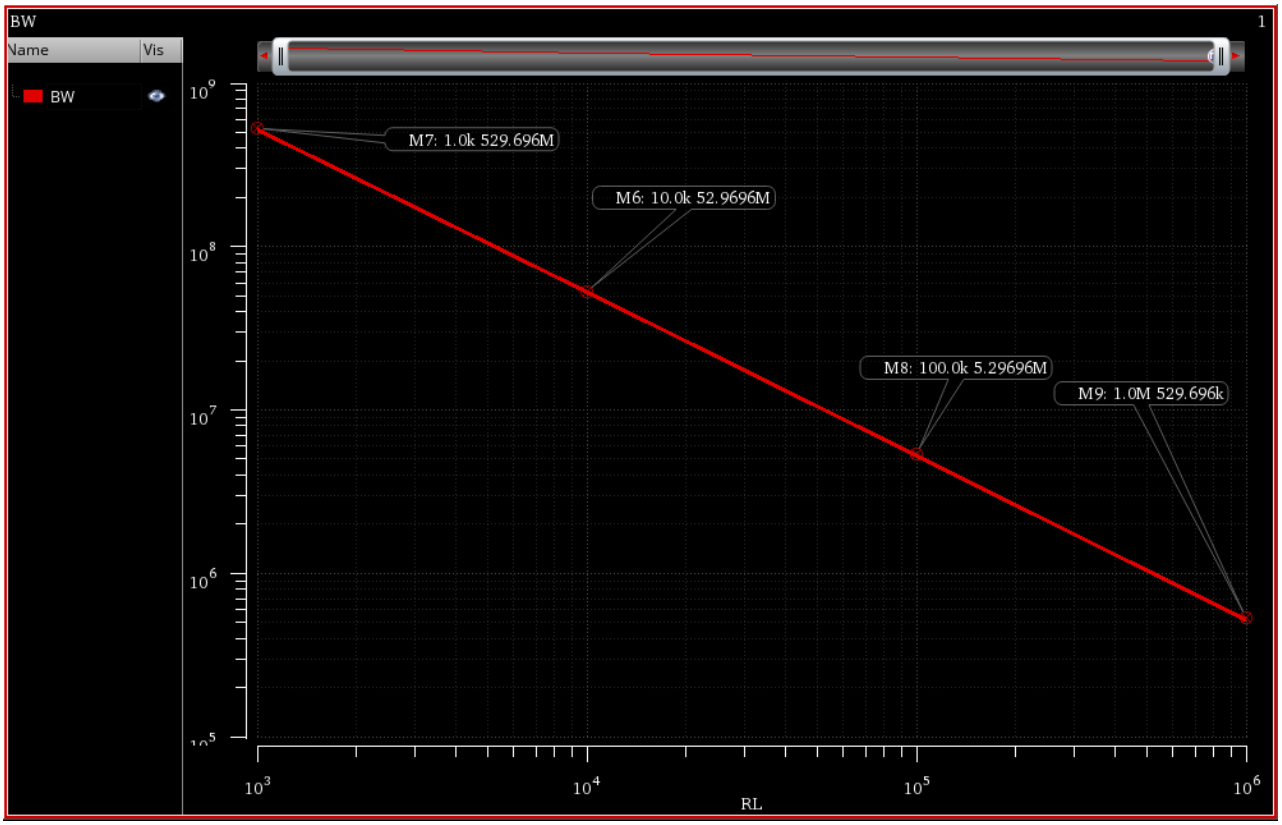
$BW = \frac{1}{RC}$ rad/sec. BW is Inversely proportional to R.

The information presented in the table and charts indicates that the 3 dB bandwidth is declining in relation to the resistance value. This outcome aligns with the initial expectations, as the analytical formula established earlier specifies that the 3 dB bandwidth is inversely proportional to the RC constant. Therefore, as the resistance or capacitance is increased, the circuit becomes more selective, resulting in a narrower bandwidth. It is important to note that the DC gain remains unaffected by changes in resistance since it is an open circuit voltage with no voltage drop on the resistance. for phase in all cases, it falls from 0 to -90 but it falls faster by increasing resistance.

Q4

BW for Parametric Sweep For R = 1, 10, 100, 1000 kΩ



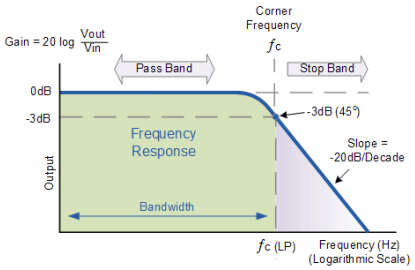


Pole Zero Analysis

Q1

Results: -

$$A_V = \frac{X_C}{R+X_C} = \frac{\frac{1}{sc}}{R+\frac{1}{sc}} = \frac{1}{SRC+1}$$



For Zeros $\rightarrow 1 = 0$ (undefined)

$\therefore$ No Zeros

For Poles $\rightarrow SCR + 1 = 0 \rightarrow S = -\frac{1}{CR} = j\omega \rightarrow |f| = \frac{1}{2\pi CR}$ (f @ pole)

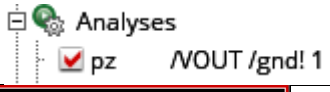
This Pole That make The Slope In The LPF Graph

Slope $= -20$ dB/Decade.

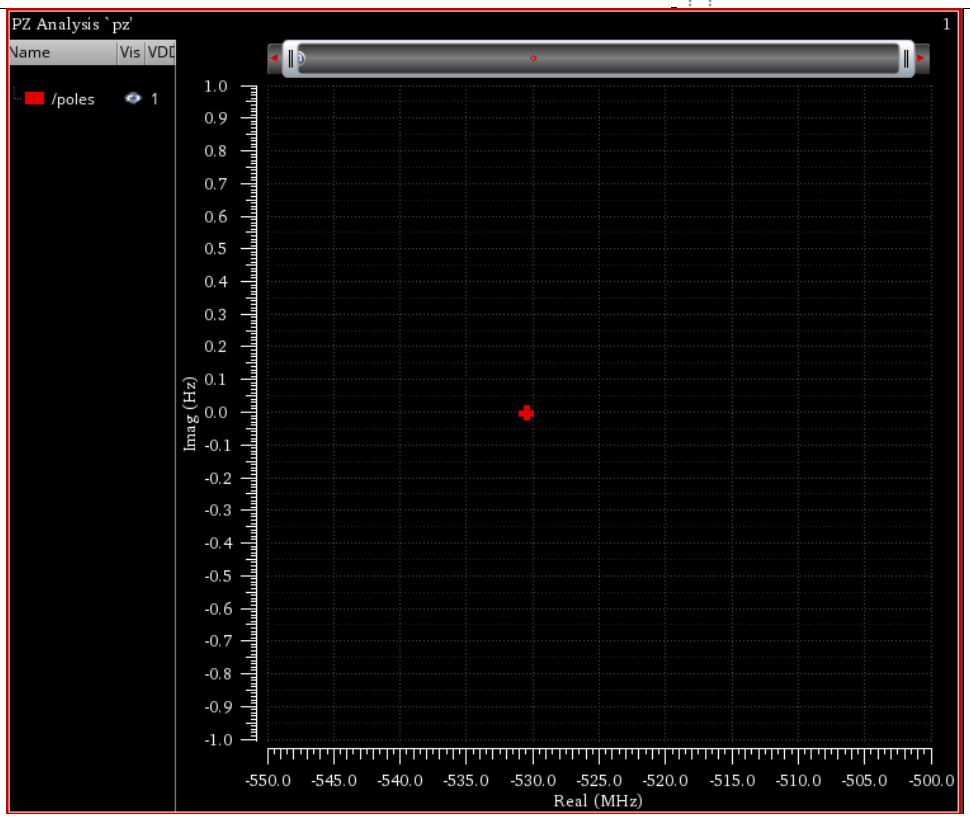
Comparison: -

We Find That The Simulation Results For PZ Analysis gives its Real Part (Frequency of Pole) Is Equal to The BW That we get From AC Analysis.

```
****************
PZ Analysis `pz'
****************
DC simulation time: CPU = 0 s, elapsed = 137.806 us.
DC simulation time: CPU = 0 s, elapsed = 31.9481 us.
                    Poles (Hz)

          Real                    Imaginary                Qfactor

   1   -5.30516e+08               0.00000e+00             5.00000e-01

  No zero is found

Accumulated DC solution time = 44.8799 ms.
Intrinsic pz analysis time =              -66.8899 ms.
Total time required for pz analysis `pz': CPU = 0 s, elapsed = 1.32704 ms.
Time accumulated: CPU = 132 ms, elapsed = 155.255 ms.
Peak resident memory used = 81.6 Mbytes.
```



Q2



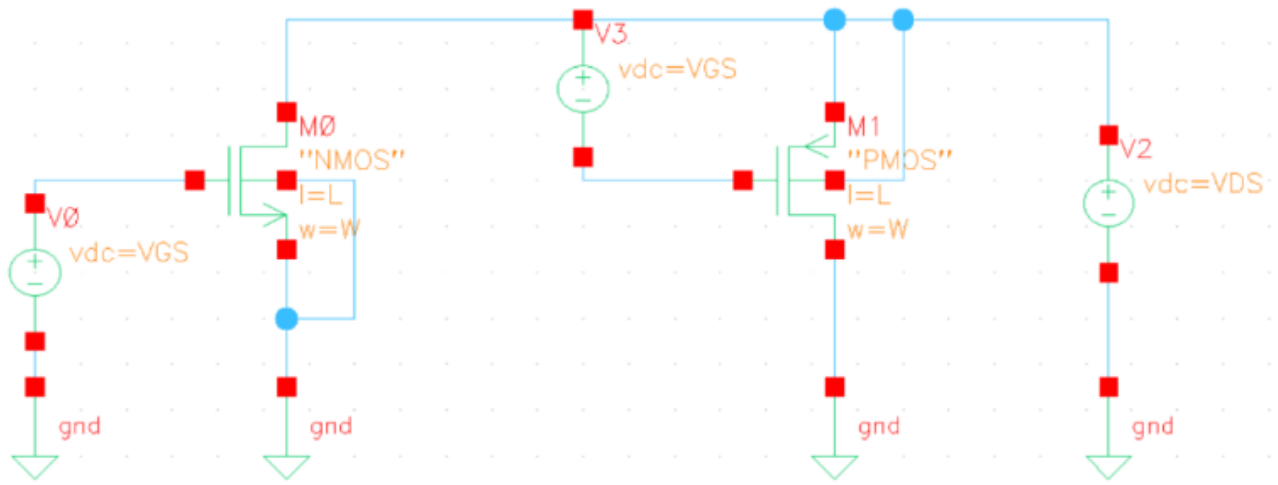
one pole exist @ $F_{simulation\ AC} = 529.7$ MHZ , $F_{Analytical} = 530.516$ MHZ.

Part 2

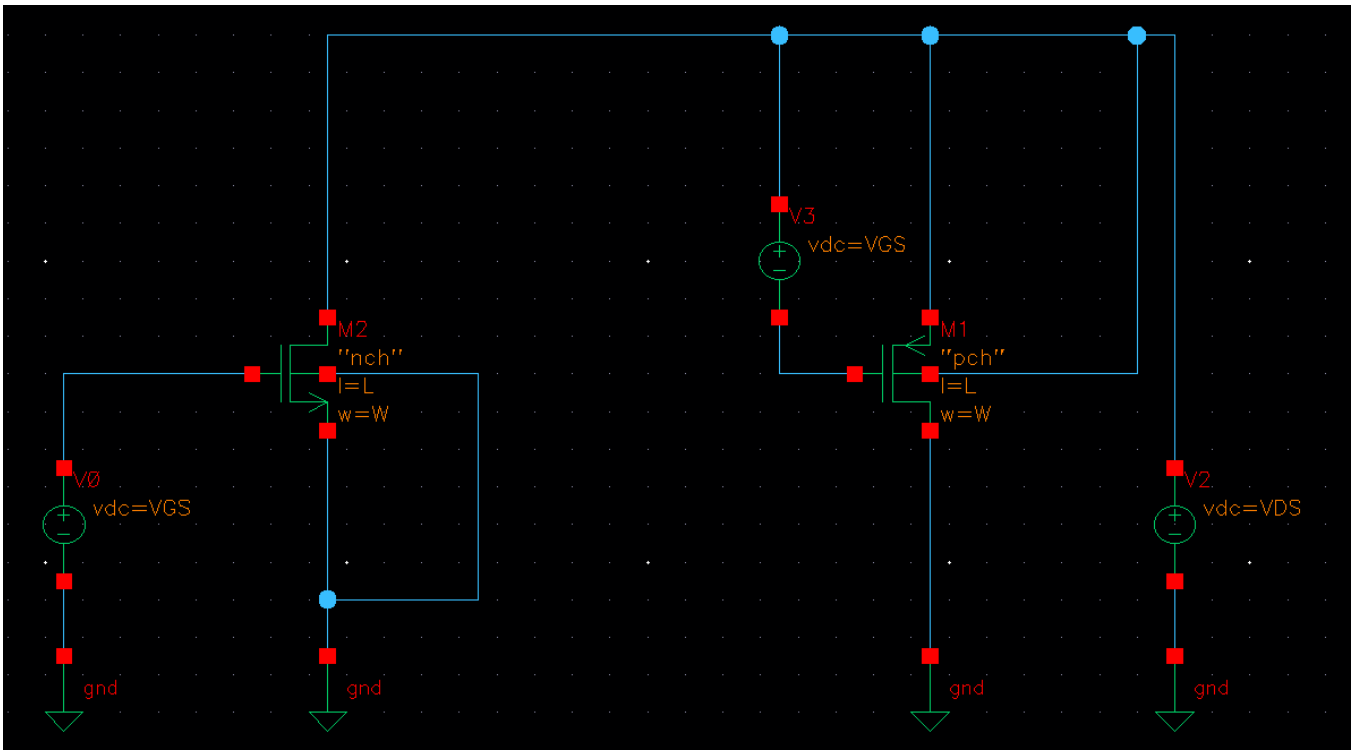
MOSFET Characteristics

Circuit

Create a testbench to characterize NMOS and PMOS devices as shown in the figure below.



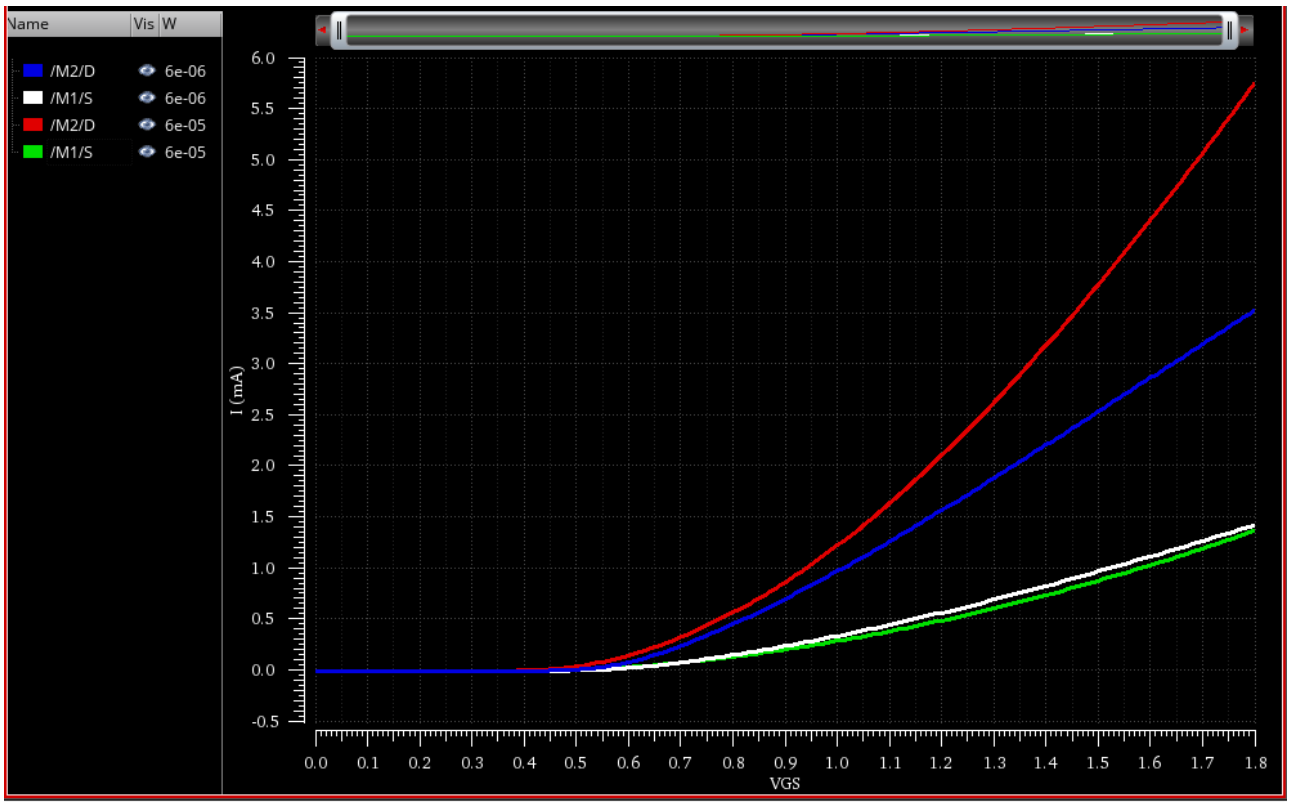
Schematic



I_D vs V_{GS}

Q1

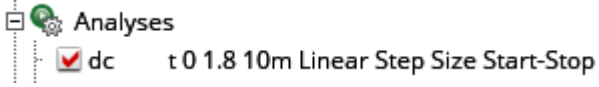
Overlaid Plotting of I_D vs V_{GS} for Long Channel and Short Channel For NMOS and PMOS.



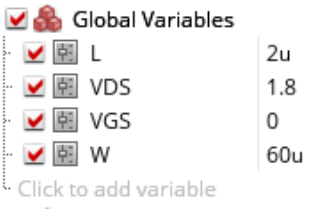
$$M_2 = \text{NMOS} \quad , \quad M_1 = \text{PMOS}$$

Green Curve: M_1 PMOS (Long Channel)
White Curve: M_1 PMOS (Short Channel)
Blue Curve: M_2 NMOS (Short Channel)
Red Curve: M_2 NMOS (Long Channel)

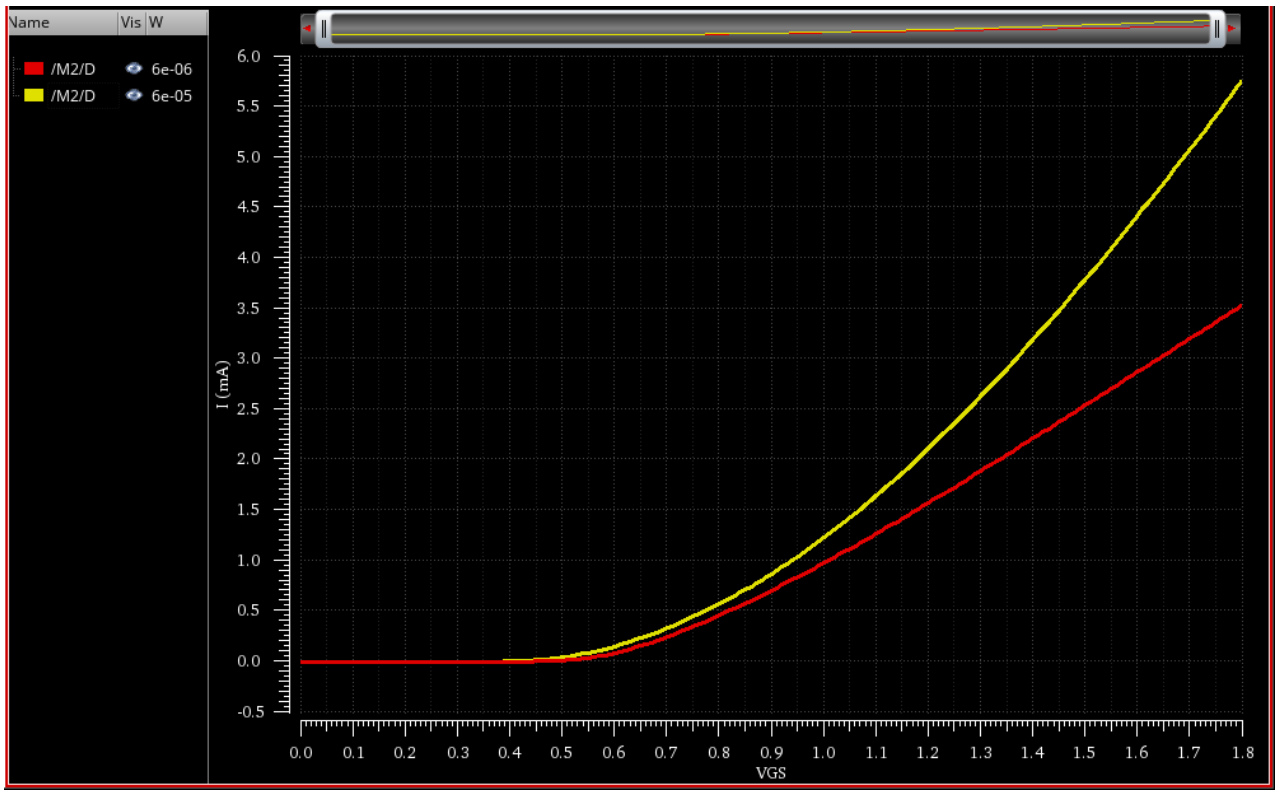
(Short Channel Values)



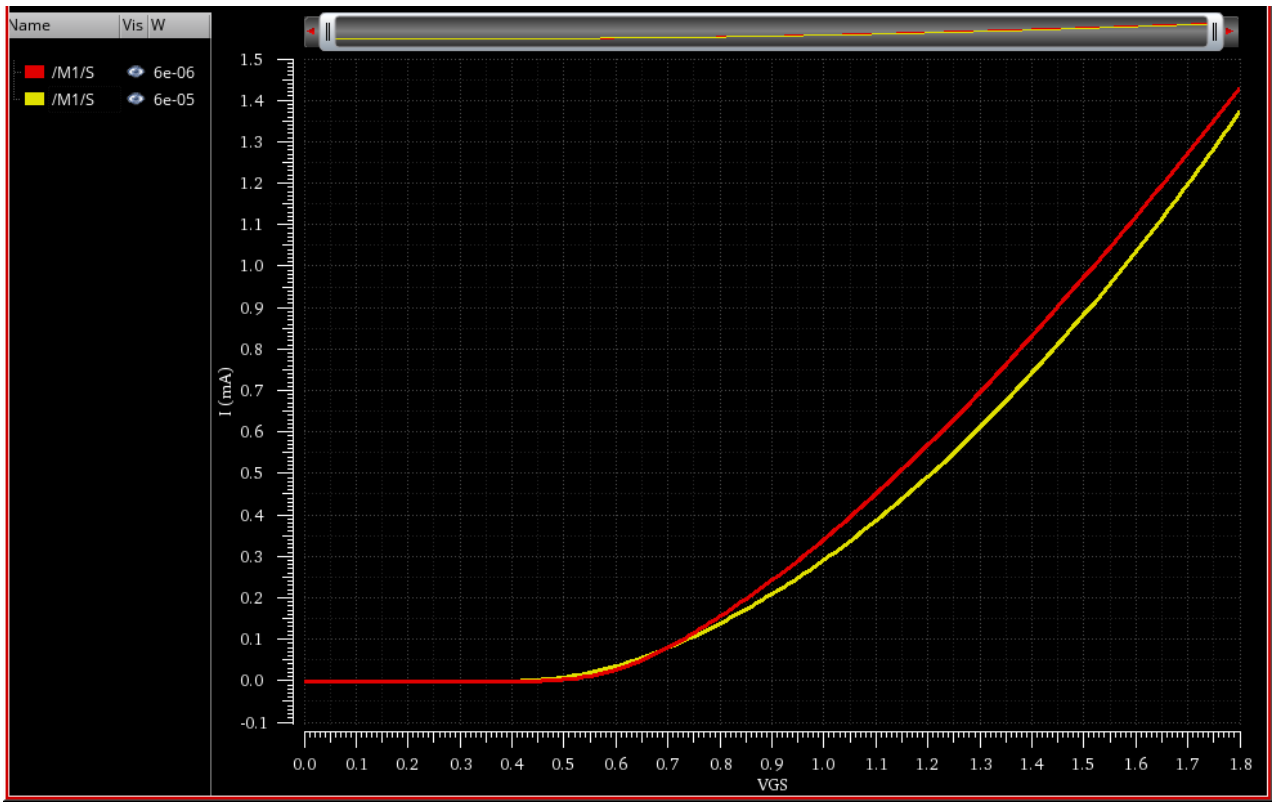
(Long Channel Values)



Q1



Red Curve: Short Channel Device NMOS.
Yellow Curve: Long Channel Device NMOS.



Red Curve: Short Channel Device PMOS.
Yellow Curve: Long Channel Device PMOS.

Q2

Q2: Comments: -

On the differences between short channel and long channel results.

We Know that the current to be constant (The Square Law Model).
for the two cases (Short and Long Channel Devices) as the ratio between the length and width remains constant.
for small channel lengths of new submicron technologies, the square law becomes unreliable anymore; that mainly refers to the short channel effects such as the velocity saturation, mobility degradation, and drain induced barrier lowering which leads to lower current than long channel.

- **Which one has the highest current? Why?**

Long Channel Device Has Higher Current Due to the Quadratic dependence on V_{GS} and due to $Velocity_{sat}$ which also gives the linear Characteristics and gives in Short Channel Device the Much Less Than the Expected Current from Quadratic Relation.

- **Is the relation linear or quadratic? Why?**

→ For Short Channel Device: -

- Starts As Quadratic Relation and tends to be Linear Relation $@V_{GS} = V_{Dsat} + V_{th}$
- The square law becomes unreliable; that refers to the short channel effects such as the velocity saturation, mobility degradation, and drain induced barrier Lowering.
- The short channel has generally lower current than that of the long channel and the relation tend to be linear $Velocity_{sat}$ effect. Velocity saturation occurs when the carriers in the channel reach a maximum drift velocity, limiting their further acceleration.

→ For Long Channel Device: -

- The square law is roughly valid, and the relation is almost Quadratic with V_{GS} due to the carrier velocity being proportional to the electric field in the channel

Q3

Q3: Comments: -

On the differences between NMOS and PMOS.

- We Find That the Current of NMOS Device is Much Greater Than PMOS Device Due to the Difference between The Mobility Ratio of NMOS and PMOS as $\mu_{NMOS \rightarrow Electrons} > \mu_{PMOS \rightarrow Holes}$
- Due to this effect, the following parameters are affected. Mobility of charge carrier in the channel. The threshold voltage changed due to the shorter length of the channel. Drain current also changed as threshold voltage changed.

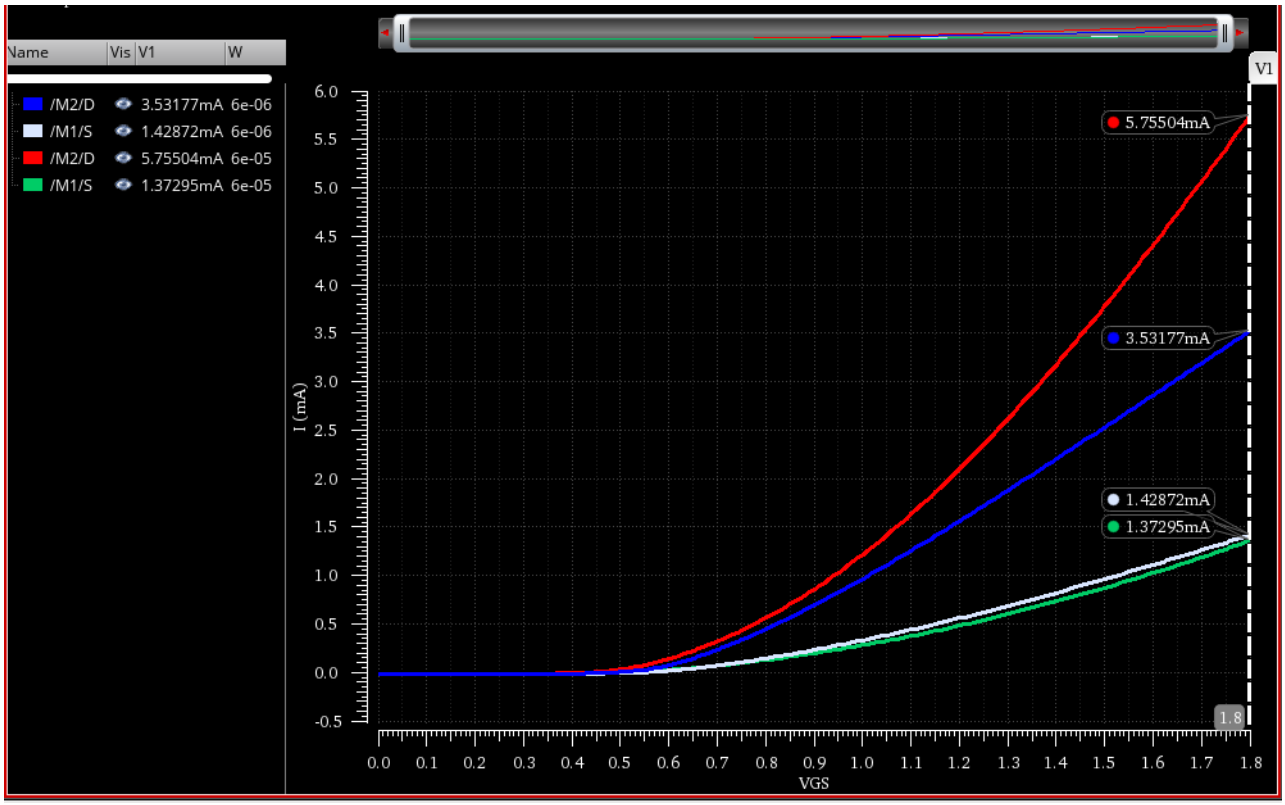
- **Which one has the highest current? Why?**

- The NMOS has a higher current due to higher mobility as electrons are almost 4 times that of holes for the same temperature.

→ For PMOS (Short & Long Channel Devices)

- The Two Curves are Much approach to each other. As PMOS Device is Less Affected by $Velocity_{sat}$ and NMOS is easy go to $Velocity_{sat}$.

NMOS VS PMOS



What is the ratio between NMOS and PMOS currents at $V_{GS} = V_{DD} = 1.8$ Volt ?

- Long channel:
  NMOS Current at $(V_{GS} = V_{DD}) = 5.75504 \times 10^{-3}$ A
  PMOS Current at $(V_{GS} = V_{DD}) = 1.37295 \times 10^{-3}$ A
  → The ratio between NMOS and PMOS currents at
  $(V_{GS} = V_{DD}) = 4.19$
- Short channel:
  NMOS Current at $(V_{GS} = V_{DD}) = 3.53177 \times 10^{-3}$ A
  PMOS Current at $(V_{GS} = V_{DD}) = 1.42872 \times 10^{-3}$ A
  → The ratio between NMOS and PMOS currents at
  $(V_{GS} = V_{DD}) = 2.472$

Which one is more affected by short channel effects?

- The NMOS is More Affected by short channel effect due to its higher mobility that makes it reach the velocity saturation more easily than PMOS as The Two Curves are Much approach to each other.
  As PMOS Device is Less Affected by Velocity_{sat} and
  NMOS is easy go to Velocity_{sat} and the square law becomes more unreliable.

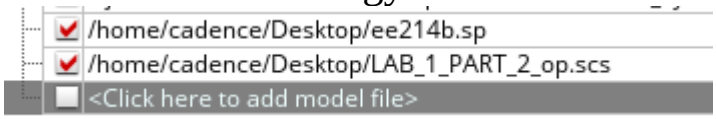
g_m vs V_{GS}

Q1

LAB_1_PART_2_op.scs

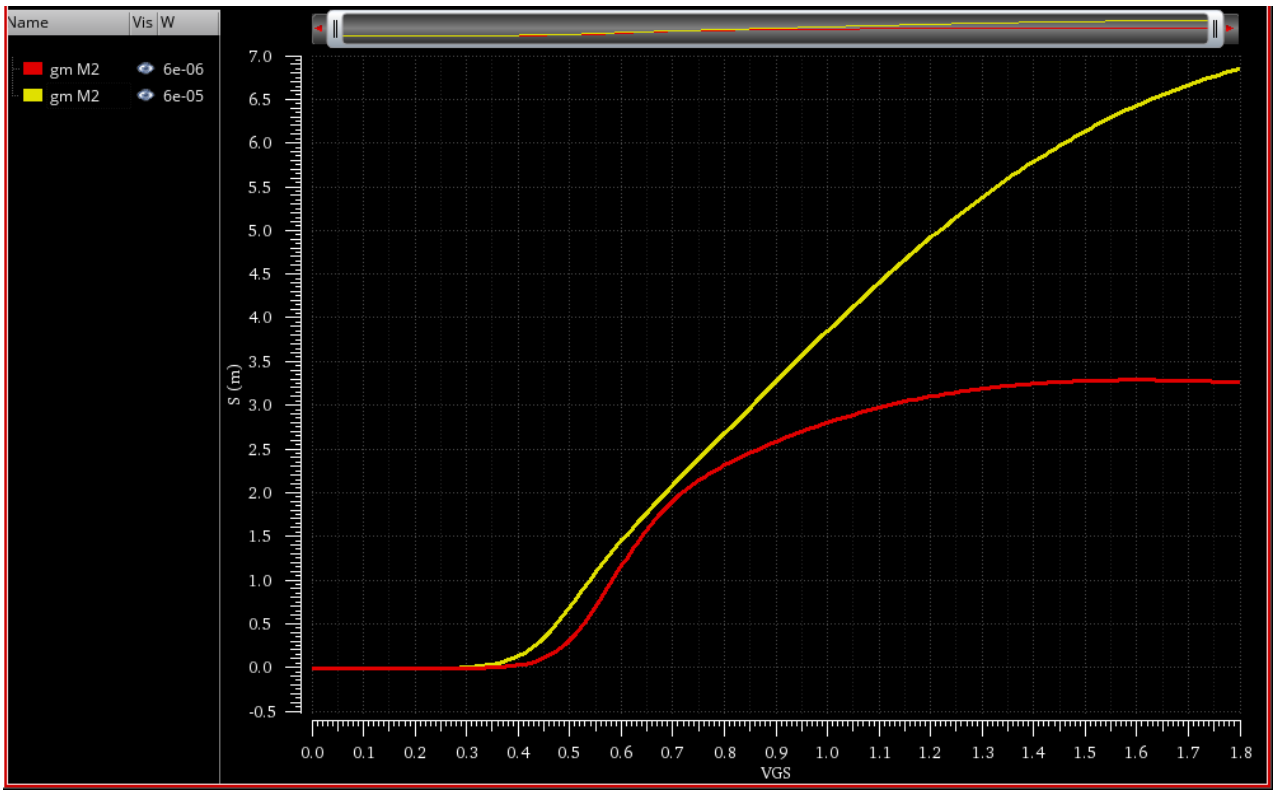
```
1  save *:gm sigtype=dev
2  save *:oppoint sigtype=dev
3
```

First Make This File to Save The Operating Point in Our Analysis.
Operating Point Parameters: g_m , I_D , V_{GS} , V_{DS} .
add with it ee214b Technology PDK in Model Libraries.



Q1

Overlaid Plotting of g_m vs V_{GS} for Long Channel and Short Channel for NMOS.



M_2 = NMOS
Red Curve: M_2 NMOS (Short Channel)
Yellow Curve: M_2 NMOS (Long Channel)

Q2

Q2: Comments: -

On the differences between short channel and long channel results.

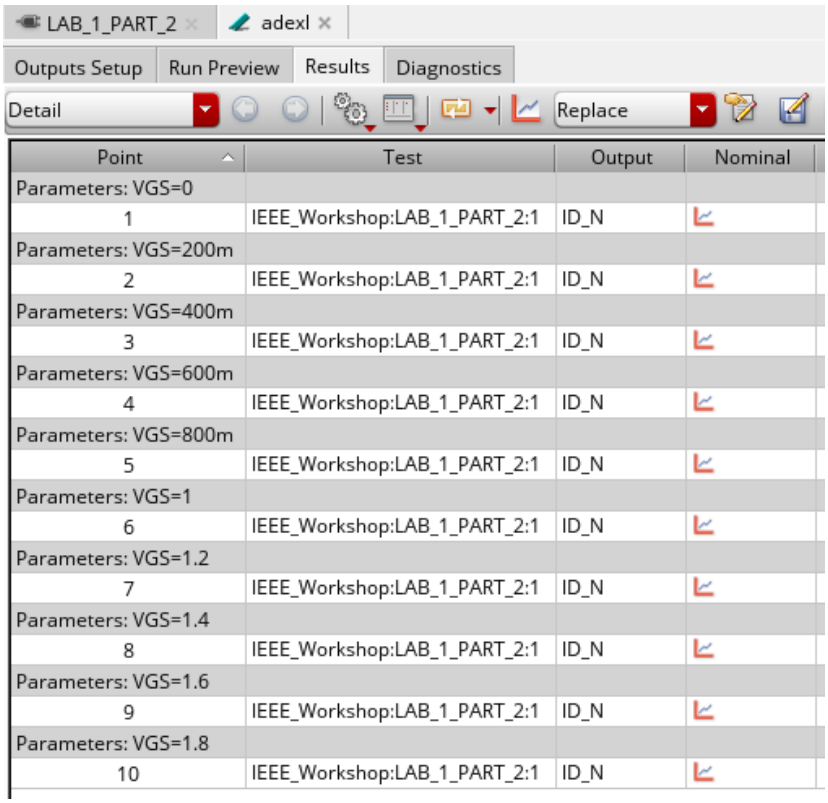
- **Does gm increase linearly? Why?**
  - gm increases linearly for small values of V_{GS} and only for long channel because the square law is still valid, as $g_m = \frac{\partial I_{ds}}{\partial V_{ds}}$ and the differentiation of the quadratic relation (I_{ds}) is a linear relation (g_m)
    For short channel, the linear relation is not valid due to short channel effects.
- **Does gm saturate? Why?**
  - For high values of V_{GS}, g_m appears to be saturated
    has constant value as I_d also be Constant from this Relation,
    $g_m = \sqrt{2\,K\,I_d}$ & Because of the velocity saturation effect where long channel saturates at larger V_{GS} while short channel saturates at lower V_{GS} where V_{DSAT} is inversely proportional to channel length so
    short channel saturates much earlier than long channel.

I_D vs V_{DS}

Q1

Short Channel

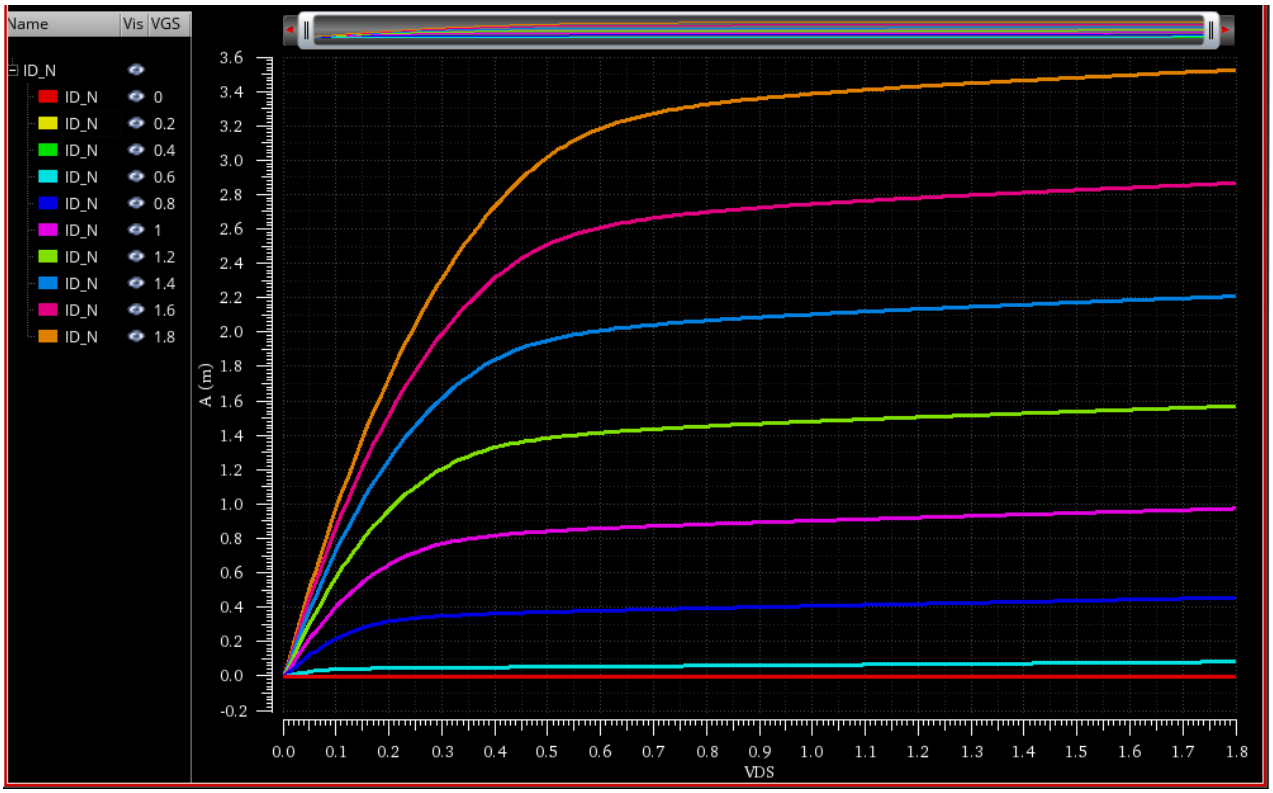
Long Channel



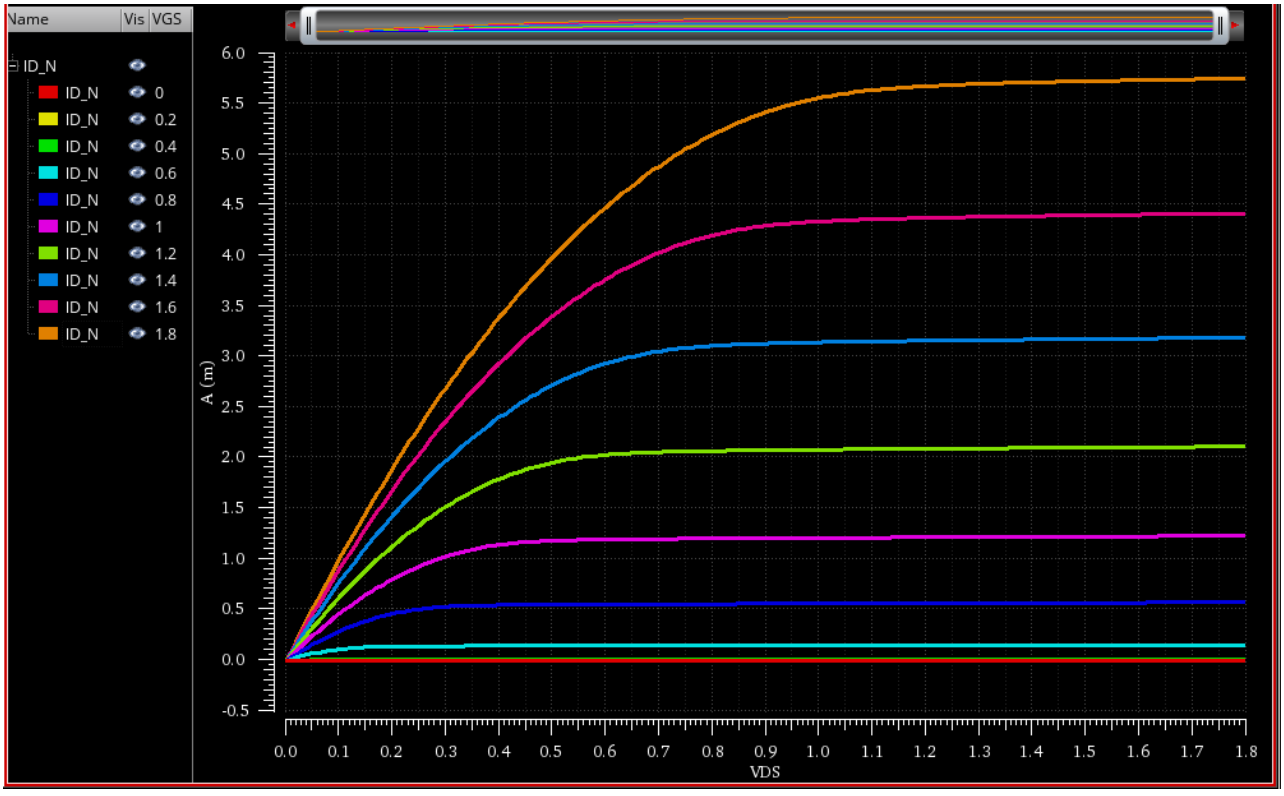
Point	Test	Output	Nominal
Parameters: VGS=0			
1	IEEE_Workshop:LAB_1_PART_2:1	ID_N	
Parameters: VGS=200m			
2	IEEE_Workshop:LAB_1_PART_2:1	ID_N	
Parameters: VGS=400m			
3	IEEE_Workshop:LAB_1_PART_2:1	ID_N	
Parameters: VGS=600m			
4	IEEE_Workshop:LAB_1_PART_2:1	ID_N	
Parameters: VGS=800m			
5	IEEE_Workshop:LAB_1_PART_2:1	ID_N	
Parameters: VGS=1			
6	IEEE_Workshop:LAB_1_PART_2:1	ID_N	
Parameters: VGS=1.2			
7	IEEE_Workshop:LAB_1_PART_2:1	ID_N	
Parameters: VGS=1.4			
8	IEEE_Workshop:LAB_1_PART_2:1	ID_N	
Parameters: VGS=1.6			
9	IEEE_Workshop:LAB_1_PART_2:1	ID_N	
Parameters: VGS=1.8			
10	IEEE_Workshop:LAB_1_PART_2:1	ID_N	

Q1

Overlaid Plotting of I_D vs V_{GS} for Short Channel NMOS .



Overlaid Plotting of I_D vs V_{GS} for Long Channel NMOS



Q2

Q2: Comments: -

On the differences between short channel and long channel results.

- **Which one has the highest current? Why?**

  - As We See in The Graphs Above the Maximum Current in Long Channel. (tends to 6 mA for NMOS).
  - As We See in The Graphs Above the Maximum Current in Short Channel. (tends to 3.6 mA for NMOS).
  - So, Long channel has the Highest current compared to that of the short channel for the same V_{GS} for NMOS due to Pinch off at V_{ov} & Short channel has lower current due to its effect by Short Channel Effects and mobility and $Velocity_{sat}$.
  - The relation between I_D and V_{DS} for certain V_{GS} is well predicted using the square law model with 5 regions: cutoff, subthreshold, triode, saturation, and breakdown.

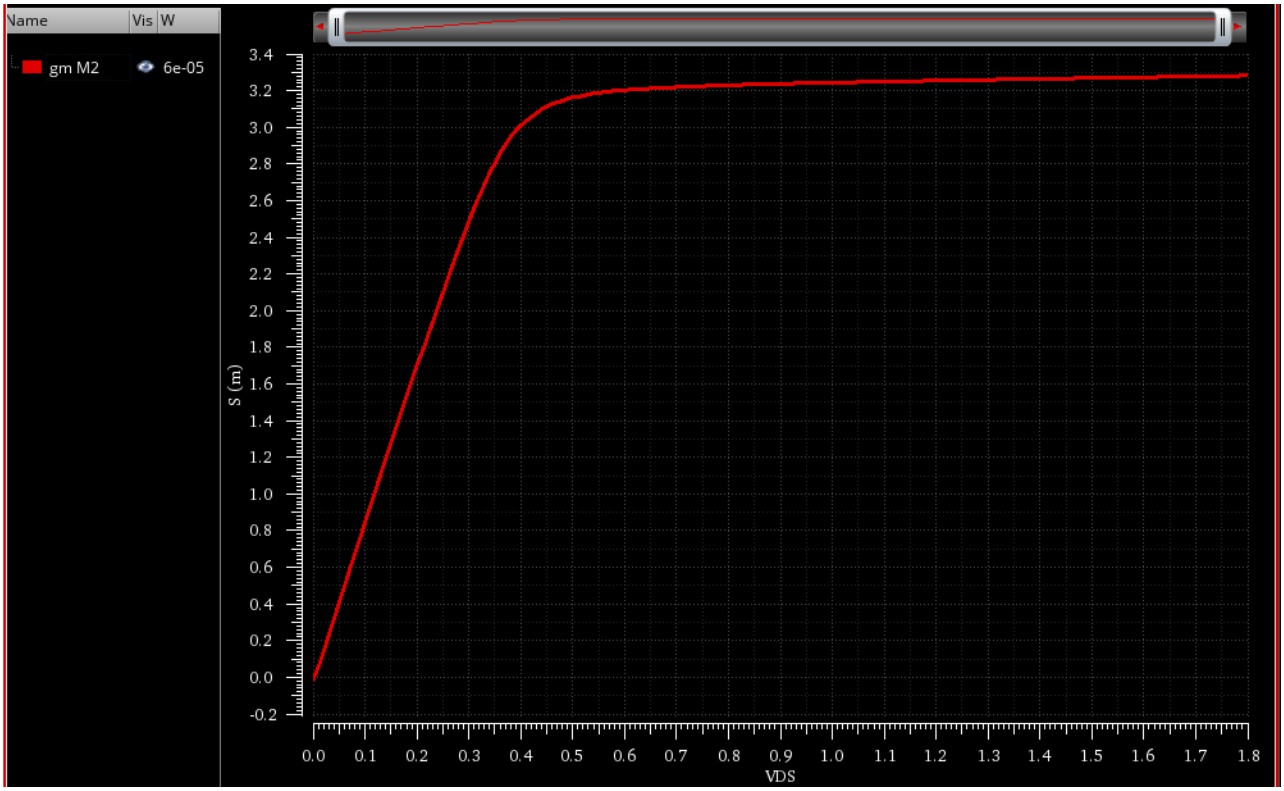
- **Which one has the highest slope in the saturation region? Why?**

  - Slope of Current for the Short Channel Device $>$ Slope for long Channel Device in Saturation Region for NMOS.
  - As the relation between r_o & L is that r_o is inverse proportional with L $r_o \propto \frac{1}{L}$ in long channel MOSFETs have less change of current with V_{DS} in Saturation region $(V_{DS} > V_{GS} - V_{th})$ so Higher output resistance (r_o) and then Low Slope as the Slope $= \frac{1}{r_o}$ so, the slope of long channel is less than that of the short channel.
  - so, the Slope Short Channel $>$ Slope Long Channel.
  - And the Relation Between r_o & L is $\frac{1}{slope} = r_o = \frac{\frac{V_{E.L}}{\Delta L} + V_{DS}}{I_{DS}}$

g_m and r_o: (In Triode and Saturation Region)

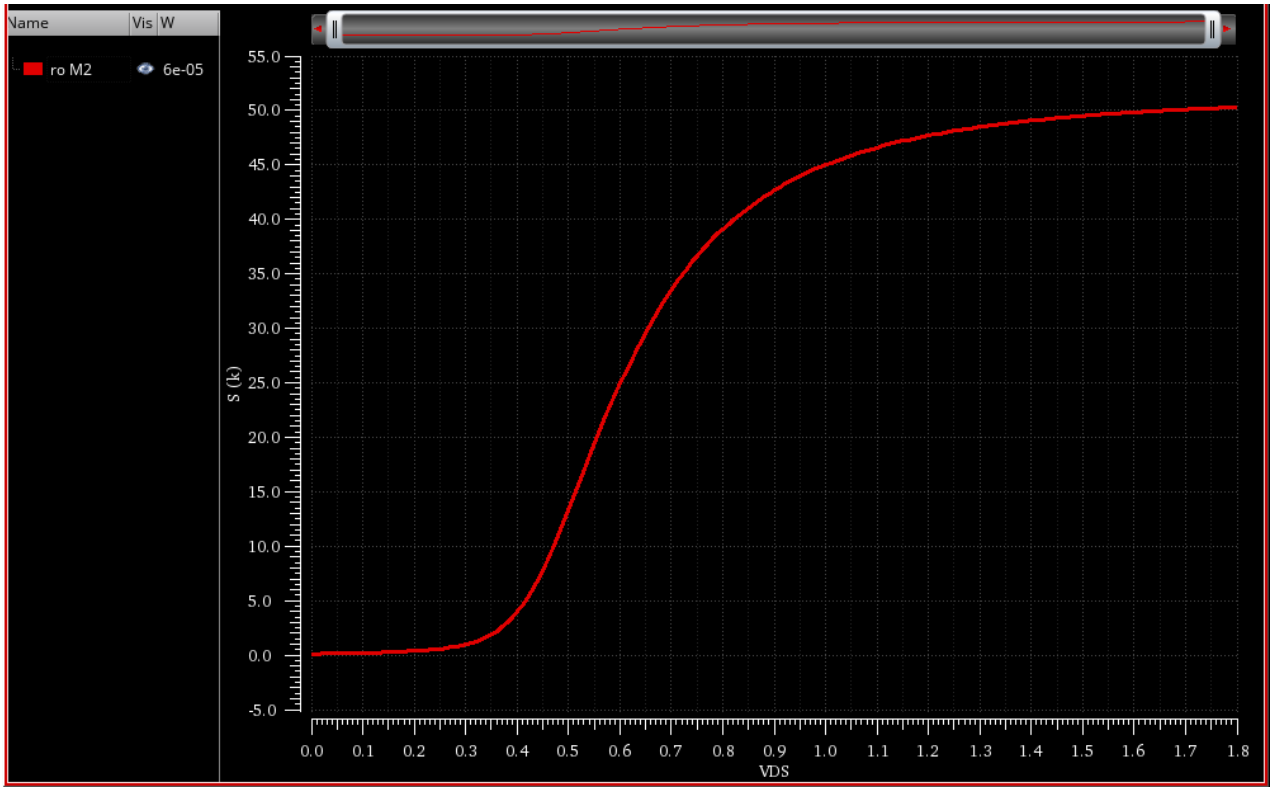
Q1

Plotting of g_m vs V_{DS} for Long Channel NMOS.



Q1

Overlaid Plotting of $r_o = \frac{1}{g_{ds}}$ vs V_{DS} for Long Channel NMOS.



Q2

Q2: Comments: -

On the Variation of g_m vs V_{DS} As We See in Graphs Above.

- **In the first part of the curve, is the relation linear? Why?**

  - Yes, g_m is Linear in the first Part of the curve.
    As it is In the Triode Region (Linear Region) in this Region I_{DS} Increase with the increase of V_{DS} Increases from the Relation $g_m = \frac{2\, I_{DS}}{V_{ov}} = \sqrt{2\, K\, I_d}$ is linear for Same V_{GS}.

- **Does g_m saturate? Why?**

  - For high values of V_{DS} , g_m appears to be saturated has constant value as I_d also be Constant from this Relation, $g_m = \sqrt{2\, K\, I_d}$ In Saturation region as it represents a square root graph.

- **Where do you want to operate the transistor for analog amplifier applications?**

  - Amplifier Works at Saturation Region in MOSFET.
    When $V_{GS} > V_{TH}$ to make the Transistor ON and Create the Channel & When $V_{DS} > V_{GS} - V_{TH}$ or $V_{DS} > V_{ov}$.
    Because the Current is somehow with Constant Value.

Q3

Q3: Comments: -

On the Variation of r_o vs V_{DS} As We See in Graphs Above.

- **Does r_o saturate just after the transistor enters saturation similar to g_m? Why?**

  - No, it's Not Saturate, as $r_o = \frac{1}{g_{ds}}$ and r_o represents the variation between I_D & V_{DS} and this variation can't be constant.

- **Does r_o increase if the transistor is biased more into saturation?**

  - Yes, as V_{DS} Increases, I_{DS} Increases then g_m Increases and also r_o Increases as r_o represents the variation between I_D & V_{DS}.

- **Should we operate the transistor at the edge of saturation?**

  - A MOS device is useful as an amplifier only if operated in the saturation region with drain - source voltage higher than the pinch - off voltage (edge of saturation).

  - Operating the MOSFET at the edge of saturation can have advantages in some applications, such as in switching circuits where fast switching speed is desired. In these cases, operating the MOSFET in the saturation region can minimize the switching time and reduce power dissipation during switching.

- **Where do you want to operate the transistor for analog amplifier applications? Why?**

  - As We Know Amplifier Works in Saturation Region,
    When $V_{GS} > V_{TH}$ to make the Transistor ON and Create the Channel & When $V_{DS} > V_{GS} - V_{TH}$ or $V_{DS} > V_{ov}$.
    Because the Current is somehow with Constant Value.