Cadence Virtuoso

LAB (2) Report

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Analog IC Design

Contents: -

Common Source Amplifier

Part 1

Sizing Chart

P1:

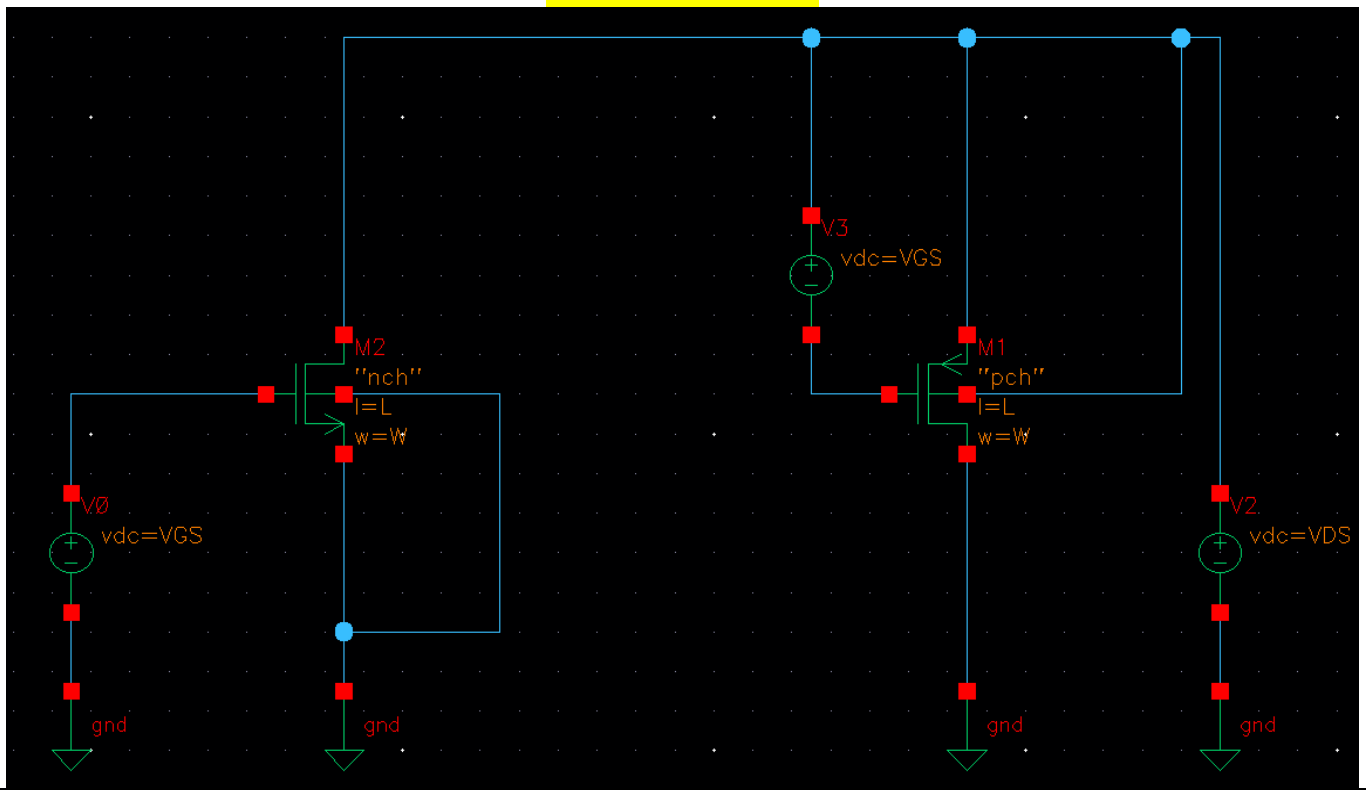
We would like to design a resistive loaded CS amplifier that meets the specifications in the Table below.

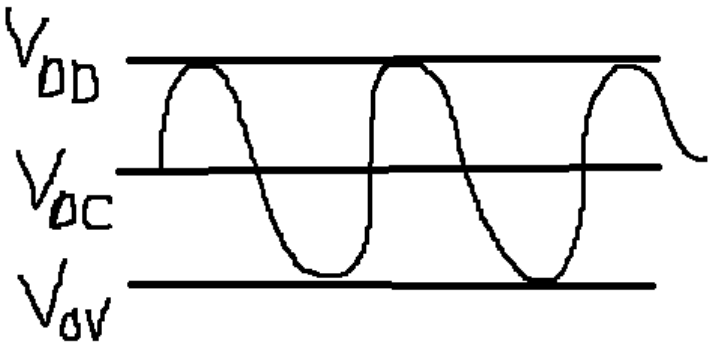
The design process involves selecting the sizing of the transistor $(\mathbf{W}\ \&\ \mathbf{L})$, the bias point $(\mathbf{V_{GS}})$ and the resistive load $(\mathbf{R_D})$.

Specs (Specifications)

DC Gain $(\mathbf{A_v})$	**-6**
Supply $(\mathbf{V_{DD}})$	**1.8 V.**
Current Consumption $(\mathbf{I_D})$	**150 µA.**

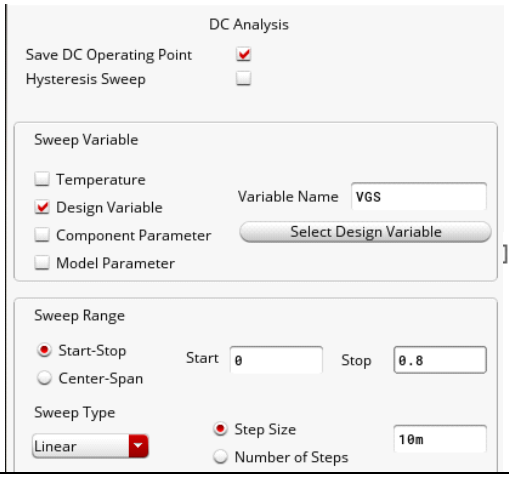
Schematic

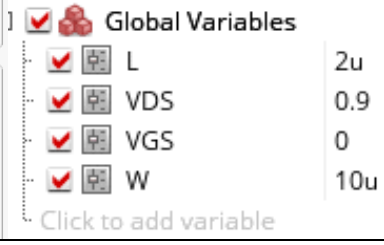


P2	**The first design decision is to choose L. Since there is no spec on bandwidth (speed), we may choose a relatively long L to provide large r_o and avoid short channel effects. Note that r_o appears in parallel with RD. Assume we will choose $L = 2\mu m$.**
P3	**→ Square Law.** $\|A_v\| \approx g_m R_D = \frac{2I_D}{V_{ov}} \times R_D = \frac{2V_{R_D}}{V_{ov}} \rightarrow$ **We used** $g_m = \frac{2I_D}{V_{ov}}, V_{ov} = \frac{2I_D}{g_m}$ $V^* = V_{ov}$ **→ For Real MOSFET.** $V_{ov} \neq \frac{2I_D}{g_m} \rightarrow$ **Define** $V^* = \frac{2I_D}{g_m} \Leftrightarrow g_m = \frac{2I_D}{V^*}$, $\|A_v\| \approx \frac{2V_{R_D}}{V^*}$
P4	 $V_{DC} = \frac{V_{DD}}{2} = V_{CM_o} = V_{R_D} = I_D \times R_D$ $V_{R_D} = \frac{V_{DD}}{2} = \frac{1.8}{2} = 0.9\ V \rightarrow I_D \times R_D = V_{R_D} \rightarrow 150\ \mu A \times R_D = 0.9$ $R_D = 6\ k\Omega$.
P5	Given $\|A_v\| = 6$ and $V_{R_D} = 0.9\ V$ $(V^* \neq V_{ov})$ $\|A_v\| = g_m R_D = \frac{2V_{R_D}}{V^*} \rightarrow V^* = \frac{2V_{R_D}}{\|A_v\|} = \frac{2 \times 0.9}{6} = 0.3\ V.$ $V_Q^* = 300\ mV.$
P6	**The remaining variable in the design is to calculate W.** **Since the square – law is not accurate,** **we cannot use it to determine the sizing. Instead,** **we will use a sizing chart generated from simulation.** **Create a testbench for NMOS and PMOS characterization** **(we will use the PMOS later in Part 2 of this lab).** **Use $W = 10\ \mu m$ (we will understand why shortly).** **and $L = 2\ \mu m$ (the same L that we chose before).**

P7

Sweep V_{GS} from 0 to $\approx V_{TH} + 0.4V = 0.8$ with 10 mV step. Set $V_{DS} = \frac{V_{DD}}{2}$.



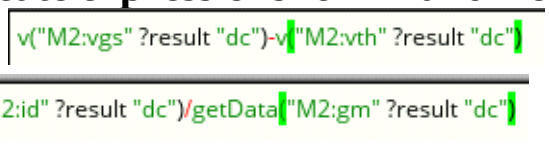


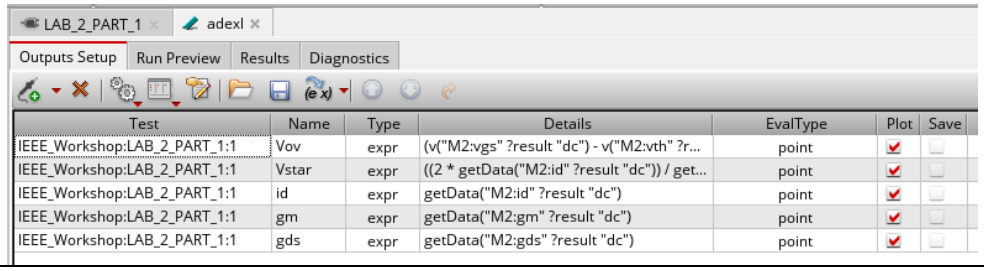
P8

We want to compare $V^* = \frac{2I_D}{g_m}$ and $V_{ov} = V_{GS} - V_{TH}$ by plotting them overlaid. Use the calculator to create expressions for V^* and Vov .

$$V_{ov} = V_{GS} - V_{th}$$

$$V^* = \frac{2I_D}{g_m}$$

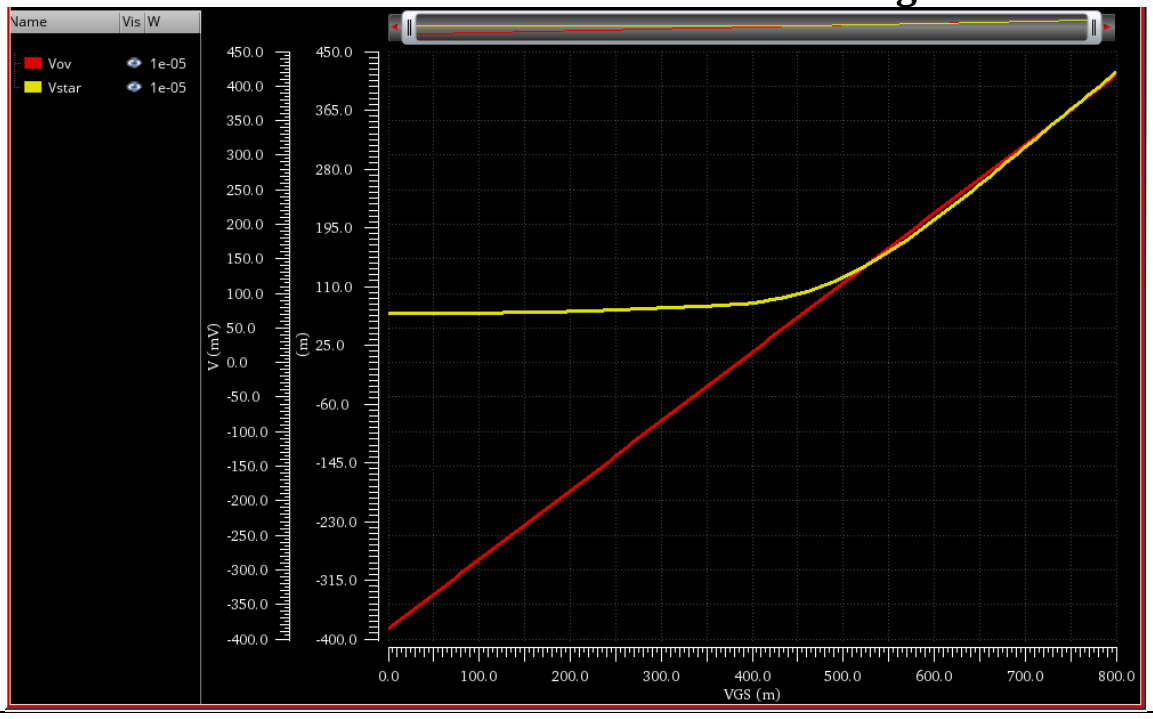




Test	Name	Type	Details	EvalType	Plot	Save
IEEE_Workshop:LAB_2_PART_1:1	Vov	expr	(v("M2:vgs" ?result "dc") - v("M2:vth" ?r...	point	☑	☐
IEEE_Workshop:LAB_2_PART_1:1	Vstar	expr	((2 * getData("M2:id" ?result "dc")) / get...	point	☑	☐
IEEE_Workshop:LAB_2_PART_1:1	id	expr	getData("M2:id" ?result "dc")	point	☑	☐
IEEE_Workshop:LAB_2_PART_1:1	gm	expr	getData("M2:gm" ?result "dc")	point	☑	☐
IEEE_Workshop:LAB_2_PART_1:1	gds	expr	getData("M2:gds" ?result "dc")	point	☑	☐

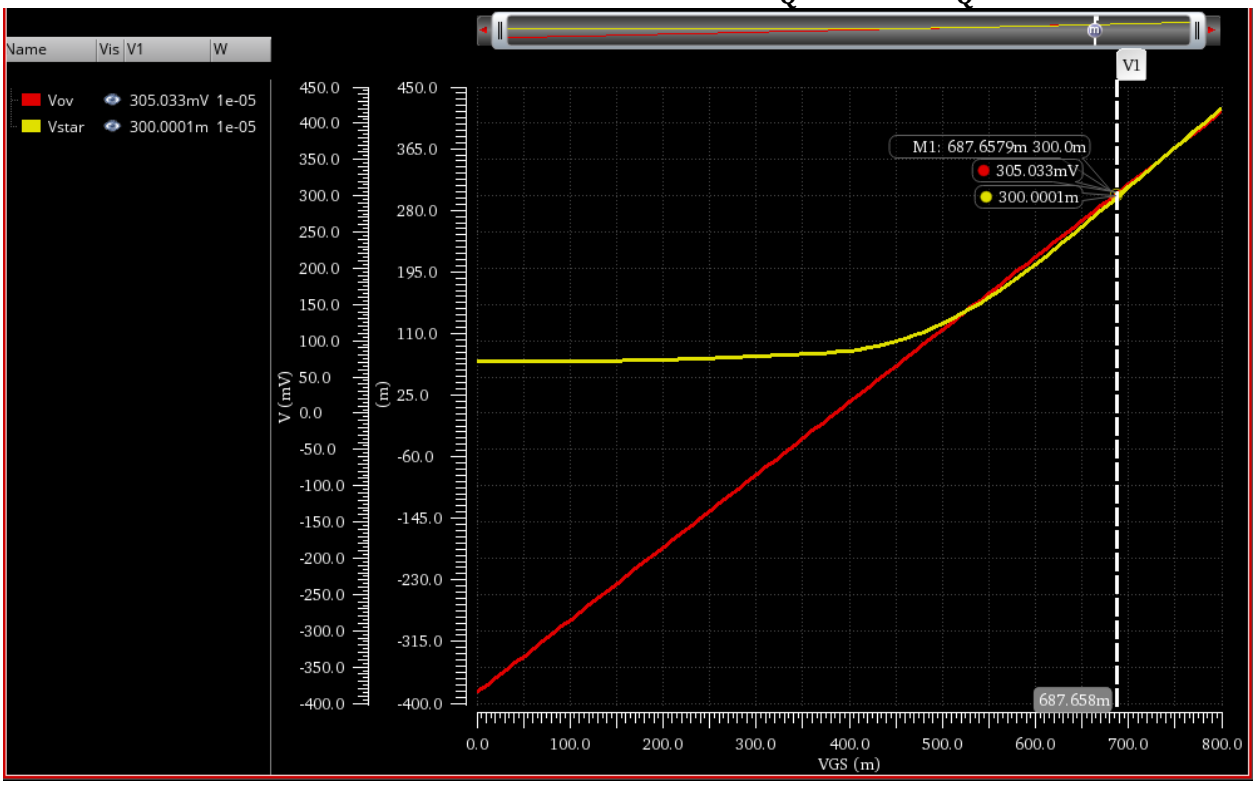
P9

Plot V^* and V_{ov} Overlaid vs V_{GS}
Y-axis of Both Curves Has Same Range



P10

On the V^* and V_{ov} Chart Locate the Point at Which $V^* = V_Q^*$ Find the Corresponding V_{ov_Q} and V_{GS_Q}.

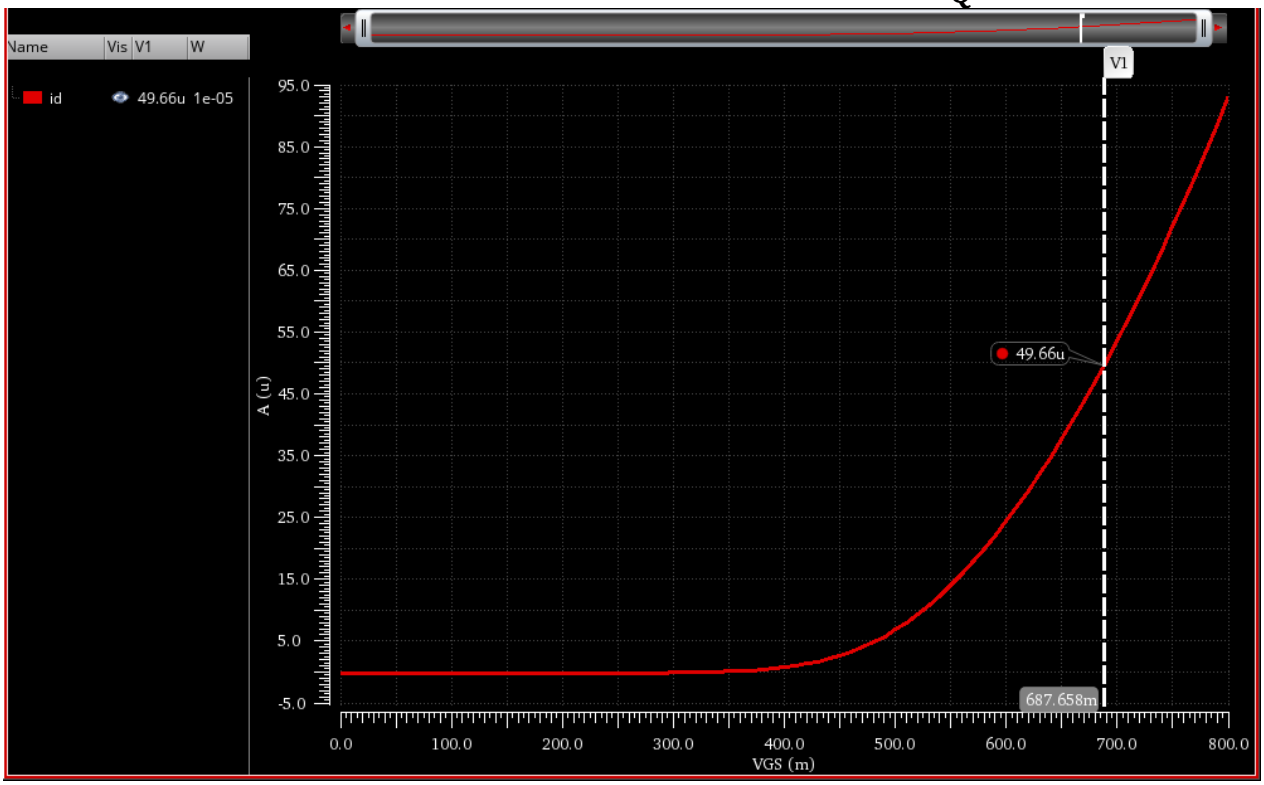


$$@\ V_Q^* = 300\ \text{mV} \rightarrow V_{ov_Q} = 305.033\ \text{mV}.$$

$$\rightarrow V^* = 300.0001\ \text{mV} \rightarrow V_{GS_Q} = 687.658\ \text{mV}.$$

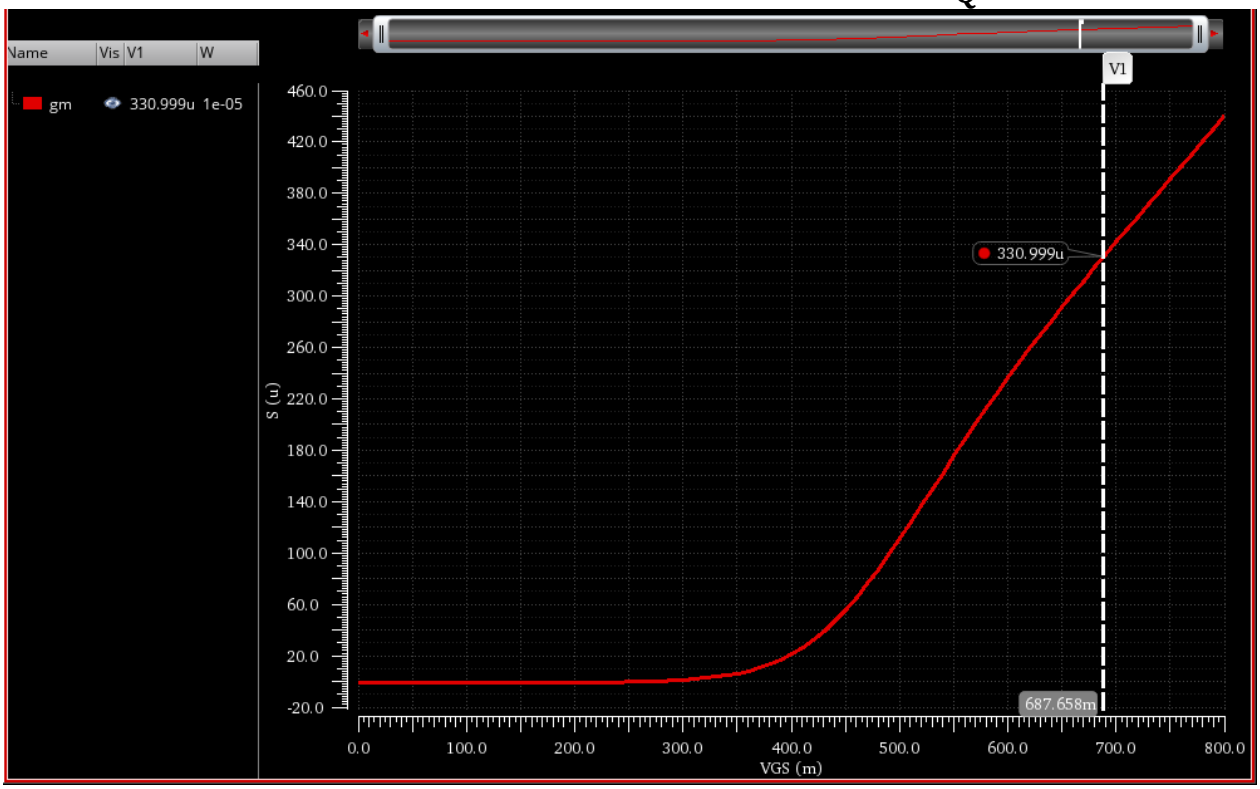
P11

Plot I_D vs V_{GS}. Find its Values at V_{GS_Q}



$$@V_{GS_Q} = 687.658\ \text{mV} \rightarrow I_{D_X} = 49.66\ \mu\text{A}.$$

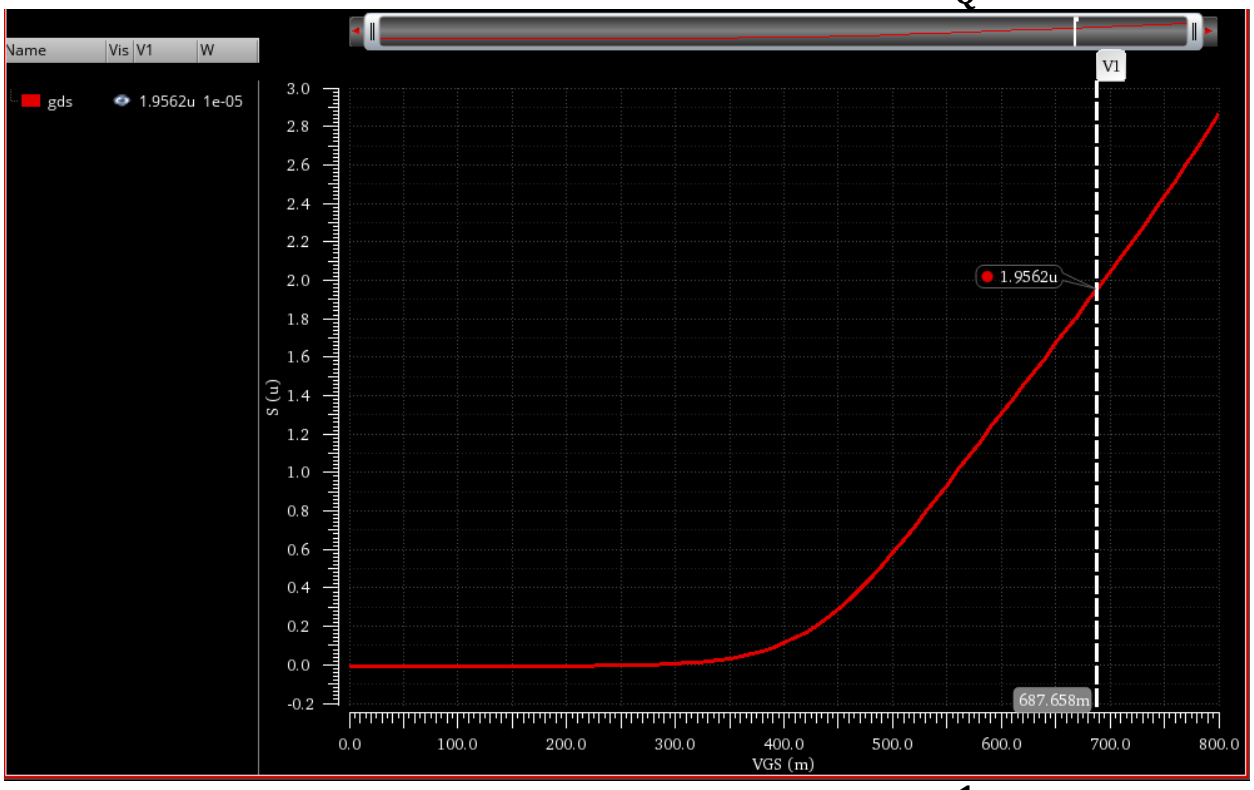
Plot g_m vs V_{GS}. Find its Values at V_{GS_Q}



$$@V_{GS_Q} = 687.658\ \text{mV} \rightarrow g_{m_X} = 330.999\ \mu\text{S}.$$

P11

Plot g_{ds} vs V_{GS}. Find its Values at V_{GS_Q}



$$@V_{GS_Q} = 687.658\ \text{mV} \rightarrow g_{ds_X} = 1.9562\ \mu\text{S} \rightarrow r_o = \frac{1}{g_{ds_x}} = 511.2\ \text{k}\Omega$$

P12

Now back to the assumption that we made that $W = 10\mu m$.
This is not the actual value that we will use for our design.
But the good news is that I_D is always proportional to W irrespective of the operating region and the model of the MOSFET (regardless square – law is valid or not). Thus, we can use ratio and proportion (cross-multiplication) to determine the correct width at which the current will be $I_{D_Q} = 150\ \mu A$ as given in the specs.
Calculate W as shown below.

W	I_D
$W_{assumed} = 10\ \mu m$	I_{D_X} @ V_Q^* (From The Chart)
$W_{required} = ?$	$I_{D_Q} = 150\ \mu A$ (From The Specs)

W	I_D
$W_{assumed} = 10\ \mu m$	I_{D_X} @ V_Q^* (From The Chart) $= 49.66\ \mu A$
$W_{required} = ?$	$I_{D_Q} = 150\ \mu A$ (From The Specs)

$$W_{required} = 30.21\ \mu m.$$

P13

Now we are almost done with the design of the amplifier.
Note that g_m is also proportional to W as long as V_{ov} is constant.
On the other hand, $r_o = \frac{1}{g_{ds}}$ is inversely proportional to W (I_D) as long as L is constant. Before leaving this part, calculate g_{m_Q} and g_{ds_Q} using ratio and proportion (cross-multiplication) and double check that $A_v = -g_m(R_D||r_o)$ meet the required gain spec.

g_m	W
$g_{m_X} = 330.999\ \mu S$	$W_{assumed} = 10\ \mu m$
$g_{m_{required}} = ?$	$W_{required} = 30.21\ \mu m$

$$g_{m_{required}} = 999.95\ \mu S.$$

g_{ds}	W
$g_{ds_X} = 1.9562\ \mu S$	$W_{assumed} = 10\ \mu m$
$g_{ds_{required}} = ?$	$W_{required} = 30.21\ \mu m$

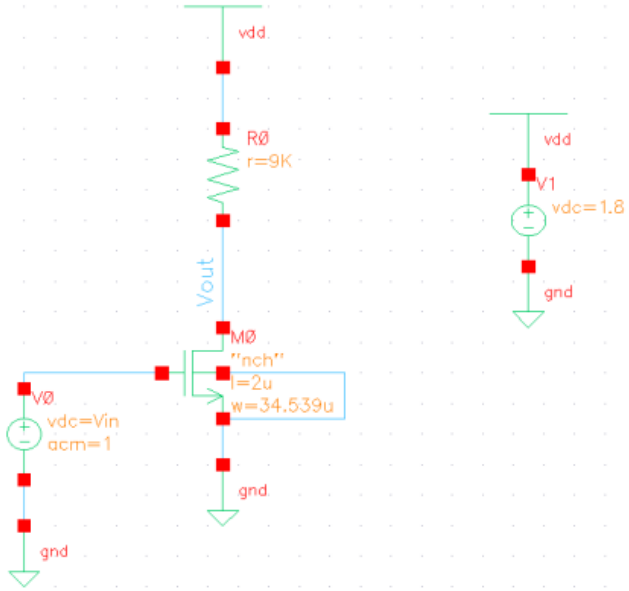
$$g_{ds_{required}} = 5.91\ \mu S \rightarrow r_o = 169.214\ k\Omega$$

Check The Gain: $|A_v| = g_m(R_D||r_o) = 5.794$
Compared by $|A_v| = 6$ this error due to ignoring r_o we can raise it by increase L or R_D.

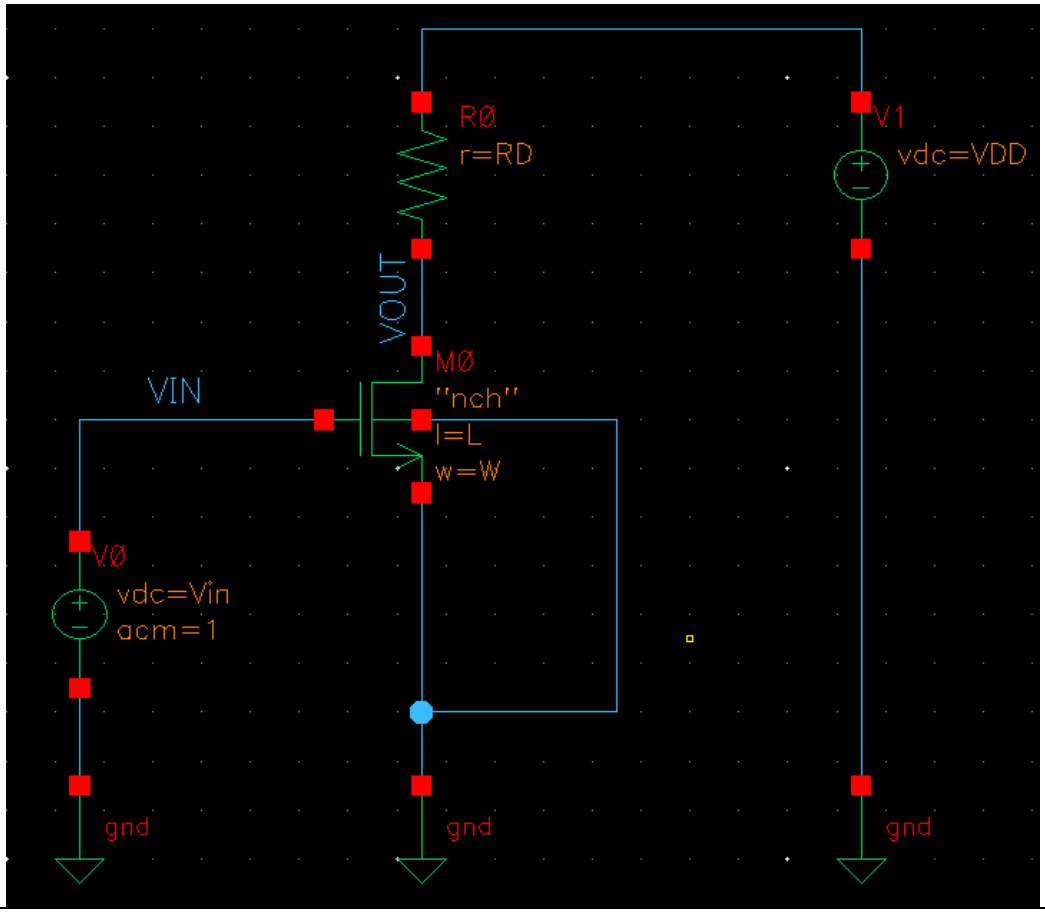
Part 2

CS Amplifier

Circuit



Schematic



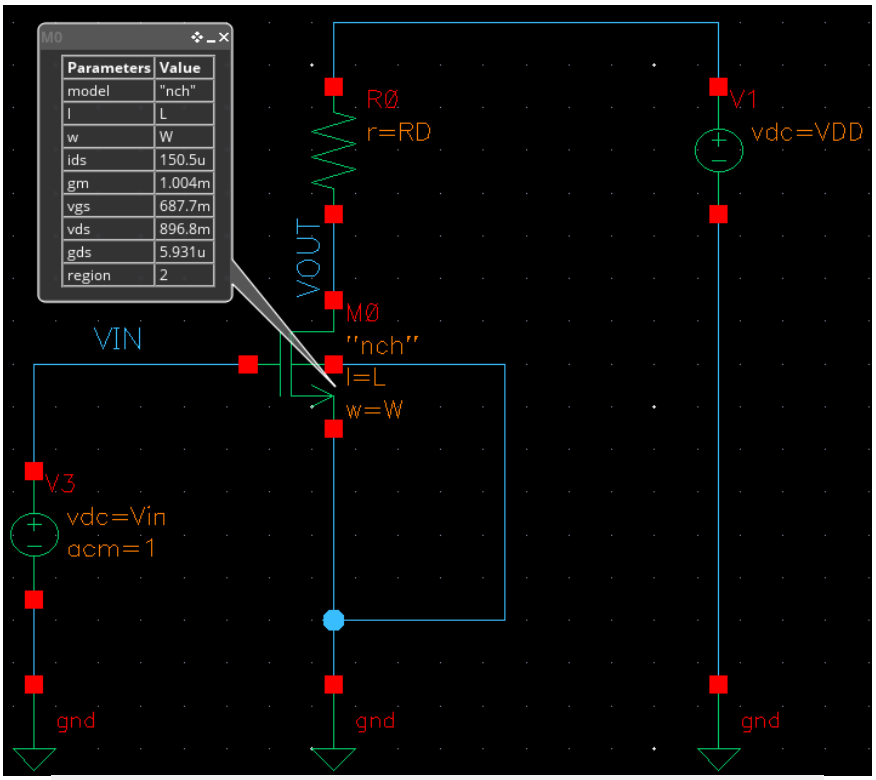
OP and AC Analysis

Q1

Create a testbench for the resistive loaded CS amplifier using the V_{GS_Q} , R_D, L, and W that you got from the previous part.

Global Variables	
L	2u
RD	6k
VDD	1.8
Vin	687.658m
W	30.21u
Click to add variable	

Q2



Label	Display Mode	Expression	Annotate	Balloon
Terminal:cdsTerm(B)	none		☑	☑
Terminal:cdsTerm(D)	none		☑	☑
Terminal:cdsTerm(G)	none		☑	☑
Terminal:cdsTerm(S)	none		☑	☑
Parameter:cdsParam(1)	Component Parameter	☐ model	☑	☑
Parameter:cdsParam(2)	Component Parameter	☑ l	☑	☑
Parameter:cdsParam(3)	Component Parameter	☑ w	☑	☑
Parameter:cdsParam(4)	DC Operating Point	☑ ids	☐	☑
Parameter:cdsParam(5)	DC Operating Point	☑ gm	☐	☑
Parameter:cdsParam(6)	DC Operating Point	☑ vgs	☐	☑
Parameter:cdsParam(7)	DC Operating Point	☑ vds	☐	☑
Parameter:cdsParam(8)	DC Operating Point	☑ gds	☐	☑
Parameter:cdsParam(9)	DC Operating Point	☑ region	☐	☑
Name:cdsName()	Instance Name		☑	☑

$$I_{DS} = 150.5\ \mu A\ ,\ g_m = 1.004\ mS\ ,\ V_{GS} = 687.7\ mV\ ,$$
$$V_{DS} = 896.8\ mV,\ g_{ds} = 5.931\ \mu S\ ,\ \text{Region} = 2\ (\text{Saturation}).$$

Q2

DC OP	Part 1	Part 2	Error
I_{DS}	150 µA	150.5 µA	0.33 %
g_m	999.95 µS	1.004 mS	0.4 %
g_{ds}	5.91 µS	5.931 µS	0.36 %
V_{DS}	900 mV	896.8 mV	0.36 %
V_{GS}	687.658 mV	687.7 mV	0.0061 %

Q3

- **Compare r_o and R_D Is the assumption of ignoring r_o justified in this case? Do you expect the error to remain the same if we use min L?**
  - For this case: $r_o = \frac{1}{g_{ds}} = 168.61\ k\Omega\ , R_D = 6\ k$
    Since, $r_o \gg R_D$ and r_o & R_D Connected Parallel to each other.
    Therefore, We Can Ignore r_o for (Long Channel)
    (The assumption of ignoring r_o justified in this case)
  - The Error is Very Small.
  - $|A_V| = g_m R_D = 6.024\ , |A_V| = g_m(r_o // R_D) = 5.817$
  - For short channel lengths, r_o would be comparable to R_D, and this approximation would not be reliable anymore.

Q4

- **Calculate the intrinsic gain of the transistor. $|A_i| = g_m r_o$**
  - $|A_v| = g_m R_D = 6.024\ \ ,\ \ |A_i| = 1.004m \times \frac{1}{5.931\mu} = 169.28$

Q5

- **Calculate the amplifier gain analytically.**
  What is the relation (≪, <, ≈, >, ≫) between the amplifier gain and the intrinsic gain?
  - $|A_v| = g_m R_D = 6.024\ ,\ |A_i| = g_m r_o = 169.28$
  - Amplifier Gain ≪ Intrinsic Gain.
  - Intrinsic Gain is the maximum Gain can the Transistor Reach.

Q6

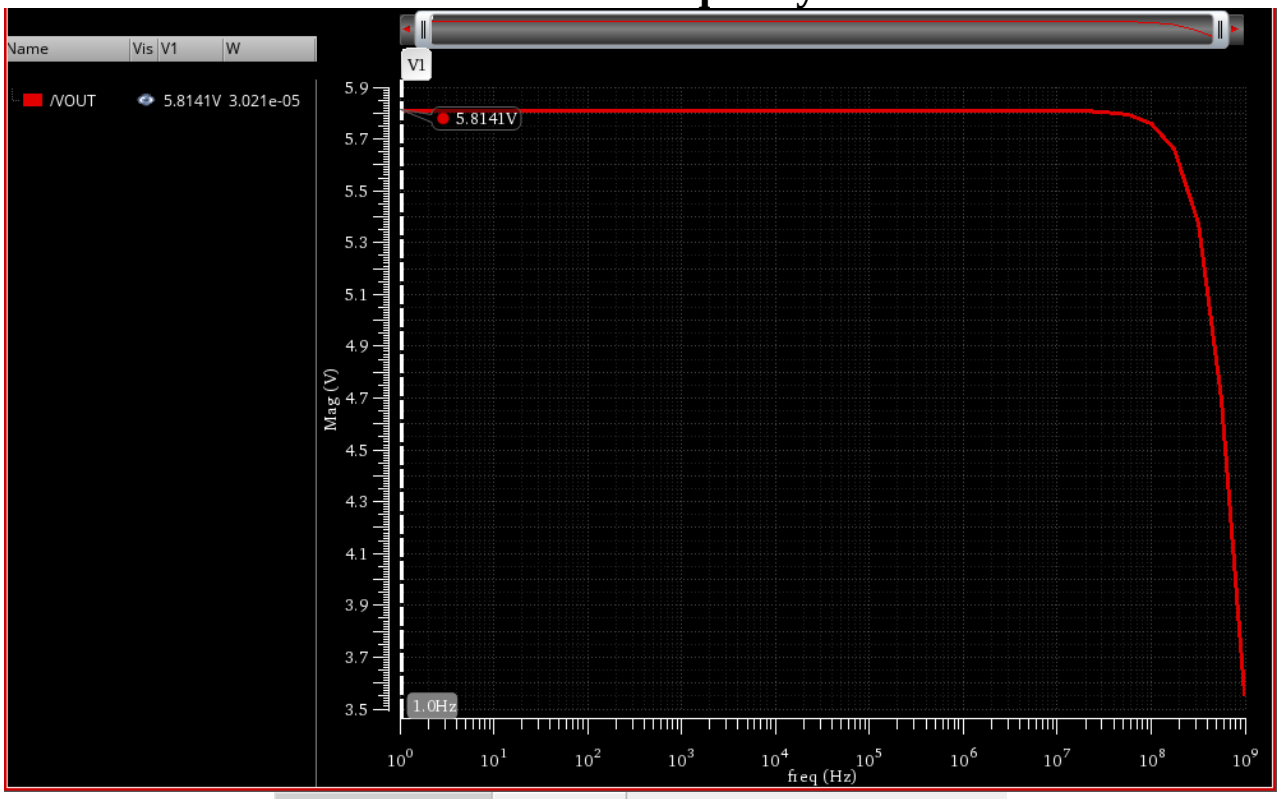
Create a new simulation configuration and run AC analysis (from 1 Hz to 1 GHz).

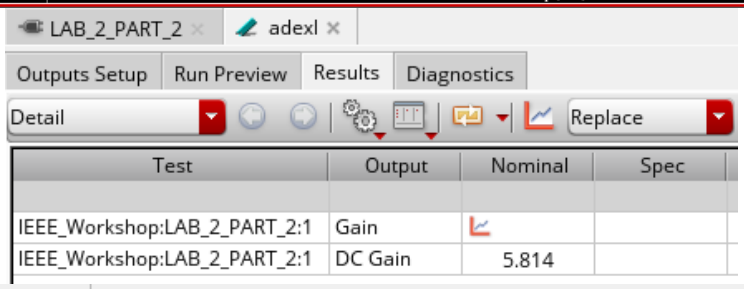
Report the gain vs frequency.

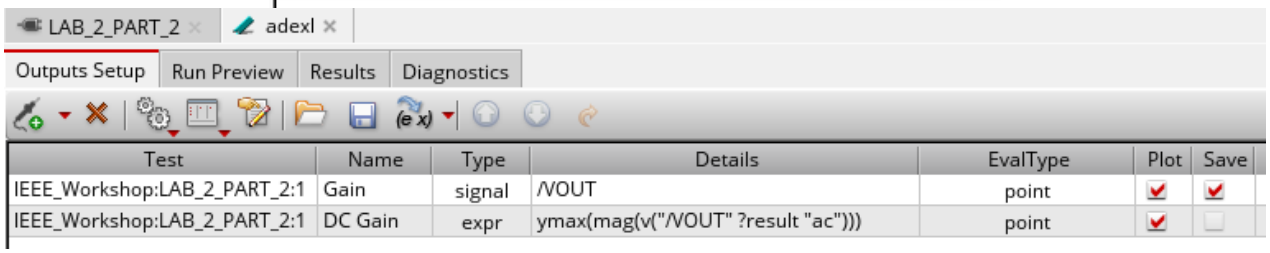
Annotate the DC gain and make sure it meets the spec.

$$\text{Gain} = \frac{V_{out}}{AC-Vin} = \frac{V_{out}}{1} = V_{out}$$

Gain Vs Frequency







$\text{Gain} = 5.814$, $|A_v| = 6$ (Specs) , $\text{Error} = 3.1\ \%$

The DC gain roughly meets the spec, and This Error Due to in Specs $\text{Gain} = g_m R_D = 6$ Neglecting the r_o.

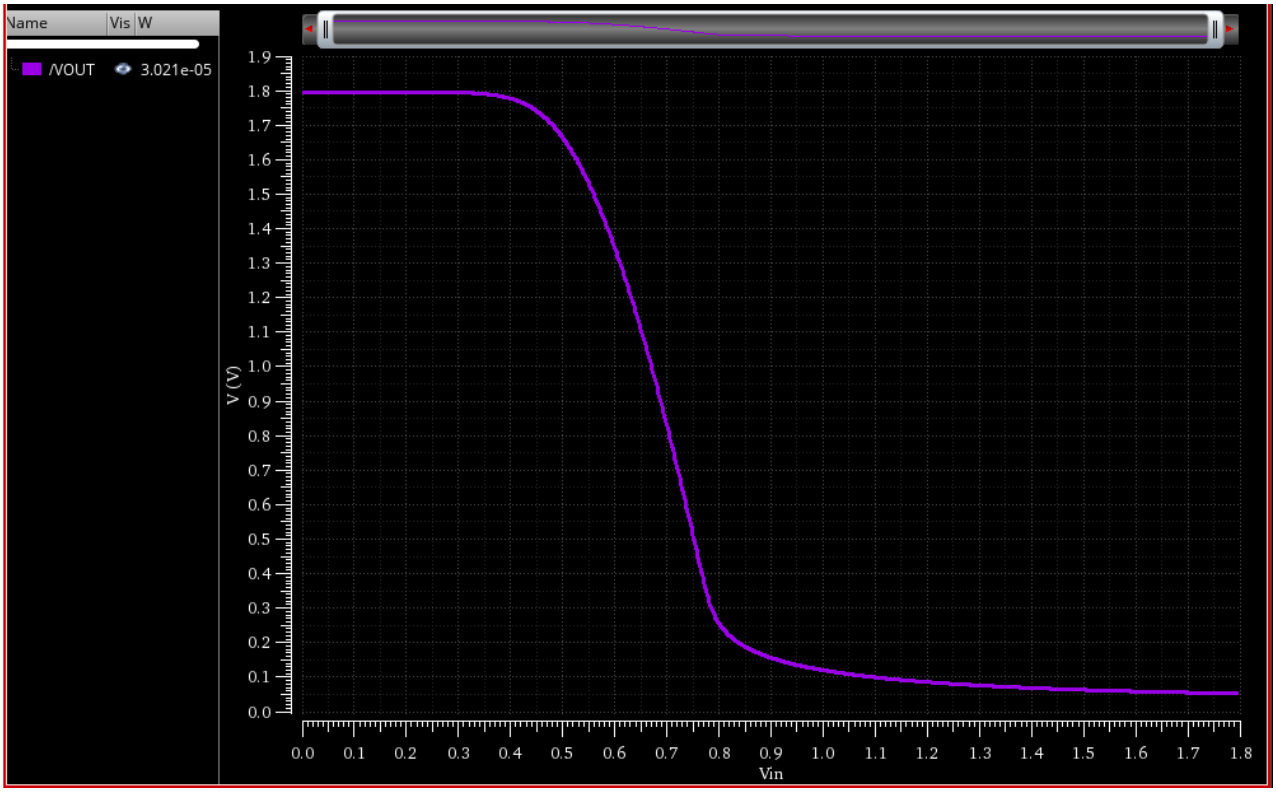
The Simulation $\text{Gain} = g_m(R_D||r_o) = 5.814$ take r_o into consideration.

To make this gain approach to the Specs Gain then we Want to Increase (L because L is inverse proportional to r_o) or (R_D) .

Gain Non – Linearity

Q1

Create a new simulation configuration. Perform a DC sweep for the input voltage from 0 to V_{DD} with 2 mV step.



Q2

Report V_{out} vs V_{in}. Is the relation linear? Why?

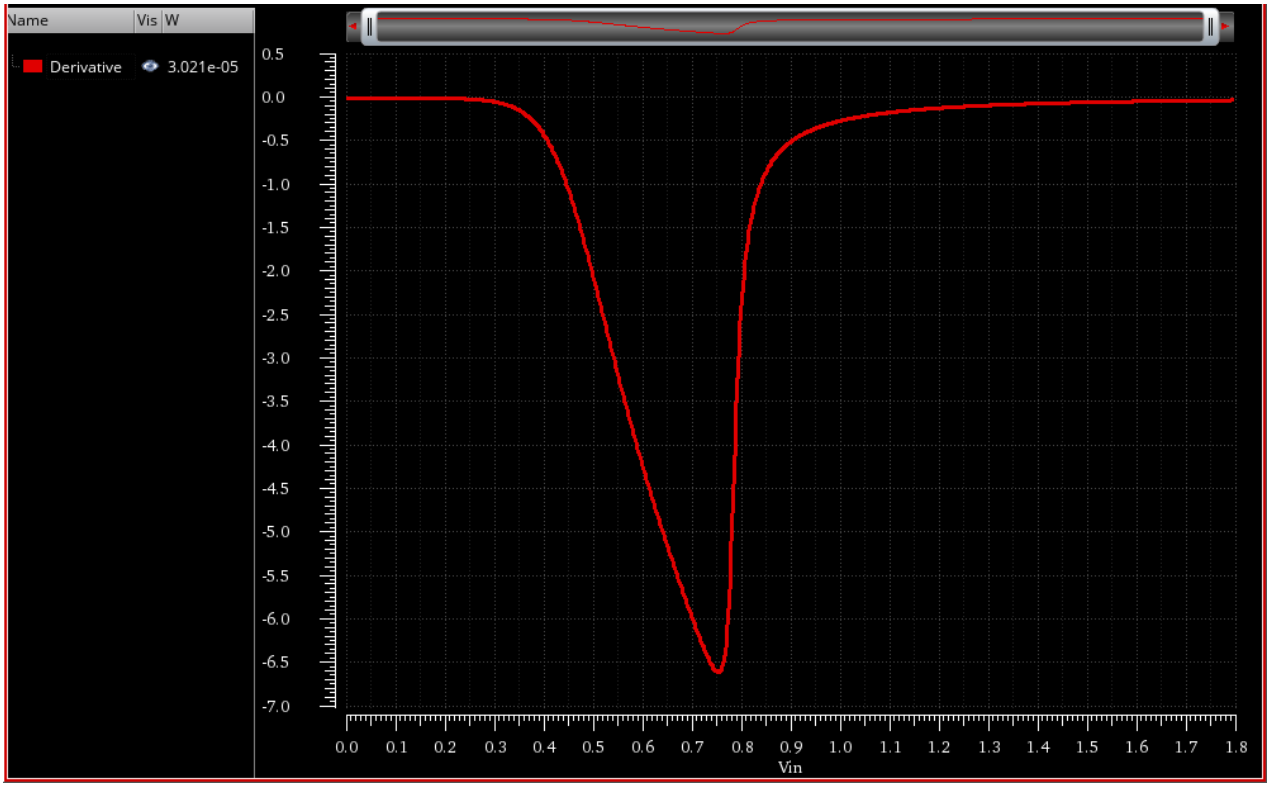
- The relation between V_{out} and V_{in} is nonlinear because changing V_{in} will change gm (function of V_{in}) so the gain changes (function of V_{in}) so V_{out} changes, but we can say that it almost linear in saturation region when input signal is small, and linearity improves as input signal amplitude decreases.
  - Before V_{th} , I_D approximately is zero before it starts to change in subthreshold region then, $V_{out} = V_{DD}$.
  - After V_{th} & $(V_{GS} = V_{in}) < V_{DS} + V_{TH}$, the transistor acts in saturation region. (Linear relation)
  - After reaching $(V_{GS} = V_{in}) > V_{DS} + V_{TH}$, the transistor acts in triode region. (Non - Linear relation)

Q3

→ Calculate the derivative of V_{out} using calculator.

```
deriv(v("/VOUT" ?result "dc"))
```

Plot the derivative vs V_{in}. The derivative is itself the small signal gain.



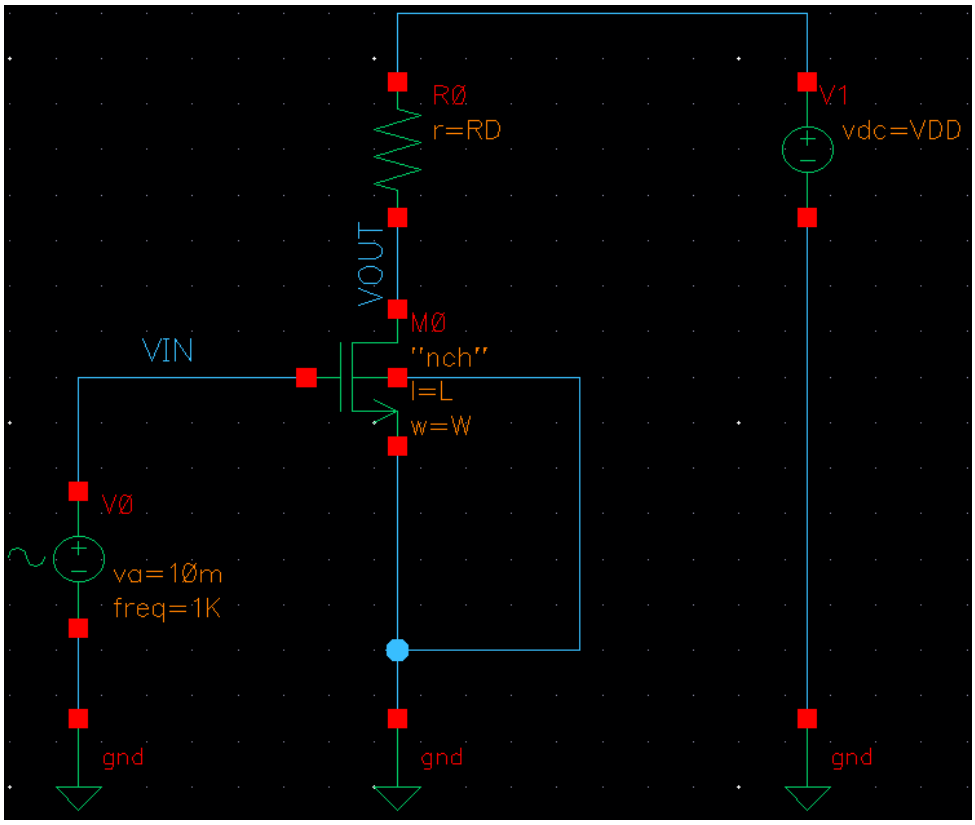
Is the gain linear (independent of the input)? Why?

- It's non-linear (dependent on the input), because for each bias voltage (V_{GS}), there's different transconductance. The gain of amplifier is non – linear and depends on the transconductance, $g_m = K(V_{GS} - V_{TH})$. However, for small signals, the gain is roughly constant and depends only on the dc bias voltage.

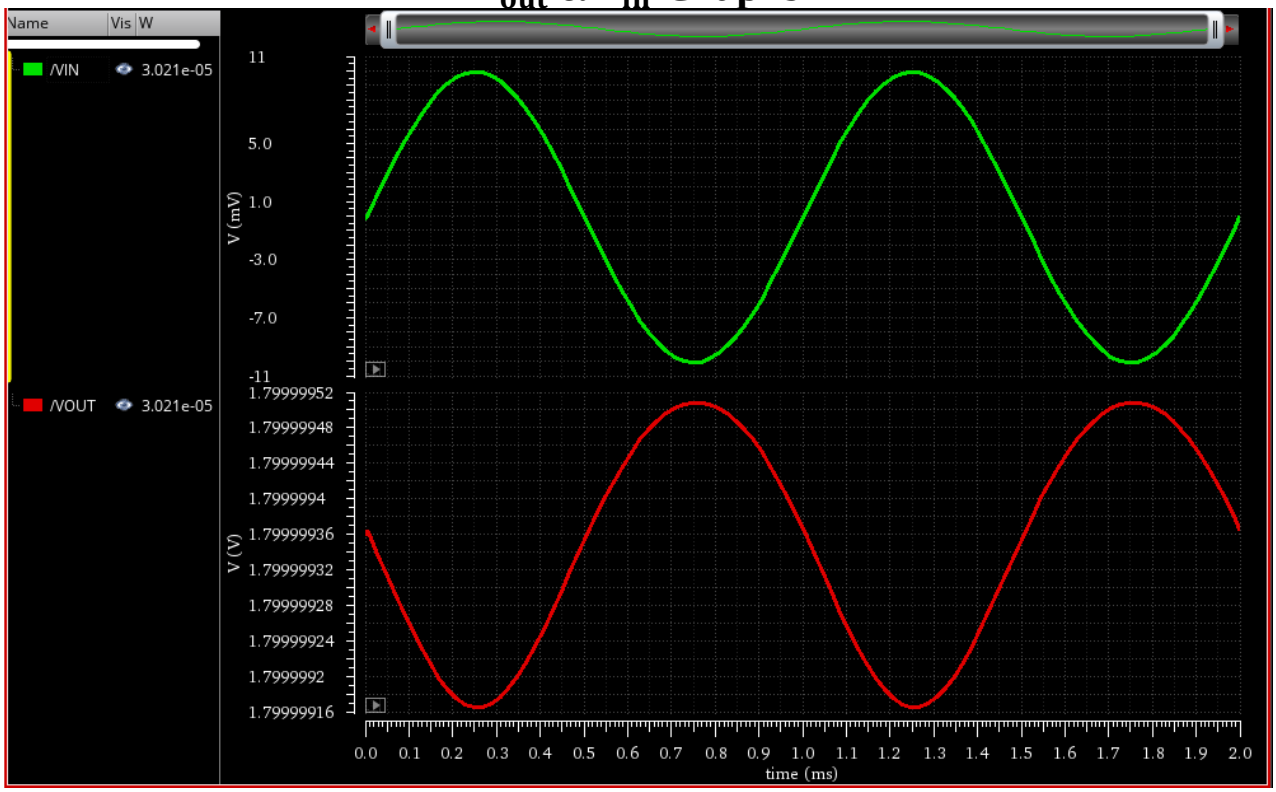
- The gain is nonlinear where it is function of (V_{in}) and gain isn't constant for different V_{in} where gain increases in saturation region by increasing V_{in} until it reaches max value at edge of saturation then it decreases again in triode region.

Q4

Set the properties of the voltage source to apply a transient stimulus (sine wave of 1kHz frequency and 10 mV amplitude superimposed on the DC input voltage).



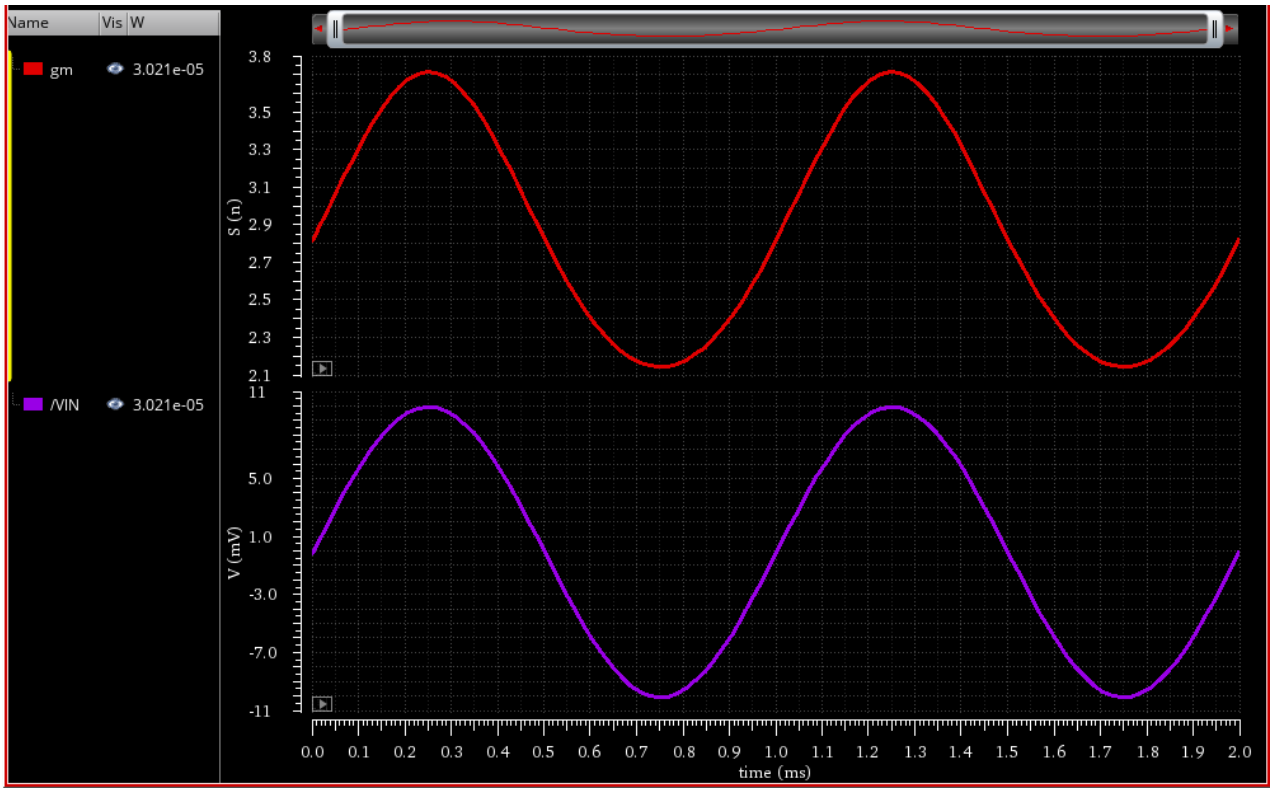
V_{out} & V_{in} Graphs



Green Curve = V_{in} , Red Curve = V_{out}

Q5

Create a new simulation configuration.
Run transient simulation for 2ms. Plot g_m vs time.



Purple Curve = V_{in} , Red Curve = g_m

- **Does g_m vary with the input signal? What does that mean?**
  - Yes, g_m Vary With V_{in} As gm varies like the input signal with same frequency, but around the dc transconductance. (Changes in micro siemens) as g_m is function of V_{in} and the gain is non-linear.

Q6

- **Is this amplifier linear? Comment.**
  - No, it's Not Linear.
    The amplifier is non – linear for large signal model (DC, Transient) because its gain varies with the input voltage. However, for small signals (AC) like the 10mv signal here, it could be approximated to say it's linear. In the above graph, we can see that V_{out} is an amplified version of vin with no distortion, and that was my conclusion.