Cadence Virtuoso
LAB (6) Report

By: Magdy Ahmed Abbas Abdelhamid

Analog Electronics Workshop

Differential Amplifier

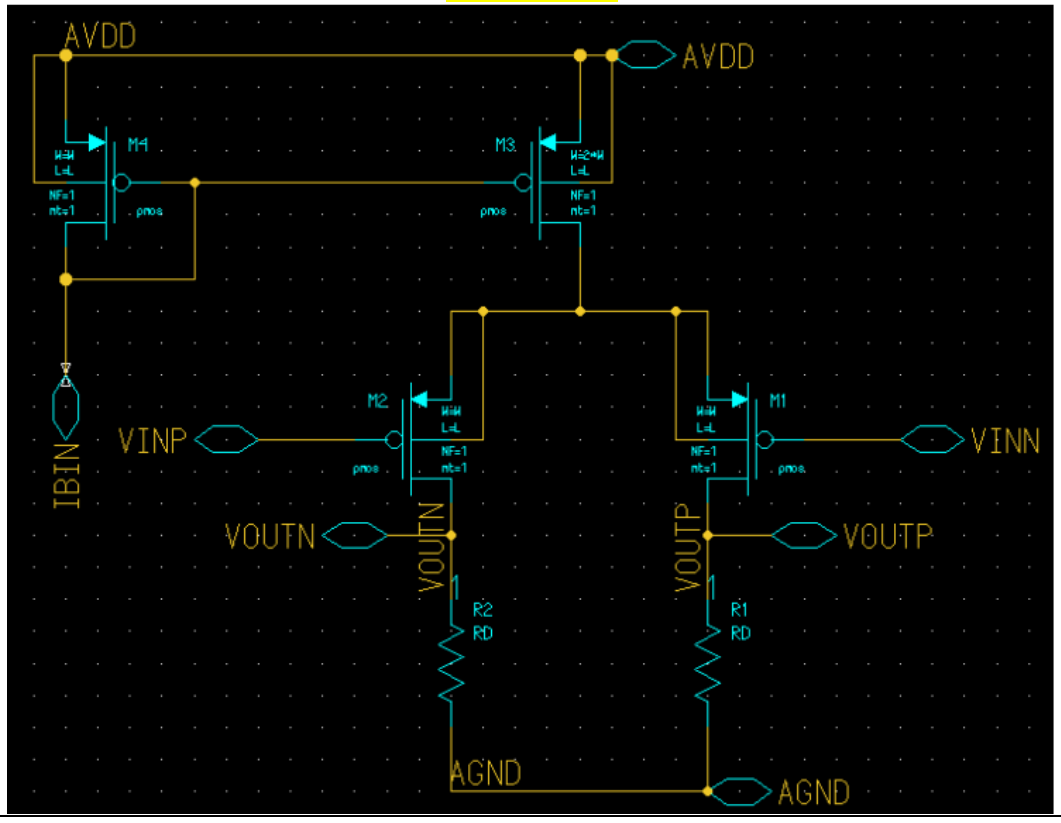
Part 1

Sizing Chart

Specs (Specifications)

For Each Transistor (I_D)	20 µA.
Supply (V_{DD})	1.8 V.
Bias Current (I_{SS})	40 µA.
Length (L)	1 µm.
CM Output Level	0.7
Differential Gain	8
Width (W)	22.5 µm.
g_m	229.5 µS.
g_{ds}	1.644 µS.

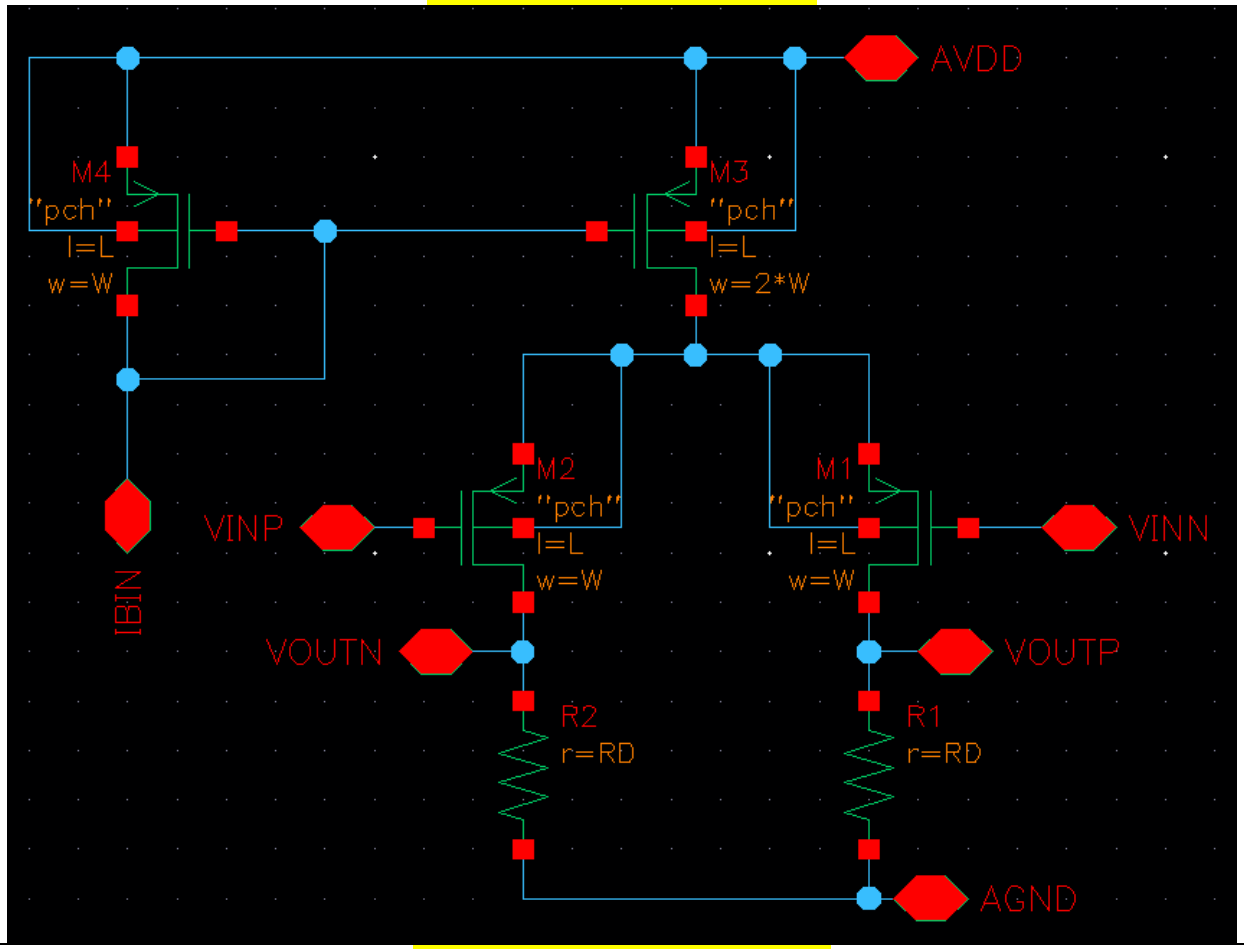
Circuit



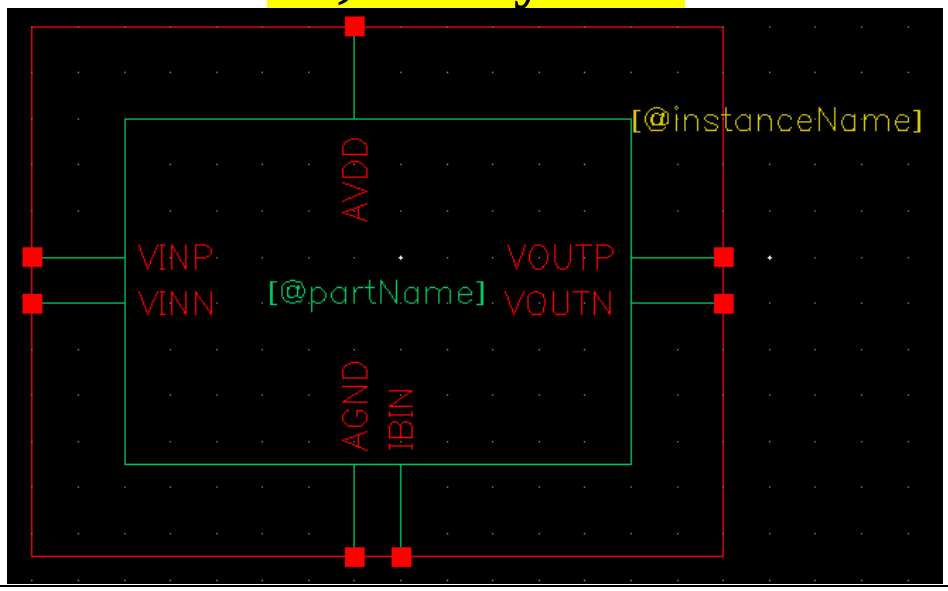
Part 2

Diff Amplifier

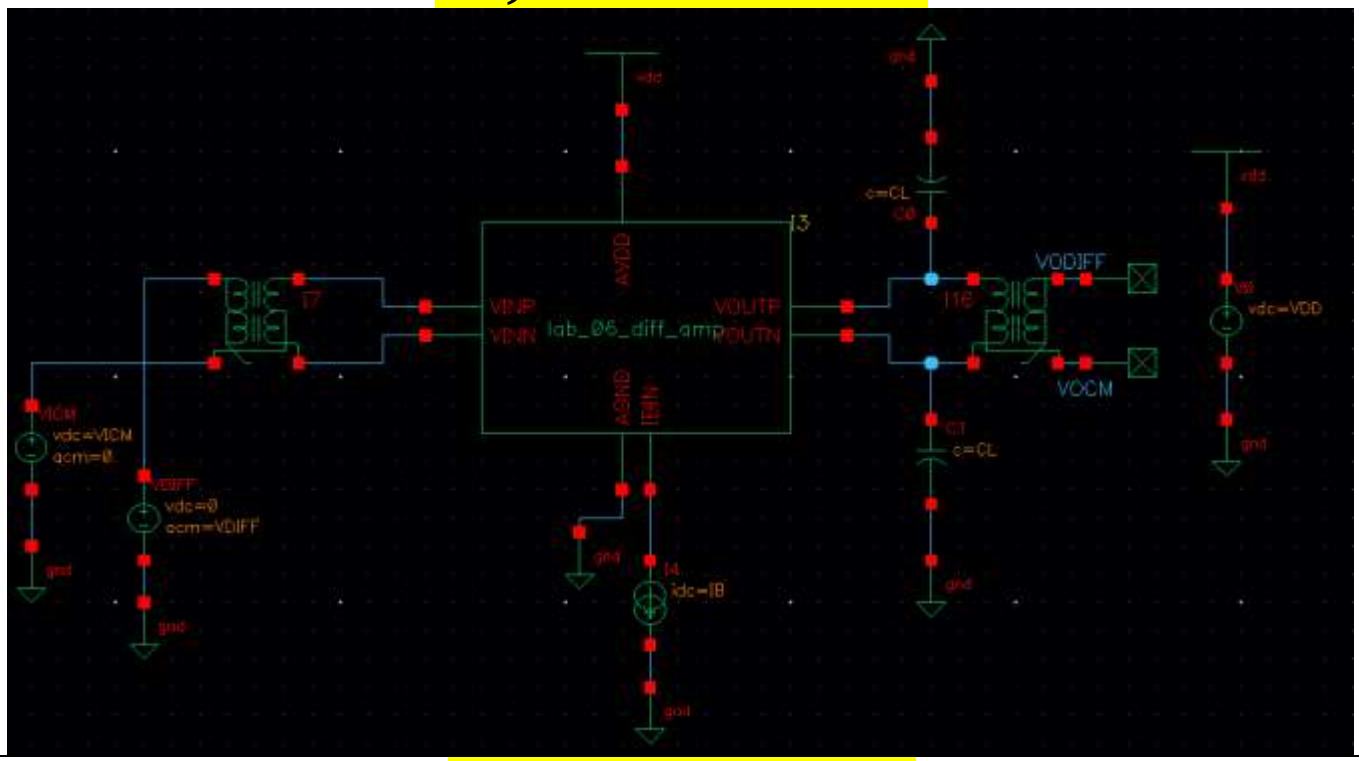
P1: Schematic



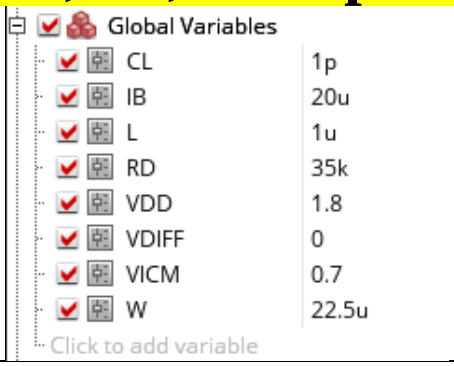
P2, P3: Symbol



P4, P5: Schematic



P6, P7, P8: Specs



P9

- **Analytically calculate the valid range for Vicm: the common mode input range (CMIR). Set Vicm at the center of this range.**

$\rightarrow$ To Make M_1 & M_2 In Saturation

$$V_g = VICM > V_D - |V_{th}|, R_D = \frac{V_{outCM}}{I_D} = \frac{0.7\ V}{20\ \mu A} = 35\ k\Omega$$

$$Since, V_D = 0.7\ V, V_{th} = 0.41\ V.$$

$$VICM \geq -|V_{th}| + \frac{1}{2} I_{SS} R_D$$

$$VICM_{Min} = V_D - V_{th} = 0.29\ V.$$

$\rightarrow$ To Make M_3 In Saturation

$$V_{DD} = V_{ov_3} + V_{sg_1} + VICM_{Max}$$

$$VICM_{Max} = V_{DD} - V_{ov_3} - (V_{ov_1} + |V_{th}|)$$

$$Since, V_{ov_3} = V_{ov_1} = 170.5\ mV., V_{th} = 0.41\ V.$$

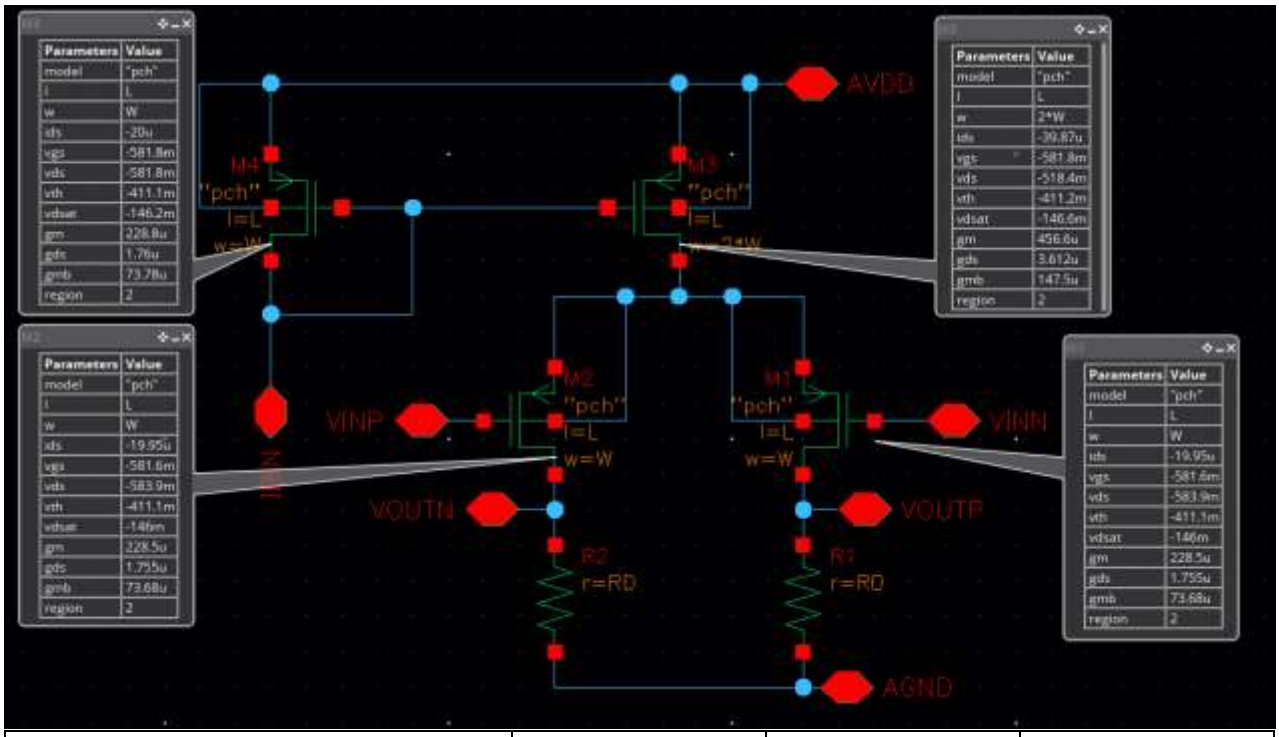
$$VICM_{Max} = V_{DD} - 2V_{ov} - |V_{th}| = 1.049\ V.$$

Report The Following: -

(1) OP Simulation

Q1

Report the schematic of the diff pair with DC OP point clearly annotated: $i_d, v_{gs}, v_{ds}, v_{th}, v_{dsat}, g_m, g_{ds}, g_{mb}$, region.



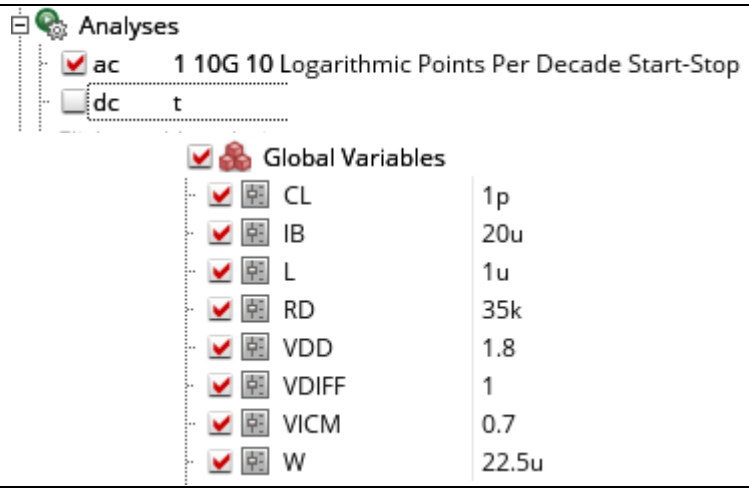
For M_1 & M_2		Parameters	For M_3	For M_4
I_{ds}	$-19.95\ \mu A$	I_{ds}	$-39.87\ \mu A$	$20\ \mu A$
V_{gs}	$-581.6\ mV$	V_{gs}	$-581.8\ mV$	$-581.8\ mV$
V_{ds}	$-583.9\ mV$	V_{ds}	$-518.4\ mV$	$-581.8\ mV$
V_{th}	$-411.1\ mV$	V_{th}	$-411.2\ mV$	$-411.1\ mV$
V_{dsat}	$-146\ mV$	V_{dsat}	$-146.6\ mV$	$-146.2\ mV$
g_m	$228.5\ \mu S$	g_m	$456.6\ \mu S$	$228.8\ \mu S$
g_{ds}	$1.755\ \mu S$	g_{ds}	$3.612\ \mu S$	$1.76\ \mu S$
g_{mb}	$73.68\ \mu S$	g_{mb}	$147.5\ \mu S$	$73.78\ \mu S$
region	2	region	2	2

Q2

- **Check that all transistors operate in saturation.**
  - **From Above All Transistors have Region = 2 (In Saturation Region).**

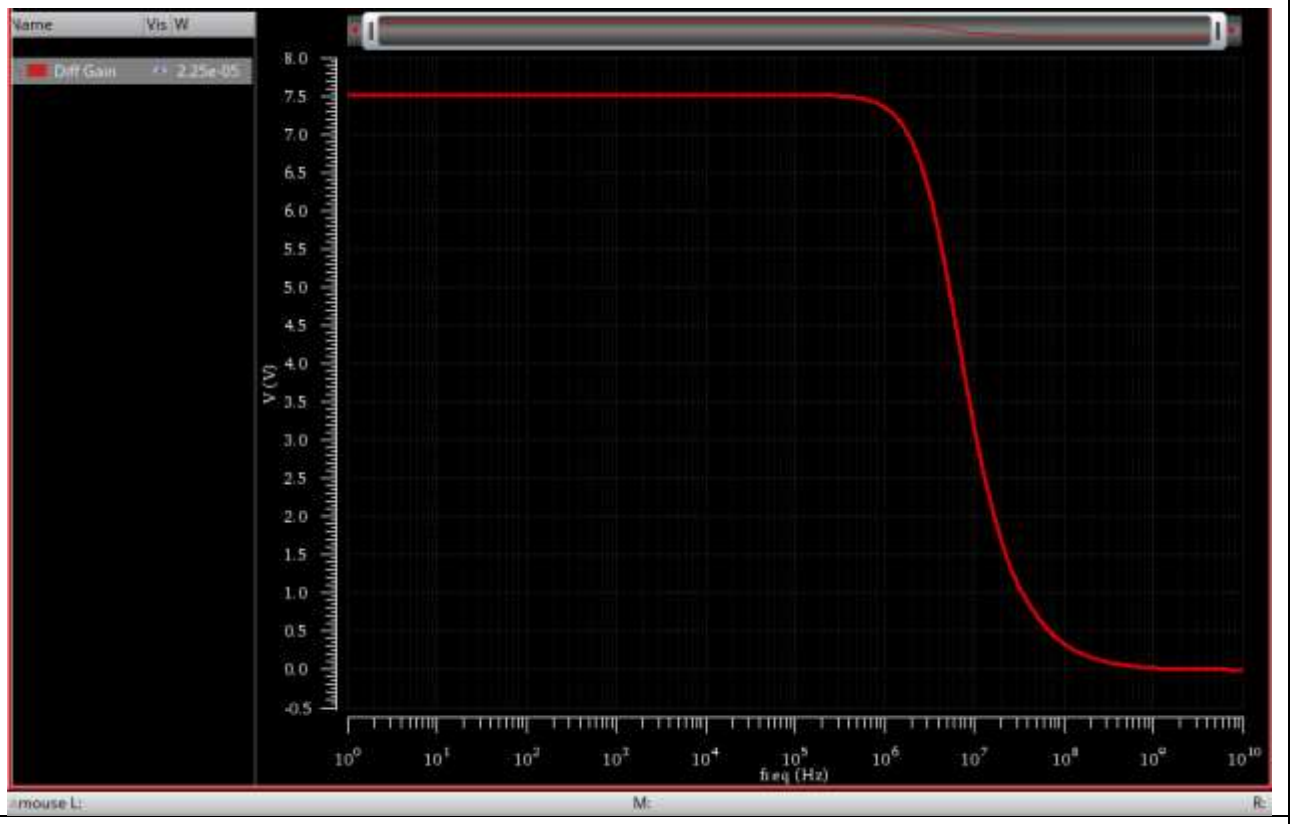
(2) Diff. Small Signal CCS.

Q1, Q2, Q3



Q4

Report the Bode plot of small signal diff gain.



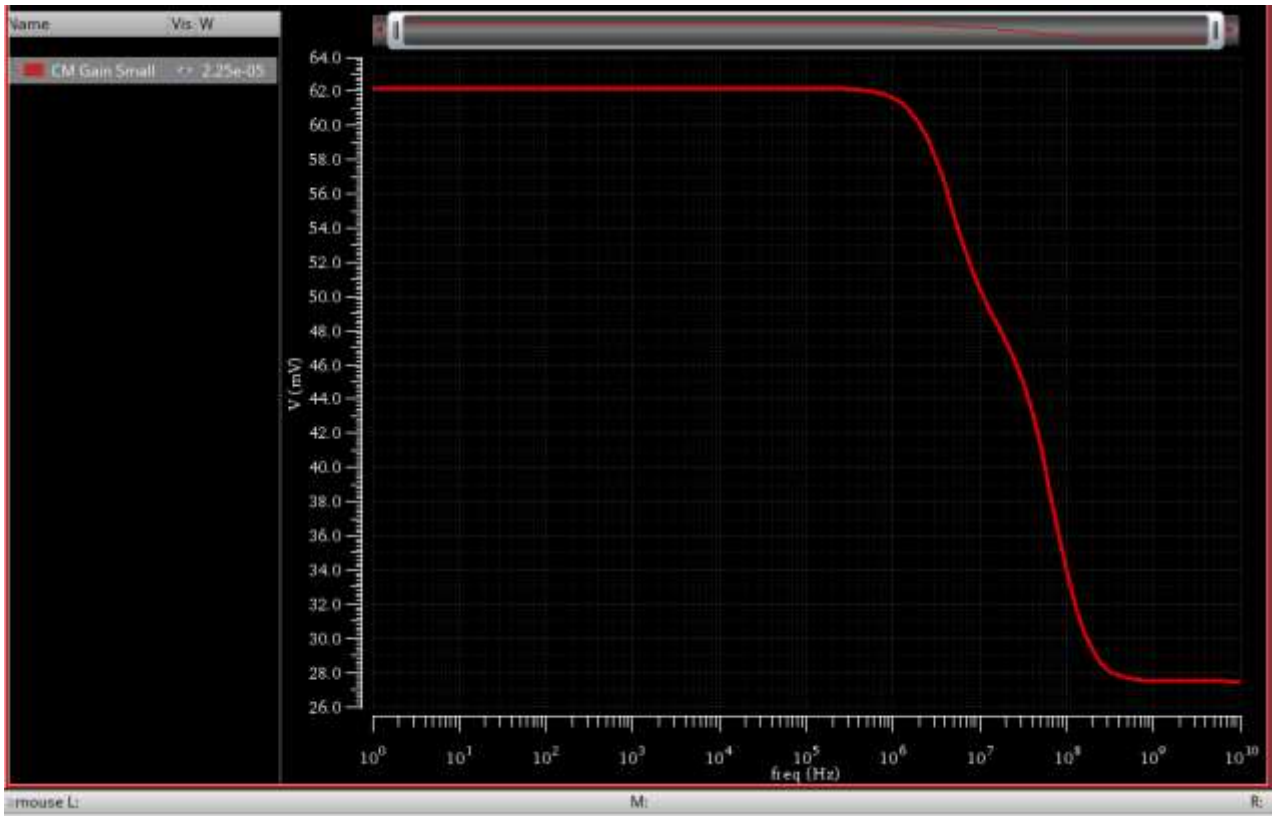
Q5

Compare the DC diff gain and BW with hand analysis in a table.

P.O.C	Simulation	Hand Analysis
Diff Gain (A_{Diff})	7.53	$A_V = g_m * (R_D // r_o)$
BW	4.678 MHZ	$BW = \frac{1}{2\pi R_D C_L} = 4.54$ MHZ

(3) CM Small Signal CCS.

Q1 **Report the Bode plot of small signal CM gain.**



Q2

Q3

Q4 **Compare the DC CM gain with hand analysis in a table.**
Is it smaller than "1"? Why?

POC	Simulation	Hand Analysis
CM Gain (A_{CM})	61 mV/V	$A_{CM} = \frac{g_m R_D}{1+2g_m r_{o3}} = 63$ mV/V

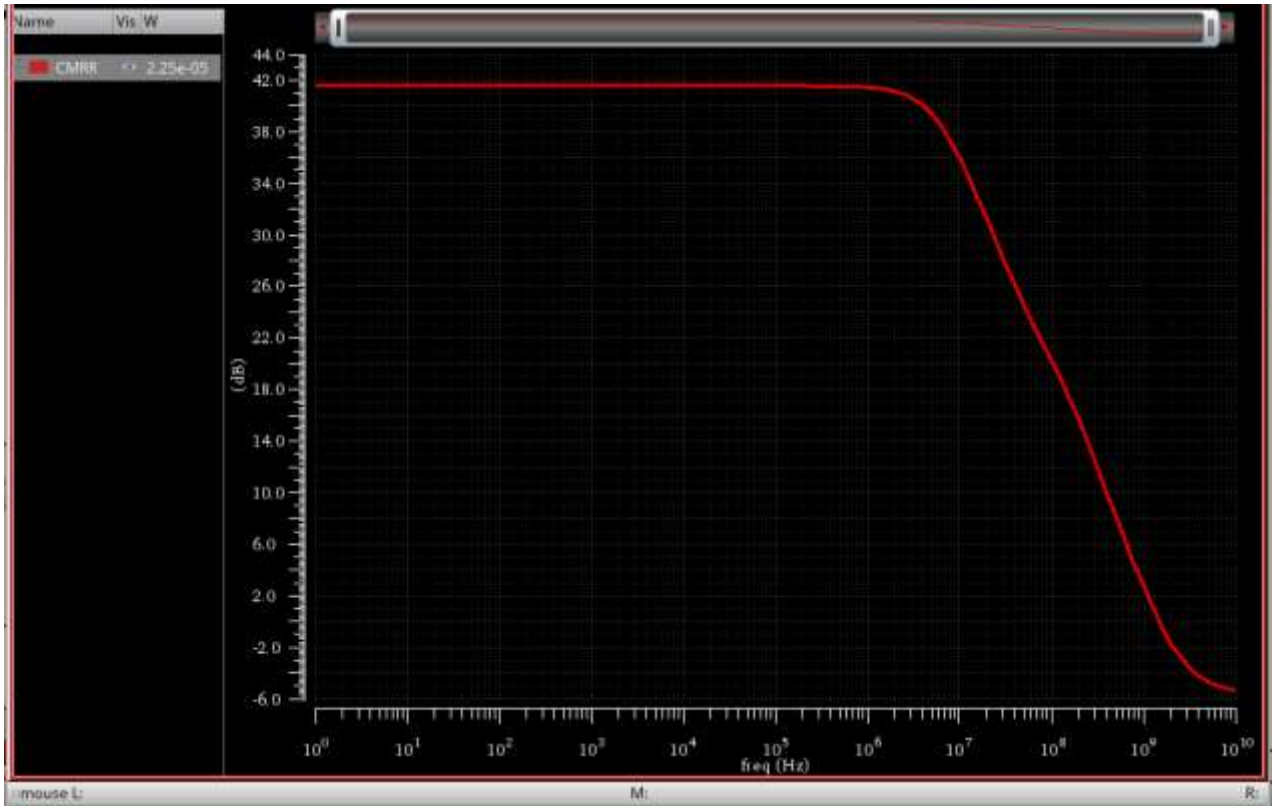
Yes, it is Smaller than 1 Because R_{SS} is R_{LFD} Which Has too large Value to make the Current Source Ideal.

Q5

- **Justify the variation of A_{vcm} vs frequency.**
  - **A_{vCM} is Decreasing with Frequency as the Capacitor act as Open Circuit at low Frequencies, and Short Circuit at High Frequencies (Shunt) to ground.**

Q6

Plot A_{vd}/A_{vcm} in dB. Compare A_{vd}/A_{vcm} @ DC with Hand Analysis in A Table.



P.O.C	Simulation	Hand Analysis
CMRR	41.92 dB	$\text{CMRR} = \left(\frac{A_{vd}}{A_{CM}}\right) = 1 + 2g_m R_{ss} = 42.38$ dB

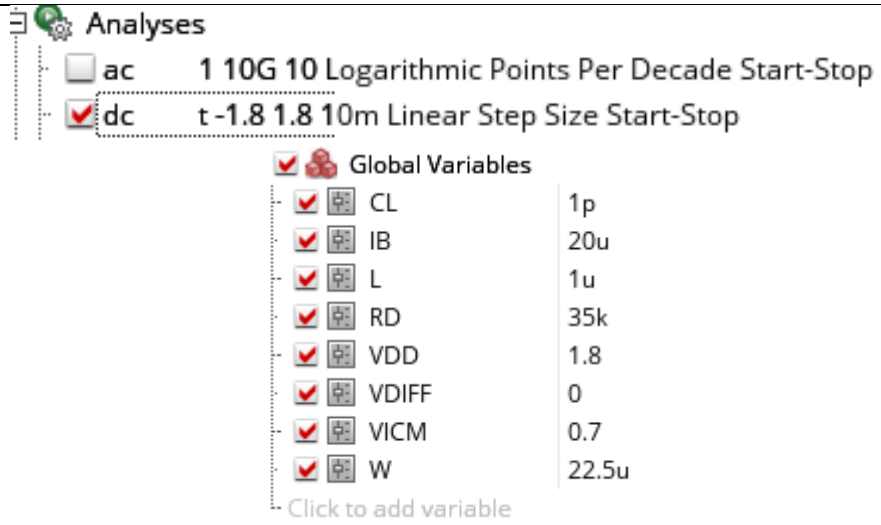
Q7

- **Justify the variation of A_{vd}/A_{vcm} with frequency.**

  - **It is Nearly Constant at Low Frequencies while when Frequency Increases it will Decrease then the Pole make it decrease by a Slope $= -20$ dB/Decade. Parasitic capacitors which are in parallel with R_{ss} begins to contribute with lower impedance, so R_{ss} is getting lower at high frequencies.**

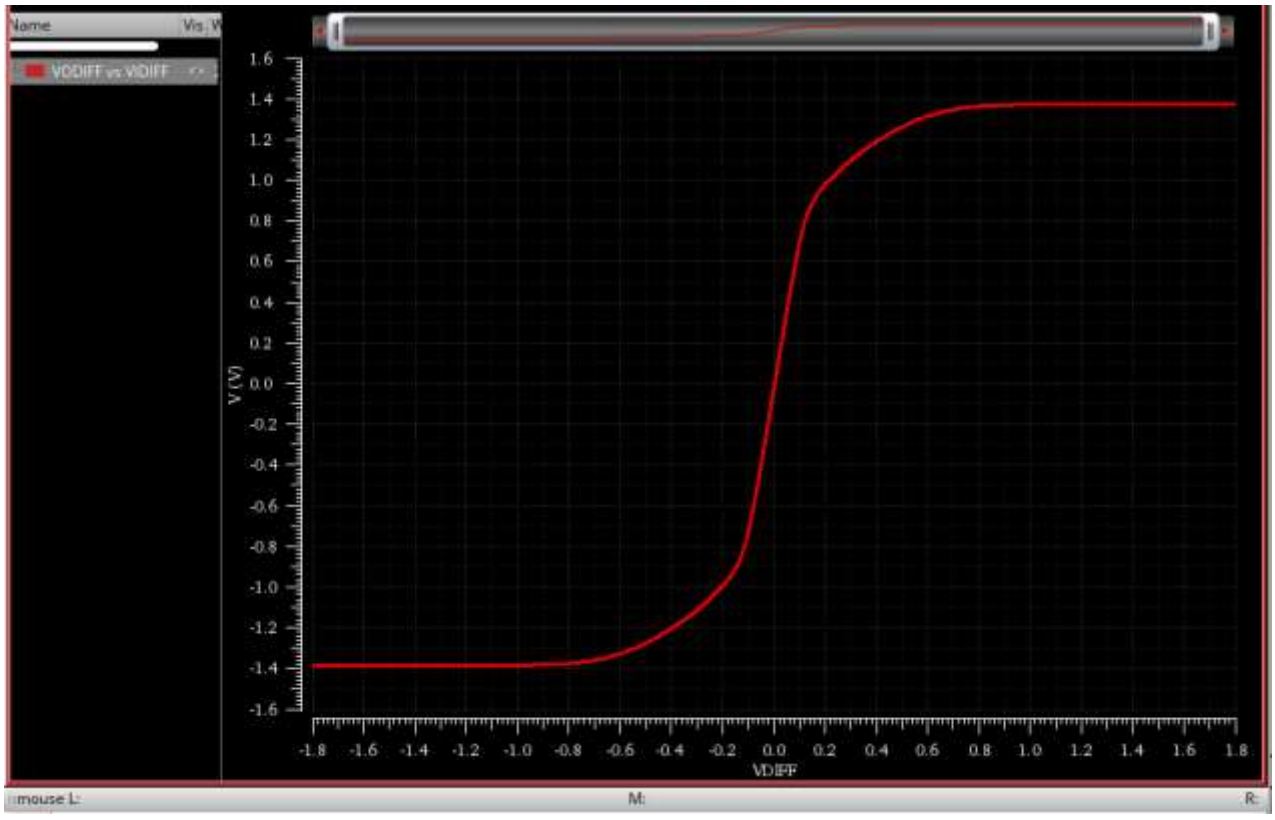
(4) Diff. Large Signal CCS.

Q1



Q2

Report diff large signal ccs (VODIFF vs VIDIFF).



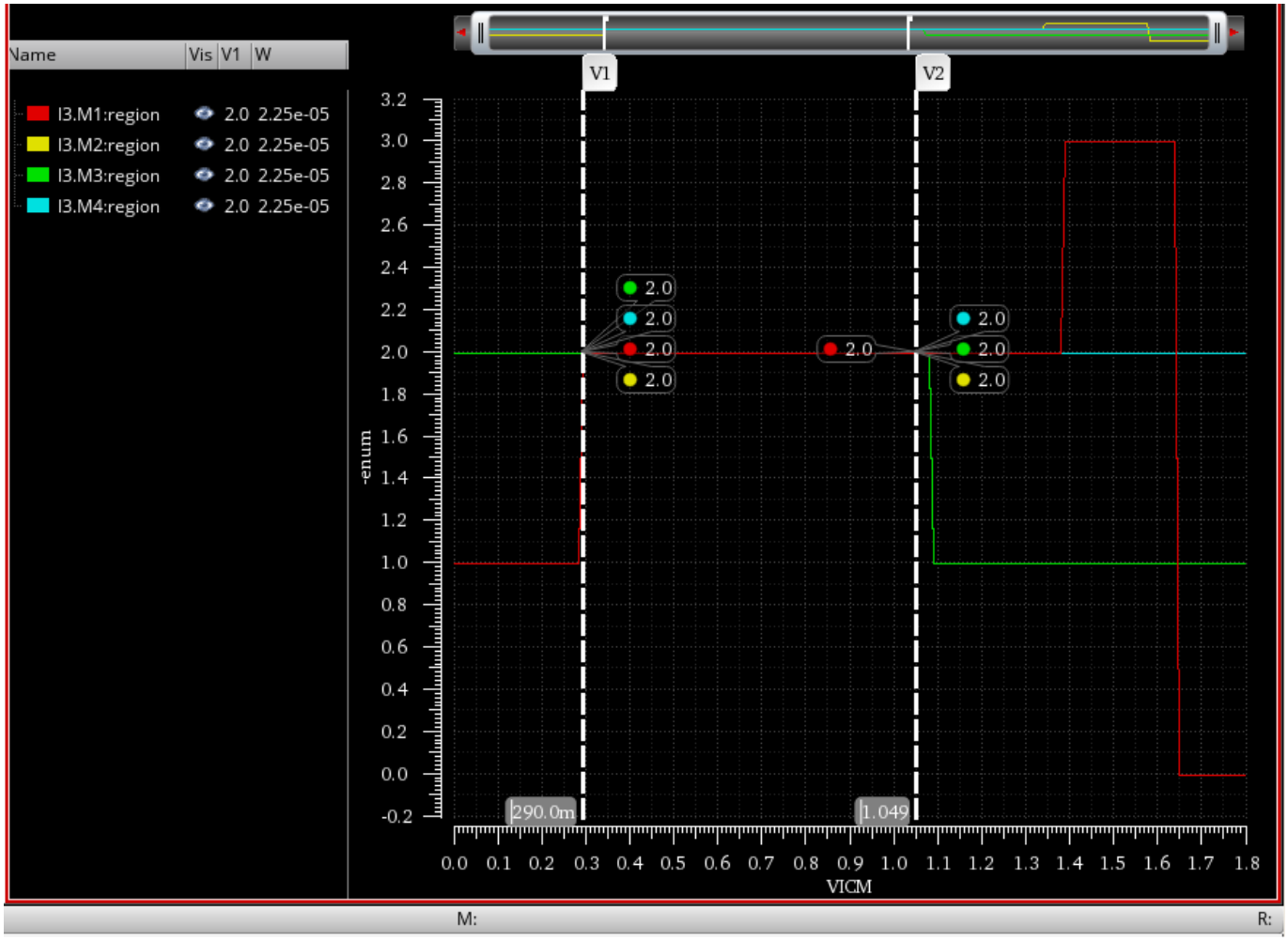
- **Compare the extreme values with hand analysis in a table.**
  - **Full Switching Occur (All Current Flows in M_1):**
    $I_d = I_{SS} = 40\ \mu A\ ,\ V_{out} = I_d R_d = 40\mu * 35k = 1.4\ V.$

P.O.C	Simulation	Hand Analysis
V_{out} Diff.	1.3792 V	1.4 V

(5) CM Large Signal CCS. (Region vs VICM)

Plot "region" OP parameter vs VICM for the input pair and the tail current source.

Region	Meaning
0	Cut – off
1	Triode
2	Saturation
3	Sub – Threshold
4	Breakdown

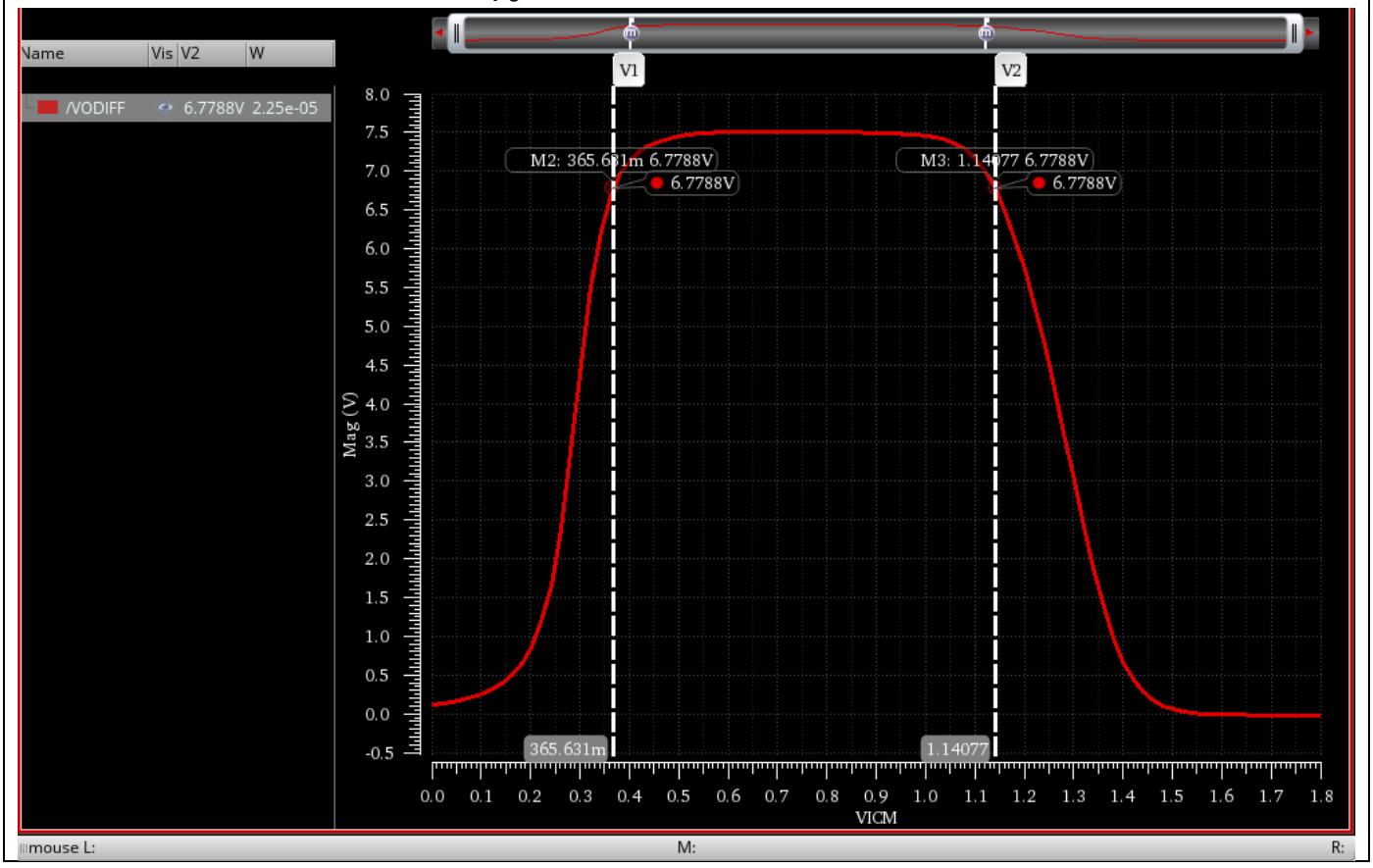


- **Find the CM input range (CMIR).**
  Compare with hand analysis.
  → To Make M_1 & M_2 In Saturation
  $$V_g = VICM > V_D - |V_{th}|, R_D = \frac{V_{out}CM}{I_D} = \frac{0.7\ V}{20\ \mu A} = 35\ k\Omega$$
  $$Since, V_D = 0.7\ V, V_{th} = 0.41\ V.$$
  $$VICM \geq -|V_{th}| + \frac{1}{2} I_{SS} R_D$$
  $$VICM_{Min} = V_D - V_{th} = 0.29\ V \quad (1).$$
  → To Make M_3 In Saturation
  $$V_{DD} = V_{ov_3} + V_{sg_1} + VICM_{Max}$$
  $$VICM_{Max} = V_{DD} - V_{ov_3} - (V_{ov_1} + |V_{th}|)$$
  $$Since, V_{ov_3} = V_{ov_1} = 170.5\ mV., V_{th} = 0.41\ V \quad (2).$$
  $$VICM_{Max} = V_{DD} - 2V_{ov} - |V_{th}| = 1.049\ V.$$
  - **As Shown in Figure above in the CMIR all Transistors is in Sat.**

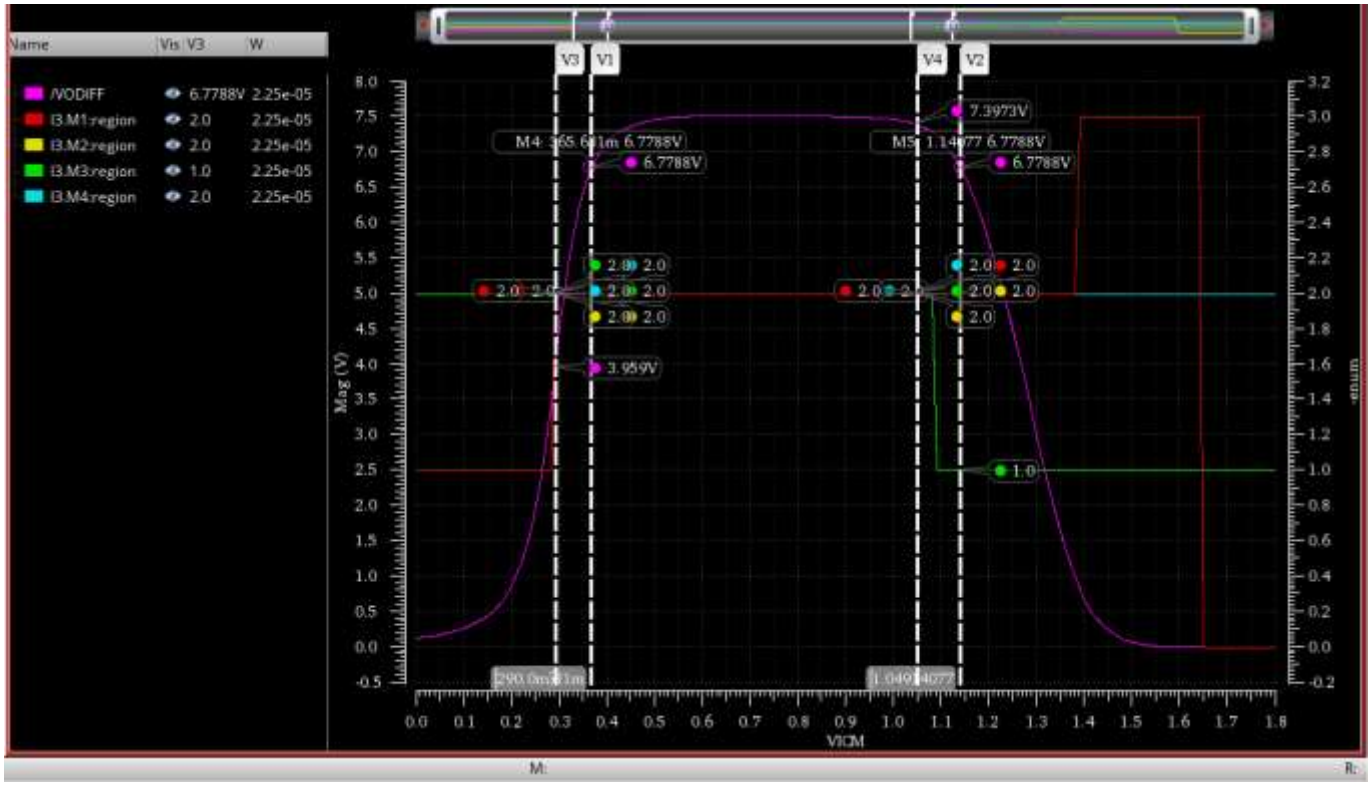
(6) CM Large Signal CCS. (GBW vs VICM)

IEEE_Workshop:lab_06_diff_amp_tb:1	Diff Gain Large	
IEEE_Workshop:lab_06_diff_amp_tb:1	max gain	7.532

Max. Gain = 7.532
90% Max. Gain = 6.7788



Plot the results overlaid on the results of the previous method (region parameter).



Find the CM input range. Compare with the previous method in a table.

From the Graphs Above.

VICM	Regions	90% A_{vd}
Minimum	0.29 V.	0.365 V.
Maximum	1.049 V.	1.14 V.