Faculty of Enigeering

Cairo University

Analog Electronics Project # 2

CMOS Operational Amplifier Design - Folded Cascode

Presented for **ELC 3060** Cadence Project

Presented to:

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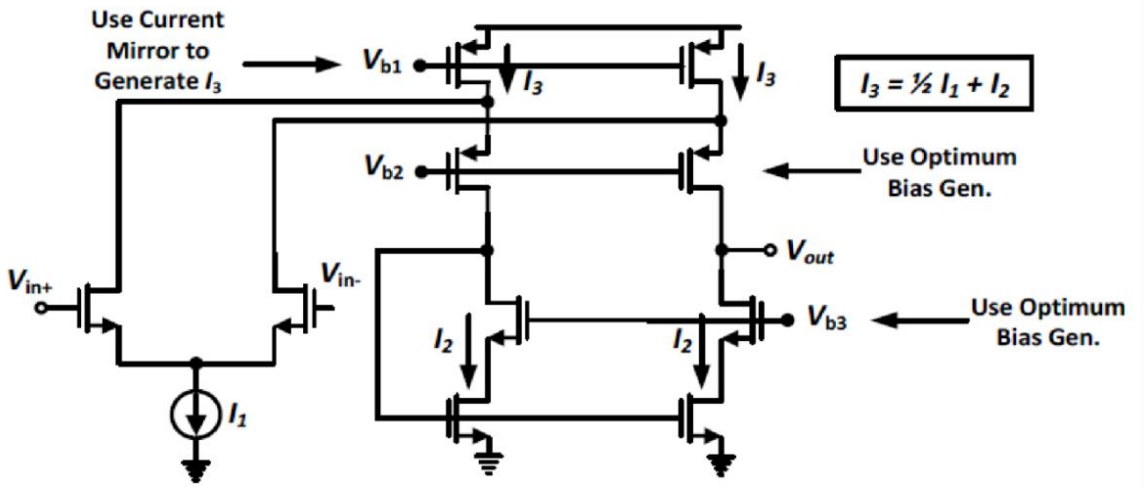
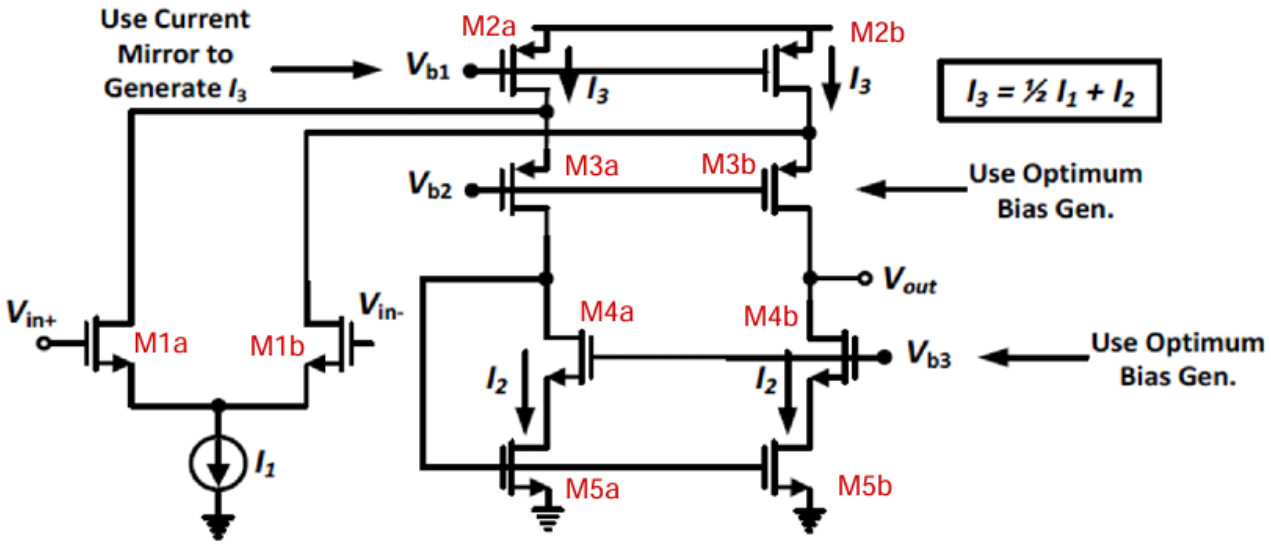


Folded Cascode

Design



CMOS Operational Amplifier Design

Folded Cascode OTA Required Specifications

DC Currents Assumptions (1:1 splitting ratio)	$I_1 = 200\ \mu A\ , I_2 = 100\ \mu A\ , I_3 = 200\ \mu A$
Supply (V_{DD})	$3.3\ V$
$V_{inCM} = \frac{V_{DD}}{2}$	$1.65\ V$
C_L	$2\ pF$
DC Diff. Gain (A_{DC})	$> 55\ dB$
GBW	$> 100\ MHz$
Slew Rate	$> 100\ V/\mu sec$
Output Swing	$> 1.5\ V_{PP}$
Input referred thermal noise (V_{i_n})	$< 10\ nV/\sqrt{Hz}$
Phase Margin (PM)	$> 60°$
Power Consumption	Minimize

Overview For g_m/I_D Design Methodology:

- Traditionally, square law was used in hand analysis to obtain initial design point.
- But short channel and moderate/weak inversion devices do not obey the square law.
- Square law is seldom used in nowadays designs.
- The popular approach nowadays is using g_m/I_D design methodology.
- Perform DC sweeps for both PMOS and NMOS to generate design charts vs g_m/I_D.
- g_m/I_D is a key MOSFET FoM (Figures - of - Merit)
- Use these charts (LUTs) to design your circuit to meet required specs.
- g_m/I_D captures the relation between the basic function of the transistor (the transconductance) and the most valuable resource (the power consumption).
- The range of g_m/I_D values doesn't differ much from one device to another and from one technology to another.
- g_m/I_Dcan be thought of as a normalized measure for the device inversion level.
- Plot Everything vs g_m/I_D !!

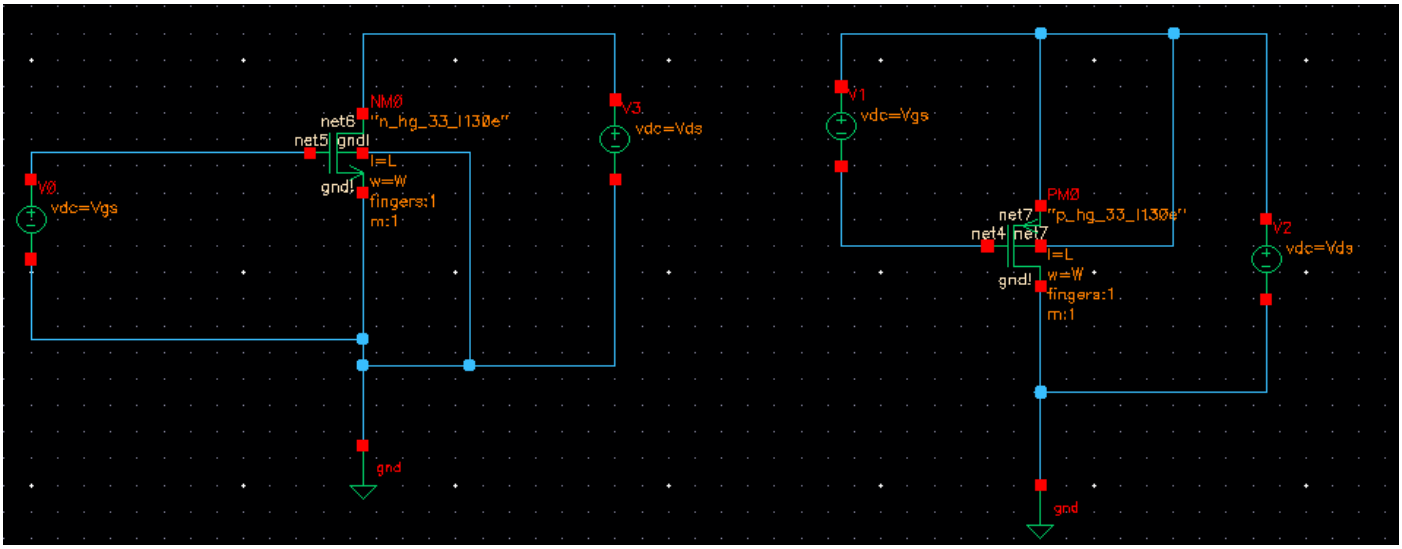


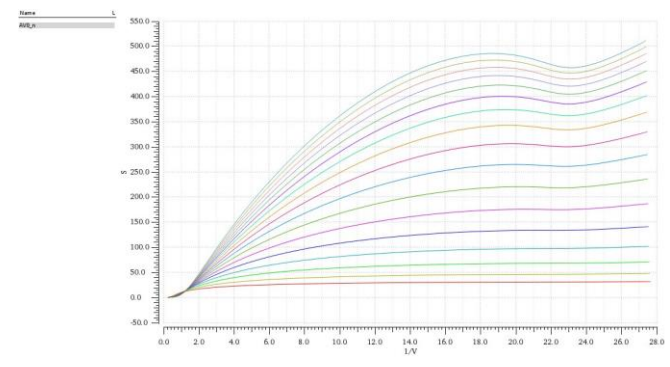
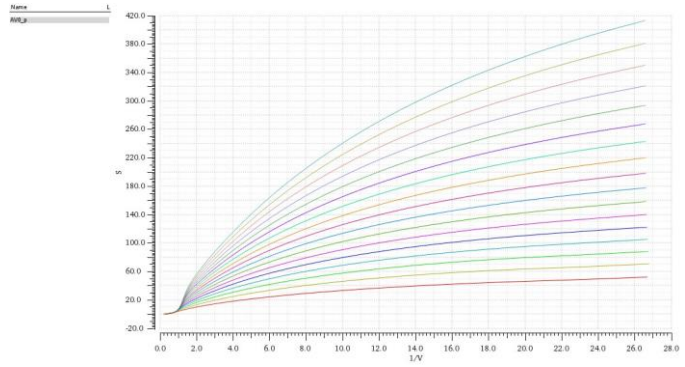
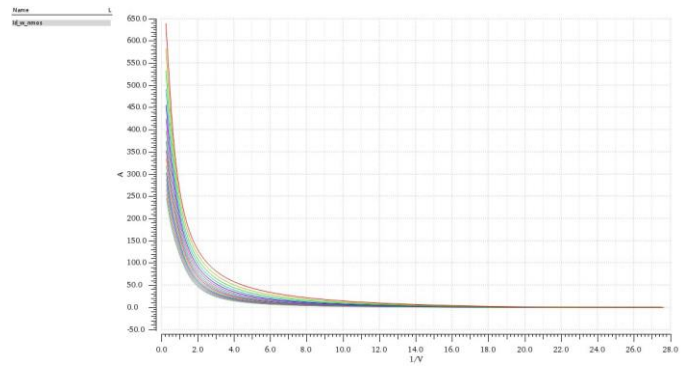
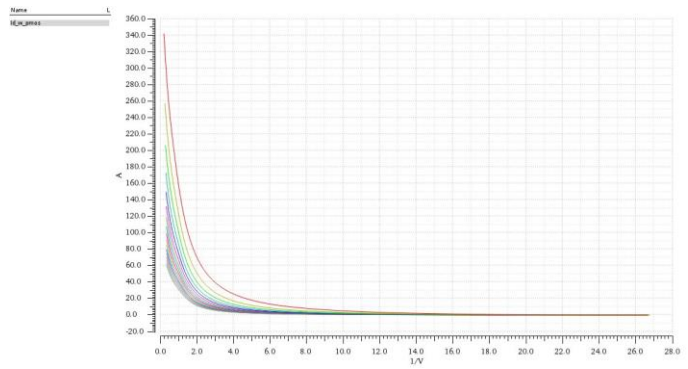
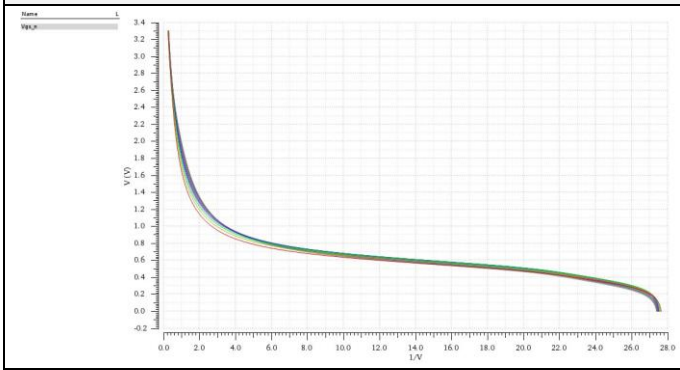
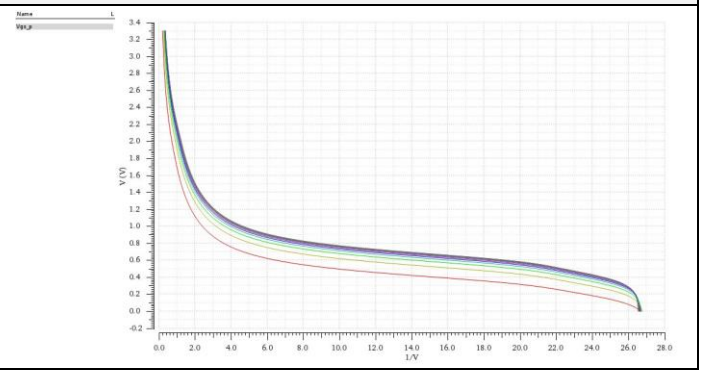
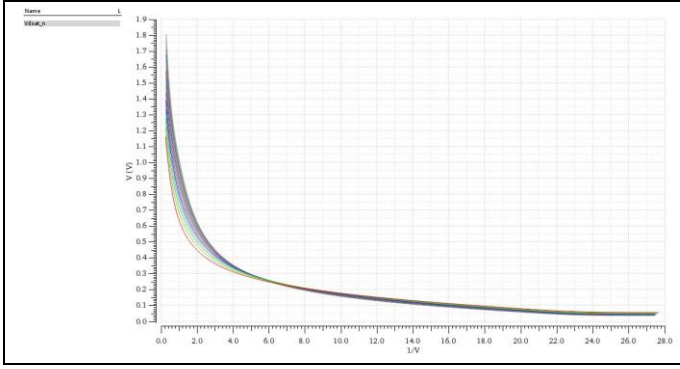
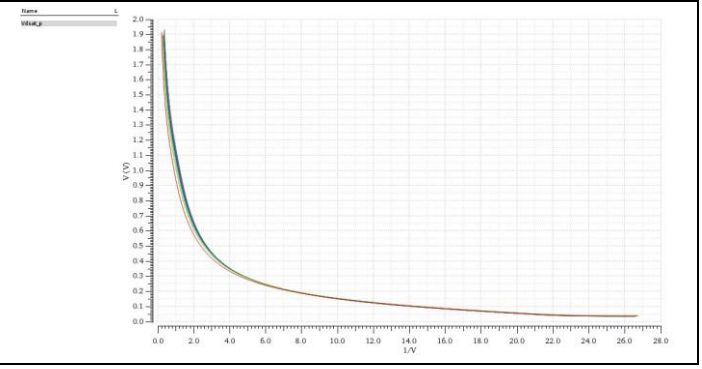
Figure 1: NMOS and PMOS Schematic Used for gm/ID Charts

The g_m/I_D Charts Shown Below is an Example for gm/id charts for the used technology **(UMC 130 nm)** with typical NMOS **(N_HG_33_L130E)** and PMOS **(P_HG_33_L130E)**.

Note:

The Design Has limiting body effect that shift the desired results, so we know that we go to do some tuning to enhance the required specs.

GM / I D Design Charts

NMOS	PMOS
Intrinsic Gain $\left(\frac{g_m}{g_{ds}} = g_m r_o\right)$	
	
Current Driving Capability $\left(\frac{I_D}{W}\right)$	
	
Gate - Source Voltage (V_{gs})	
	
Saturation Voltage (V_{dsat})	
	

Note:

As Shown in the Above Sizing Equations and Charts $\frac{g_m}{I_D}$ on x - axis and $\frac{I_D}{W}$ on y - axis and also have a Proportional Relation with the Width (W), So by Cross Multiplication we get the Values of W for Each Transistor as $W = \frac{I_D}{\frac{I_D}{W}}$

DESIGN EQUATIONS

1) **Gain spec:**

$$A_{v_d} = gm_1 R_{out}$$

$$R_{out} \approx (ro_4(1 + gm_4 ro_5))//(ro_3(1 + gm_3(ro_1//ro_2)))$$

$$R_{out} \sim A_{v_{0_4}} ro_5 // A_{v_{0_3}}(ro_1//ro_2)$$

2) **Slew Rate:**

$SR = \frac{min(I_1, I_2)}{C_L}$ → **Assume equal current splitting.**

$$Hence, \quad SR = \frac{I_1}{C_L}$$

3) **GBW:**

$GBW = \frac{G_m}{C_{out}} \approx \frac{gm_1}{C_L}$ **(Neglecting the parasitic caps for now)**

4) **Noise:**

$$\overline{V^2_{n,in_{thermal}}} = 8KT \frac{\gamma}{g_{m1(a,b)}} \left(1 + \frac{g_{m2(a,b)}}{g_{m1(a,b)}} + \frac{g_{m5(a,b)}}{g_{m1(a,b)}}\right)$$

5) **PM:**

→ ω_{nd} **is either due to the folding node or the high-swing current mirror node.**

→ **Hence,**

$$\omega_{nd} \approx \frac{gm_3}{C_{gs_3} + C_{db_1} + C_{db_2}} \; or \; \approx \frac{g_{m_5}}{C_{gs_4} + C_{db_3} + C_{gs_5}}$$

6) **Output Swing:**

We can't envision the possible gain compression, but we can initiate the design by assuming $V_{o_{CM}} = 0.8$ then tune using the Bias voltages (V_{B_2}, V_{B_3})

DESIGN PROCEDURE

Sizing:

Let $V_o|_{CM} = 0.8\,V \;\therefore V_{ds2} + V_{ds3} = 2.5\,V$

Let $V_{ds2}: V_{ds3} = 3:2$

$V_{ds2} > V_{ds3} \rightarrow$ to have large r_o without using $Large\ L \rightarrow Large\ W \rightarrow Large\ Area.$

$\therefore V_{ds2} = 1.5\,V \quad , \quad V_{ds3} = 1\,V$

$\therefore V_{ds1} + V_{ds}|_{CM} = 2.3$

$Let\ V_{ds1} = 1.265\,V \quad , \quad V_{ds}|_{CM} = 1.035\,V$

For $M_1\ (a, b)$:

$g_{m1} > 1.2566\,ms \rightarrow \therefore Let\ g_{m1} = 1.266\,ms \quad \rightarrow (1)$

$I_1 > 200\ \mu A \rightarrow \therefore Let\ I_1 = 200\ \mu A \quad \rightarrow (2)$

From (1) & (2):

$$\left.\frac{g_m}{I_d}\right|_1 = 12.566\,V^{-1}$$

$V_{gs} = V_{in}|_{CM} - V_{ds2} = 615\,mV$

$g_{m1} = 1.2594\,ms \quad , \quad r_{o1} = 260\,k\Omega\ , \quad V_{dsat} = 130.74\,mV$

$Choose\ \mathbf{L_1 = 650\,nm} \quad , \quad \mathbf{W_1 = 42.611\ \mu m} \quad , \quad V_{gs} = 616.88\,mV$

Current Mirror:

$V_{ds} = 1.035\,V, \quad Let\ L = 1\ \mu m$

$$\frac{g_m}{I_d} = 10\,V^{-1}$$

$V_{gs} = 643.4\,mV \quad , \quad V_{dsat} = 159.07\,mV$

$\mathbf{W = 81.0172} \rightarrow M = 7.881$

REF:

$V_{gs} = V_{ds} = 643.4\,mV \rightarrow \frac{g_m}{I_d} = 10.0023\,V^{-1}$

$\mathbf{W = 10.28\ \mu m}$

From noise spec:

$\bar{V}^2{}_{n,m} = \frac{8KT\gamma}{g_m}\left[1 + \frac{g_{m2}+g_{m5}}{g_m}\right] < 10^{-1.6}\ V^2/Hz$

$Let\ \gamma = 1 \quad \rightarrow [worst\ case\ scenario] \quad , \quad T = 27^oC$

$g_{m2} + g_{m5} < 3.52726\ ms \quad , \quad Let\ V_{ds4} = V_{ds5} = 0.4\ mV$

For $M_5\ (a, b)$:

$V_{gs5} = V_o|_{CM} = 0.8\ mV \rightarrow \therefore \boldsymbol{\frac{g_m}{I_d} = 6\ V^{-1}}$

$V_{dsat5} = 258.94\ mV \quad , \quad \boldsymbol{L_5 = 500\ nm}, \quad \boldsymbol{W_5 = 7.42\ \mu m}$

$r_{o5} = 27.457 * \frac{10}{7.42 * 10^{-6}} \rightarrow r_{o5} = 36.984\ k\Omega$

$V_{dsat5} = 255.32\ mV \quad , \quad g_{m5} = 0.6\ ms$

$Let\ \boldsymbol{\frac{g_m}{I_d}\Big|_2 = 8\ V^{-1}} \rightarrow g_{m2} = 1.6\ ms$

$\therefore g_m + g_{m2} = 2.2 < 3.5\ ms$

For $M_2\ (a, b)$:

$\boldsymbol{\frac{g_m}{I_d}\Big|_2 = 8\ V^{-1}} \quad , \quad V_{ds2} = 1.5\ mV$

$A_v \approx g_{m_1}([g_{m4} * r_{o4} * r_{o5}\ //\ \ g_{m4} * r_{o3}(r_{o1}\ //\ r_{o2})])$

$\therefore R_{out} \approx 446.515\ k\Omega$

$Let\ \boldsymbol{L_2 = 300\ nm}$

$\therefore \boldsymbol{W_2 = 52.16\ \mu m}$

$\therefore r_{o2} = 350662\ k\Omega \quad , \quad g_{m2} = 1.6\ ms$

$V_{gs2} = 730.43\ mV \quad , \quad V_{dsat} = 191.28\ mV$

For $M_3\ (a, b)$:

We need to decrease the width of M_4 to decrease the capacitance @ the folding node but we need to boost A_v by A_{v3}

$V_{ds3} = 1\ V \rightarrow$ Let $A_{v3} = 40$, $\frac{g_m}{I_d} = 8.26691 \rightarrow L = 250\ nm$

$W = 21.597\ \mu m$, $V_{dsat3} = 185.58\ mV \quad , \quad V_{gs3} = 665.97\ mV$

$V_{B2} = V_{DD} - V_{gs3} - V_{sd2} = 1.13703$

For $M_4\ (a, b)$:

$V_{ds} = 0.4\ V$, Let $A_v|_{req} = 50 \rightarrow \frac{g_m}{I_d}|_4 = 10.0517$, $L = 500\ nm$

$W = 19.24723\ \mu m$

$V_{gs4} = 678\ mV$, $V_{dsat4} = 168.27\ mV$

$V_{B2}|_{max} = V_{DD} - V_{gs3} - V_{dsat2} = 2.44275\ V$

$V_{B2}|_{min} = 0.26\ V$

CL	2p
Ibias	25u
L1	550n
L2	350n
L3	250n
L4	500n
L5	500n
Lcm	1u
M_mirr	8
VB1	2.5275
VB2	1.1
VB3	1.2
Vdd	3.3
VinCM_ac	0
VinCM_dc	Vdd/2
VinDIFF_ac	1
VinDIFF_dc	0
W1	60u
W2	57.6u
W3	21.6u
W4	19.2u
W5	7.42u
Wcm	10.28u

Biasing: (V_{B1}, V_{B2}, V_{B3})

$V_{B1} = V_{DD} - V_{gs2} = 2.56957\ V$

$V_{B1}|_{min} = V_d - |V_{th2}| = V_{dsat3} + V_{gs5} - (V_{gs2} - V_{dsat2}) \cong 0.4$

$V_{B2} = V_{DD} - V_{gs3} - V_{sd2} = 1.322\ V$

$V_{B2}|_{max} = V_{DD} - V_{sg3} - V_{dsat2} = 2.63\ V$

$V_{B2}|_{min} = V_{gs5} - |V_{th2}| = V_{gs5} - (V_{gs2} - V_{dsat2}) = 0.26\ V$

$V_{B3} = V_{gs4} + V_{ds5} = 1.1043\ V$

$V_{B3}|_{max} = V_{DD} + V_{gs3} - V_{dsat2} - V_{dsat3} - V_{dsat4} = 3.258\ V$

$V_{B3}|_{min} = V_{gs4} + V_{dsat5} = 0.95963\ V$

$V_{B3} = V_{gs4} + V_{ds5} = 687\ mV + 0.4 = 1.087\ V$

$V_{B3}|_{max} = 3.42084\ V$

$V_{B3}|_{min} = 0.93332\ V$

Note: V_{b1} , V_{b2} & V_{b3} are sweeped to Sustain the Saturation of the Transistors and the Current Split Ratio Required

SIZING SUMMARY

Transistors	Length (L)	Width (W)
$M_1(a, b)$	$650\ nm$	$42.611\ \mu m$
$M_2(a, b)$	$300\ nm$	$52.16\ \mu m$
$M_3(a, b)$	$200\ nm$	$25.113\ \mu m$
$M_4(a, b)$	$350\ nm$	$10.60225\ \mu m$
$M_5(a, b)$	$500\ nm$	$7.42\ \mu m$

Simulations

Biasing Circuit Design Procedure

After using ideal sources to bias the folded - cascode circuit, it's time to design a biasing circuit that will provide the optimum biasing voltage. The circuit concept as shown in figure (2) is very simple, for Vb1 the ideal current source will be mirrored to 200 micro-Amp. (same current in M1) then add a diode connected PMOS. With the current of the PMOS device set by the mirroring devices we can configure its sizing to obtain the required biasing voltage by assuming an appropriate length (0.5um - 1um) and sweeping over the width as shown in figure (3).

Same procedure for Vb2 but mirror a current of 100uAmperes. For Vb3 we have to mirror the ideal current source running in a NMOS to another NMOS so we will add a PMOS stage then follow the same procedure in previous devices as shown in figure (4). The final biasing circuit schematic is shown in figure (5).

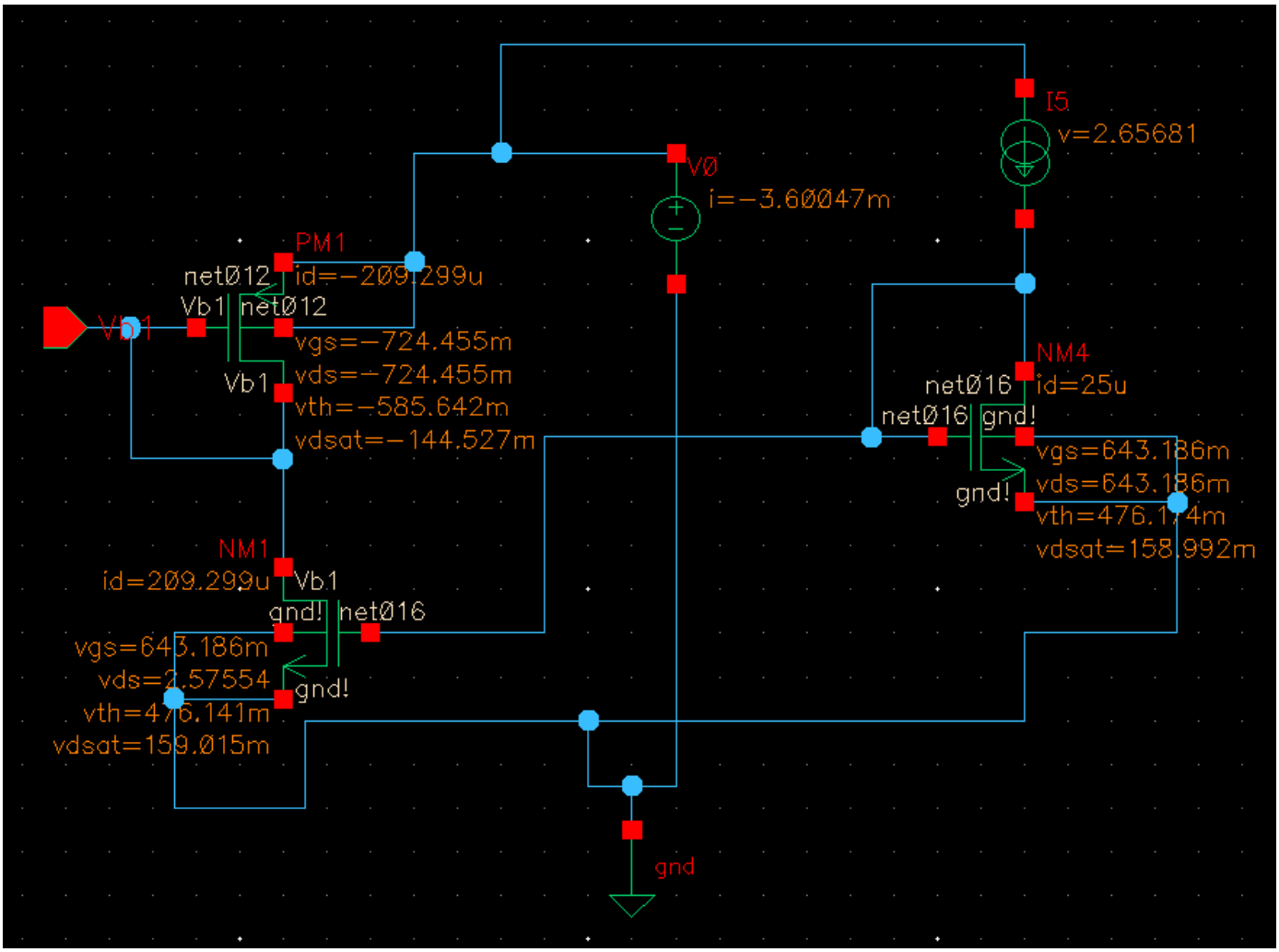


Figure 2: Biasing Circuit for Vb1 and Vb2

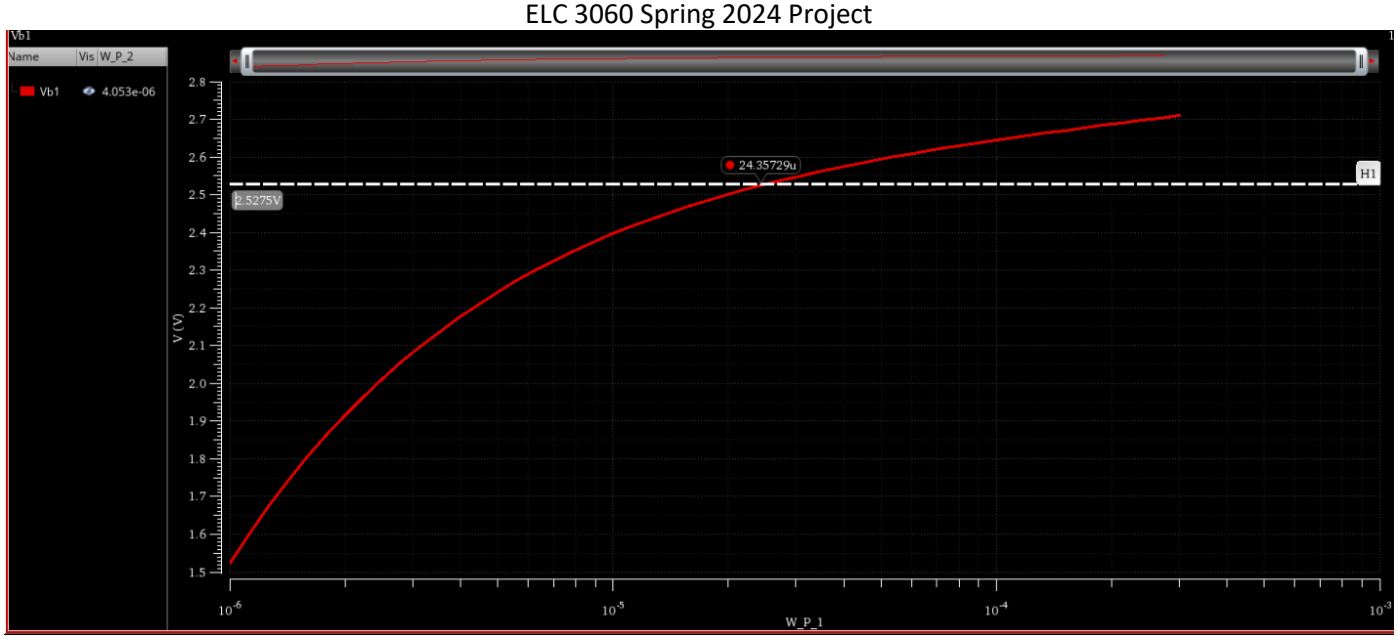


Figure 3: Sweeping over Width to Obtain the Optimum Biasing Voltage

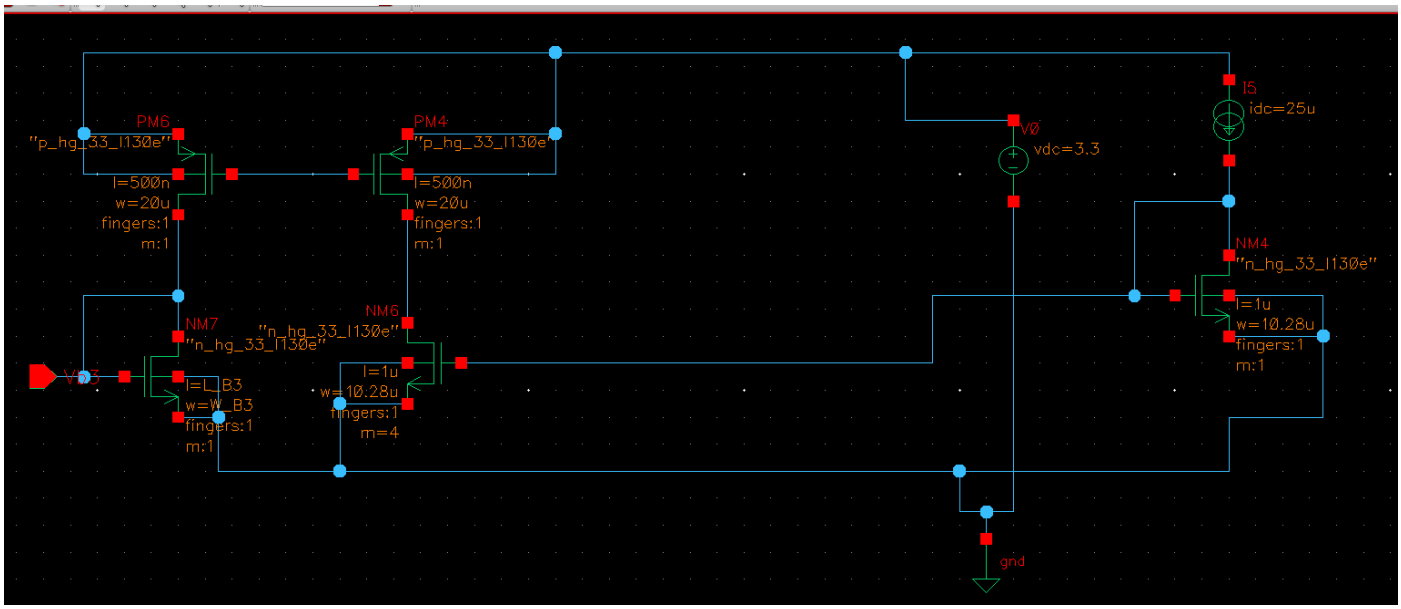


Figure 4: Biasing Circuit to Obtain Optimum Value of Vb3

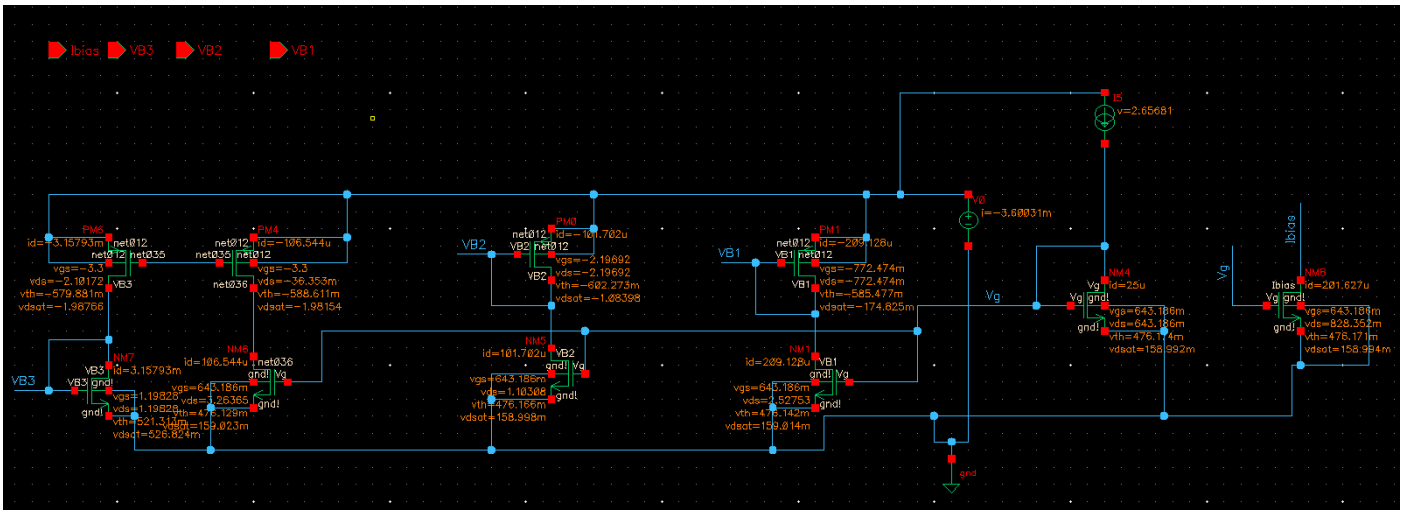


Figure 5: Biasing Circuit Schematic

Biasing Voltage Node	Optimum Value	Obtained Value	Configured Device Width	Configure Device Length
V_{b1}	$2.5275\ V$	$2.52751\ V$	$24.35729 \times 6 = 146.14374\ \mu m$	$0.5\ \mu m$
V_{b2}	$1.1\ V$	$1.10376\ V$	$4.0536\ \mu m$	$1.2\ \mu m$
V_{b3}	$1.2\ V$	$1.19832\ V$	$47.2551\ \mu m$	$0.5\ \mu m$

Open Loop Simulations

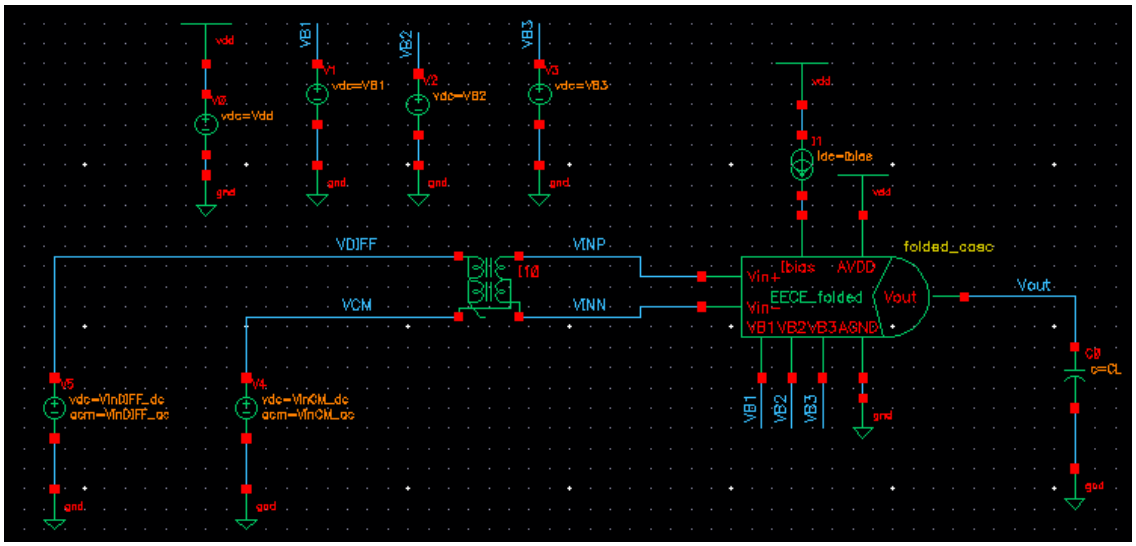


Figure 6: Schematic Before Biasing

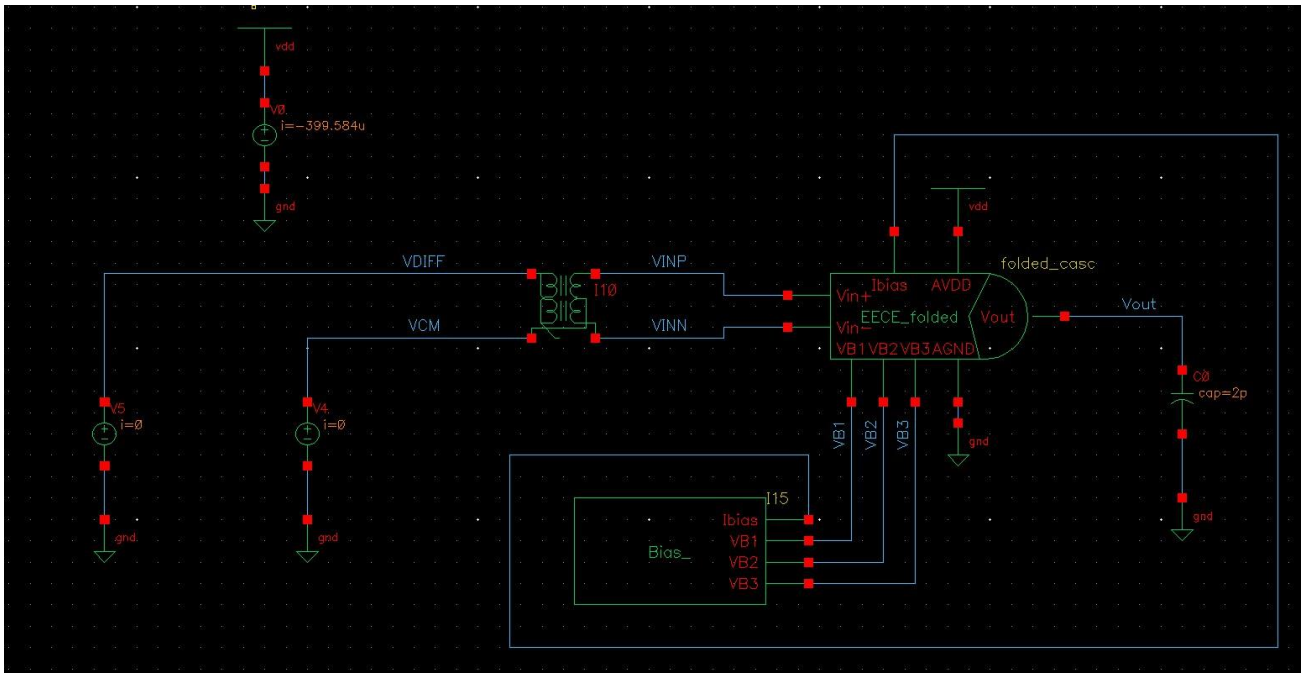


Figure 7: Schematic After Biasing

DC Analysis (DCOP)

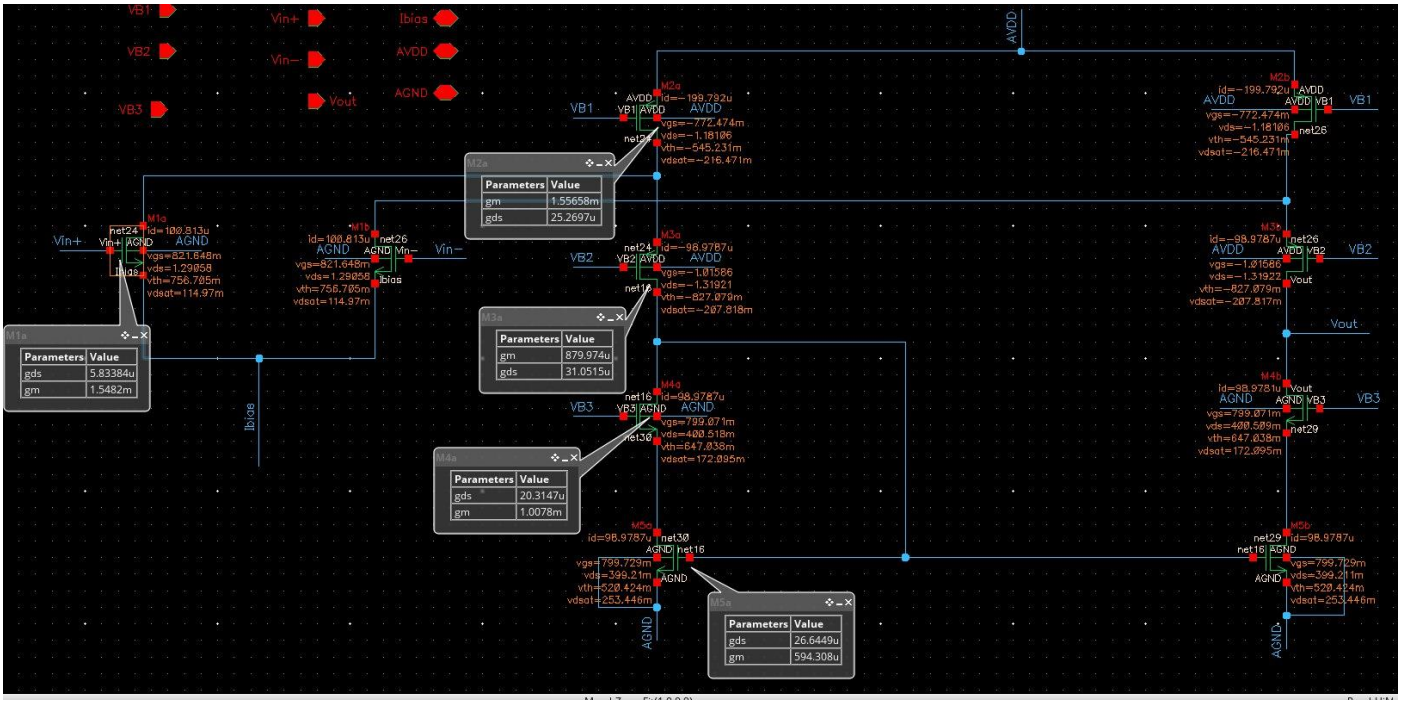


Figure 8: DC OP Showing All Transistors at Saturation region and all Current as Expected

AC Analysis

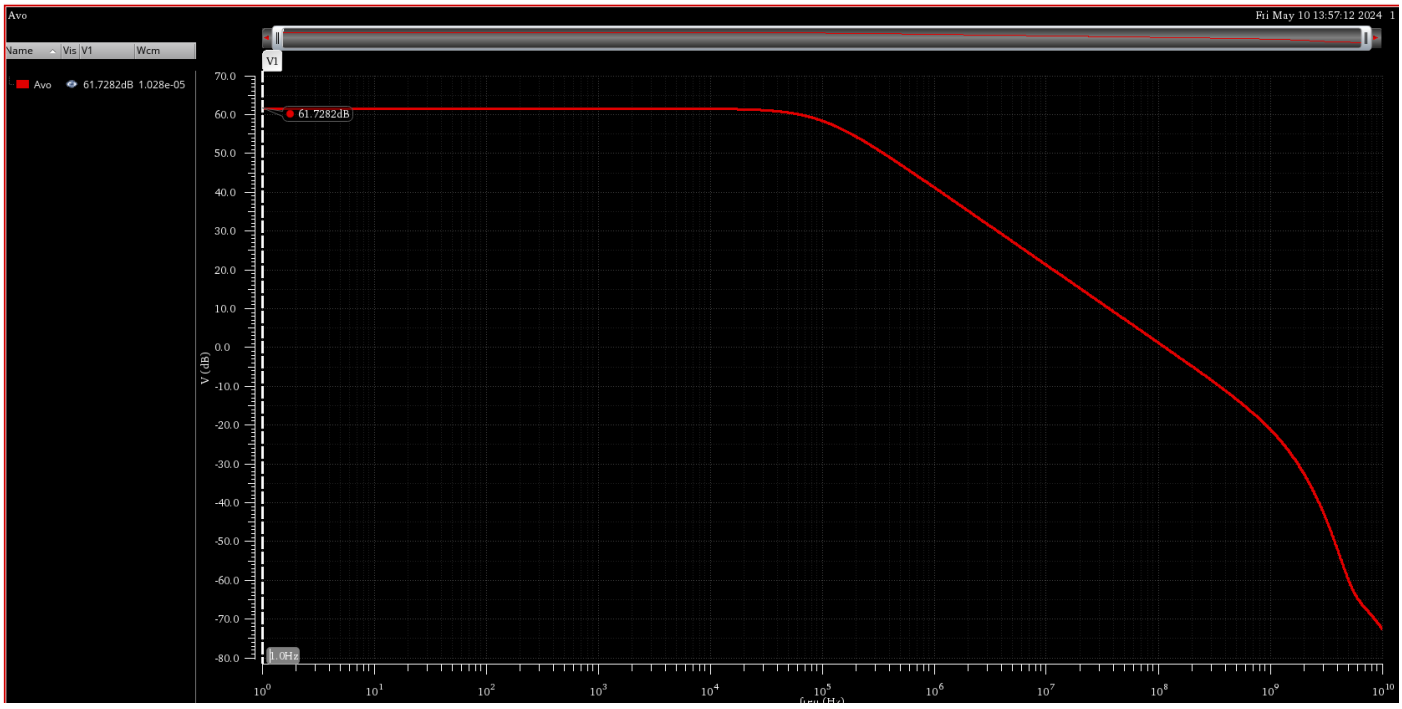


Figure 9: Gain vs Frequency Showing the DC Gain

DC Gain = 61.7282 dB

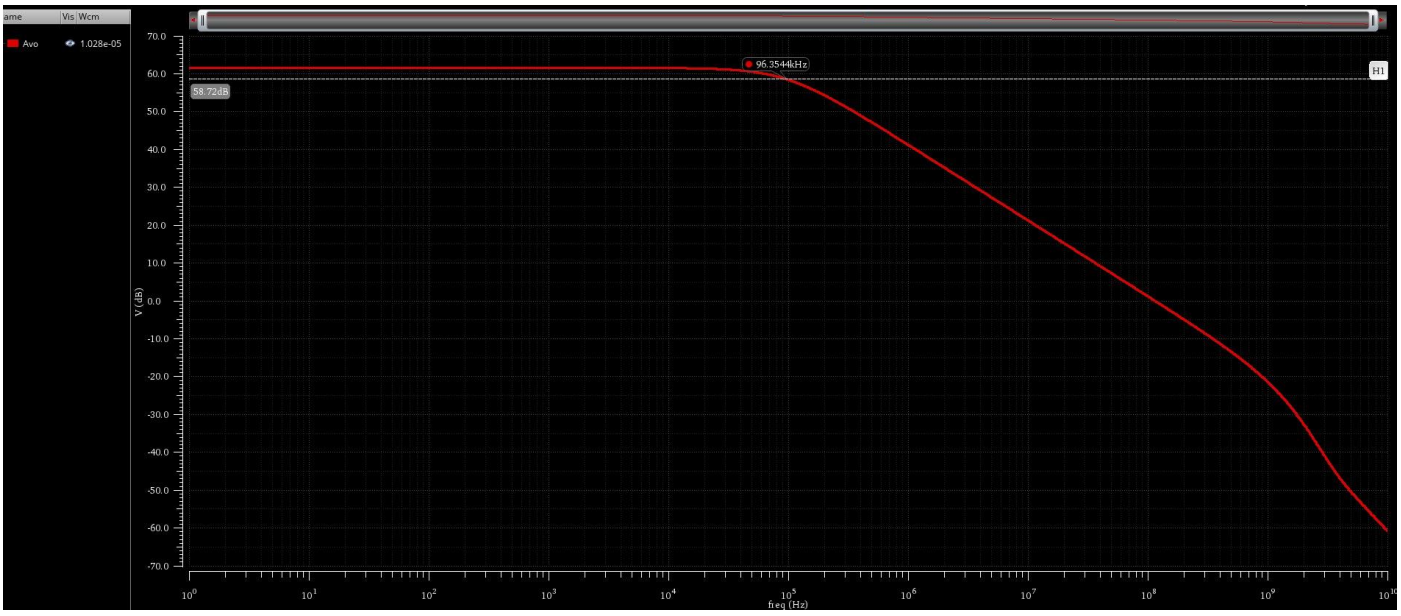


Figure 10: Gain vs Frequency Showing -3dB BW.

$$\mathbf{BW = 96.3544\ kHz}$$

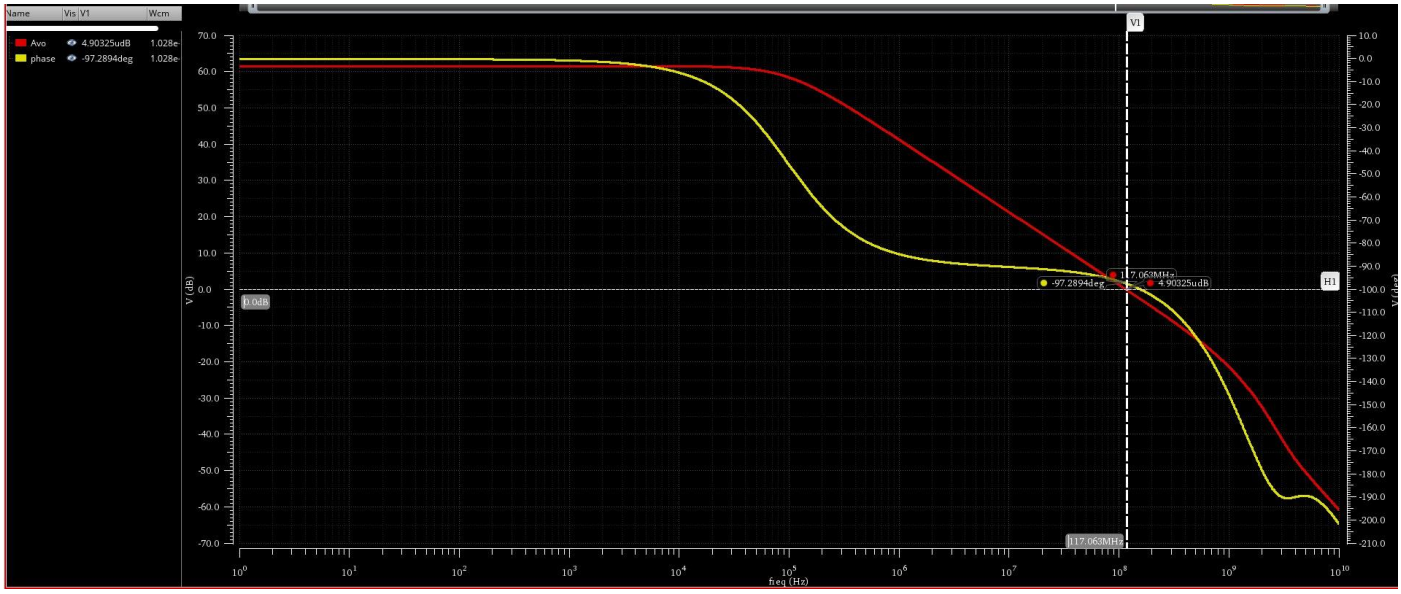


Figure 11: Phase vs Frequency Showing PM and GBW

$$\mathbf{PM = 180 - 97.2894 = 82.7106^{\circ}\ ,\ GBW = 117.063\ MHz}$$

Hand Analysis:

From the graph: $A_{OL} = 61.7282\ dB$

By Hand analysis:

$A_{OL}(DC-Gain) = g_{m1(a,b)} * (((g_{m4(a,b)}r_{o4(a,b)}+1)r_{o5(a,b)} + r_{o4(a,b)})//(((g_{m3(a,b)}r_{o3(a,b)}+1)(r_{o2(a,b)}//r_{o1(a,b)}) + (r_{o3(a,b)}))$

$A_{OL}(DC-Gain) = 1.5482\ m(\ 1847K\ //\ 925K) \approx 63.1193\ dB = 1432.072$

Phase-Margin: $PM = 82.7106^{o}$

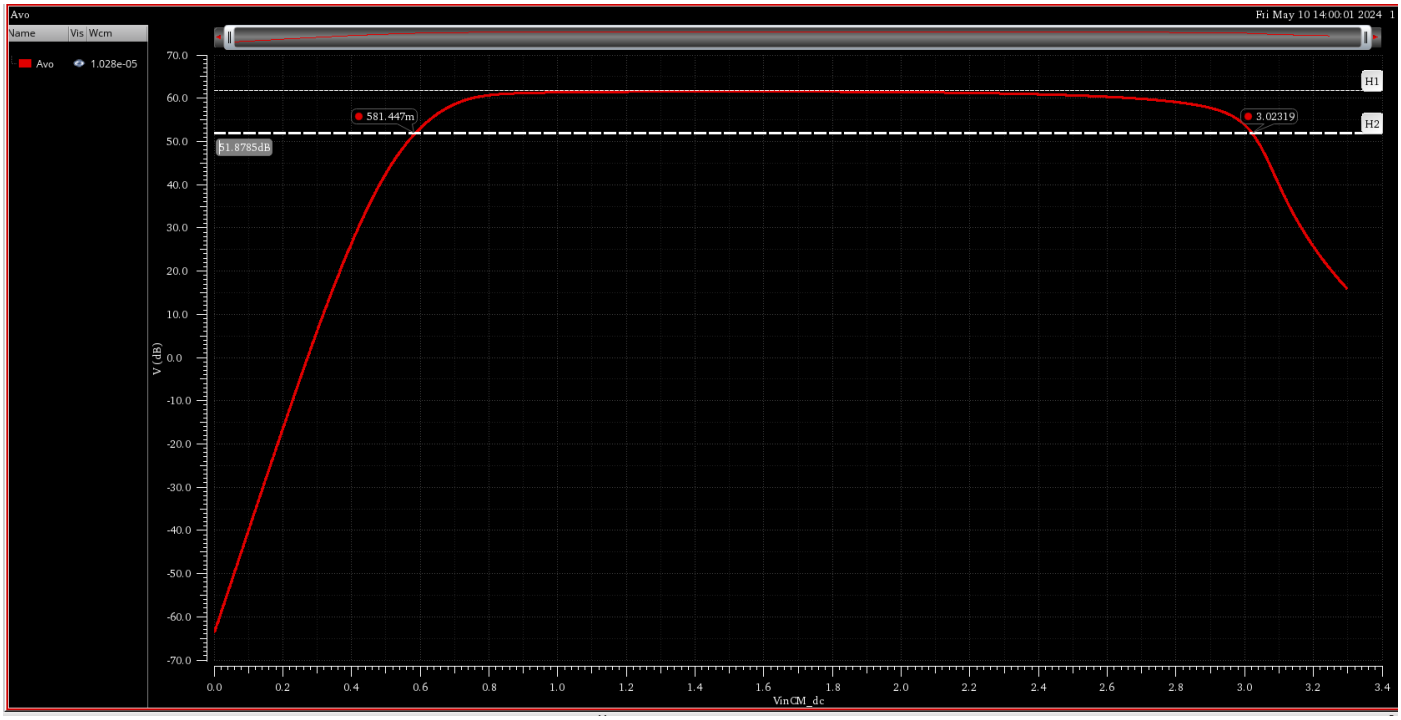


Figure 12: Gain vs $VinCM\_dc$ Showing Output Swing

Output Swing $= 3.02319 - 581.447\ m = 2.441743\ V_{pp}$

XF Analysis

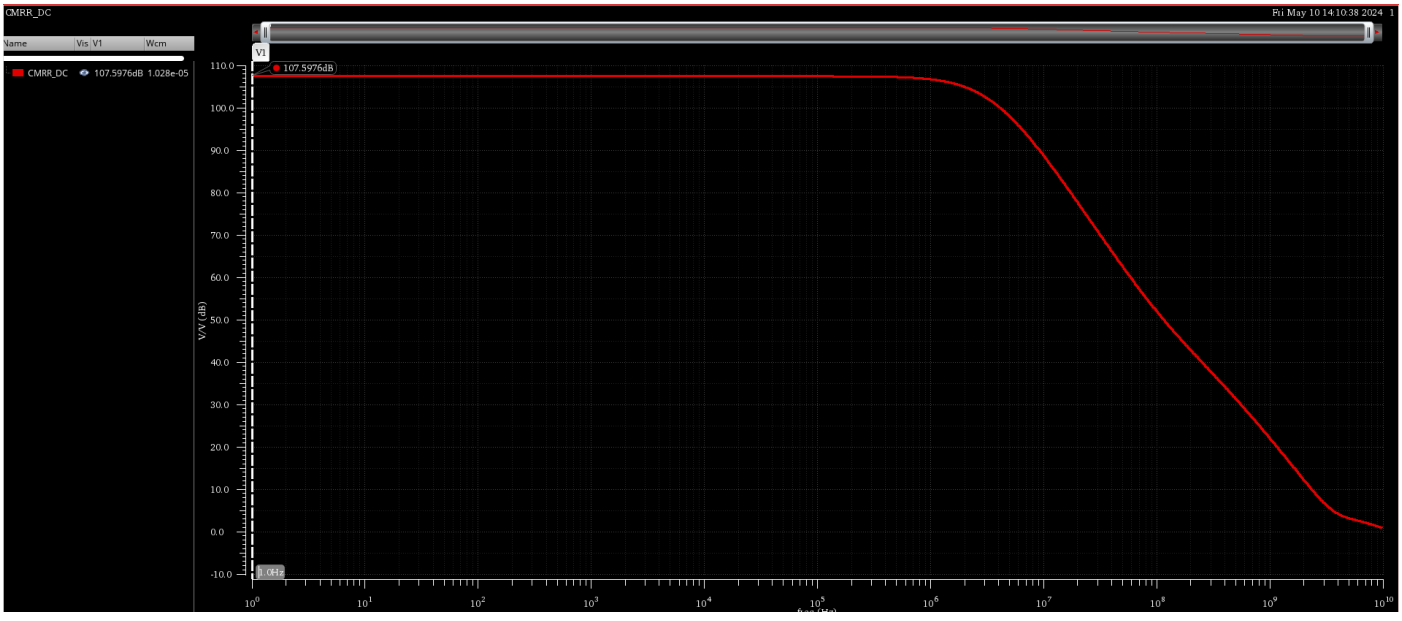


Figure 13: CMRR vs Frequency.

Common Mode Rejection Ratio (CMRR) $= 107.5976\ dB$

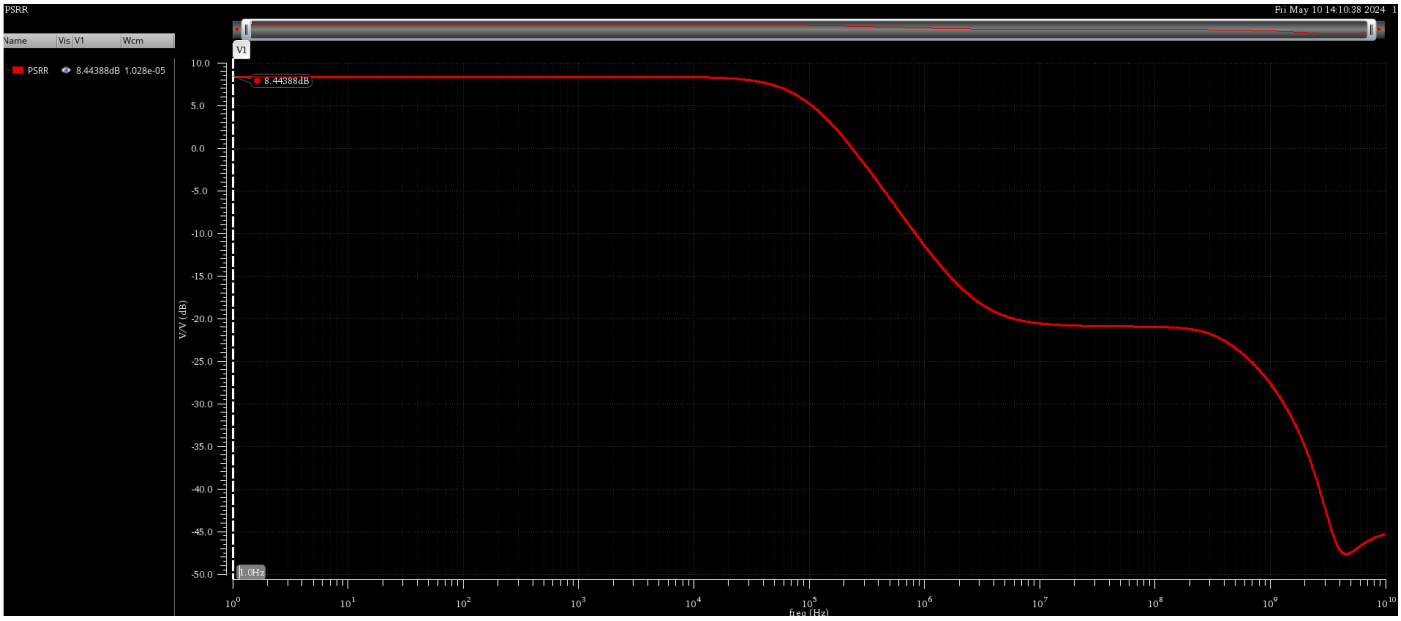


Figure 14: PSRR vs Frequency.

Power Supply Rejection Ratio (PSRR) = $8.44388\ dB$

Closed Loop Simulations

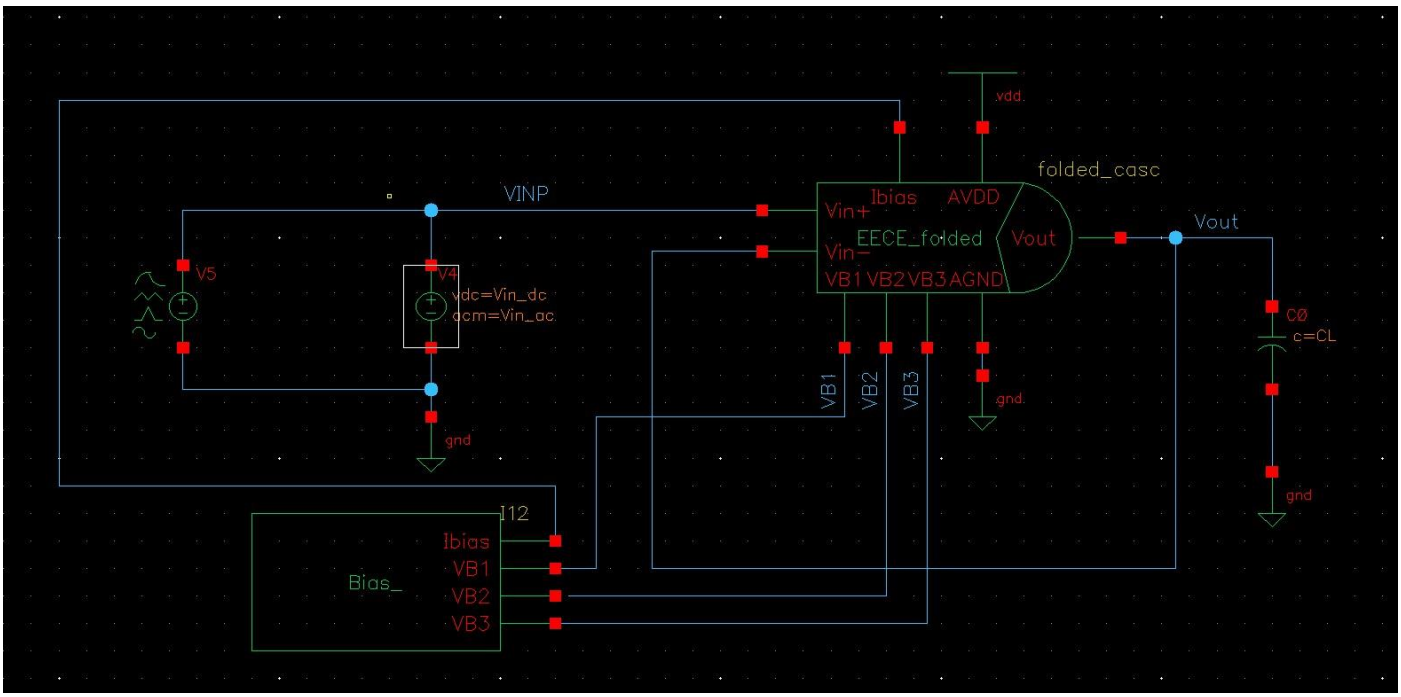


Figure 15: Closed Loop Schematic After Biasing

STB Analysis and IPROBE

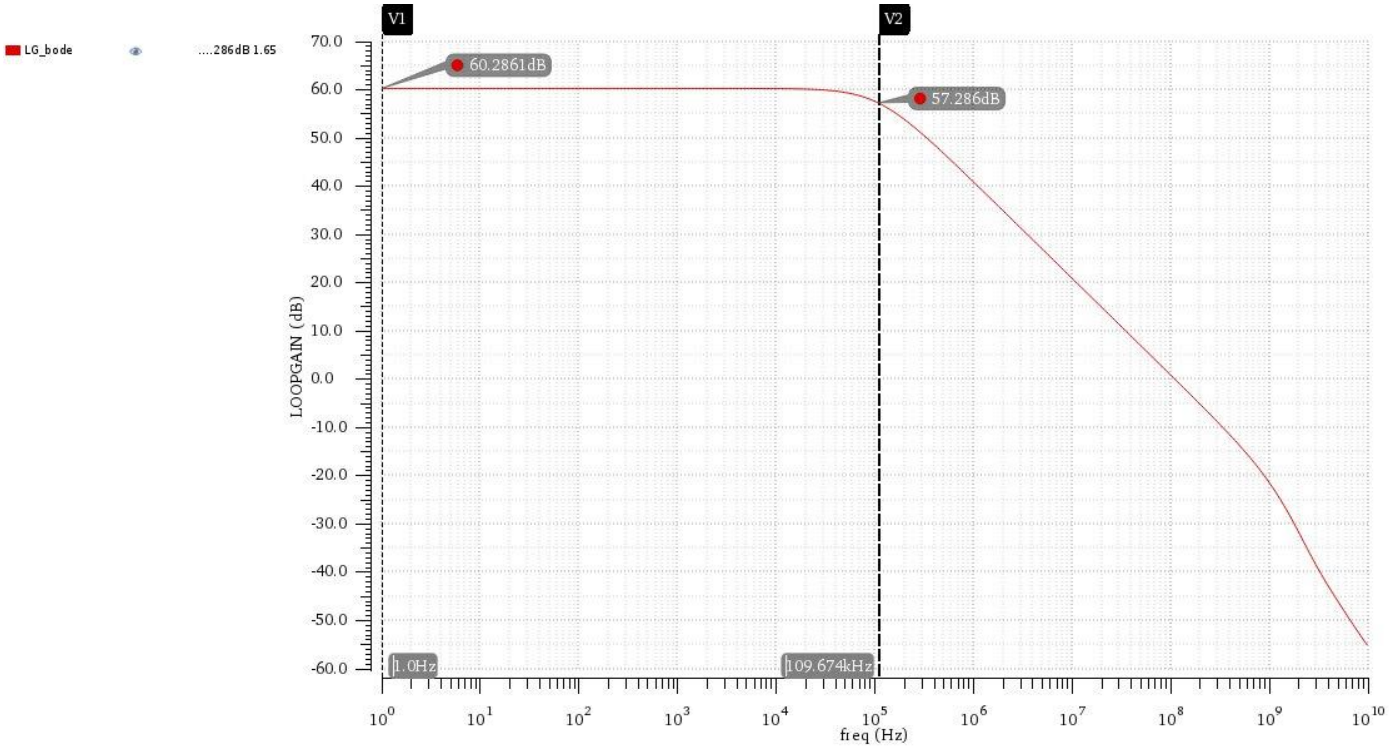


Figure 16: Loop Gain Bode Plot

STB Gain and Phase Vs Frequency (AC)

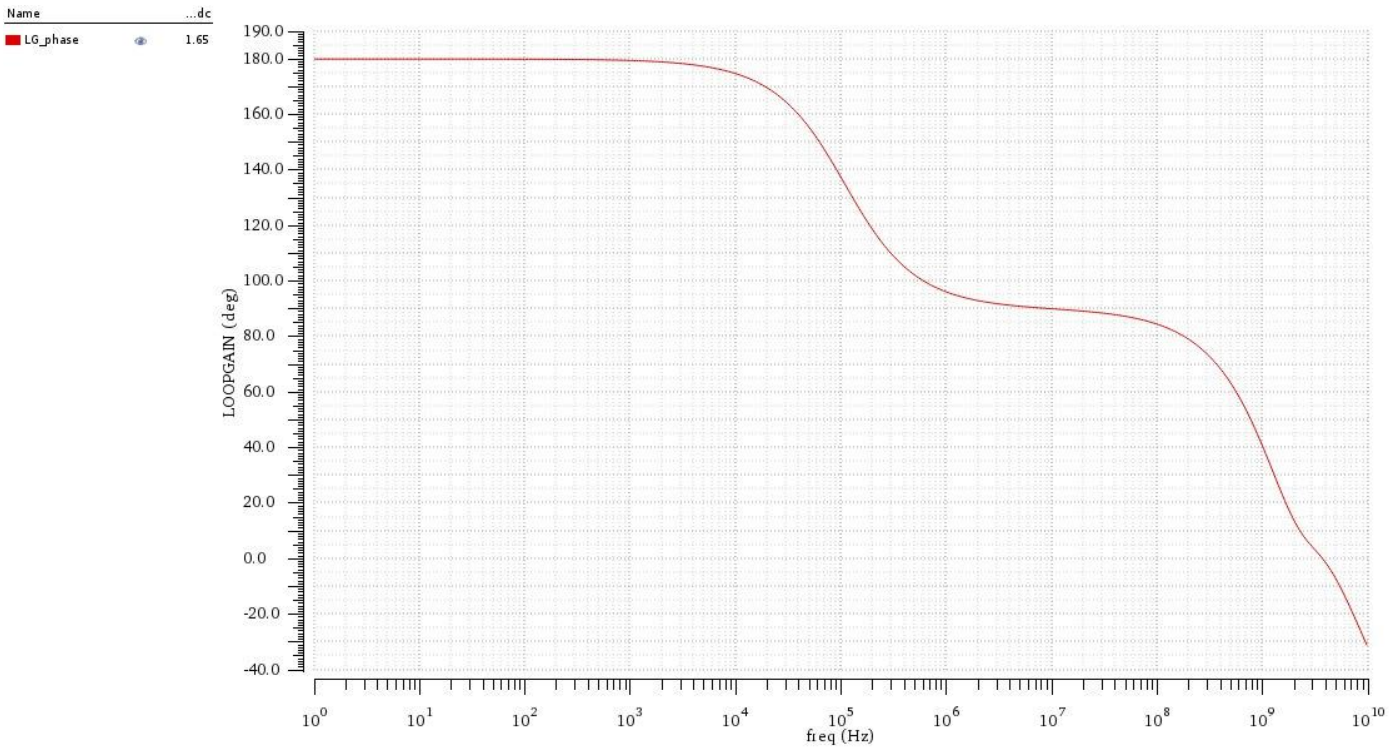


Figure 17: Loop Gain Phase Plot

Calculate Open Loop Gain and PM and GBW in STB Analysis

LG_bode	
LG_phase	
LG_dc	60.29
LG_PM	83.9
LG_GBW	113.6M

Figure 18: STB Summary

P.O.C	Open Loop Simulations	STB Analysis
DC gain	$(61.73)_{dB} = (1.22\ KV/V)_{linear}$	$(60.29)_{dB} = (1.034\ KV/V)_{linear}$
Comments	This Difference is Due to Non-Idealities as Buffer Doesn't Seen infinite input Resistance as $A_{(STB)} = KA_o$ & $A_{OL} = A_o$	
PM	$82.7106°$	$83.9°$
GBW	$117.063\ MHz$	$113.6\ MHz$
Comments	As The Feedback factor is function of frequency which in return the is affected by the input capacitance of the input pair creating an extra non dominant pole decreasing the PM and the GBW.	

Closed Loop Gain (A_{CL}) and Closed Loop BW (BW_{CL})

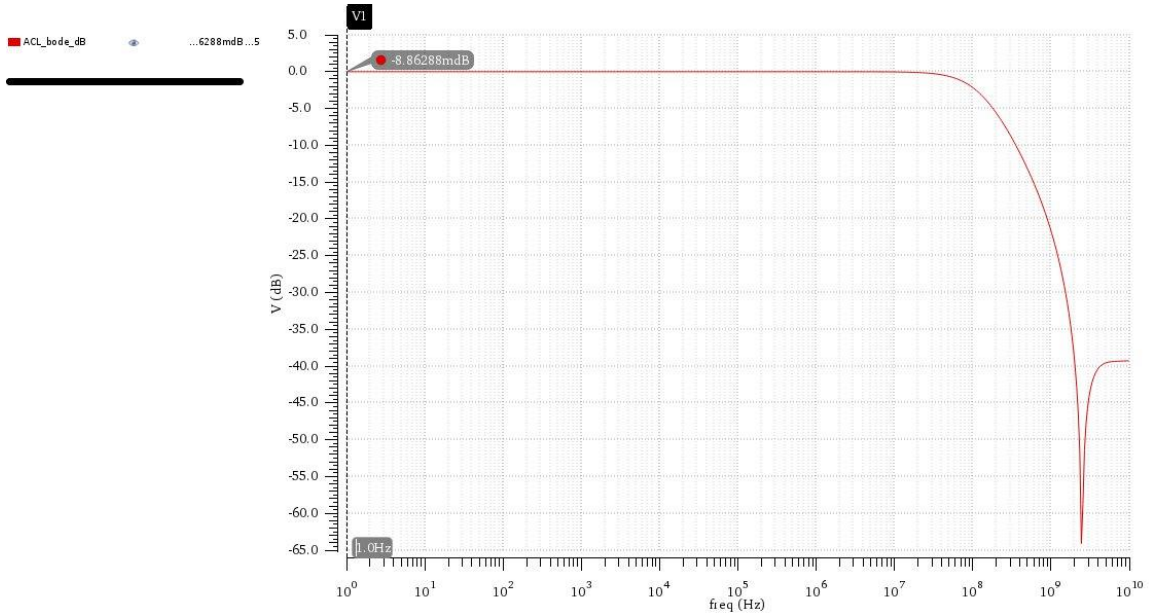


Figure 19: Closed Loop Bode Plot

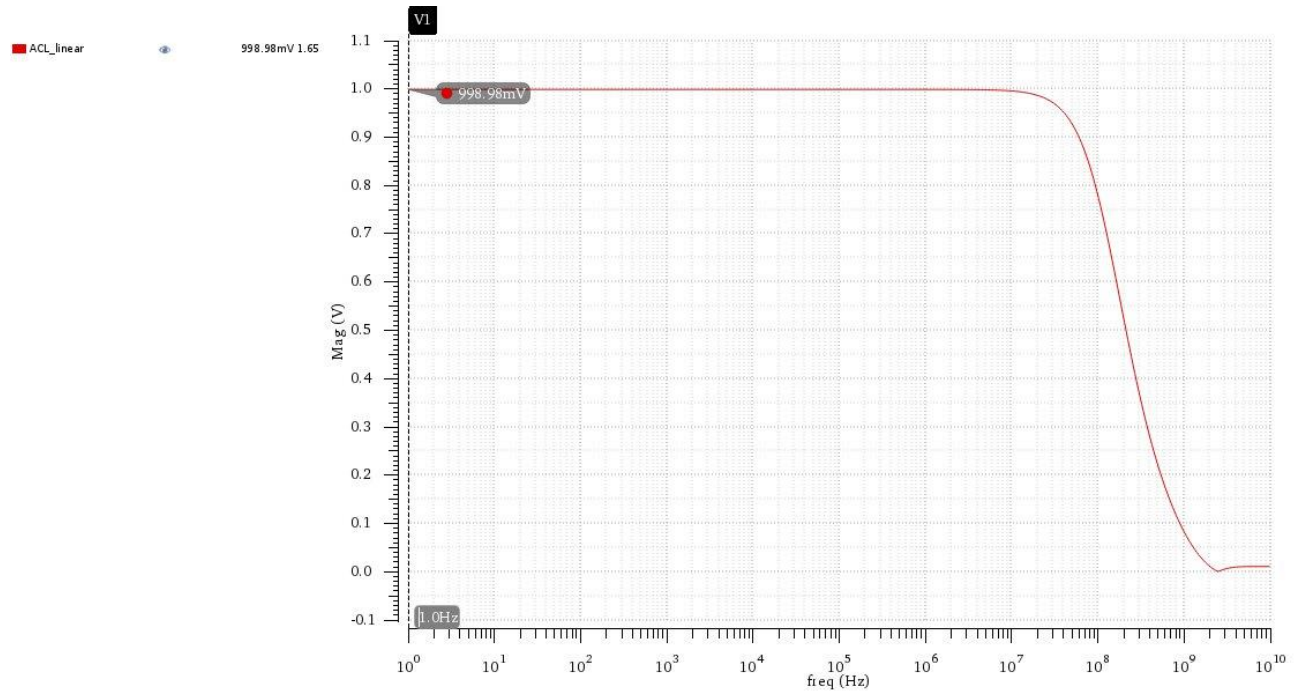


Figure 20: Closed Loop Linear Plot

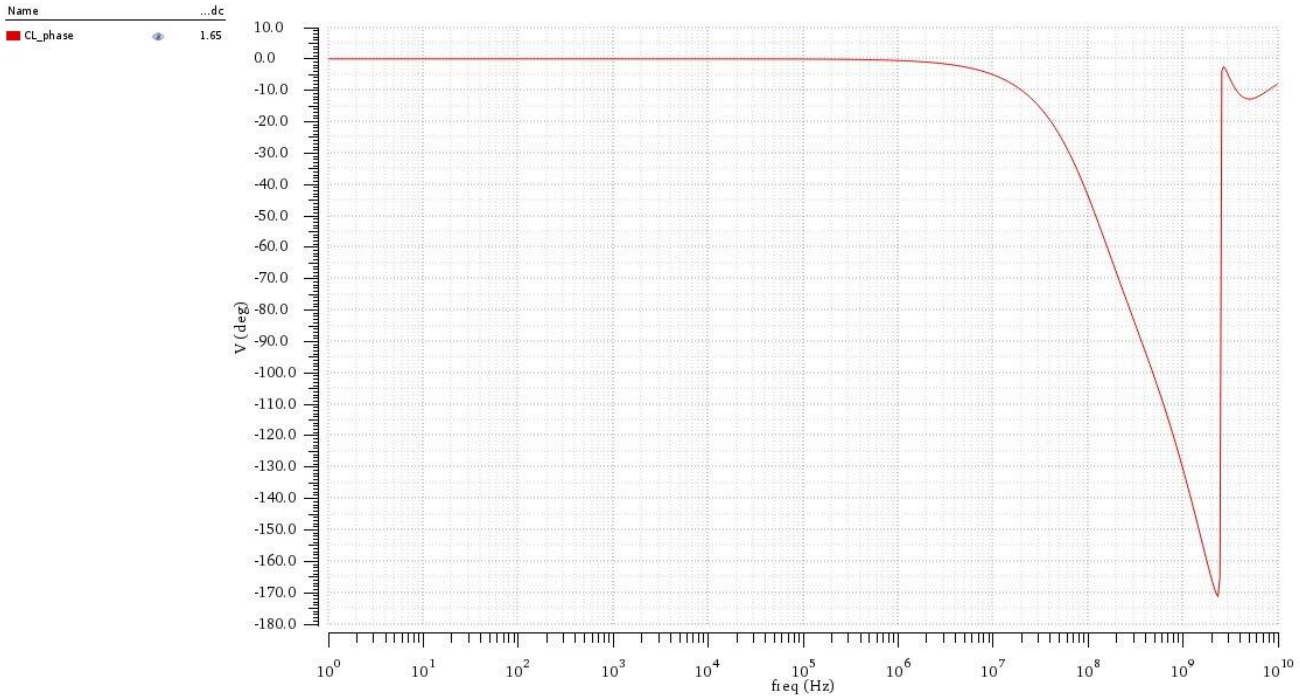


Figure 21: Closed Loop Phase Plot

ACL_dc_dB	-8.863m
ACL_dc_linear	complex(999m, -8.613n)
BW_CL	127.4M

Figure 22: CL Summary

Comments:

As per expected , the negative feed back trades the high gain to support linearity & therefore BW extension with nearly constant GBW.

Hand Analysis:

Closed-loop Gain:

From the graph:

$A_{CL} = 0.29\ dB = 1.034\ (Linearly)$

From Hand analysis:

$A_{CL} = \frac{A_{OL}}{1+KA_{OL}} = \frac{1432.072}{1+1432.072} = 0.9993 \approx 1$

Closed-loop Bandwidth:

From the graph:

$BW_{CL} = 138.082\ KHz$

By Hand analysis:

$BW_{CL} = BW_{OL}(1 + KA_{OL}) = 96.3544\ kHz * (1 + 1432.072) = 138.083\ MHz$

There is a difference between the calculated value and the value from the graph because of the loading effect.

Simulate input-referred noise and tabulate top 4 contributors @10 MHz

Device	Param	Noise Contribution	% Of Total
/I0/M1b	id	2.86422e-09	24.92
/I0/M1a	id	2.8632e-09	24.90
/I0/M2a	id	1.99993e-09	12.15
/I0/M2b	id	1.99644e-09	12.11
/I0/M5b	id	1.53145e-09	7.12
/I0/M5a	id	1.52987e-09	7.11

```
Spot Noise Summary (in V/sqrt(Hz)) at 100M Hz Sorted By Noise Contributors
Total Summarized Noise = 5.73752e-09
Total Input Referred Noise = 7.28639e-09
The above noise summary info is for noise data
```

Comments:

As we expected the top contributed for the thermal noise are M1 , M2 and M5 and the noise of M3 , M4 are nearly Neglected due to having degenerative transconductance.

Its noting that we simulated the input refered noise at 100 MHz instead of 10 MHz to be far from the flicker noise corner to nearly neglect the flicker noise contribution.

The percentage of the total noise accounts for the flicker noise contirbution.

Noise Analysis:

$$\overline{V_{n,in_{thermal}}^2} = 8KT\frac{\gamma}{g_{m1(a,b)}}\left(1+\frac{g_{m2(a,b)}}{g_{m1(a,b)}}+\frac{g_{m5(a,b)}}{g_{m1(a,b)}}\right)$$

From the Simulation:

$g_{m1(a,b)} = 1.51938\,mS$

$g_{m2(a,b)} = 1.36883\,mS$

$g_{m5(a,b)} = g_{m5(a,b)} = 0.4323\,mS$

$\overline{V_{n,in_{thermal}}^2} = 3.068255 * 10^{-17}\ (V^2/Hz)$

$\overline{V_{n,in\_thermal}} = 5.53918 * 10^{-9}\ (V/\sqrt{Hz})$

Simulate the slew rate and verify the specifications.

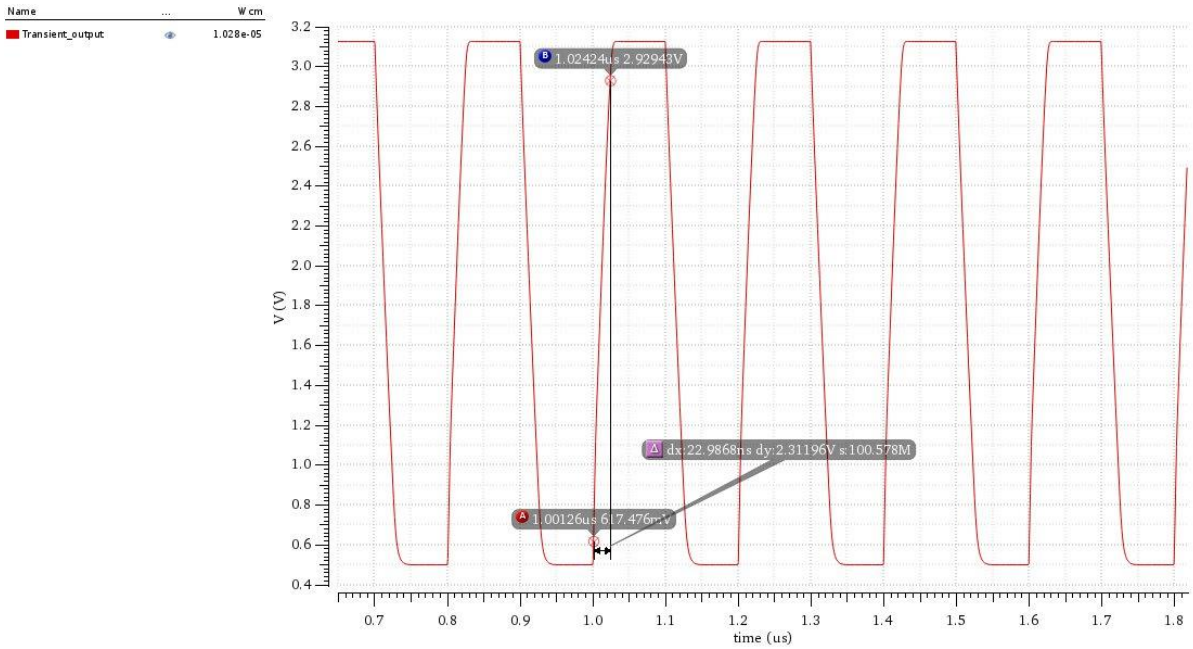
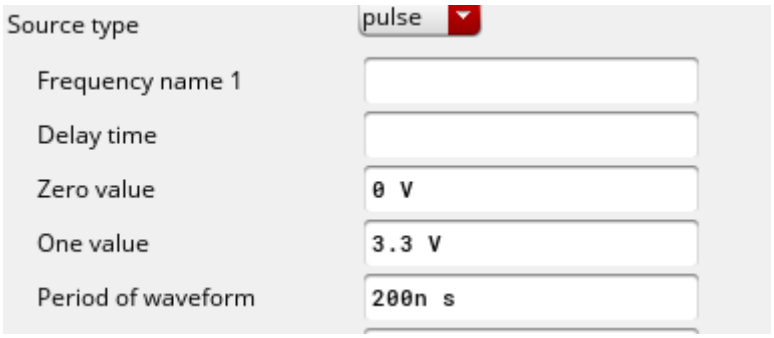


Figure 23: Transient Output Due to Pulse Step input Showing the Slew Rate

Slew Rate $= 100.578\ MV/sec$

Apply a sine input signal of 1Vpp @ 10 MHz and plot Vout (Add proper input DC value). Plot DFT (in dB) and calculate harmonic distortion (HD2, HD3, and THD) in dB.



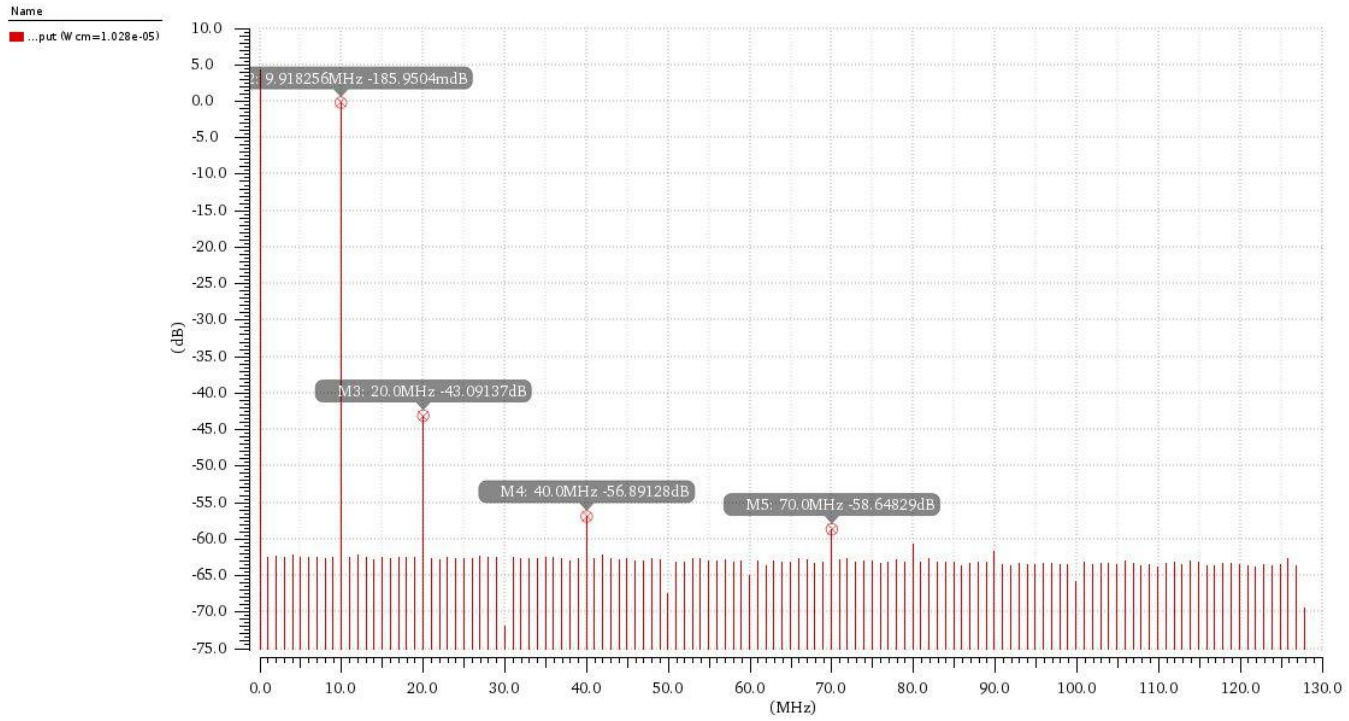


Figure 24: DFT (in dB)

THD	838.2m

THD hand analysis:

$$THD = \frac{P_{Harmonics}}{P_{fundamental}} = \frac{\sqrt{10^{\frac{-43.09137}{10}} + 10^{\frac{-56.89128}{10}} + 10^{\frac{-58.64829}{10}}}}{10^{\frac{-0.18595}{10}}} \times 100 = 0.756\ \%$$

P.O.C.	Simulated	Hand Analysis
THD	0.8382 %	0.756 %

Plot Vout for a small step input of 100mV (Add proper input DC value).

Calculate the fractional gain error (FGE) and 1% settling time.

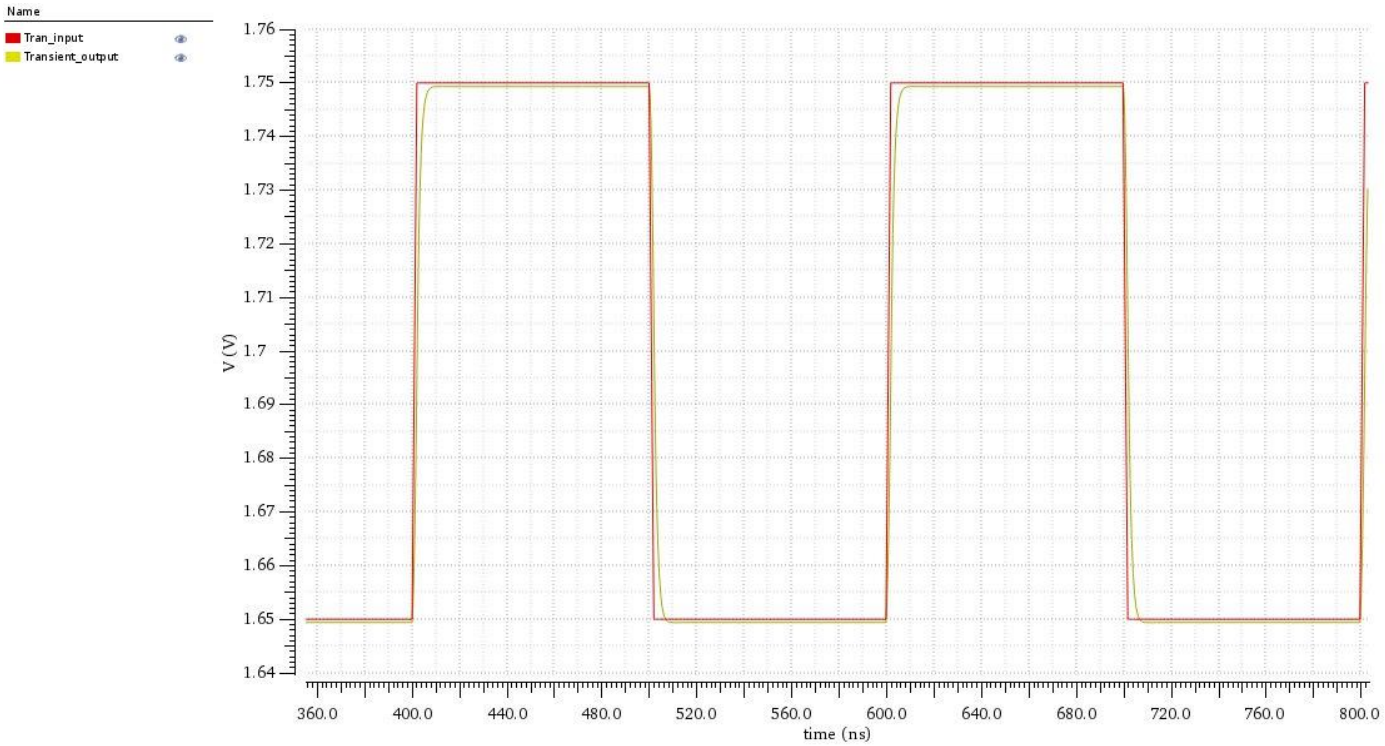


Figure 25: Fractional Gain Error

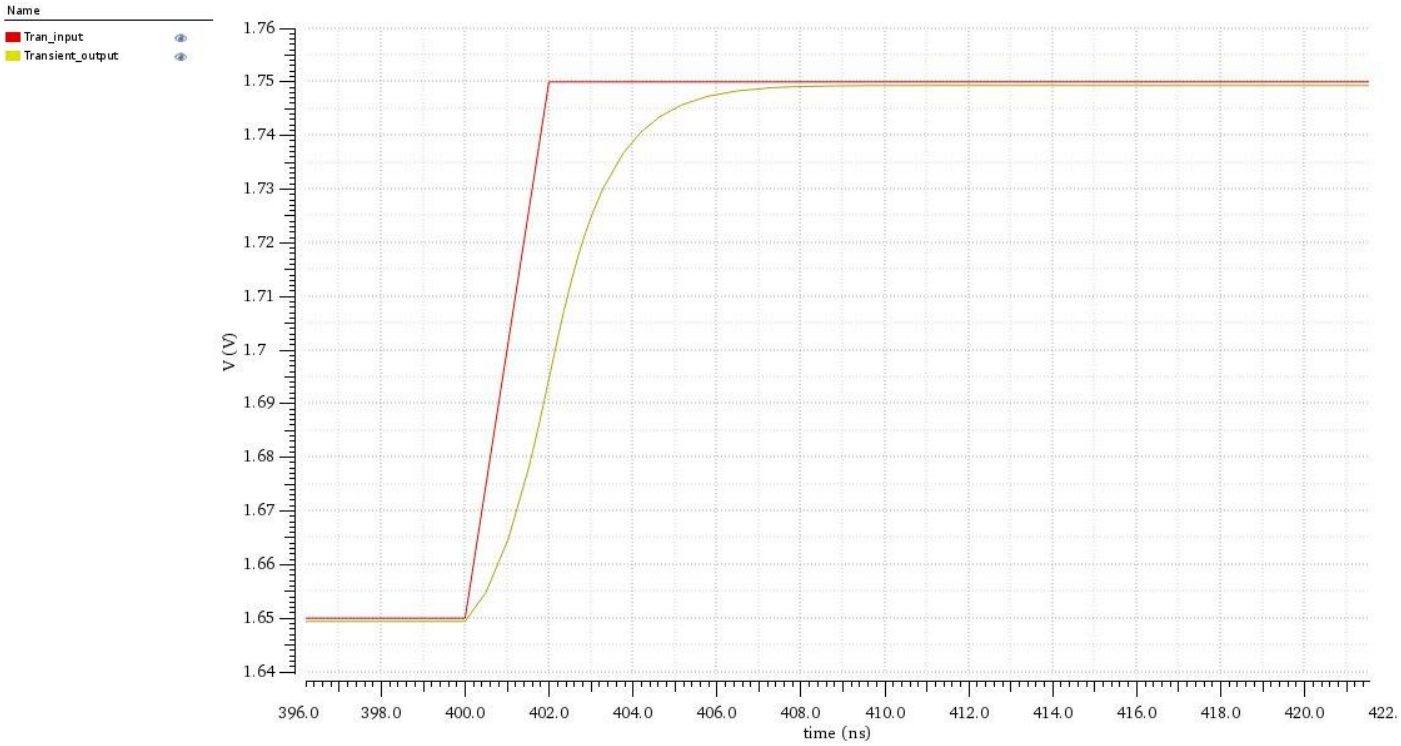


Figure 26: Zoomed FGE

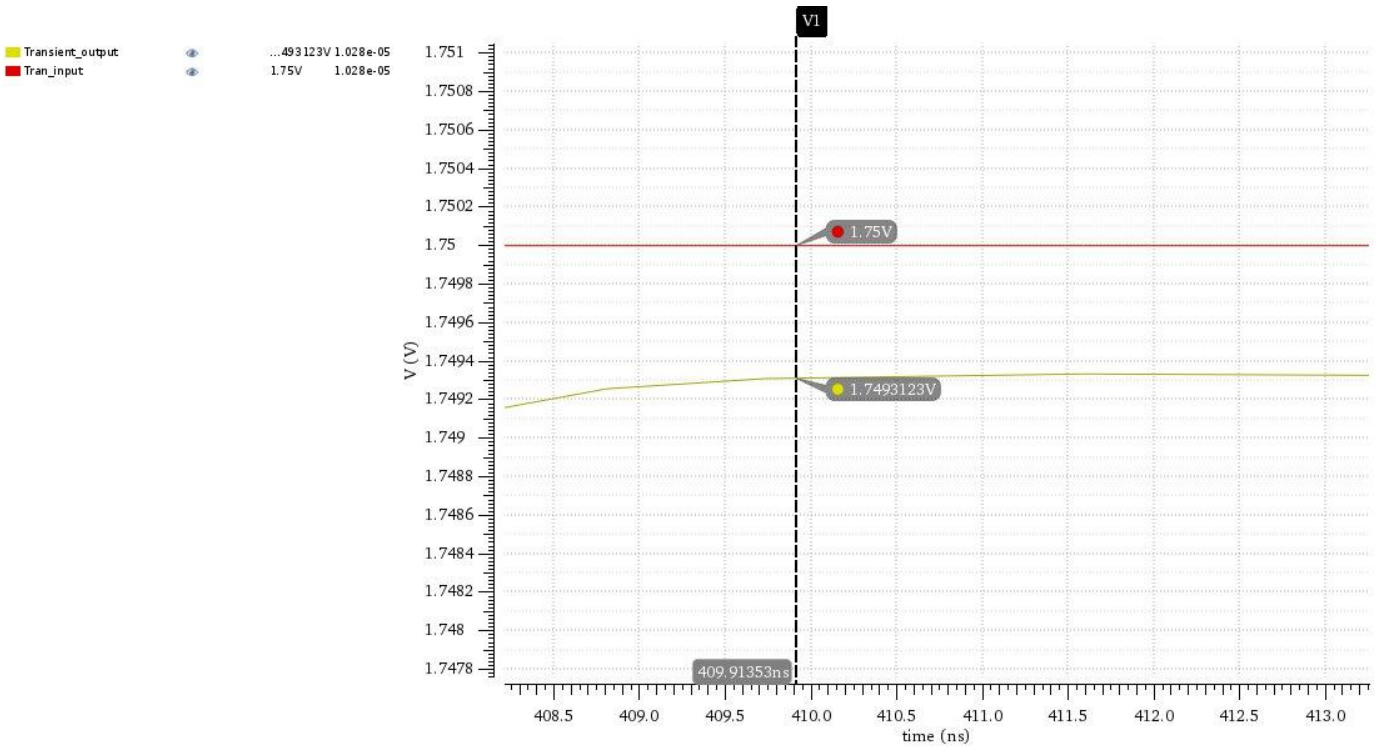


Figure 27: Zoomed FGE Showing the Error Values

$$\boldsymbol{Simulated\ FGE = \frac{1.75 - 1.7493}{1.75} \times 100 = 0.04\ \%}$$

Hand Analysis:

FGE Hand Analysis:

$$FGE = \frac{1}{feedback\ factor * DC\ gain} * 100 = \frac{1}{10^{\frac{63.1193}{20}}} * 100 = 0.069\%$$

It's unity feedback then the feedback factor is 1
$DC\ gain\ =\ 60.29\ dB\ =\ 1.034\ (linearly)$

$$\boldsymbol{1\%\ settling\ time\ \approx \frac{4}{2\pi * closed\ loop\ BW}\ \approx \frac{4}{2\pi * 138\ KHZ}\ = 4.61\ \mu s}$$

The results from hand analysis and simulation are approximately the same (the used expression in hand analysis is for 98% settling so the simulated value is different than the calculated one)

Discussion

Results & Conclusions

- The folded cascode topology serves some advantages that appears in the open-loop simulations as:
  - High gain
  - High output swing (with decoupled input & output ranges)
  - High GBW due to having simpler nodes than the typical telescopic cascode.

- But it shows some drawbacks related to the power consumption to supply enough slewing immunity → Higher power consumption.

- The buffer closed - loop simulations show the worst-case scenarios of the negative feedback simulations
  (since the typical operation uses $0 < \beta < 1$)

- The transient simulations test the non-linear operation from which we conclude that high gain (= Low FGE) , acceptable PM (= No overshooting) , high output swing (= low gain compression)can introduce the designed opamp for high frequency operations with minimal drawbacks as long as we are working in the required band of operations that insures low attenuation with minimal distortion.

Specs. Achieved

Specs.	Required	Achieved
DC Currents Assumptions	$I_1 = 200\ \mu A, I_2 = 100\ \mu A, I_3 = 200\ \mu A$	
Supply (V_{DD})	$3.3\ V$	
$V_{inCM} = \frac{V_{DD}}{2}$	$1.65\ V$	
C_L	$2\ pF$	
DC Diff. Gain (A_{DC})	$> 55\ dB$	$61.7282\ dB$
GBW	$> 100\ MHz$	$117.063\ MHz$
Slew Rate	$> 100\ V/\mu sec$	$100.578\ MV/sec$
Output Swing	$> 1.5\ V_{PP}$	$2.441743\ V_{PP}$
Input referred thermal noise (V_{i_n})	$< 10\ nV/\sqrt{Hz}$	$7.28639\ nV/\sqrt{Hz}$
Phase Margin (PM)	$> 60°$	$82.7106°$
Power Consumption	Minimized	

The END Thank You