Cadence Virtuoso LAB (5) Report

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Analog Electronics Workshop

Simple vs Low Compliance Cascode Current Mirror

Part 1

Sizing Chart

P1:

→ **Square Law.**

We used $g_m = \frac{2I_D}{V_{ov}}, V_{ov} = \frac{2I_D}{g_m}$

$V^* = V_{ov}$

→ **For Real MOSFET.**

$V_{ov} \neq \frac{2I_D}{g_m} \rightarrow$ **Define** $V^* = \frac{2I_D}{g_m} \Leftrightarrow g_m = \frac{2I_D}{V^*}$

In Simulation $(V^* = 200\ mV)$.

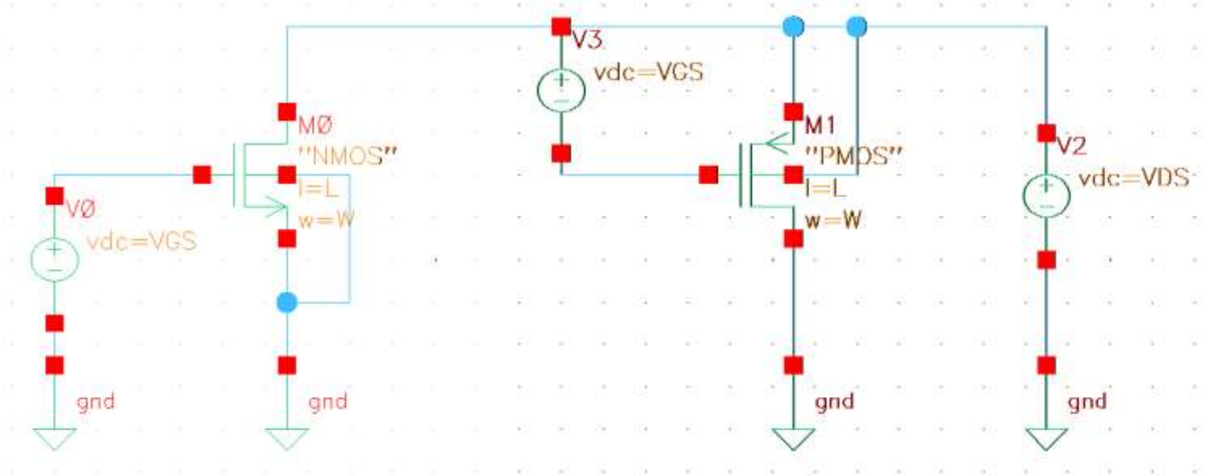
P2:

We want to design Current Mirrors with the parameters below.

Specs (Specifications) $M_1 = PMOS, M_2 = NMOS$

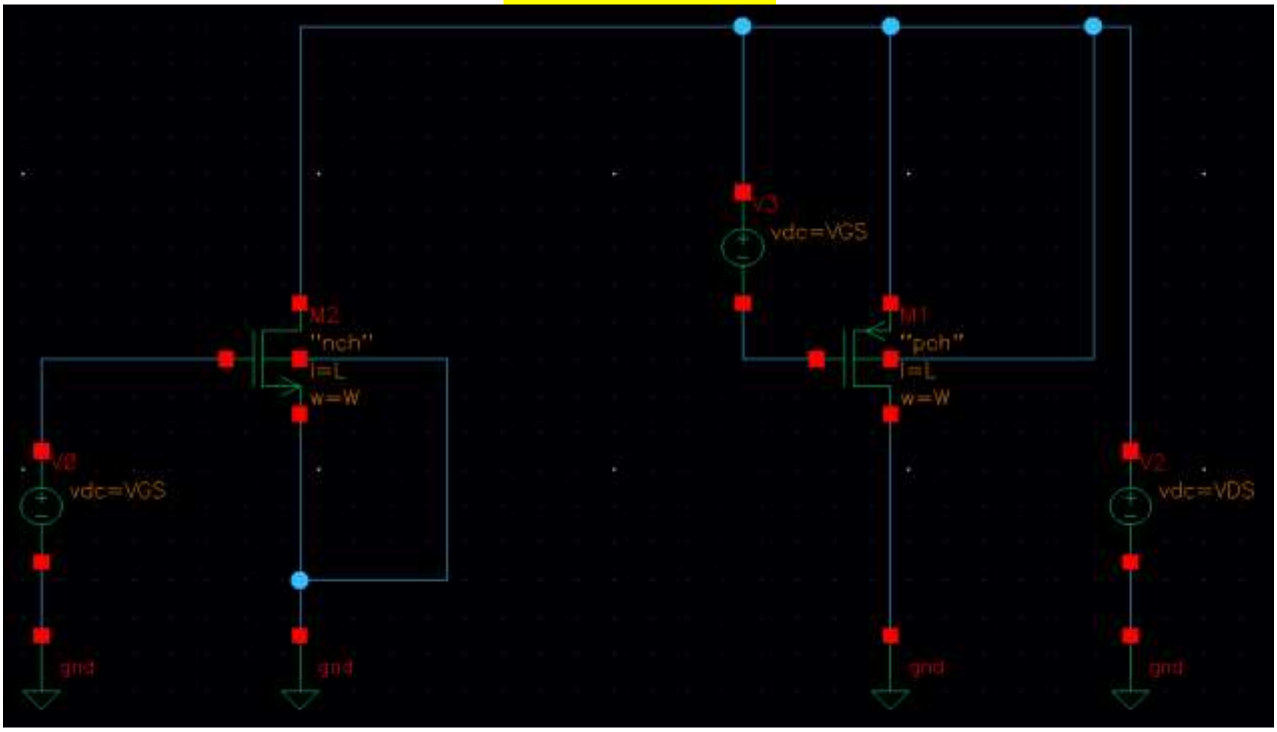
$V_{Star}\ (V^*)$	$200\ mV.$
Supply (V_{DD})	$1.8\ V.$
Reference Current (I_{REF})	$20\ \mu A.$
Length (L)	$1\ \mu m.$
Width (W)	$10\ \mu m.$

Circuit



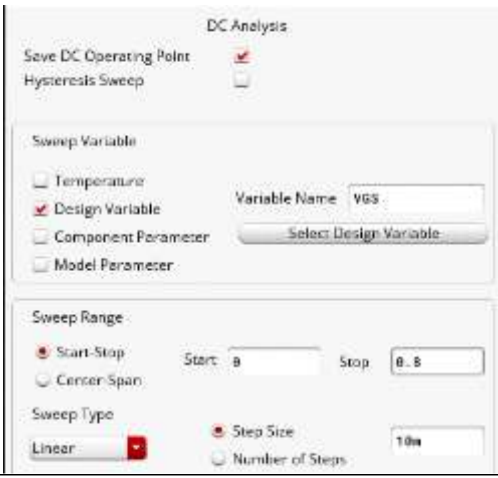
P3

Schematic



P4

Sweep V_{GS} from 0 to $\approx V_{TH} + 0.4V = 0.8$ with 10 mV step. Set $V_{DS} = \frac{V_{DD}}{2}$.



P5

We want to compare $V^* = \frac{2I_D}{g_m}$ and $V_{ov} = V_{GS} - V_{TH}$ by plotting them overlaid. Use the calculator to create expressions for V^* and V_{ov} .

V_{ov} For PMOS: v("M1:vgs" ?result "dc")-v("M1:vth" ?result "dc")

V^* For PMOS: 2*getData("M1:id" ?result "dc")/getData("M1:gm" ?result "dc")

V_{ov} For NMOS: v("M2:vgs" ?result "dc")-v("M2:vth" ?result "dc")

V^* For NMOS: 2*getData("M2:id" ?result "dc")/getData("M2:gm" ?result "dc")

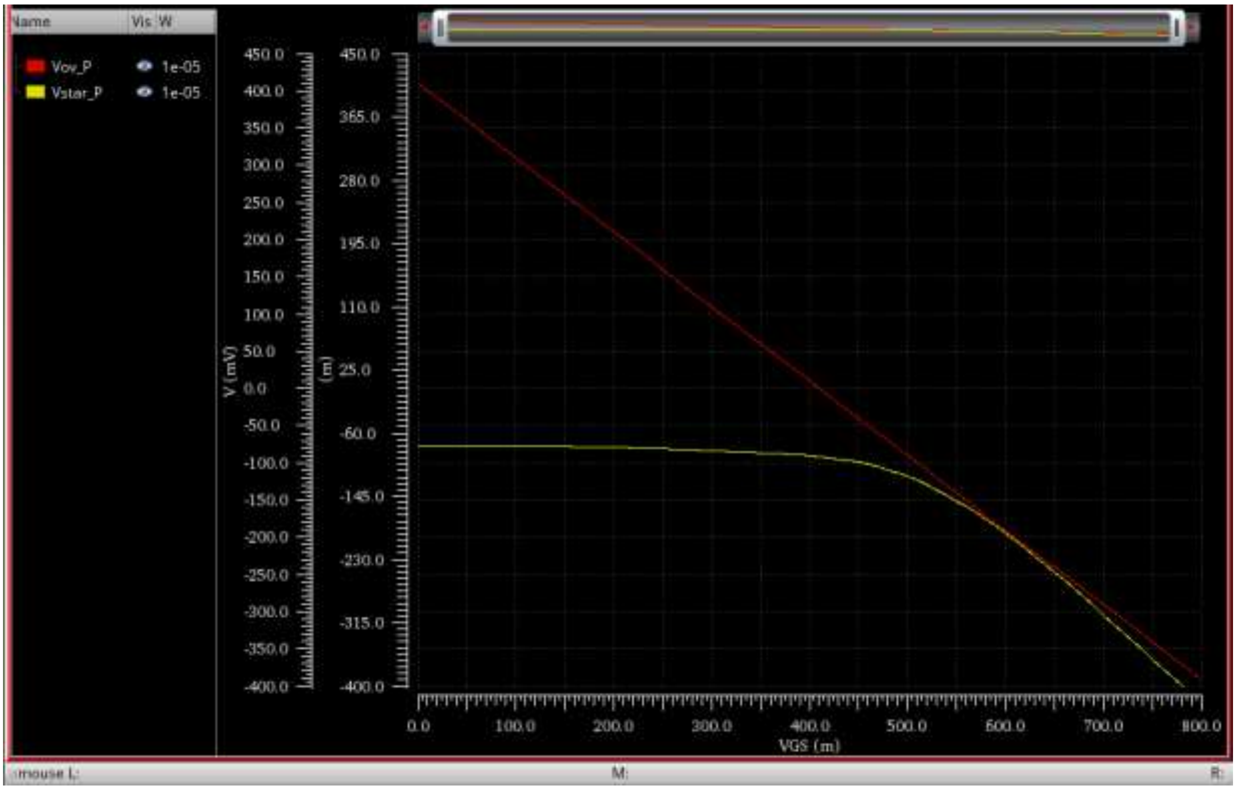
LAB_5_PART_1 | adexl

Outputs Setup | Run Preview | Results | Diagnostics

Test	Name	Type	Details	EvalType	Plot	Save
IEEE...	Vov_P	expr	(v("M1:vgs" ?result "dc") - v("M1:vth" ?result "dc"))	point	✔	
IEEE...	Vstar_P	expr	((2 * getData("M1:id" ?result "dc")) / getData("M1:gm" ?result "dc"))	point	✔	
IEEE...	id_P	expr	getData("M1:id" ?result "dc")	point	✔	
IEEE...	gm_P	expr	getData("M1:gm" ?result "dc")	point	✔	
IEEE...	gds_P	expr	getData("M1:gds" ?result "dc")	point	✔	
IEEE...	Vov_N	expr	(v("M2:vgs" ?result "dc") - v("M2:vth" ?result "dc"))	point	✔	
IEEE...	Vstar_N	expr	((2 * getData("M2:id" ?result "dc")) / getData("M2:gm" ?result "dc"))	point	✔	
IEEE...	id_N	expr	getData("M2:id" ?result "dc")	point	✔	
IEEE...	gm_N	expr	getData("M2:gm" ?result "dc")	point	✔	
IEEE...	gds_N	expr	getData("M2:gds" ?result "dc")	point	✔	

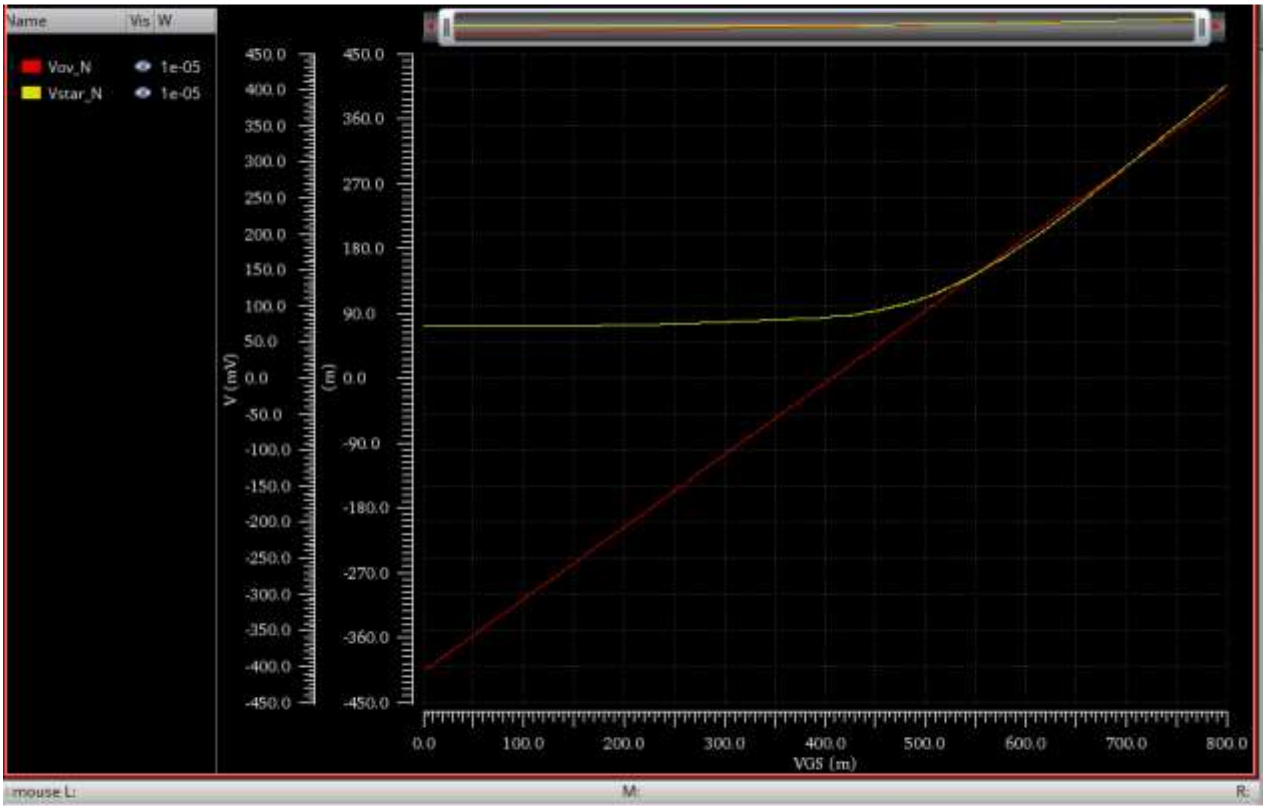
P6

Plot V^* and V_{ov} Overlaid vs V_{GS}
Y-axis of Both Curves Has Same Range For M_1 = PMOS



Plot V^* and V_{ov} Overlaid vs V_{GS}

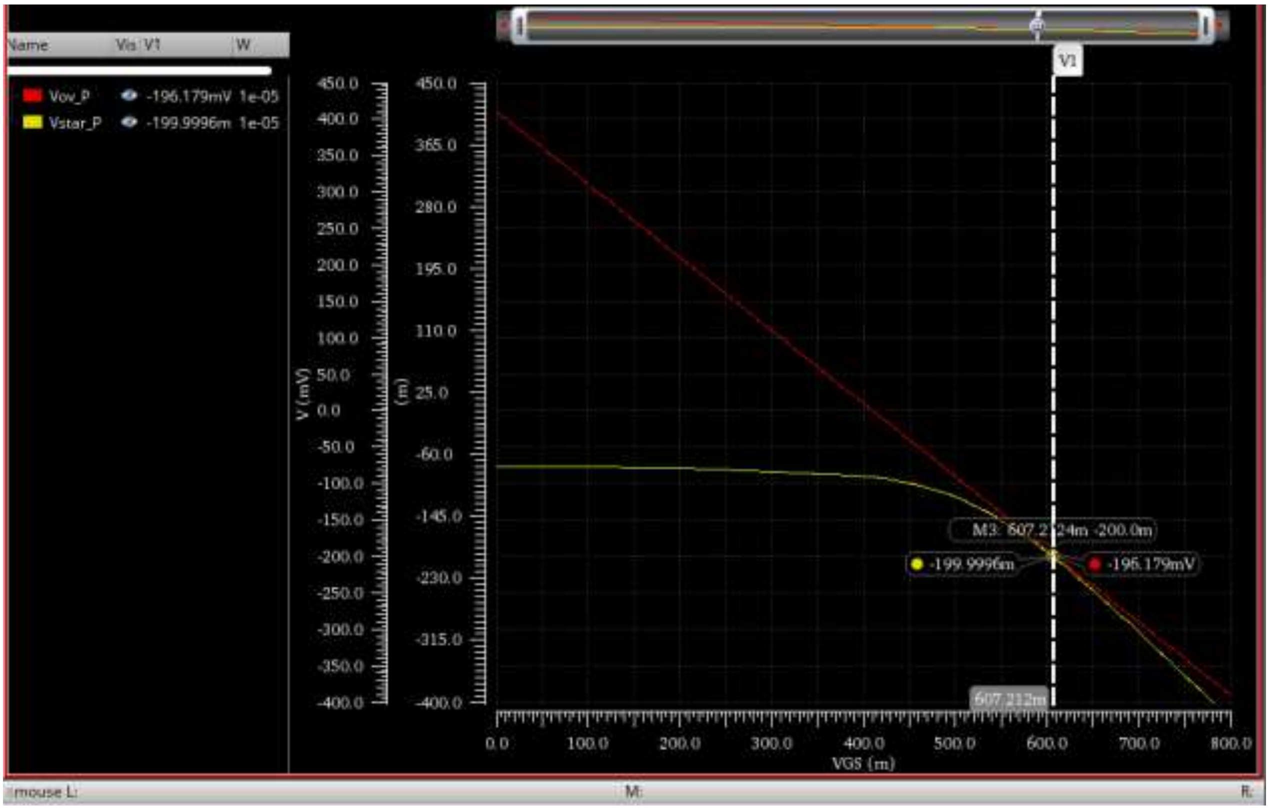
Y-axis of Both Curves Has Same Range For $\mathbf{M_2} = \mathbf{NMOS}$



We will notice that at the beginning of the strong inversion region, $\mathbf{V^*}$ and $\mathbf{V_{ov}}$ are relatively close to each other (i.e., square – law is relatively valid). For deep strong inversion (large $\mathbf{V_{ov}}$: velocity saturation and mobility degradation) or weak inversion (near – threshold and subthreshold operation) the behavior is quite far from the square – law.

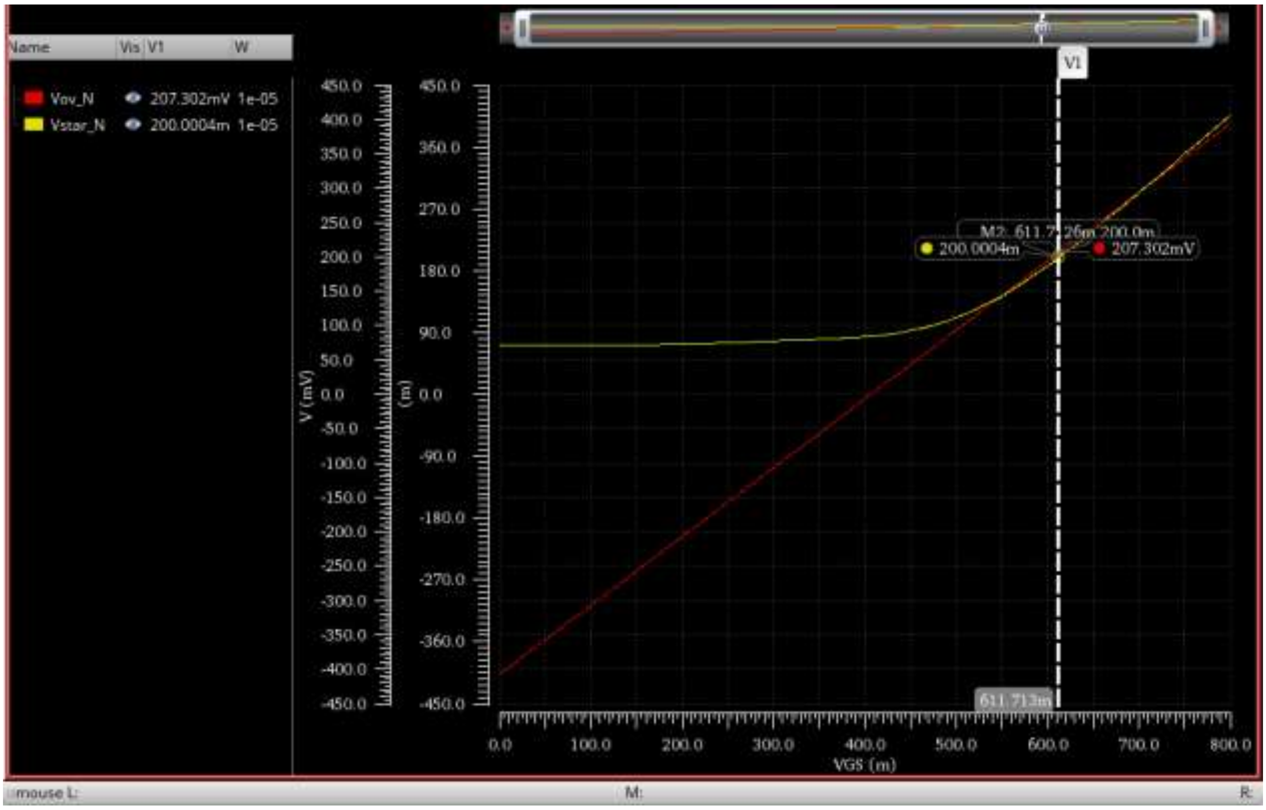
On the V^* and V_{ov} Chart Locate the Point at Which $V^* = 200$ mV. Find the Corresponding V_{ov_Q} and V_{GS_Q} For $M_1 = $ PMOS.

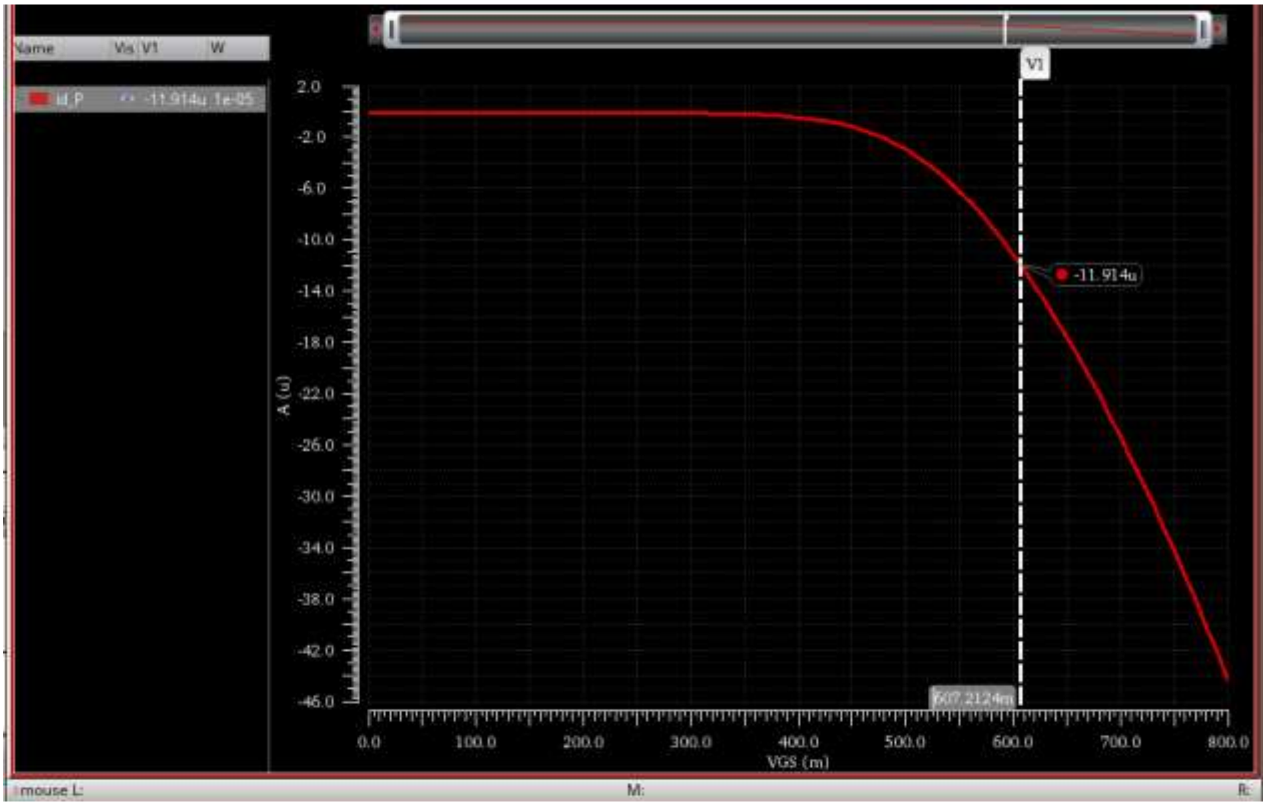
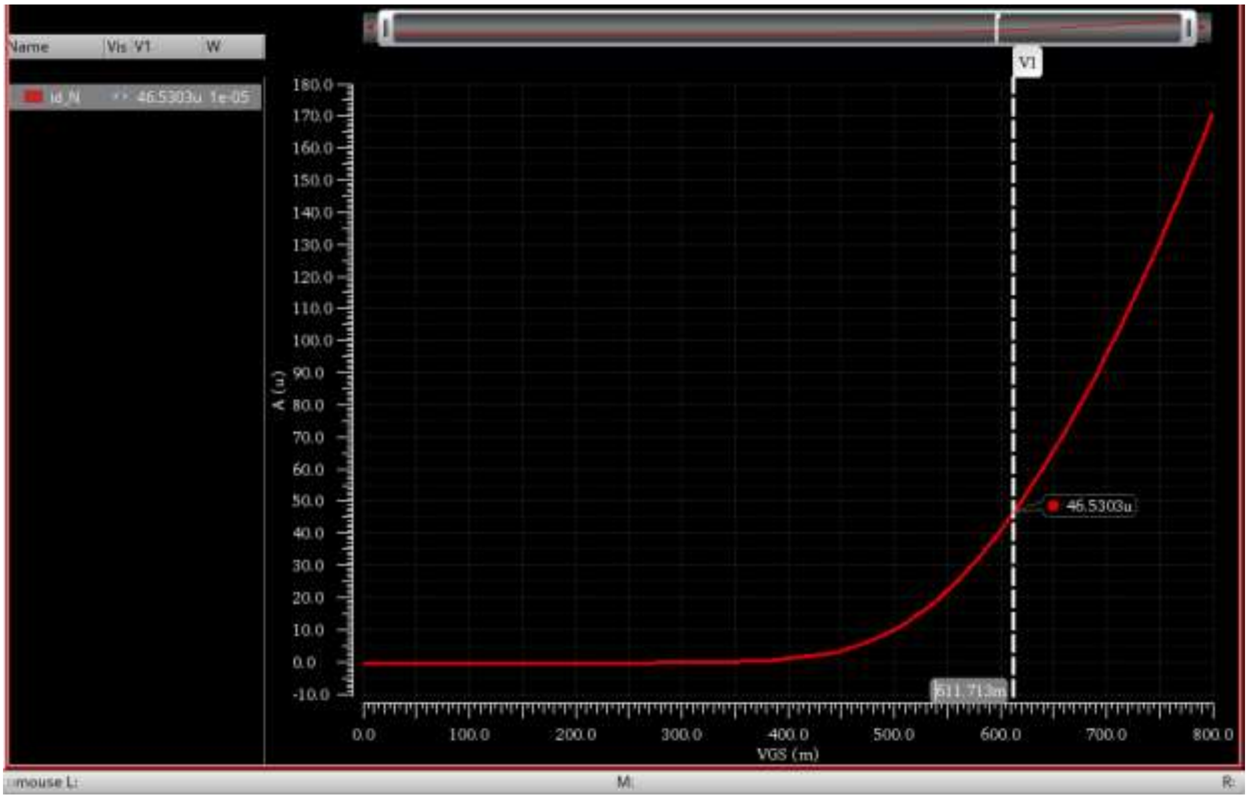
P7



$$@\ V^*_Q = -200\ \text{mV} \rightarrow V_{ov_Q} = -196.179\ \text{mV}.$$

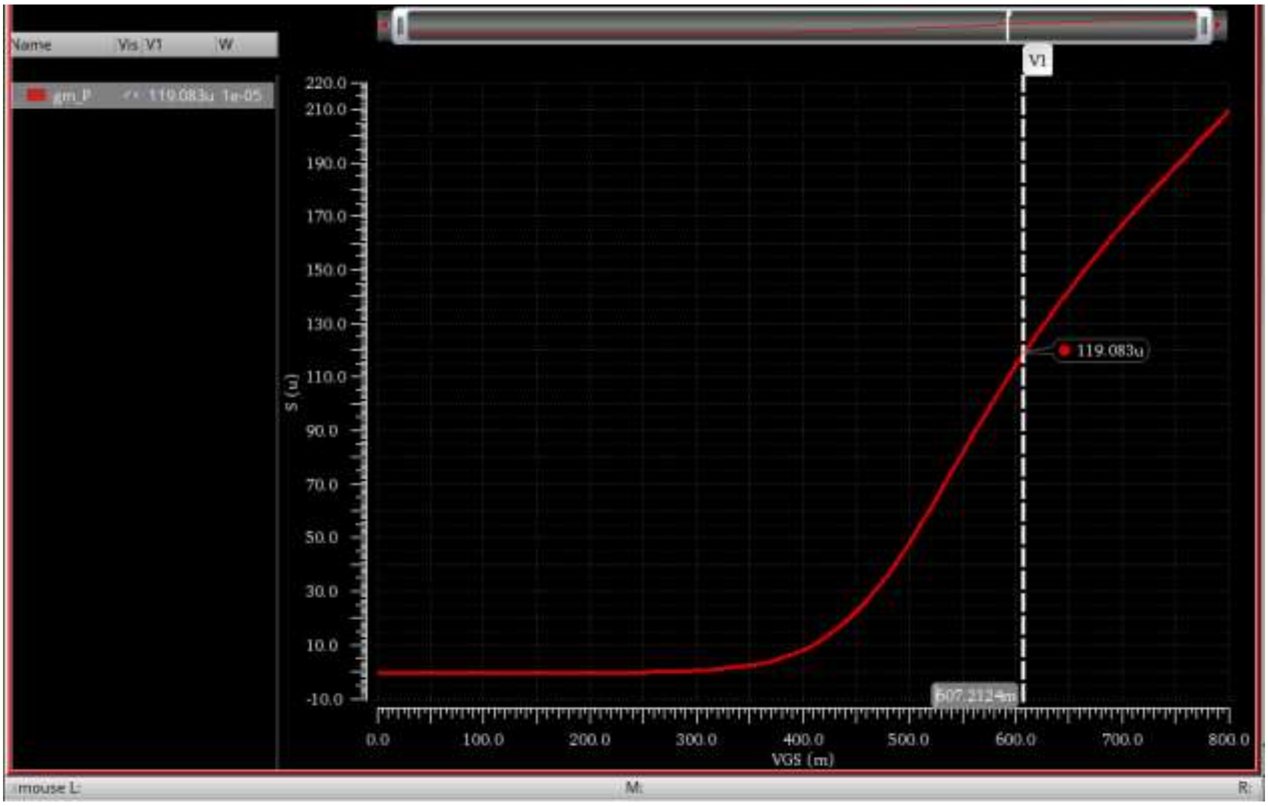
$$\rightarrow V^* = -199.9996\ \text{mV} \rightarrow V_{GS_Q} = 607.2124\ \text{mV}.\ @\ V_{TH} \approx 0.4\ \text{V}.$$

P7	**On the V^* and V_{ov} Chart Locate the Point at Which $V^* = 200\ mV$. Find the Corresponding V_{ov_Q} and V_{GS_Q} For $M_2 = NMOS$.**  $$@\ V_Q^* = 200\ mV \rightarrow V_{ov_Q} = 207.302\ mV.$$ $\rightarrow V^* = 200.0004\ mV \rightarrow V_{GS_Q} = 611.713\ mV.\ @\ V_{TH} \approx 0.4\ V.$

P8	**Plot I_D vs V_{GS}. Find its Values at V_{GS_Q} For M_1 = PMOS**  **$@V_{GS_Q} = 607.2124$ mV $\rightarrow I_{D_X} = -11.914\ \mu A$.**
P8	**Plot I_D vs V_{GS}. Find its Values at V_{GS_Q} For M_2 = NMOS**  **$@V_{GS_Q} = 611.713$ mV $\rightarrow I_{D_X} = 46.5303\ \mu A$.**

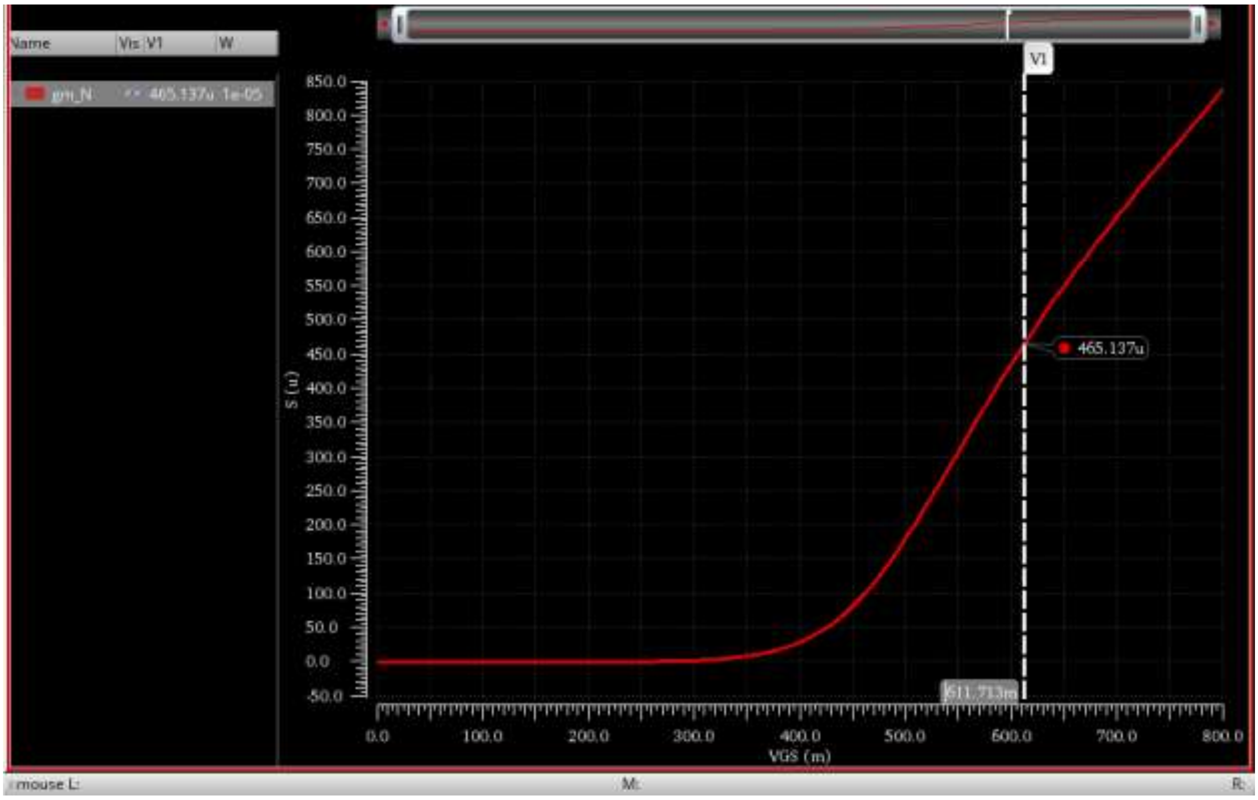
P8

Plot g_m vs V_{GS}. Find its Values at V_{GS_Q} For M_1 = PMOS



$@V_{GS_Q} = 607.2124\ mV \rightarrow g_{m_X} = 119.083\ \mu S.$

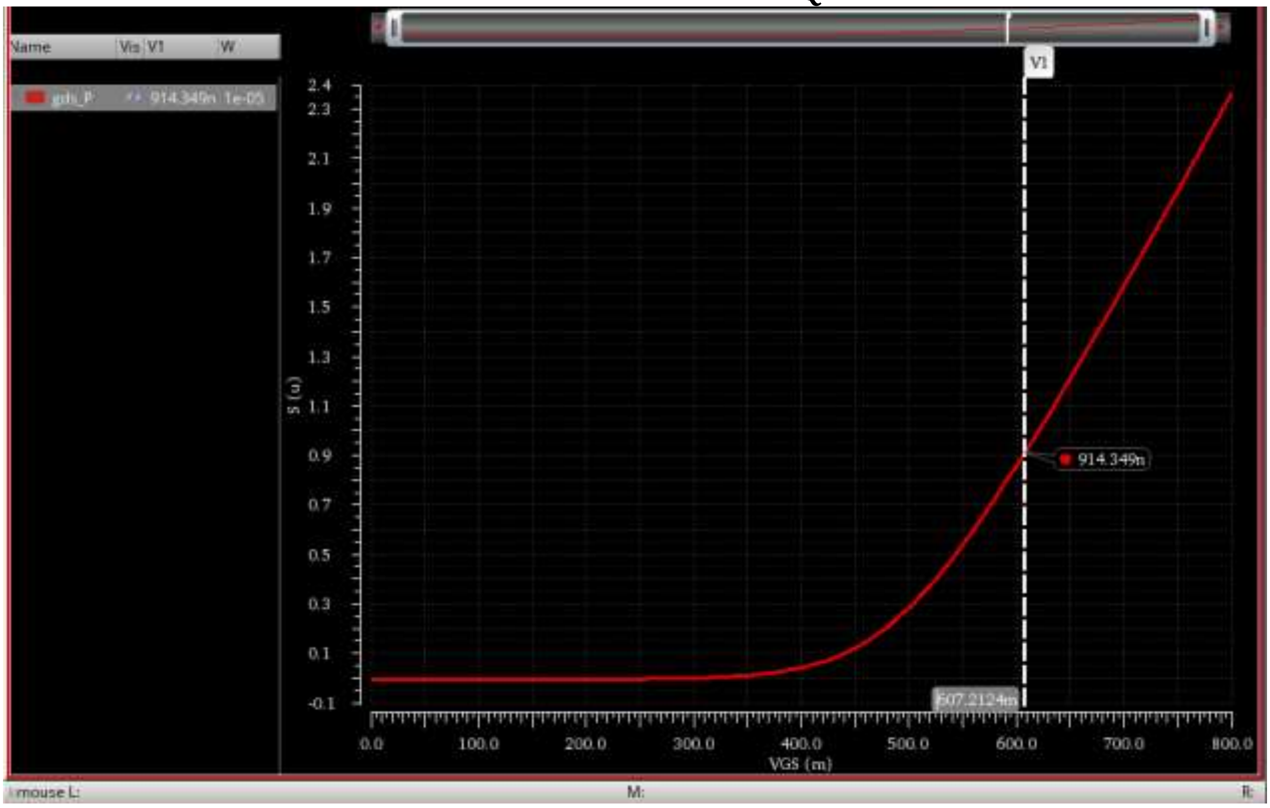
Plot g_m vs V_{GS}. Find its Values at V_{GS_Q} For M_2 = NMOS



$@V_{GS_Q} = 611.713\ mV \rightarrow g_{m_X} = 465.137\ \mu S.$

<table>
<tr>
<td rowspan="2">P8</td>
<td>

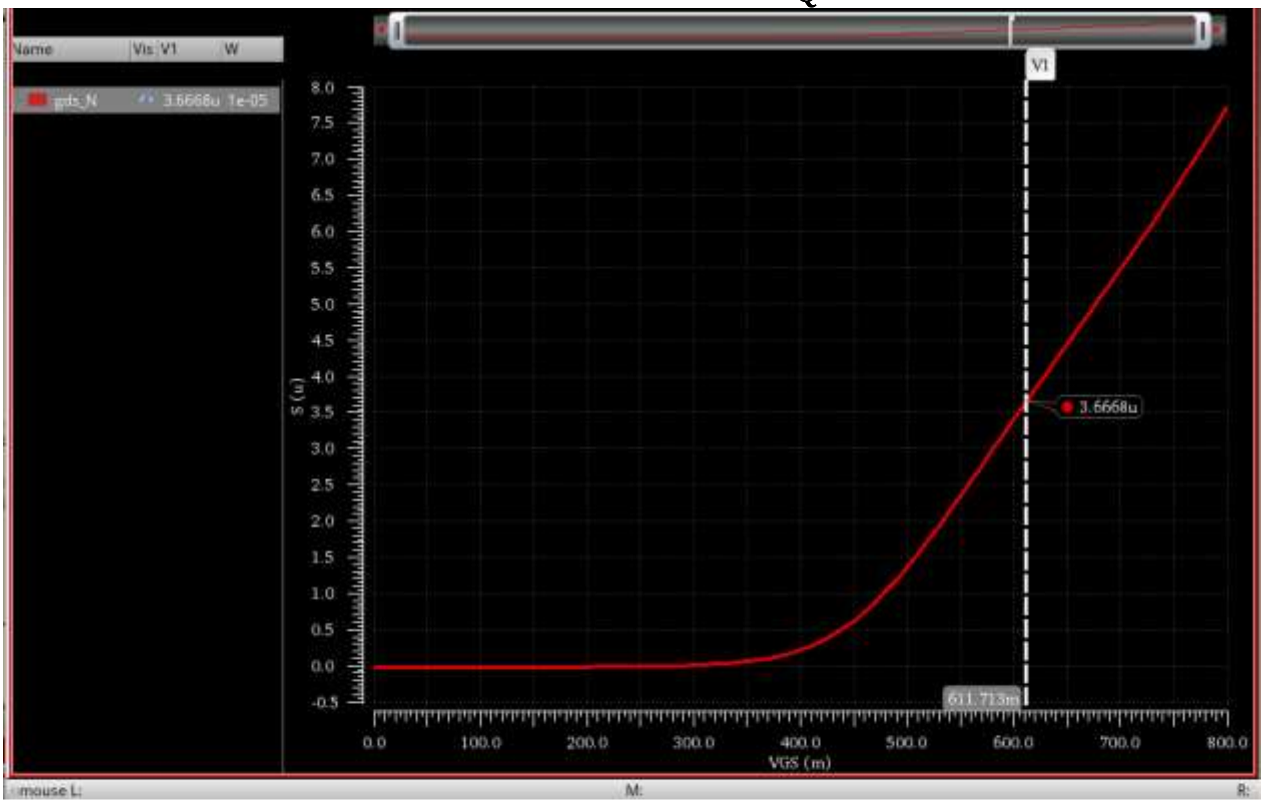
Plot g_{ds} vs V_{GS}. Find its Values at V_{GS_Q} For M_1 = PMOS.



$@V_{GS_Q} = 607.2124\ \text{mV} \rightarrow g_{ds_X} = 914.349\ \text{nS} \rightarrow r_o = \frac{1}{g_{ds_x}} = 1.1\ \text{M}\Omega$

</td>
</tr>
<tr>
<td>

Plot g_{ds} vs V_{GS}. Find its Values at V_{GS_Q} For M_2 = NMOS.



$@V_{GS_Q} = 611.713\ \text{mV} \rightarrow g_{ds_X} = 3.6668\ \mu\text{S} \rightarrow r_o = \frac{1}{g_{ds_x}} = 0.273\ \text{M}\Omega$

</td>
</tr>
</table>

P9	**Now back to the assumption that we made that $W = 10\ \mu m$.** **This is not the actual value that we will use for our design.** **But the good news is that I_D is always proportional to W irrespective of the operating region and the model of the MOSFET (regardless square – law is valid or no). Thus, we can use ratio and proportion (cross – multiplication) to determine the correct width at which the current will be $I_{D_Q} = 20\ \mu A$ as given in the specs. Calculate W as shown below. For $(M_1 = PMOS)$** <table><tr><th>W</th><th>I_D</th></tr><tr><td>$W_{assumed} = 10\ \mu m$</td><td>I_{D_X} @ V_Q^* (From The Chart)</td></tr><tr><td>$W_{required} = ?$</td><td>$I_{D_Q} = 20\ \mu A$ (From The Specs)</td></tr></table> <table><tr><th>W</th><th>I_D</th></tr><tr><td>$W_{assumed} = 10\ \mu m$</td><td>I_{D_X} @ V_Q^* (From The Chart) $= 11.914\ \mu A$</td></tr><tr><td>$W_{required} = ?$</td><td>$I_{D_Q} = 20\ \mu A$ (From The Specs)</td></tr></table> $W_{required}P = 16.787\ \mu m$. **For $(M_1 = PMOS)$.**
P 10	**Now we are almost done with the design of the amplifier.** **Note that g_m is also proportional to W as long as V_{ov} is constant.** **On the other hand, $r_o = \frac{1}{g_{ds}}$ is inversely proportional to W (I_D) as long as L is constant. Before leaving this part, calculate g_{m_Q} and g_{ds_Q} using ratio and proportion (cross multiplication).** <table><tr><th>g_m</th><th>W</th></tr><tr><td>$g_{m_X} = 119.083\ \mu S.$</td><td>$W_{assumed} = 10\ \mu m$</td></tr><tr><td>$g_{mQ_{required}} = ?$</td><td>$W_{required} = 16.787\ \mu m$</td></tr></table> $g_{mQ_{required}}P = 199.905\ \mu S.$ <table><tr><th>g_{ds}</th><th>W</th></tr><tr><td>$g_{ds_X} = 914.349\ nS.$</td><td>$W_{assumed} = 10\ \mu m$</td></tr><tr><td>$g_{ds_{required}} = ?$</td><td>$W_{required} = 16.787\ \mu m$</td></tr></table> $g_{dsQ_{required}}P = 1534.918\ nS \rightarrow r_o = 0.652\ M\Omega$

P9	**Now back to the assumption that we made that $W = 10\ \mu m$.** **This is not the actual value that we will use for our design.** **But the good news is that I_D is always proportional to W irrespective of the operating region and the model of the MOSFET (regardless square – law is valid or no). Thus, we can use ratio and proportion (cross – multiplication) to determine the correct width at which the current will be $I_{D_Q} = 20\ \mu A$ as given in the specs. Calculate W as shown below. For $(M_2 = NMOS)$**

W	I_D
$W_{assumed} = 10\ \mu m$	I_{D_X} @ V_Q^* (From The Chart)
$W_{required} = ?$	$I_{D_Q} = 20\ \mu A$ (From The Specs)

W	I_D
$W_{assumed} = 10\ \mu m$	I_{D_X} @ V_Q^* (From The Chart) $= 46.5303\ \mu A$
$W_{required} = ?$	$I_{D_Q} = 20\ \mu A$ (From The Specs)

$W_{required}N = 4.298\ \mu m$. **For $(M_2 = NMOS)$**

P 10	**Now we are almost done with the design of the amplifier.** **Note that g_m is also proportional to W as long as V_{ov} is constant.** **On the other hand, $r_o = \frac{1}{g_{ds}}$ is inversely proportional to W (I_D) as long as L is constant. Before leaving this part, calculate g_{m_Q} and g_{ds_Q} using ratio and proportion (cross multiplication).**

g_m	W
$g_{m_X} = 465.137\ \mu S.$	$W_{assumed} = 10\ \mu m$
$g_{mQ_{required}} = ?$	$W_{required} = 4.298\ \mu m$

$g_{mQ_{required}}N = 199.916\ \mu S.$

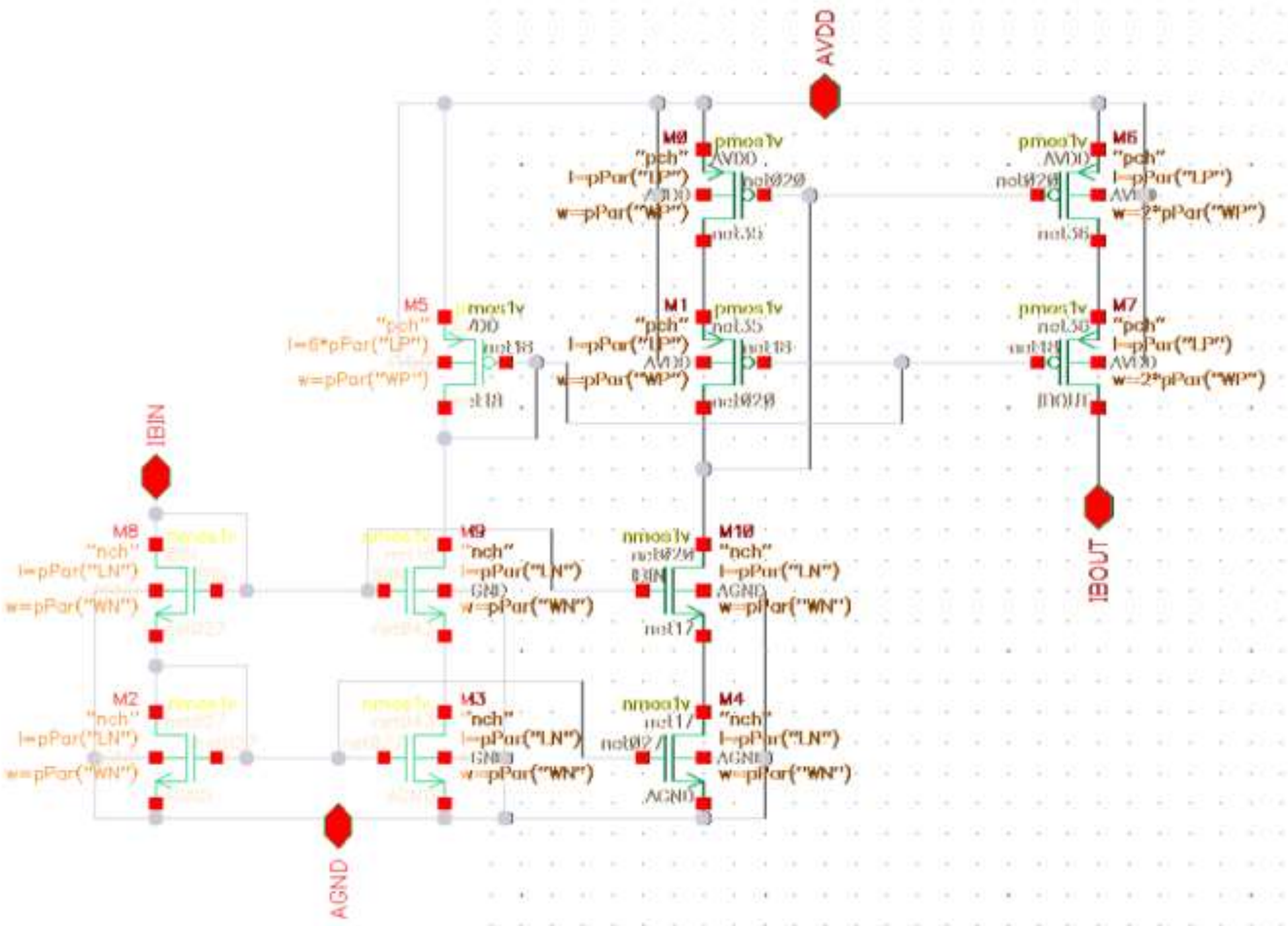
g_{ds}	W
$g_{ds_X} = 3.6668\ \mu S.$	$W_{assumed} = 10\ \mu m$
$g_{ds_{required}} = ?$	$W_{required} = 4.298\ \mu m$

$g_{dsQ_{required}}N = 1.576\ \mu S \rightarrow r_o = 0.635\ M\Omega$

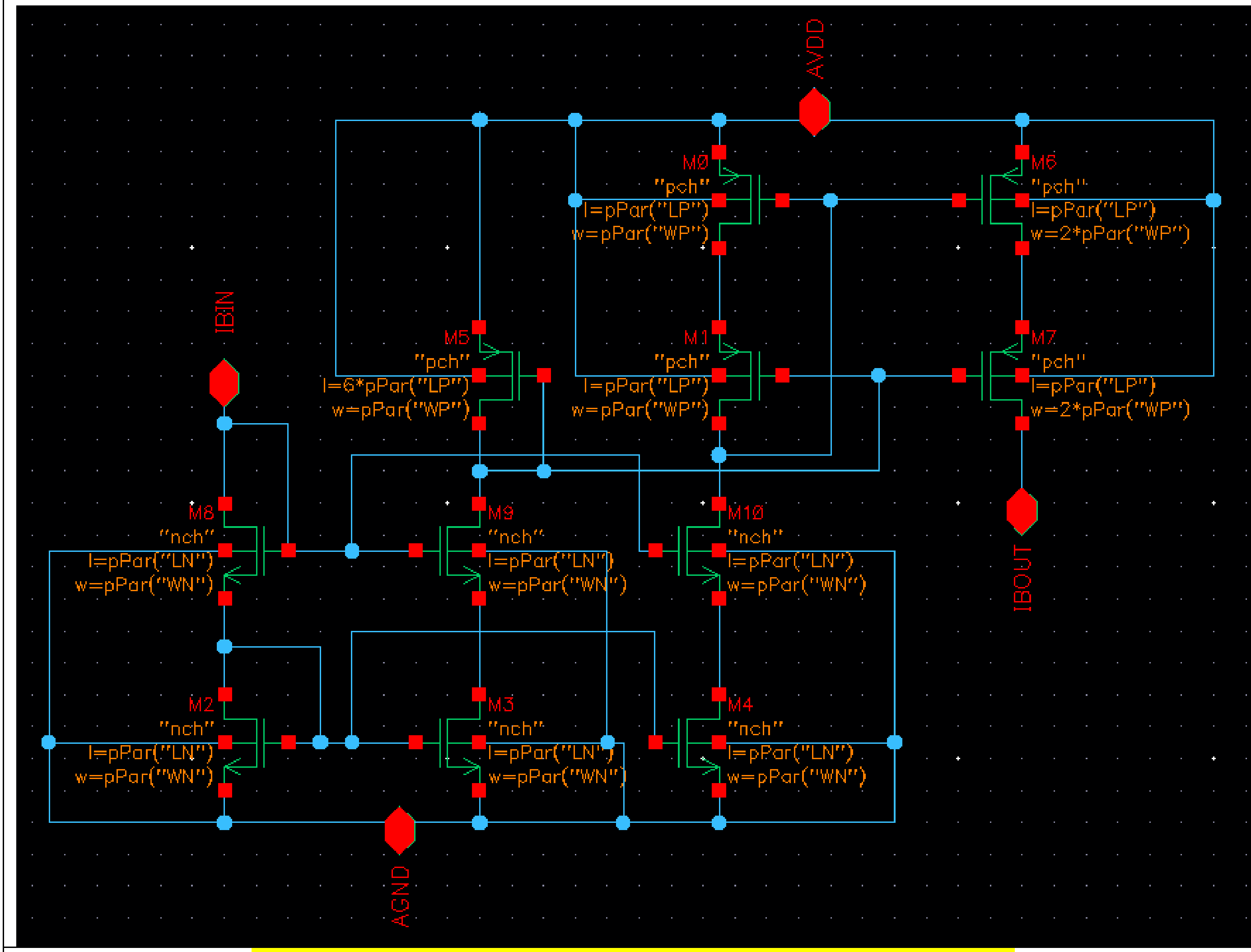
Part 2

Current Mirror

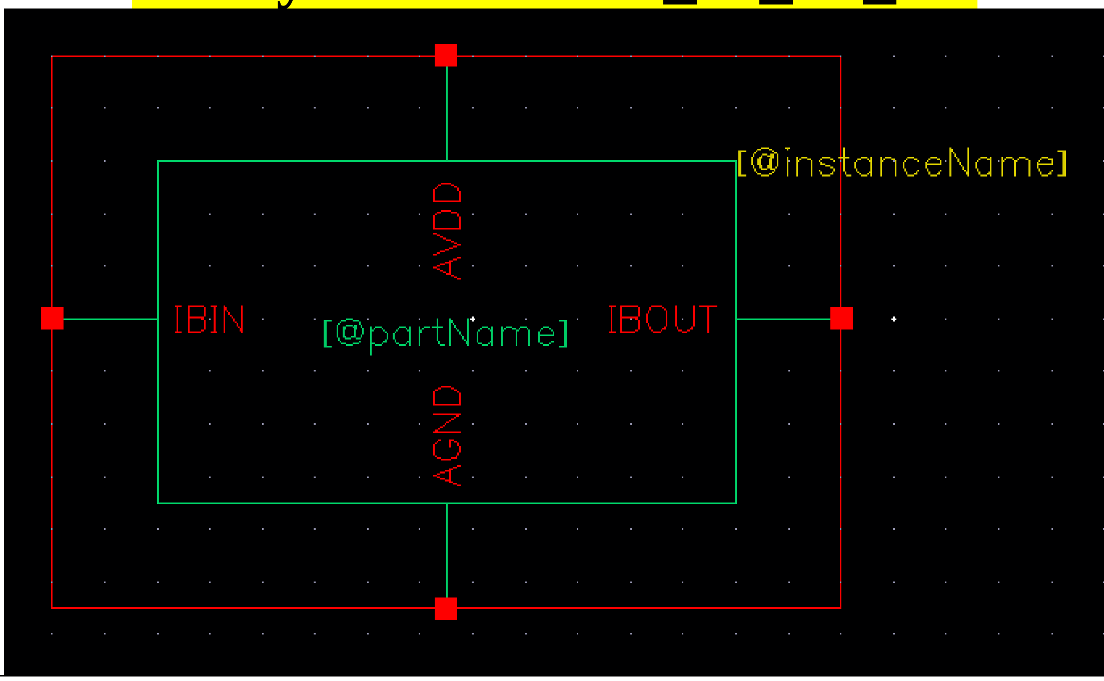
Circuit



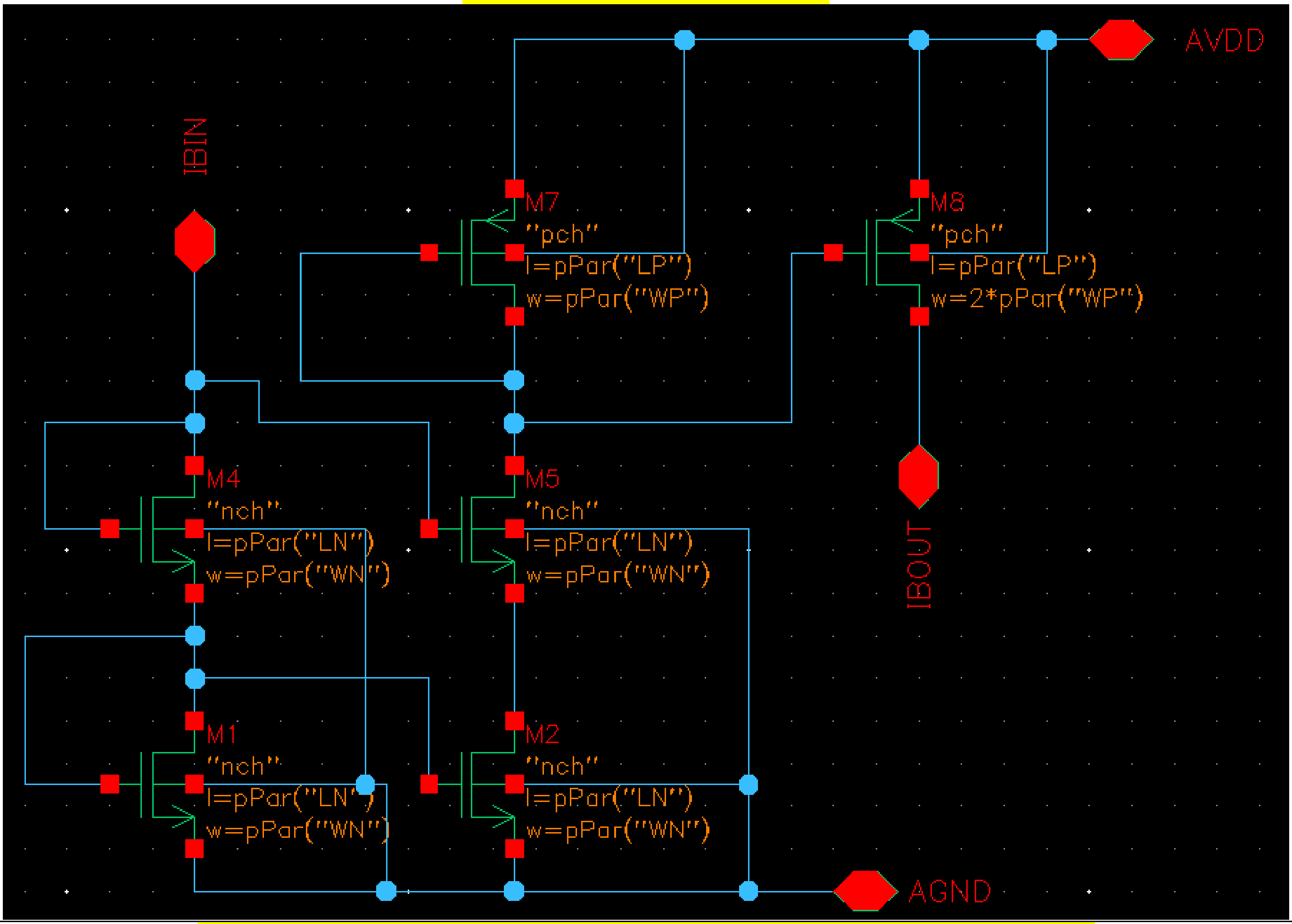
P1, P2, P3, P4: Schematic



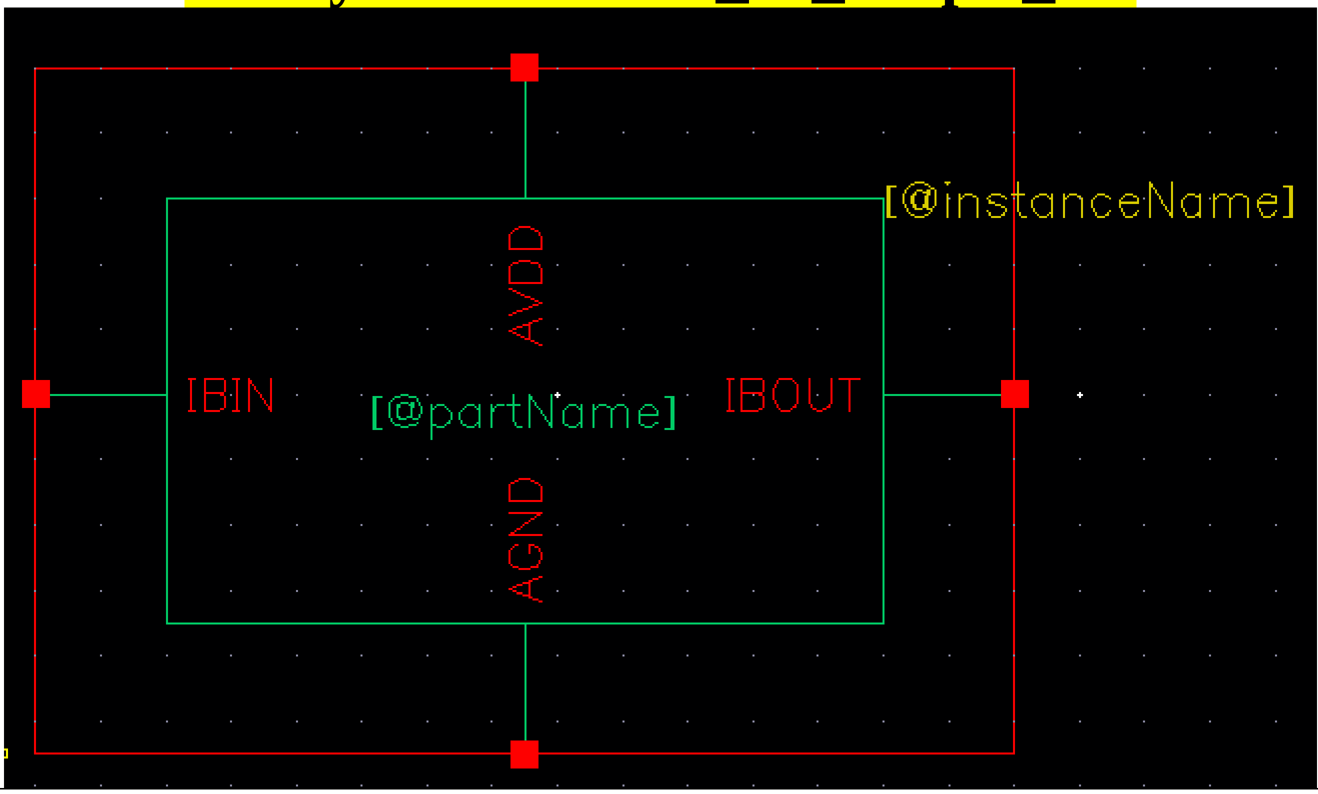
P5: Symbol For lab_05_ws_cm



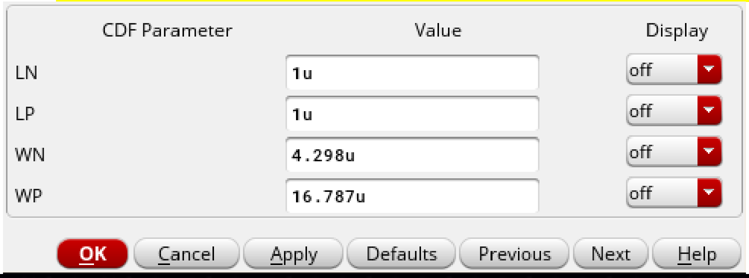
P6: Schematic

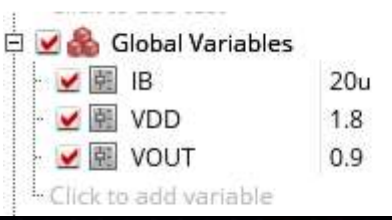


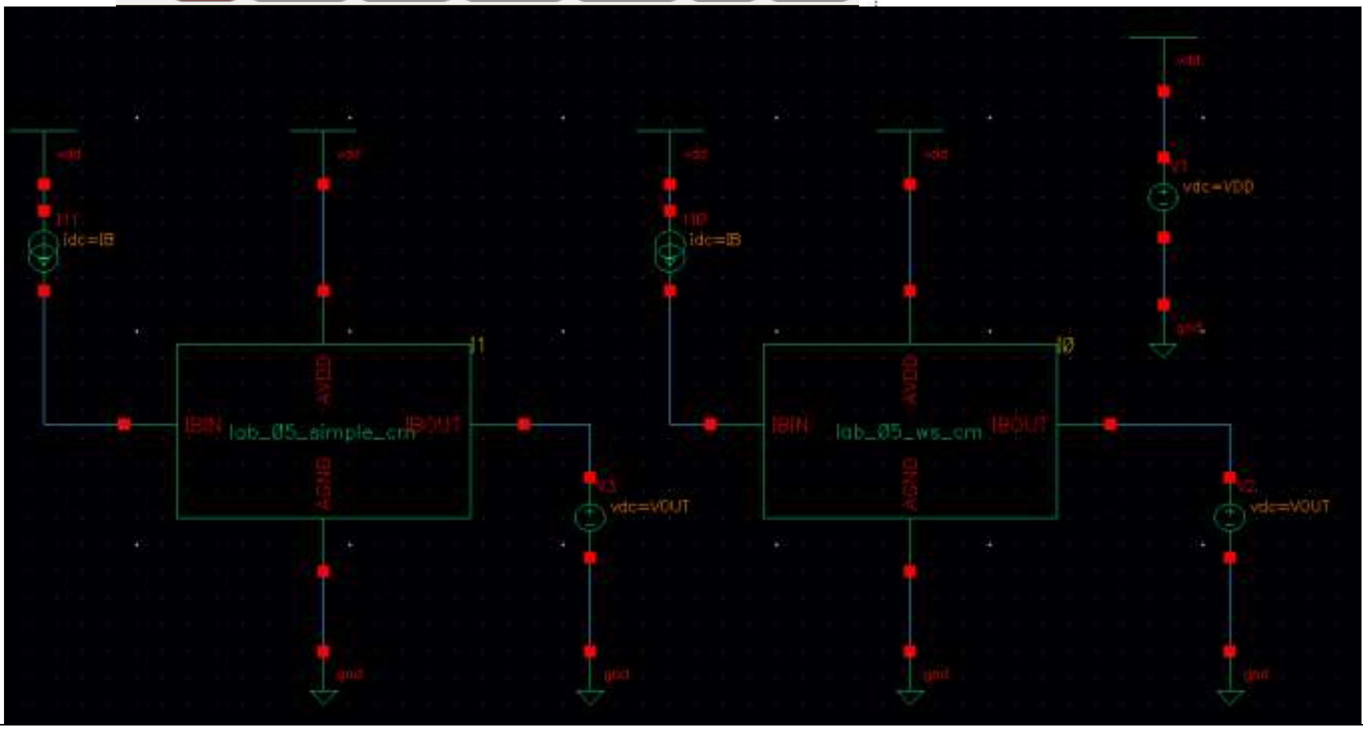
P7: Symbol For lab_05_simple_cm



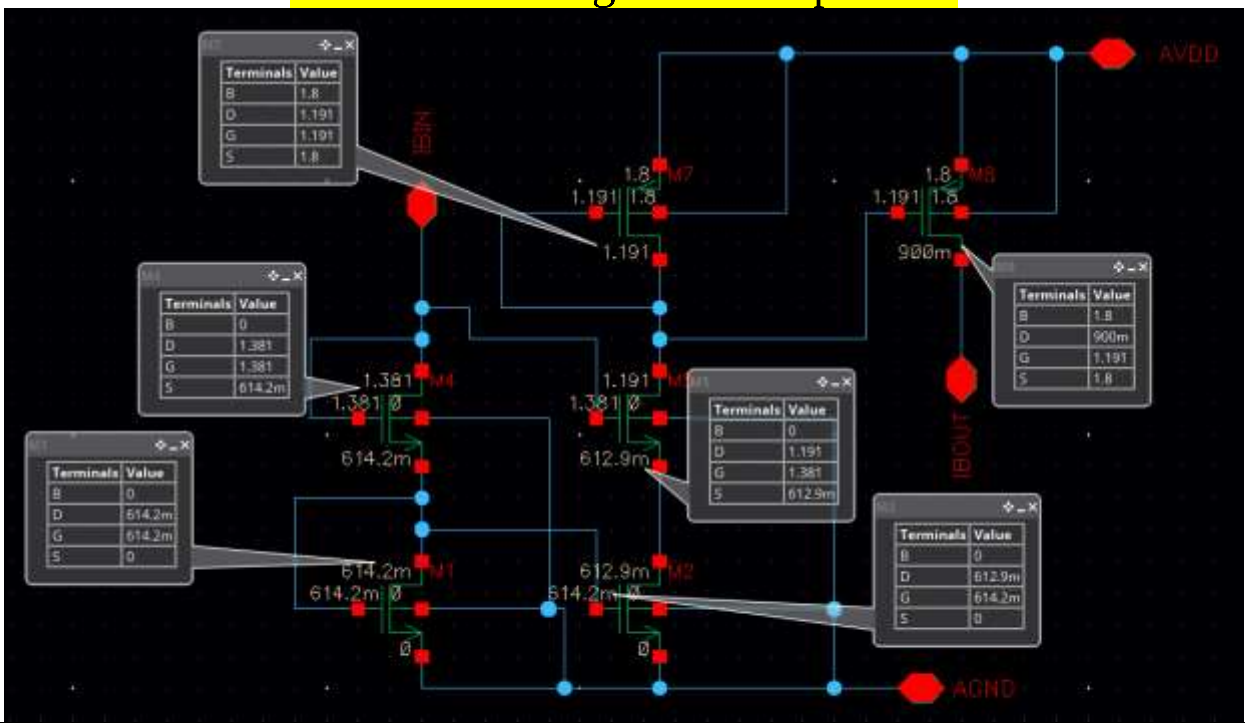
P8, P9, P10: Schematic lab_05_cm_tb





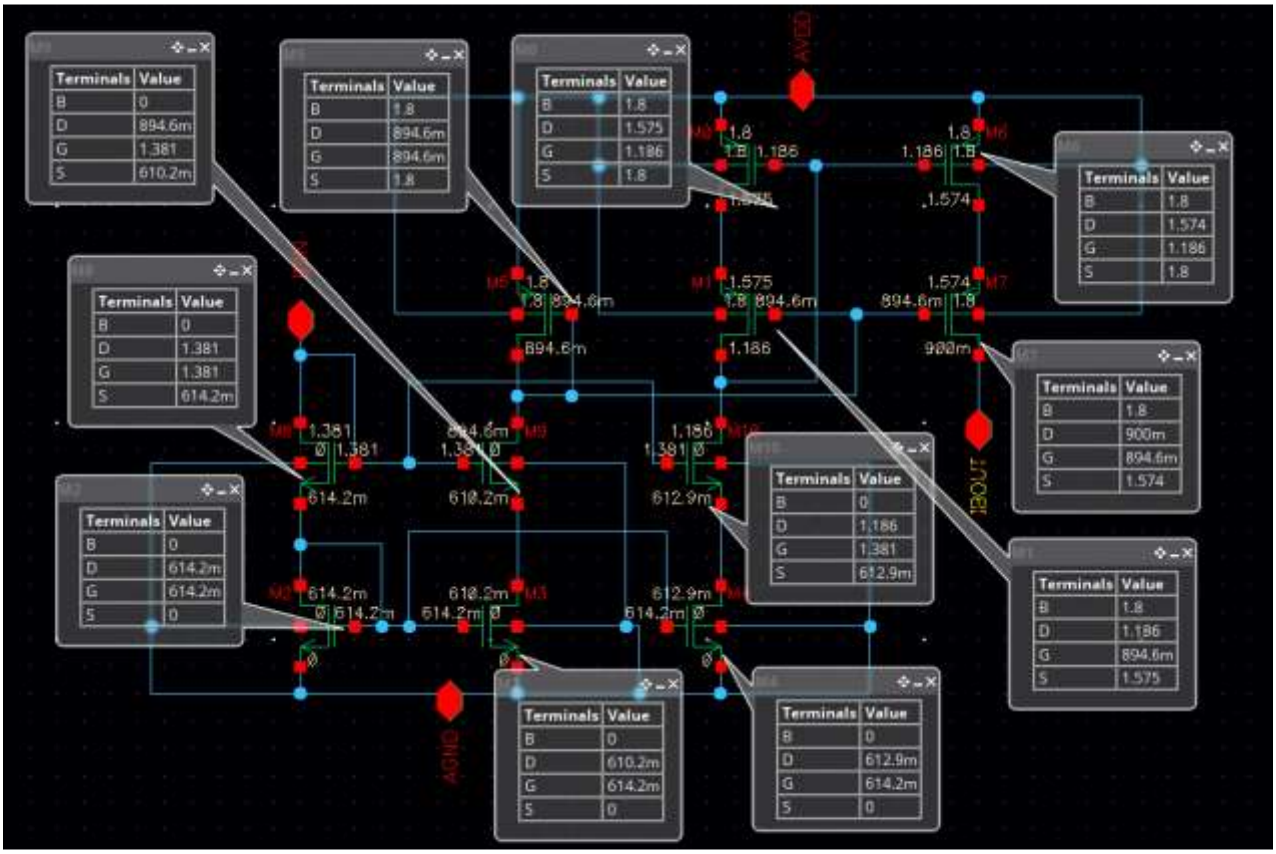


Report The Following: -

Q1	DC Node Voltages for Simple CM 

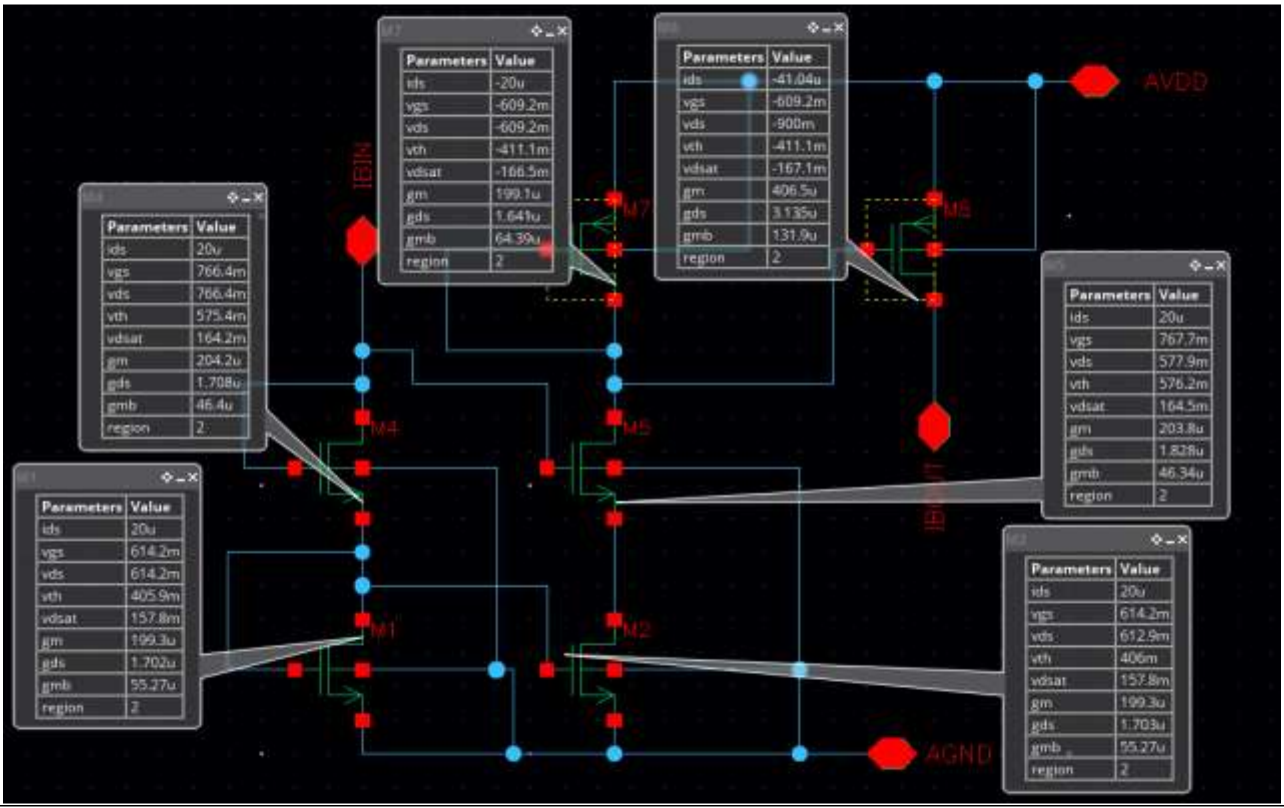
Q1

DC Node Voltages for WS CM



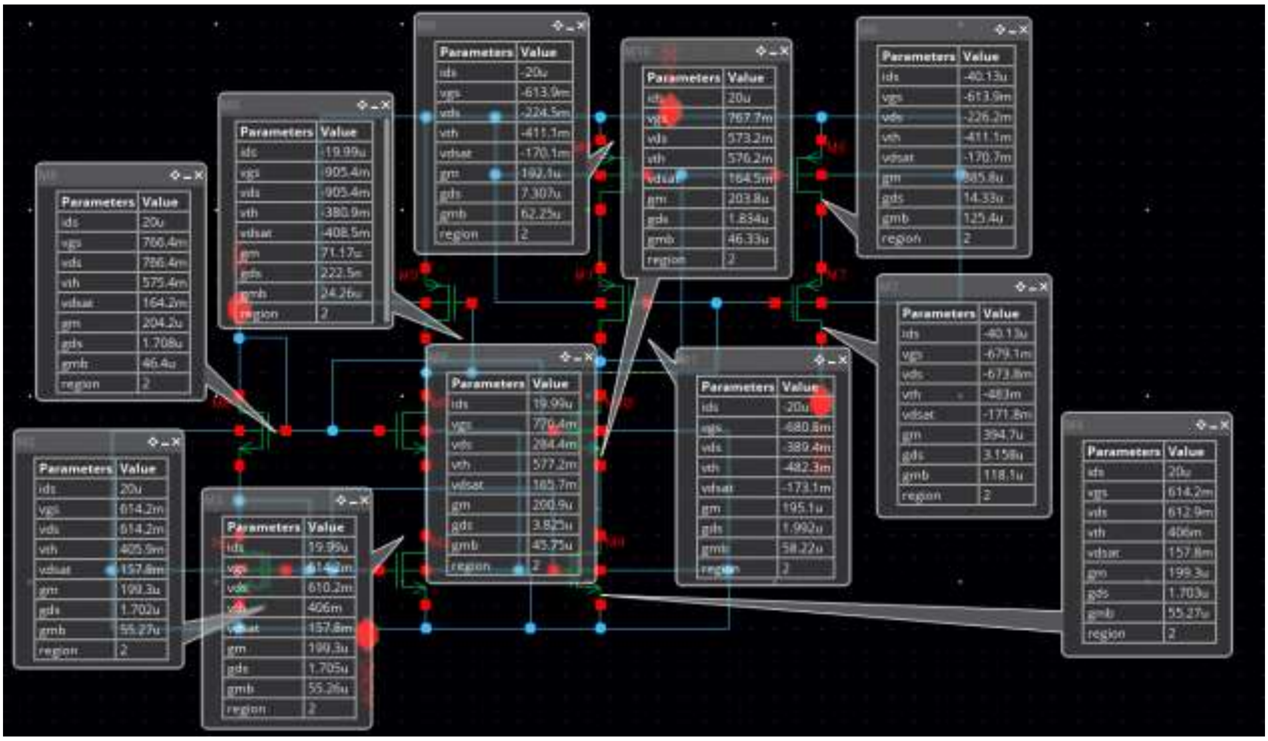
Q2

DC OP for Simple CM



Q2

DC OP for WS CM



Q3

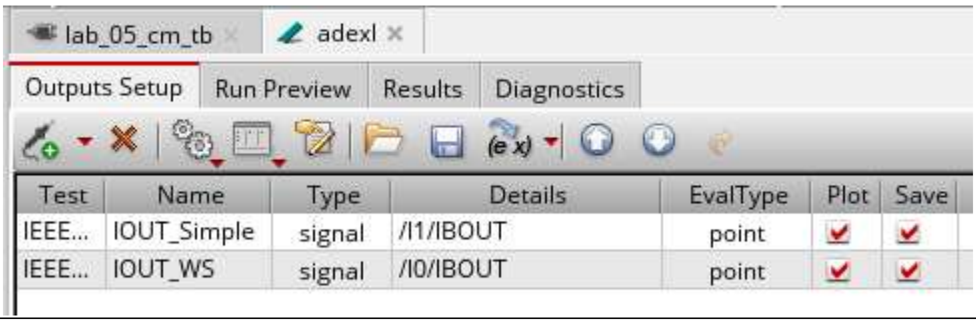
- Check that all transistors have V_{GS}, g_m and g_{ds} as designed in Part 1.
  - **Yes, All Transistors Have V_{GS}, g_m and g_{ds} as designed in Part 1.**

Q4

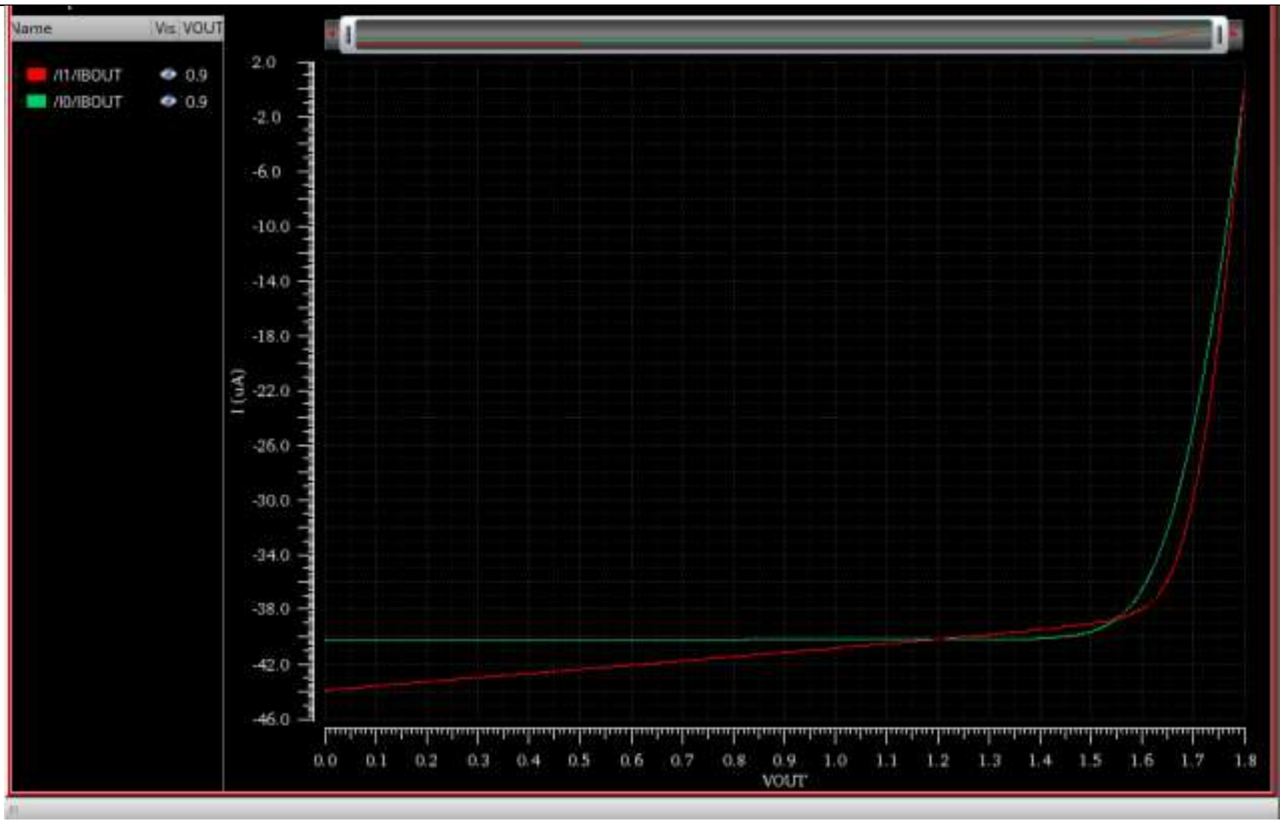
- Are all transistors operating in saturation?
  - **All transistors operate in region 2 (saturation) as shown in the schematic above.**

Q5

Perform DC sweep (not parametric sweep) using $V_{OUT} = 0{:}\,10m{:}\,V_{DD}$. Report IBOUT vs VOUT for the two CMs overlaid in the same plot.



Q5



Comment on the difference between the two circuits.

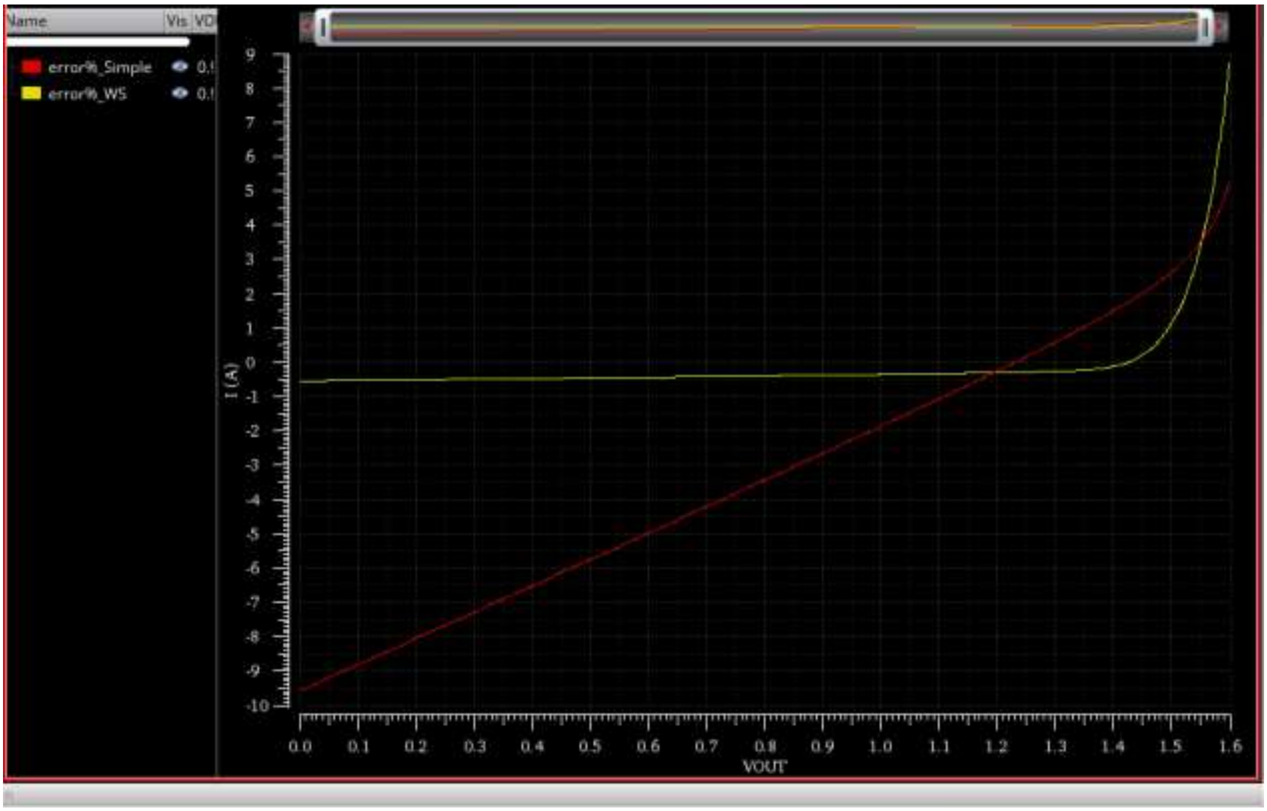
- **In WS (Wide Swing) Circuit (Green Curve) when Cascoded is added to the circuit it Gives the Accurate Current Mirroring Ratio and its Change with V_{ds} is Neglected.**
  While in Simple Circuit (Red Curve) it doesn't gives the Accurate Current Ratio, change of the output current with the output voltage because V_{ds} is changing.
- **for the case of cascoded transistors $V_{ds_1} = V_{ds_2}$, and if they have the same length, there're won't be a change in current mirroring ratio.**

IBOUT of the simple CM is exactly equal to IBIN*2 at a specific value of VOUT. Why?

- **Yes, Because at the Point $(V_{out} = 1.19\ V) = V_D$ of M_8 and to have an exact mirroring ratio, it should be equal to that of M7; this is the case at 1.19 V. From the node voltages shown above, the drain of M7 is 1.19 V.**

Percent of error in IBOUT vs VOUT (ideal IBOUT should be IBIN*2) for the two CMs in the current mirror operating region ($\mathbf{V_{OUT} = 0}$ to $\mathbf{V_{DD} - V^{*}}$) overlaid in the same plot.

Q6

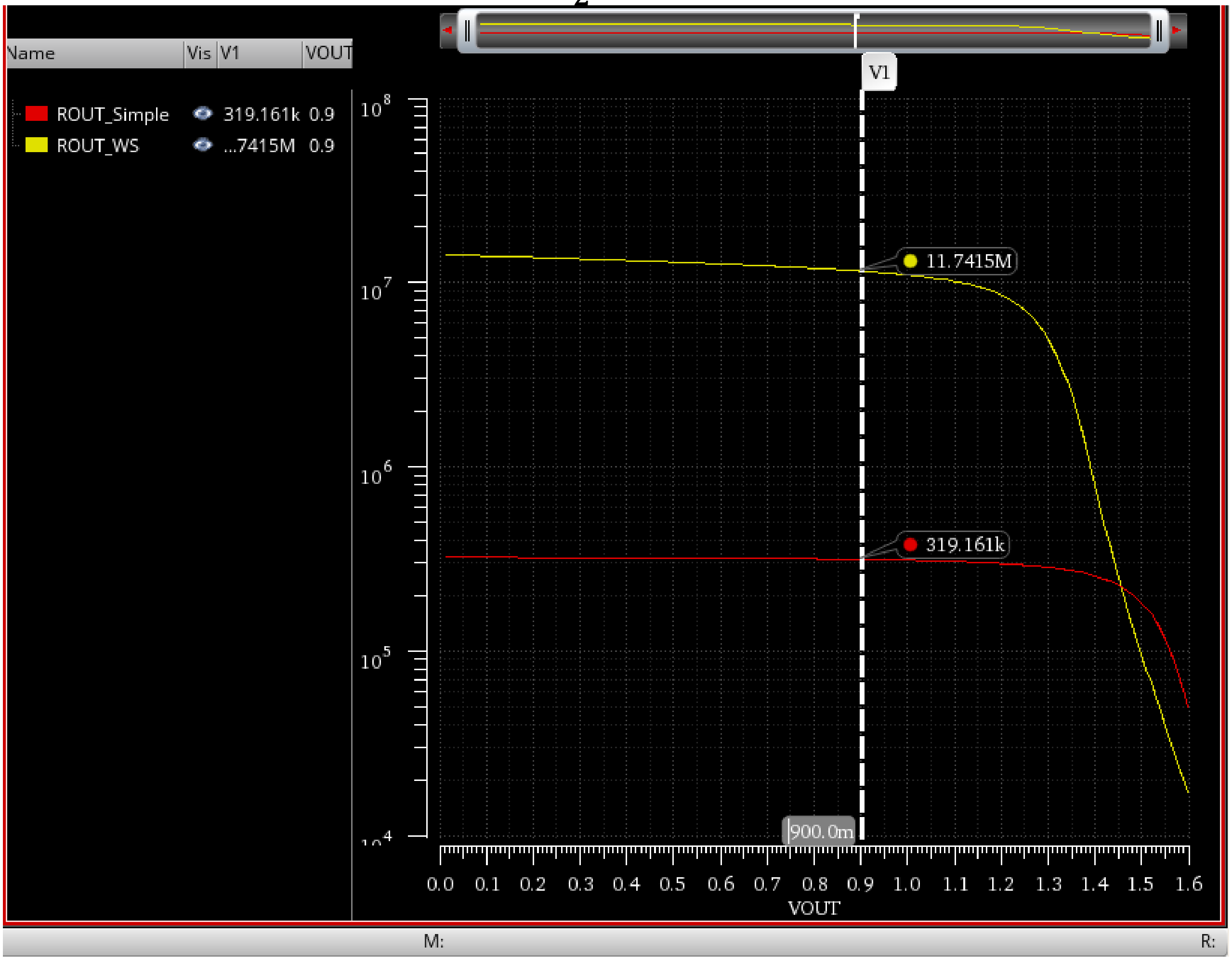


Comment on the difference between the two circuits.

- **In WS (Wide Swing) Circuit (Blue Curve) when Cascoded is added to the circuit it gives better performance and delivers more accurate current mirroring ratio as the percentage of error is 0 for the region of operation ($\mathbf{0}$ to $\mathbf{V_{DD} - V^{*} = 0{:}\,1.6\ V}$). This refers to the same reason mentioned before $\left(\mathbf{V_{ds_1} = V_{ds_2}}\right)$, While in Simple Circuit (Pink Curve) it doesn't gives the Accurate Current Ratio.**

Q7

Rout vs VOUT (take the inverse of the derivative of IBOUT plot) for the two CMs in the current mirror operating region.
(V_{OUT} = 0 to $V_{DD} - V^*$) overlaid in the same plot. Use log scale on the y-axis. Add a cursor at $V_{OUT} = \frac{VDD}{2}$



- **Comment on the difference between the two circuits.**

  - **From the above graph R_{out} of the WS circuit is higher than that of the simple current mirroring circuit, and the current is more stable at 2* IBOUT IDEAL for the WS circuit.**

- **Comment on the difference between the two circuits.**

  - **Rout $= \frac{dv}{di}$, Higher Rout gives little changes, as drain voltage is increasing; as a result, the Rout is decreasing.**

Q8	**Analytically calculate Rout of both circuits at $\mathbf{VOUT} = \frac{\mathbf{VDD}}{\mathbf{2}} = \mathbf{0.9\ V}$. Compare with simulation results in a table.** **Analytical: In WS Circuit** $\mathbf{R_{out} = r_{o_1}\left(1 + g_m r_{o_2}\right) + r_{0_2} = 9.1\ M\Omega}$ **In Simple Circuit** $\mathbf{R_{out} = r_o = 318.979\ k\Omega}$ **From Simulation:** **As Shown Above in the Graph in Q7** $\mathbf{R_{out}(\mathit{WS}) = 11.7415\ M\Omega}$ $\mathbf{R_{out}(Simple) = 319.616\ k\Omega}$