Verilog HDL

Assignment 1

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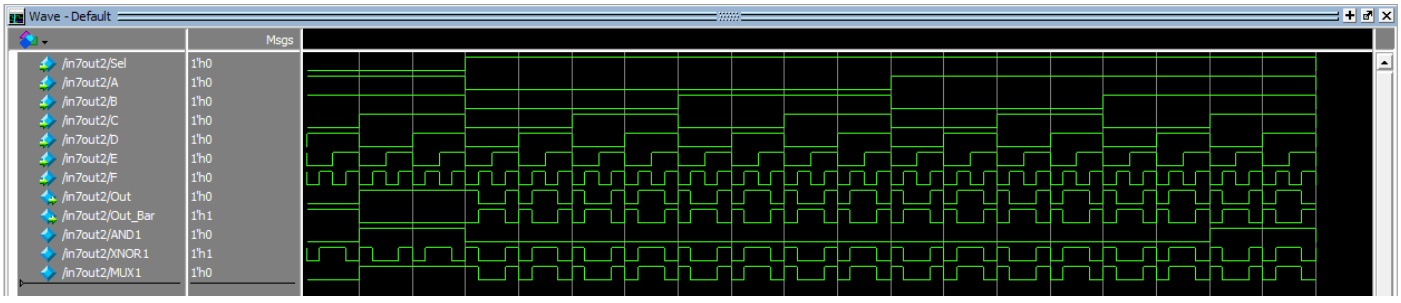
Question 1

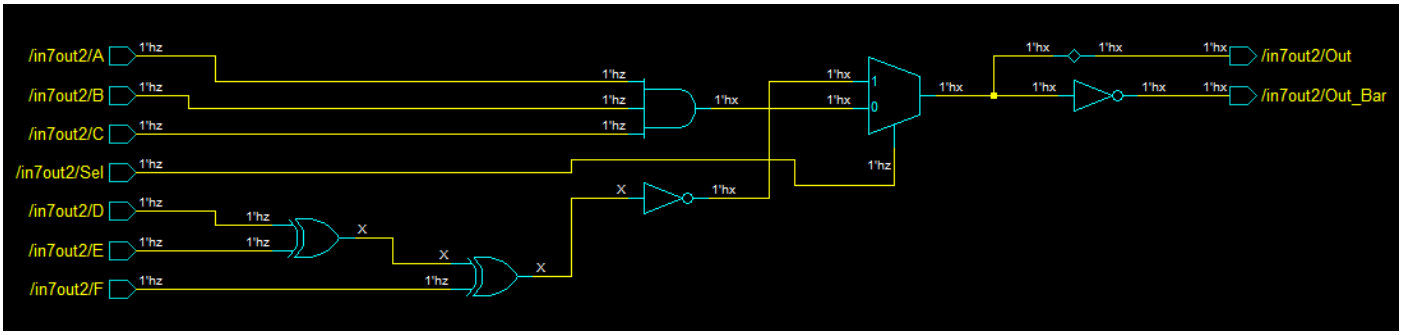
DESIGN HAS 7 INPUTS AND 2 OUTPUTS.

Verilog Code:

```
module in7out2 (A, B, C, D, E, F, Sel, Out, Out_Bar);

input A, B, C, D, E, F, Sel;
output Out, Out_Bar;

wire AND1, XNOR1, MUX1;

assign AND1 = (A & B & C);
assign XNOR1 = ~(D ^ E ^ F);

assign MUX1 = (Sel == 1)? XNOR1 : AND1;

assign Out = MUX1;
assign Out_Bar = ~MUX1;

endmodule
```

Waveform:





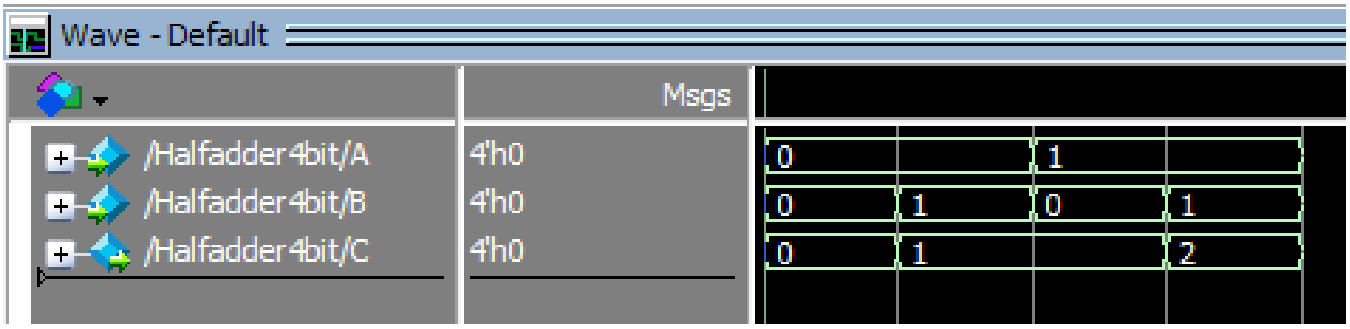
Question 2

4 - Bit Adder using addition Operator

Verilog Code:

```
module Halfadder4bit (A, B, C);

input [3: 0] A, B;
output [3: 0] C;

assign C = A + B;

endmodule
```

Waveform:



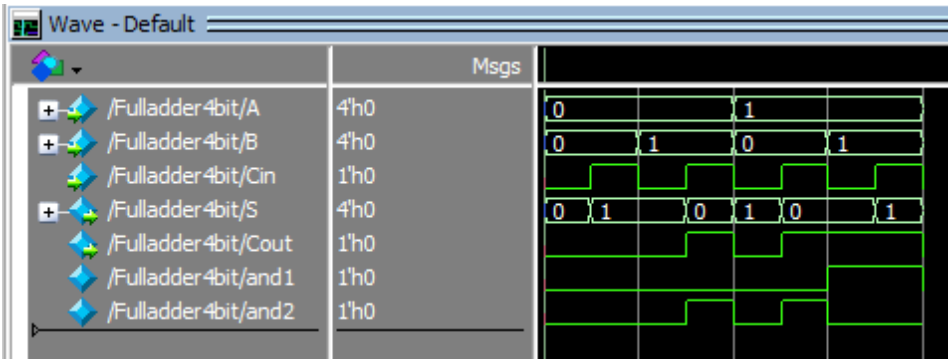
Question 3

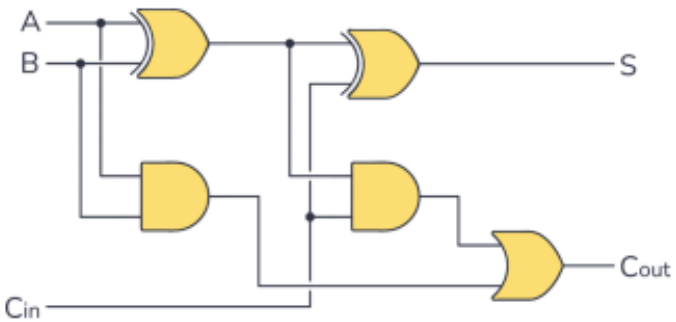
4 - Bit Adder using the Bitwise Operators

Verilog Code:

```
module Fulladder4bit (A, B, Cin, S, Cout);

input [3: 0] A, B;
input Cin;
output [3: 0] S;
output Cout;

wire and1, and2;

assign and1  =  A & B;
assign and2  =  (A ^ B) & Cin;
assign S  =  A ^ B ^ Cin;
assign Cout  =  and1 | and2;

endmodule
```

Waveform:





Question 4

2 × 4 Decoder using Conditional Operator

Verilog Code:

```
module Dec2to4(A, D);

input [1: 0] A;
output [3: 0] D;

assign D = (A == 2'b00)? 4'b0001 : (A == 2'b01)? 4'b0010 :
                  (A == 2'b10)? 4'b0100 : 4'b1000;

endmodule
```

Waveform:

A_1	A_0	D_3	D_2	D_1	D_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

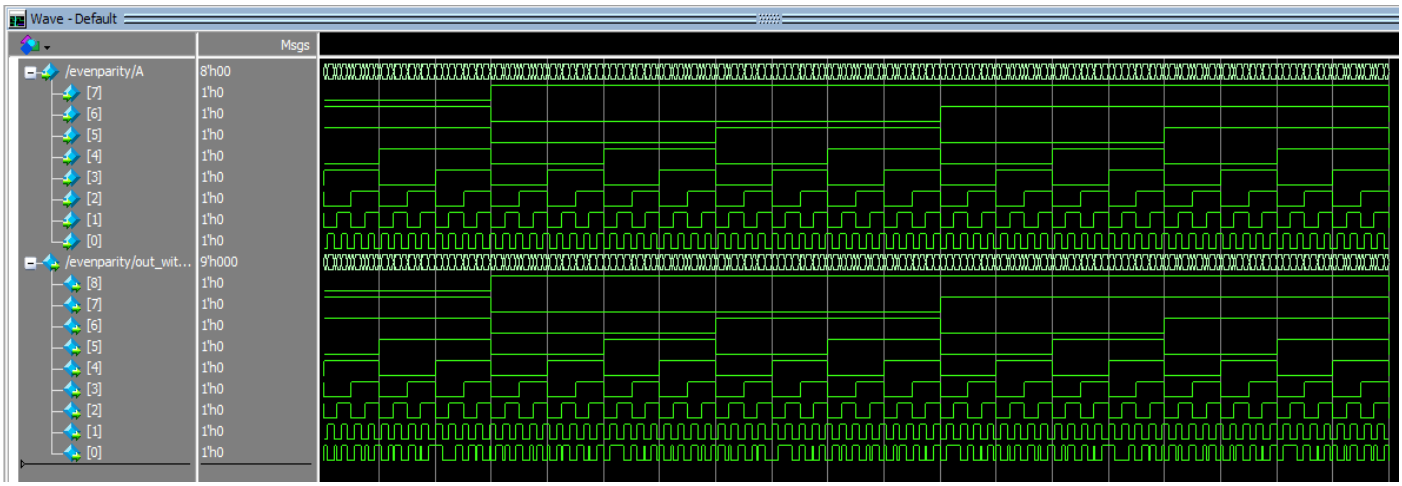
Question 5

Even Parity Generator Module

Verilog Code:

```
module evenparity (A, out_with_parity);

input [7: 0] A;
output [8: 0] out_with_parity;

assign out_with_parity  =  {A, ^A};

endmodule
```

Waveform:



Question 6

Comparator Compares 2 inputs using Conditional Operator

Verilog Code:

```
module comparator (A, B, ALTA, AGTB, AEQB);

input [3: 0] A, B;
output ALTA, AGTB, AEQB;

assign ALTA = (A < B)? 1'b1 : 1'b0;
assign AGTB = (A > B)? 1'b1 : 1'b0;
assign AEQB = (A == B)? 1'b1 : 1'b0;

endmodule
```

Waveform: