Verilog HDL

Assignment 1 Extended

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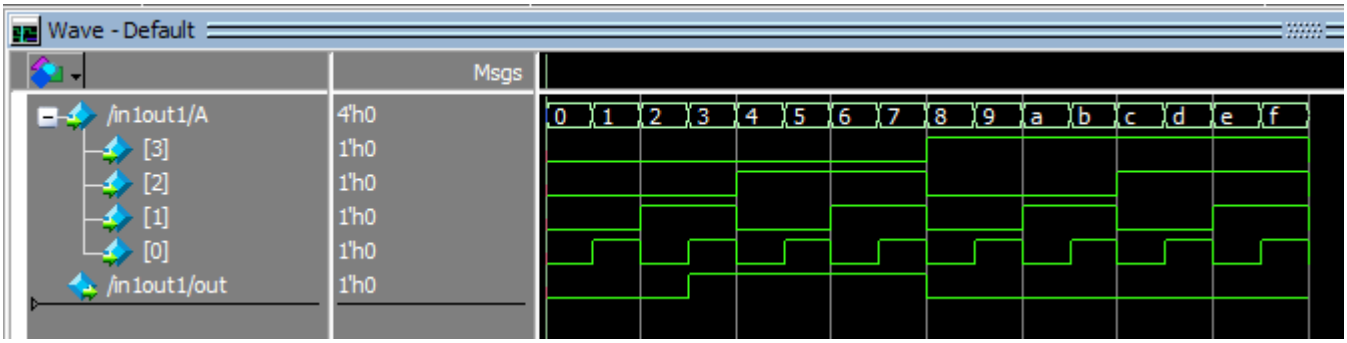
Question 1

Verilog Code:

```
module in1out1 (A, out);

input [3: 0] A;
output out;

assign out = (A > 4'b0010 && A < 4'b1000)? 1'b1 : 1'b0;

endmodule
```

Waveform:

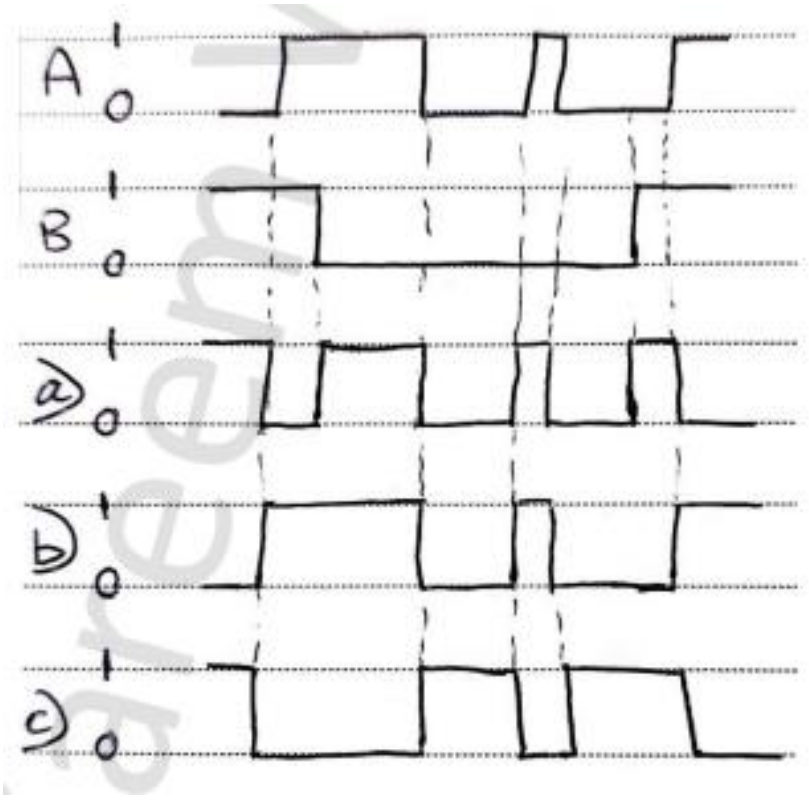


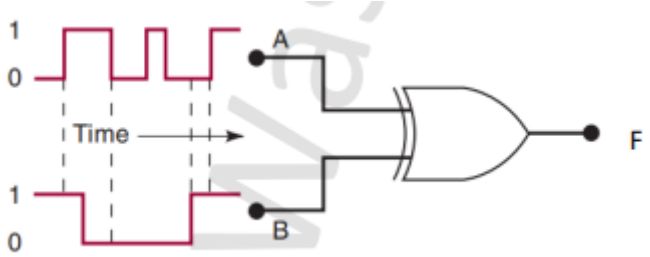
Question 2

Verilog Code:

```
module Question2_EXT (A, B, F);

input A, B;
output F;

assign F = A ^ B;

endmodule
```

Waveform:



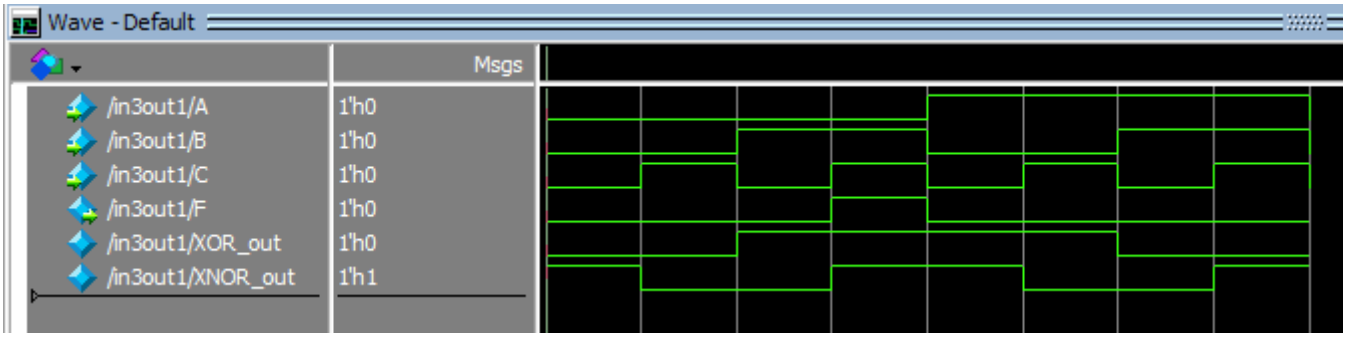


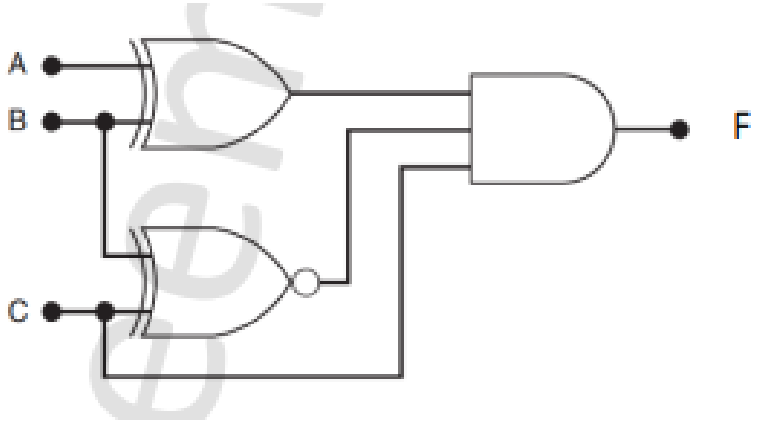
Question 3

Verilog Code:

```
module in3out1 (A, B, C, F);

input A, B, C;
output F;

wire XOR_out, XNOR_out;

assign XOR_out  =  A ^ B;
assign XNOR_out  =  ~(B ^ C);

assign F  =  XOR_out & XNOR_out & C;

endmodule
```

Waveform:





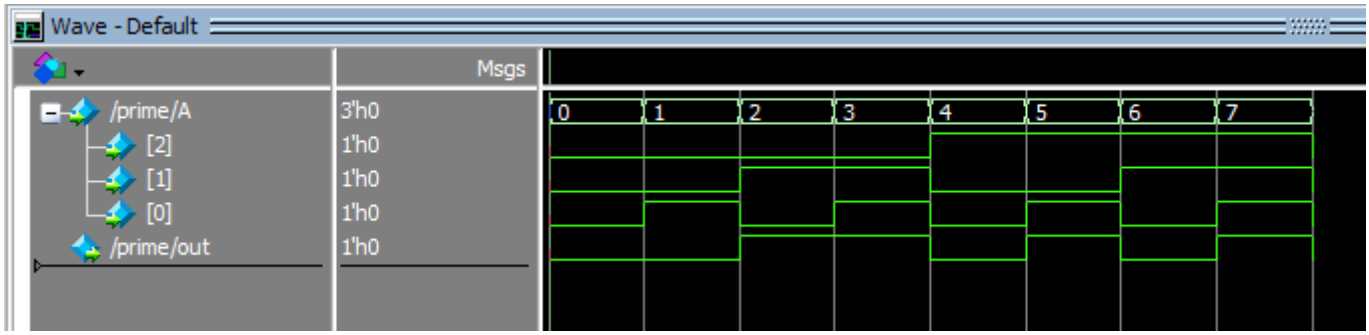
F = 1 when C is HIGH, B is HIGH, and A is LOW

Question 4

Verilog Code:

```
module prime (A,out);

input [2:0] A;
output out;

assign out = (~A[2] & A[1]) | (A[2] & A[0]);

endmodule
```

Waveform:

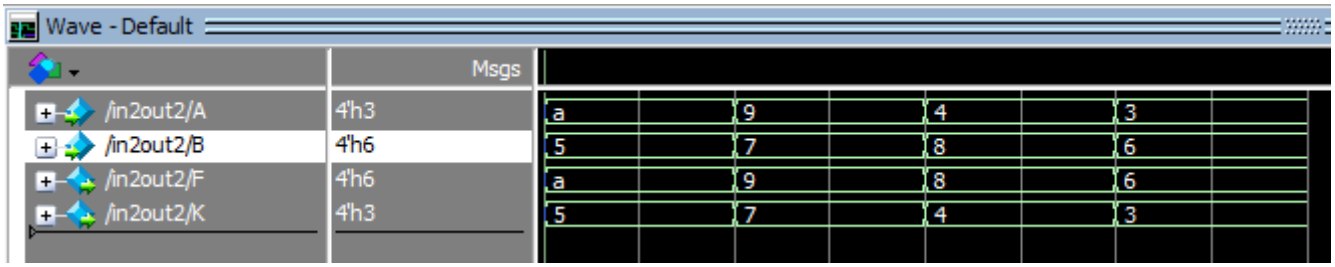


Question 5

Verilog Code:

```
module in2out2 (A, B, F, K);

input [3:0] A, B;
output [3:0] F, K;

assign F = (A >= B)? A : B;
assign K = (A <= B)? A : B;

endmodule
```

Waveform:

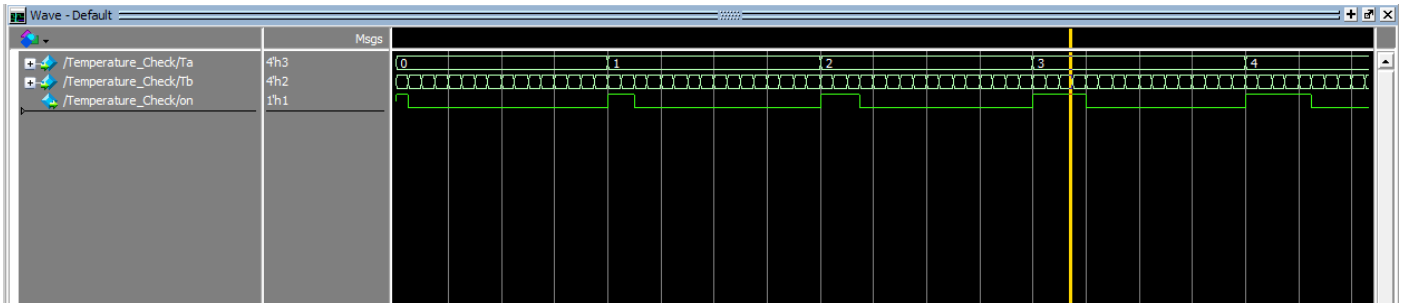


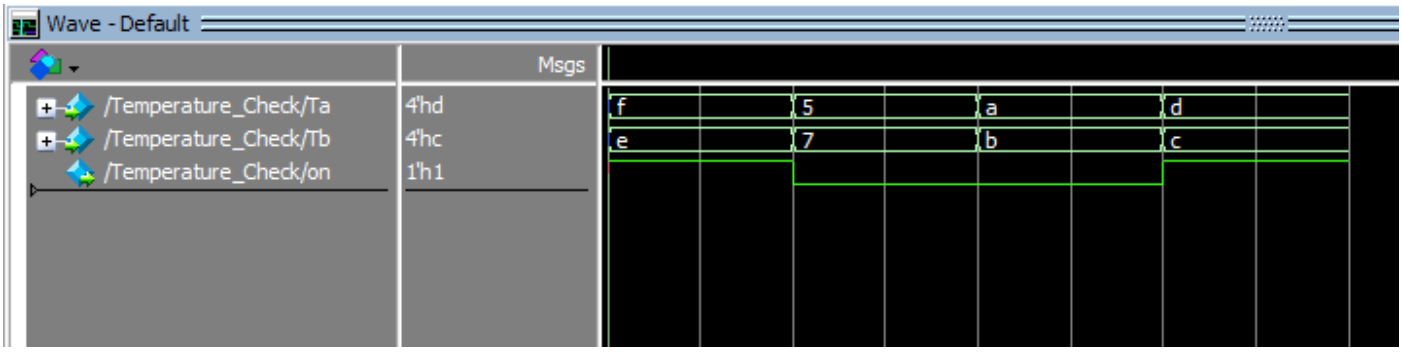
Question 6

Verilog Code:

```
module Temperature_Check (Ta, Tb, on);

input [3: 0] Ta, Tb;
output on;

assign on = (Tb <= Ta)? 1'b1 : 1'b0;

endmodule
```

Waveform:





Question 7

Verilog Code:

```
module ALU1bit (A, B, Ainvert, Binvert, CarryIn, Operation, CarryOut, Result);

input A, B, Ainvert, Binvert, CarryIn;
input [1: 0] Operation;
output CarryOut, Result;

wire MUX1_out, MUX2_out, AND_out, OR_out, Adder_out;

assign MUX1_out = (Ainvert == 0)? A : ~A;
assign MUX2_out = (Binvert == 0)? B : ~B;
assign AND_out = MUX1_out & MUX2_out;
assign OR_out = MUX1_out | MUX2_out;
assign {CarryOut, Adder_out} = MUX1_out + MUX2_out + CarryIn;

assign Result = (Operation == 0)? AND_out : (Operation == 1)? OR_out
            : Adder_out;

endmodule
```

Waveform: