



# **Verilog HDL**

## **Assignment 5**

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# Question 1

## ALSU

### Verilog Code:

```
module ALSU (A, B, opcode, cin, serial_in, direction, red_op_A, red_op_B, bypass_A, bypass_B, clk, rst, out, leds);
parameter INPUT_PRIORITY = "A";
parameter FULL_ADDER = "ON";
input clk, rst, cin, serial_in, red_op_A, red_op_B, bypass_A, bypass_B, direction;
input [2:0] A, B, opcode;
output reg [15:0] leds;
output reg [5:0] out;
reg [2:0] A_FF, B_FF, opcode_FF;
reg cin_FF, serial_in_FF, red_op_A_FF, red_op_B_FF, bypass_A_FF, bypass_B_FF, direction_FF;
always @(posedge clk or posedge rst) begin
    if (rst) begin
        A_FF <= 0; B_FF <= 0; opcode_FF <= 0; cin_FF <= 0; serial_in_FF <= 0; red_op_A_FF <= 0;
        red_op_B_FF <= 0; bypass_A_FF <= 0; bypass_B_FF <= 0; direction_FF <= 0;
    end begin
        A_FF <= A; B_FF <= B; opcode_FF <= opcode; cin_FF <= cin; serial_in_FF <= serial_in; red_op_A_FF
            <= red_op_A;
        red_op_B_FF <= red_op_B; bypass_A_FF <= bypass_A; bypass_B_FF <= bypass_B; direction_FF <
            = direction;
    end
end
always @(posedge clk or posedge rst) begin
    if (rst) begin
        out <= 0;
        leds <= 0;
    end else begin
        if ((bypass_A_FF == 1) && (bypass_B_FF == 0)) begin
            out <= A_FF; leds <= 0;
        end
        else if ((bypass_B_FF == 1) && (bypass_A_FF == 0)) begin
            out <= B_FF; leds <= 0;
        end
        else if ((bypass_A_FF == 1) && (bypass_B_FF == 1)) begin
            leds <= 0;
            case (INPUT_PRIORITY)
                "A" : out <= A_FF;
                "B" : out <= B_FF;
            endcase
        end
    end
end
```

```

case (opcode_FF)
3'b000 : begin
    if ((red_op_A_FF == 1) && (red_op_B_FF == 0)) begin
        out <= &A_FF; leds <= 0;
    end
    else if ((red_op_B_FF == 1) && (red_op_A_FF == 0)) begin
        out <= &B_FF; leds <= 0;
    end
    else if ((red_op_A_FF == 1) && (red_op_A_FF == 1)) begin
        leds <= 0;
        case (INPUT_PRIORITY)
            "A" : out <= &A_FF;
            "B" : out <= &B_FF;
        endcase
    end
    else begin
        out <= A_FF & B_FF; leds <= 0;
    end
end
3'b001 : begin
    if ((red_op_A_FF == 1) && (red_op_B_FF == 0)) begin
        out <= ^A_FF; leds <= 0;
    end
    else if ((red_op_B_FF == 1) && (red_op_A_FF == 0)) begin
        out <= ^B_FF; leds <= 0;
    end
    else if ((red_op_A_FF == 1) && (red_op_A_FF == 1)) begin
        leds <= 0;
        case (INPUT_PRIORITY)
            "A" : out <= ^A_FF;
            "B" : out <= ^B_FF;
        endcase
    end
    else begin
        out <= A_FF ^ B_FF; leds <= 0;
    end
end
3'b010 : begin
    case ({red_op_A_FF, red_op_B_FF})
        2'b01, 2'b10 : begin
            out <= 0; leds <= ~leds;
        end
        2'b00 : begin
            case (FULL_ADDER)
                "ON" : begin
                    out <= A_FF + B_FF + cin_FF; leds <= 0;
                end
                "OFF" : begin
                    out <= A_FF + B_FF; leds <= 0;
                end
            endcase
        end
    endcase
end

```

```

        end
    endcase
end
3'b011 : begin
    case ({red_op_A_FF, red_op_B_FF})
        2'b01, 2'b10, 2'b11 : begin
            out <= 0; leds <= ~leds;
        end
        2'b00 : begin
            out <= A_FF * B_FF; leds <= 0;
        end
    endcase
end
3'b100 : begin
    case ({red_op_A_FF, red_op_B_FF})
        2'b01, 2'b10, 2'b11 : begin
            out <= 0; leds <= ~leds;
        end
        2'b00 : begin
            leds <= 0;
            if (direction_FF)
                out <= {out[4:0], serial_in_FF};
            else
                out <= {serial_in_FF, out[5:1]};
            end
        end
    endcase
end
3'b101 : begin
    case ({red_op_A_FF, red_op_B_FF})
        2'b01, 2'b10, 2'b11 : begin
            out <= 0; leds <= ~leds;
        end
        2'b00 : begin
            leds <= 0;
            if (direction_FF)
                out <= {out[4:0], out[5]};
            else
                out <= {out[0], out[5:1]};
            end
        end
    endcase
end
3'b110, 3'b111 : begin
    out <= 0; leds <= ~leds;
end
endcase
end
end
endmodule

```

```

/*
module ALSU (A, B, opcode, cin, serial_in, direction, red_op_A, red_op_B, bypass_A, bypass_B, clk, rst, out, leds);
parameter INPUT_PRIORITY = "A";
parameter FULL_ADDER = "ON";
input clk, rst, cin, serial_in, red_op_A, red_op_B, bypass_A, bypass_B, direction;
input [2: 0] A, B, opcode;
output reg [15: 0] leds;
output reg [5: 0] out;
reg [2: 0] A_FF, B_FF, opcode_FF;
reg cin_FF, serial_in_FF, red_op_A_FF, red_op_B_FF, bypass_A_FF, bypass_B_FF, direction_FF;
wire invalid_red_op, invalid_opcode, invalid;
assign invalid_red_op = (red_op_A_FF | red_op_B_FF) & (opcode_FF[1] | opcode_FF[2]);
assign invalid_opcode = opcode_FF[1] & opcode_FF[2];
assign invalid = invalid_red_op | invalid_opcode;
always @(posedge clk or posedge rst) begin
    if (rst) begin
        A_FF <= 0; B_FF <= 0; opcode_FF <= 0; cin_FF <= 0; serial_in_FF <= 0; red_op_A_FF <= 0;
        red_op_B_FF <= 0; bypass_A_FF <= 0; bypass_B_FF <= 0; direction_FF <= 0;
    end begin
        A_FF <= A; B_FF <= B; opcode_FF <= opcode; cin_FF <= cin; serial_in_FF <= serial_in; red_op_A_FF
            <= red_op_A;
        red_op_B_FF <= red_op_B; bypass_A_FF <= bypass_A; bypass_B_FF <= bypass_B; direction_FF <
            = direction;
    end
end
always @(posedge clk or posedge rst) begin
    if (rst) begin
        leds <= 0;
    end else begin
        if (invalid)
            leds = ~leds;
        leds <= 0;
    end
end
always @(posedge clk or posedge rst) begin
    if (rst) begin
        out <= 0;
    end
    else begin
        if (bypass_A_FF && bypass_B_FF)
            out <= (INPUT_PRIORITY == "A")? A_FF : B_FF;
        else if (bypass_A_FF)
            out <= A_FF;
        else if (bypass_B_FF)
            out <= B_FF;
        else begin
            if (invalid) begin
                out <= 0;
            end else begin

```

```

case (opcode_FF)
  3'h0 : begin
    if (red_op_A_FF && red_op_B_FF)
      out <= (INPUT_PRIORITY == "A")? &A_FF : &B_FF;
    else if (red_op_A_FF)
      out <= &A_FF;
    else if (red_op_B_FF)
      out <= &B_FF;
    else
      out <= A_FF & B_FF;
    end
  3'h1 : begin
    if (red_op_A_FF && red_op_B_FF)
      out <= (INPUT_PRIORITY == "A")? ^A_FF : ^B_FF;
    else if (red_op_A_FF)
      out <= ^A_FF;
    else if (red_op_B_FF)
      out <= ^B_FF;
    else
      out <= A_FF ^ B_FF;
    end
  3'h2 : begin
    if (FULL_ADDER == "ON")
      out <= A_FF + B_FF + cin_FF;
    else
      out <= A_FF + B_FF;
    end
  3'h3 : out <= A_FF * B_FF;
  3'h4 : begin
    if (direction_FF)
      out <= {out[4:0], serial_in_FF};
    else
      out <= {serial_in_FF, out[5:1]};
    end
  3'h5 : begin
    if (direction_FF)
      out <= {out[4:0], out[5]};
    else
      out <= {out[0], out[5:1]};
    end
  endcase
end
end
end
endmodule */

```

## Testbench Code:

```
module ALSU_tb ();
parameter INPUT_PRIORITY = "A";
parameter FULL_ADDER = "ON";
reg clk, rst, cin, serial_in, red_op_A, red_op_B, bypass_A, bypass_B, direction;
reg [2:0] A, B, opcode;
wire [15:0] leds;
wire [5:0] out;
ALSU #(INPUT_PRIORITY(INPUT_PRIORITY), FULL_ADDER(FULL_ADDER))
DUT (A, B, opcode, cin, serial_in, direction, red_op_A, red_op_B, bypass_A, bypass_B, clk, rst, out, leds);
initial begin
    clk = 0;
    forever
        #1 clk = ~clk;
End
initial begin
    rst = 1;
    repeat (10) begin
        @(negedge clk);
        A = $random; B = $random; opcode = $urandom_range(0,7); cin = $random;
        serial_in = $random; direction = $random; red_op_A = $random;
        red_op_B = $random; bypass_A = $random; bypass_B = $random;
        if ((out != 0) && (leds != 0)) begin
            $display("The ALSU Design is Wrong! ");
            $stop;
        end
    end
    rst = 0;
    bypass_A = 1; bypass_B = 0;
    repeat (10) begin
        @(negedge clk);
        A = $random; B = $random; opcode = $urandom_range(0,7); cin = $random;
        serial_in = $random; direction = $random; red_op_A = $random;
        red_op_B = $random;
        if ((out != A) && (leds != 0)) begin
            $display("The ALSU Design is Wrong! ");
            $stop;
        end
    end
    bypass_A = 0; bypass_B = 1;
    repeat (10) begin
        @(negedge clk);
        A = $random; B = $random; opcode = $urandom_range(0,7); cin = $random;
        serial_in = $random; direction = $random; red_op_A = $random;
        red_op_B = $random;
        if ((out != B) && (leds != 0)) begin
            $display("The ALSU Design is Wrong! ");
            $stop;
        end
    end
end
```

```

bypass_A = 1;
repeat (10) begin
    @(negedge clk);
    A = $random; B = $random; opcode = $urandom_range(0,7); cin = $random;
    serial_in = $random; direction = $random; red_op_A = $random;
    red_op_B = $random;
    if ((out != A) && (leds != 0)) begin
        $display("The ALSU Design is Wrong! ");
        $stop;
    end
end

bypass_A = 0; bypass_B = 0;

repeat (100) begin
    @(negedge clk);
    A = $random; B = $random; opcode = $urandom_range(0,7); cin = $random;
    serial_in = $random; direction = $random; red_op_A = $random;
    red_op_B = $random;
end
$stop;
end

initial
$monitor("time = %0t, A = %b, B = %b, opcode = %b, cin = %b, serial_in = %b, direction
        = %b, red_op_A = %b, red_op_B = %b, bypass_A = %b, bypass_B = %b, clk = %b, rst
        = %b, out = %b, leds = %b",
        $time, A, B, opcode, cin, serial_in, direction, red_op_A, red_op_B, bypass_A, bypass_B, clk, rst, out, leds);

endmodule

```

## Do File for (ALSU) Question 1

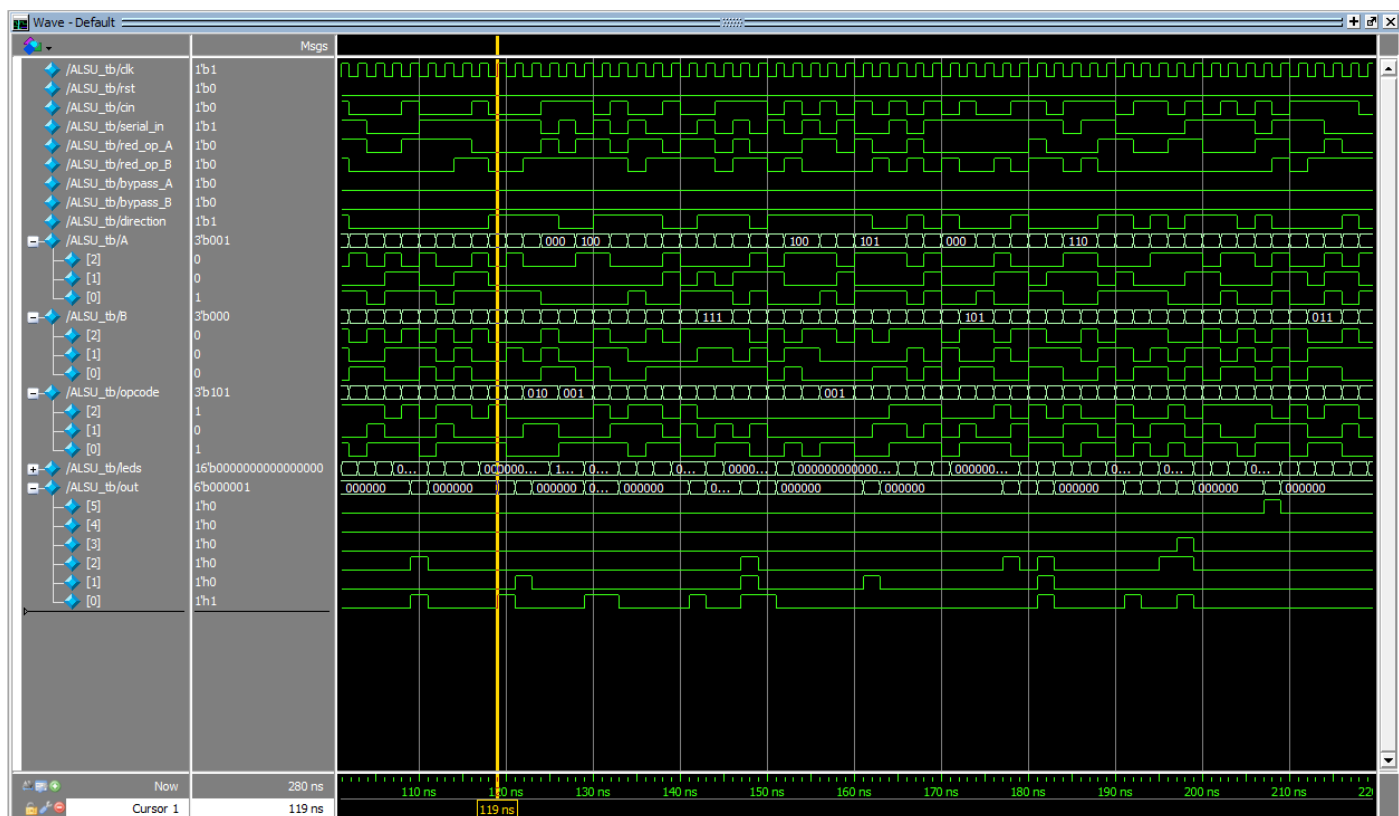
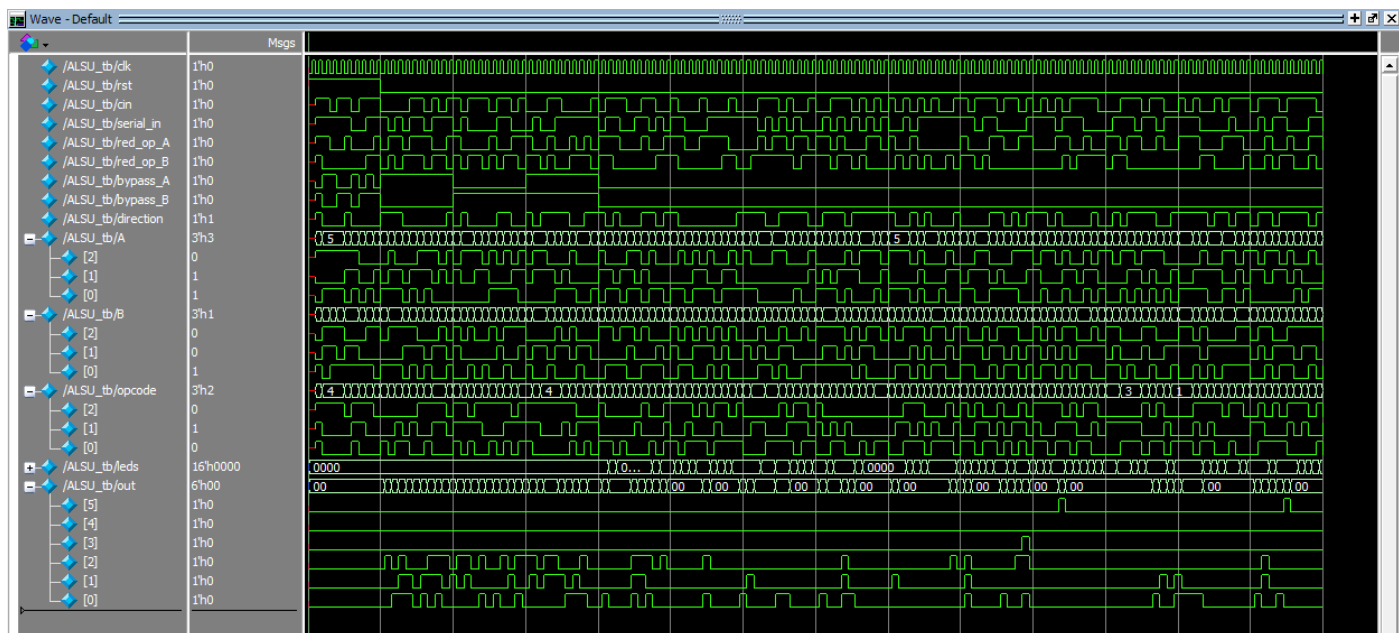
```

vlib work
vlog ALSU.v ALSU_tb.v
vsim -voptargs = +acc work.ALSU_tb
add wave *
run - all

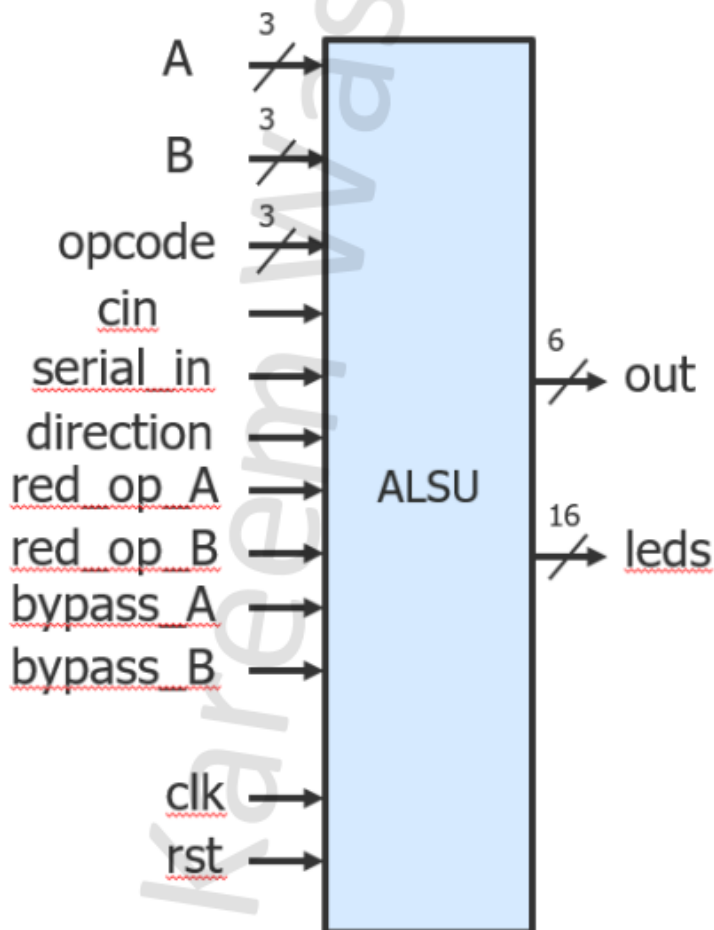
```



# Waveform:







Opcode	Operation
000	AND
001	XOR
010	Addition
011	Multiplication
100	Shift output by 1 bit
101	Rotate output by 1 bit
110	Invalid opcode
111	Invalid opcode

Input	Width	Description
clk	1	Input clock
rst	1	Active high asynchronous reset
A	3	Input port A
B	3	Input port B
cin	1	Carry in bit, only valid to be used if the parameter FULL_ADDER is "ON"
serial_in	1	Serial in bit, used in shift operations only
red_op_A	1	When set to high, this indicates that reduction operation would be executed on A rather than bitwise operations on A and B when the opcode indicates AND and XOR operations
red_op_B	1	When set to high, this indicates that reduction operation would be executed on B rather than bitwise operations on A and B when the opcode indicates AND and XOR operations
opcode	3	Opcode has a separate table to describe the different operations executed
bypass_A	1	When set to high, this indicates that port A will be registered to the output ignoring the opcode operation
bypass_B	1	When set to high, this indicates that port B will be registered to the output ignoring the opcode operation
direction	1	The direction of the shift or rotation operation is left when this input is set to high; otherwise, it is right.

Output	Width	Description
leds	16	When an invalid operation occurs, all bits blink (bits turn on and then off with each clock cycle). Blinking serves as a warning; otherwise, if a valid operation occurs, it is set to low.
out	6	Output of the ALSU

Parameter	Default value	Description
INPUT_PRIORITY	A	Priority is given to the port set by this parameter whenever there is a conflict. Conflicts can occur in two scenarios, red_op_A and red_op_B are both set to high or bypass_A and bypass_B are both set to high. Legal values for this parameter are A and B
FULL_ADDER	ON	When this parameter has value "ON" then cin input must be considered in the addition operation between A and B. Legal values for this parameter are ON and OFF

## Question 2

### DSP48A1 XILINX SPARTAN - 6 FPGA

#### Verilog Code:

```
module DSP (A, B, C, D, clk, rst_n, P);

parameter OPERATION = "ADD";

input [17:0] A, B, D;
input [47:0] C;
input clk, rst_n;
output reg [47:0] P;
reg [17:0] A_FF_1, A_FF_2, B_FF, D_FF, adder_out1;
reg [47:0] C_FF, adder_out2, multiplier_out;

always @(posedge clk or negedge rst_n) begin
    if (~rst_n) begin
        A_FF_1 <= 0; A_FF_2 <= 0; B_FF <= 0; D_FF <= 0; adder_out1 <= 0;
        C_FF <= 0; adder_out2 <= 0; multiplier_out <= 0;
    end
    else begin
        A_FF_1 <= A; A_FF_2 <= A_FF_1; B_FF <= B; D_FF <= D; C_FF <= 0;
        if (OPERATION == "ADD") begin
            adder_out1 <= D_FF + B_FF;
            adder_out2 <= multiplier_out + C_FF;
        end else if (OPERATION == "SUBTRACT") begin
            adder_out1 <= D_FF - B_FF;
            adder_out2 <= multiplier_out - C_FF;
        end
        multiplier_out <= A_FF_2 * adder_out1;
        P <= adder_out2;
    end
end

endmodule
```

## Testbench Code:

```
module DSP_tb ();

parameter OPERATION = "ADD";

reg [17:0] A,B,D;
reg [47:0] C;
reg clk,rst_n;

wire [47:0] P;

DSP #(. OPERATION(OPERATION)) DUT (A,B,C,D,clk,rst_n,P);

initial begin
    clk = 0;
    forever
        #25 clk = ~clk;
end

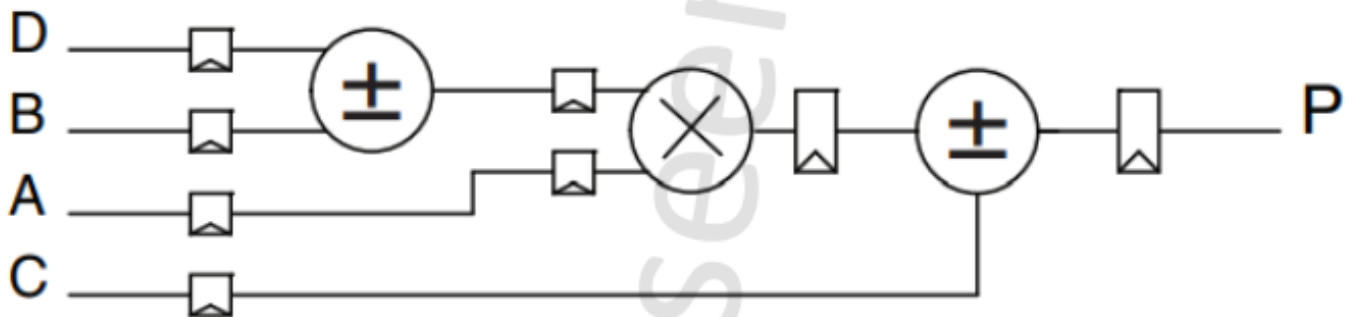
initial begin
    rst_n = 0;
    repeat (10) begin
        A = $random; B = $random;
        C = $random; D = $random;
        @(negedge clk);
        if (P != 0) begin
            $display("The DSP Design is Wrong!");
            $stop;
        end
    end
    rst_n = 1;
    repeat (100) begin
        A = $urandom_range(0,500); B = $urandom_range(0,500);
        C = $urandom_range(0,500); D = $urandom_range(0,500);
        @(negedge clk);
    end
    $stop;
end

initial
$monitor("time = %0t,A = %b,B = %b,C = %b,D = %b,CLK = %b,
        RST_N = %b,P = %b", $time,A,B,C,D,clk,rst_n,P);

endmodule
```

## Do File for (DSP) Question 2

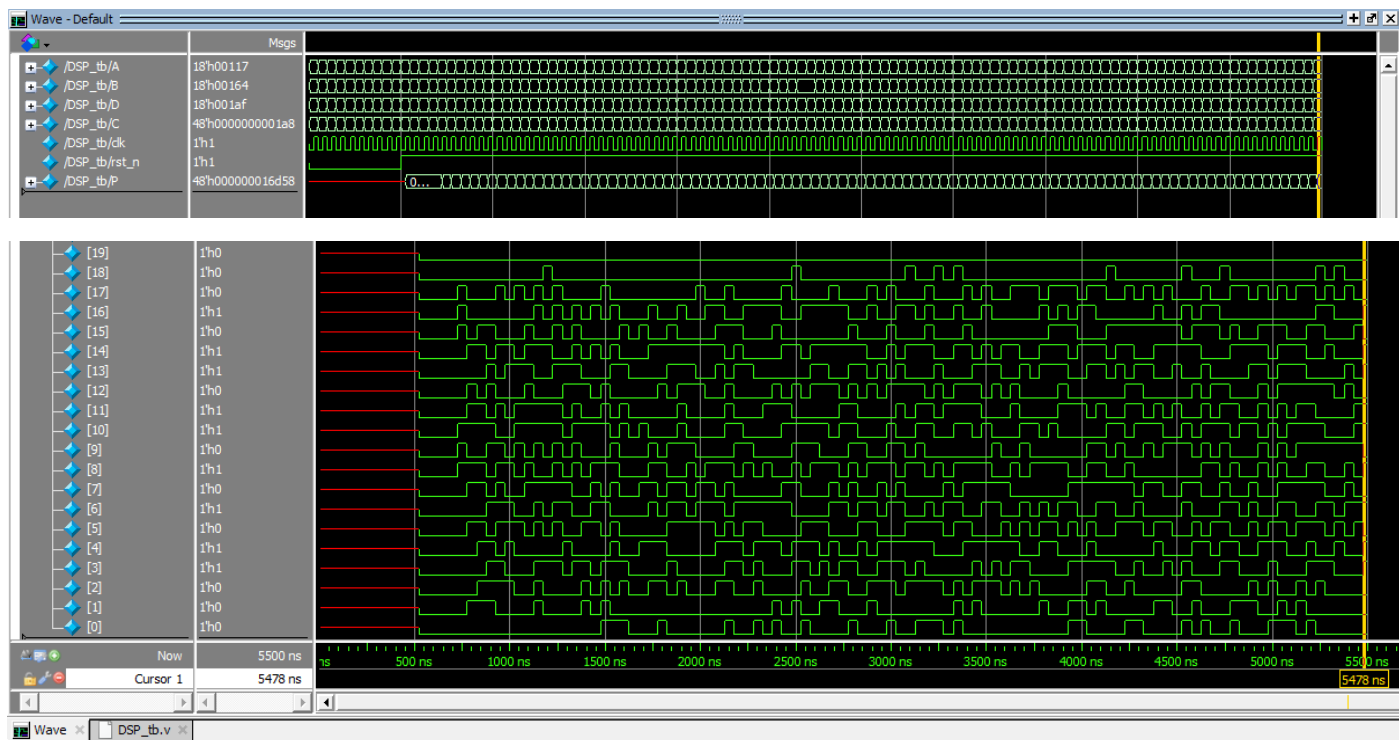
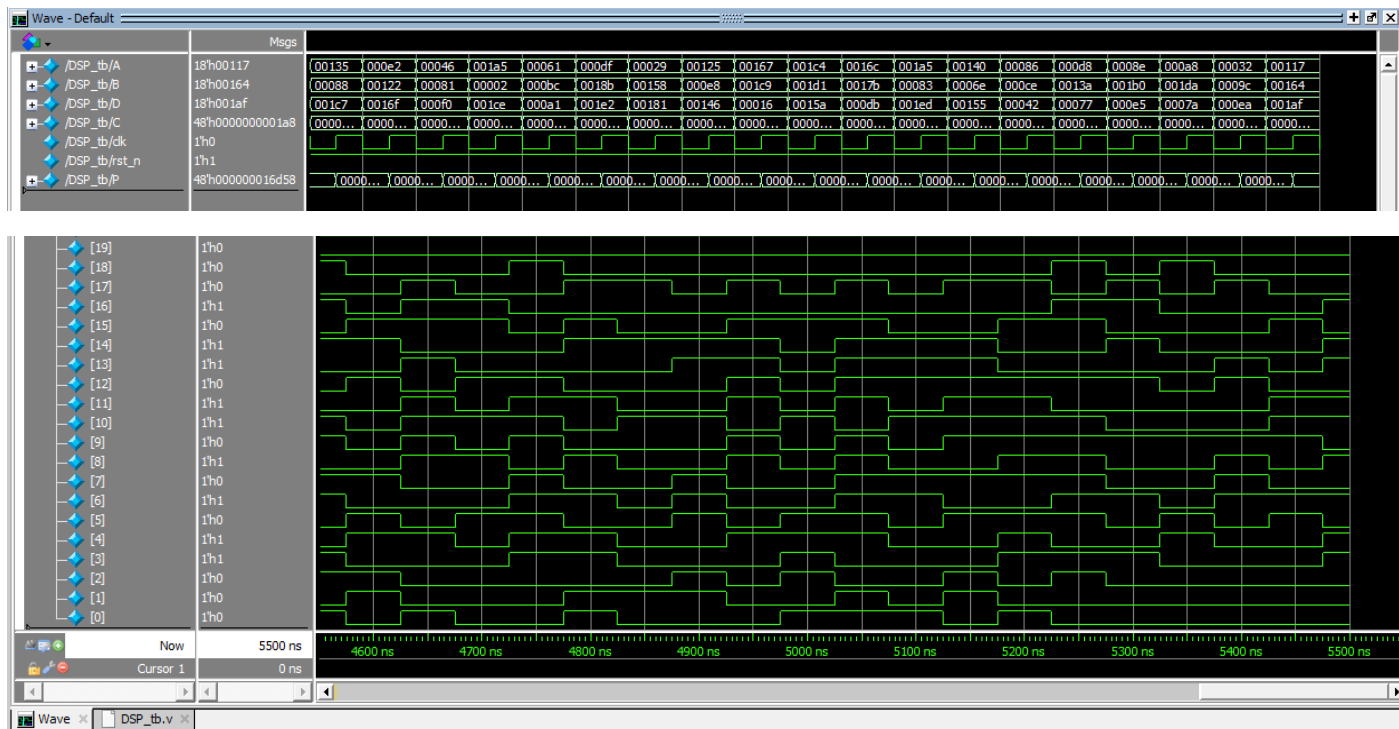
```
vlib work
vlog DSP.v DSP_tb.v
vsim -voptargs = +acc work.DSP_tb
add wave *
run -all
```



Port	Type	Width
A	Input	18
B	Input	18
C	Input	48
D	Input	18
clk	Input	1
rst_n (sync active low)	Input	1
P	Output	48



# Waveform:



[illegible][illegible]