The Linter

Project 1: Spartan6 - DSP48A1

Presented For:

Digital Design Using Verilog & FPGA Flow Using Vivado Diploma - V11

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Digital Designer
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DSP48A1

RTL Design

Overview

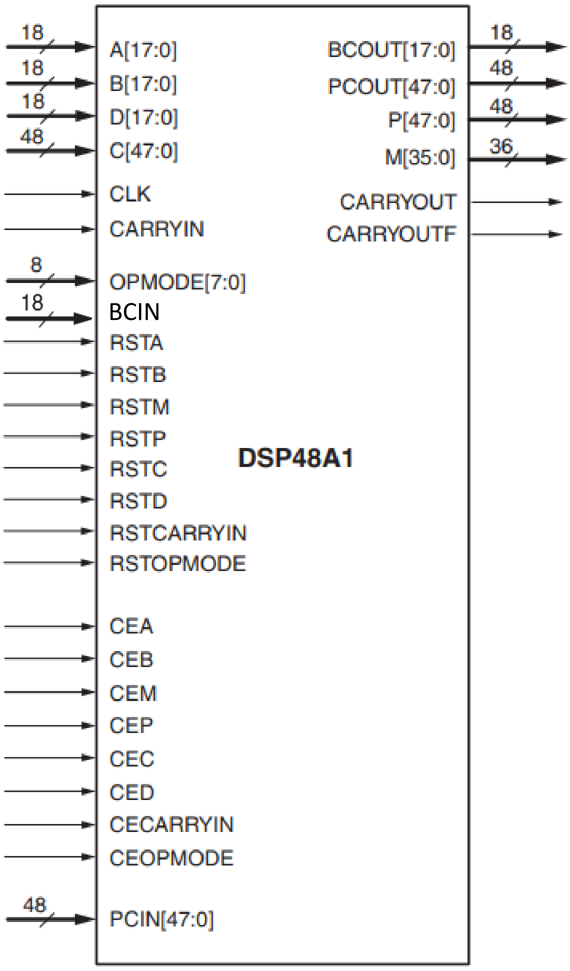
Many DSP algorithms are supported with minimal use of the general - purpose FPGA logic, resulting in low power, high performance, and efficient device utilization. At first look, the DSP48A1 slice contains an 18 - bit input pre-adder followed by an 18 x 18 - bit two's complement multiplier and a 48 - bit sign - extended adder/subtracter/accumulator, a function that is widely used in digital signal processing.

A second look reveals many subtle features that enhance the usefulness, versatility, and speed of this arithmetic building block. Programmable pipelining of input operands, intermediate products, and accumulator outputs enhances throughput. The 48 - bit internal bus allows for practically unlimited aggregation of DSP slices.

One of the most important features is the ability to cascade a result from one DSP48A1 slice to the next without the use of general fabric routing. This path provides high - performance and low - power post addition for many DSP filter functions of any tap length.

Another key feature for filter composition is the ability to cascade an input stream from slice to slice.

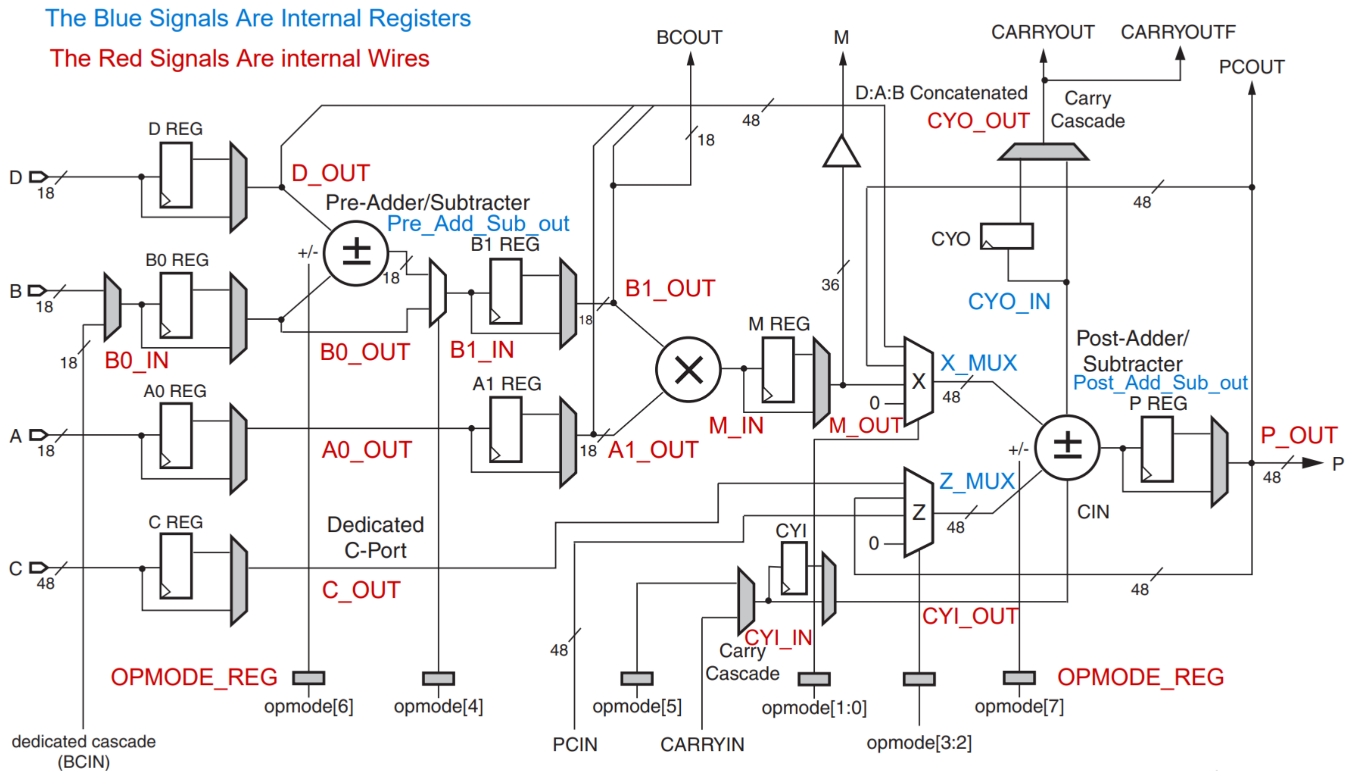
The C input port allows the formation of many 3 - input mathematical functions, such as 3 - input addition by cascading the pre - adder with the post - adder, and 2 - input multiplication with a single addition.



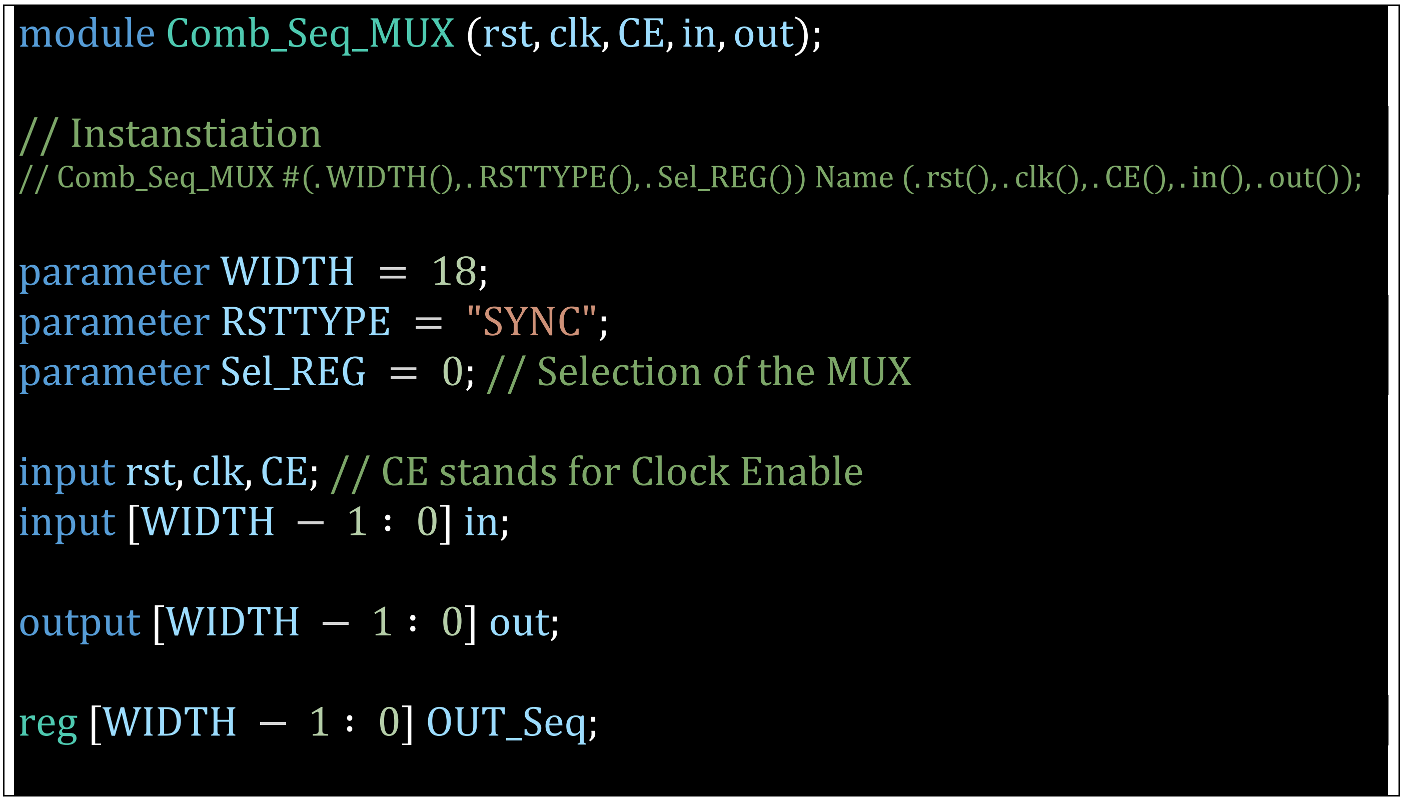
The D input allows a second argument to be used with the pre - adder to reduce DSP48A1 slice utilization in symmetric filters.

The Spartan - 6 family offers a high ratio of DSP48A1 slices to logic, making it ideal for math-intensive applications.

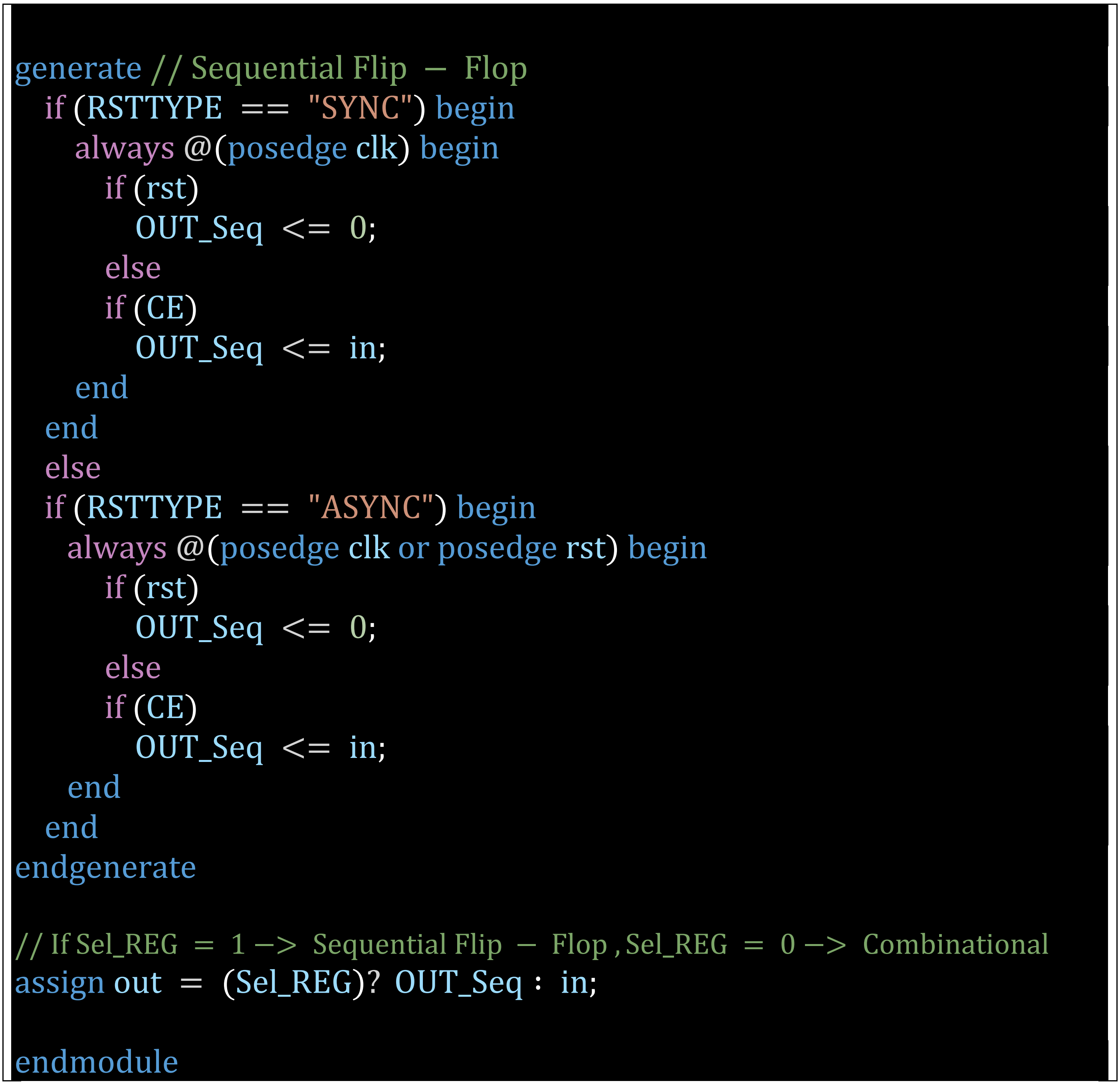
DSP48A1 Slice in Detail



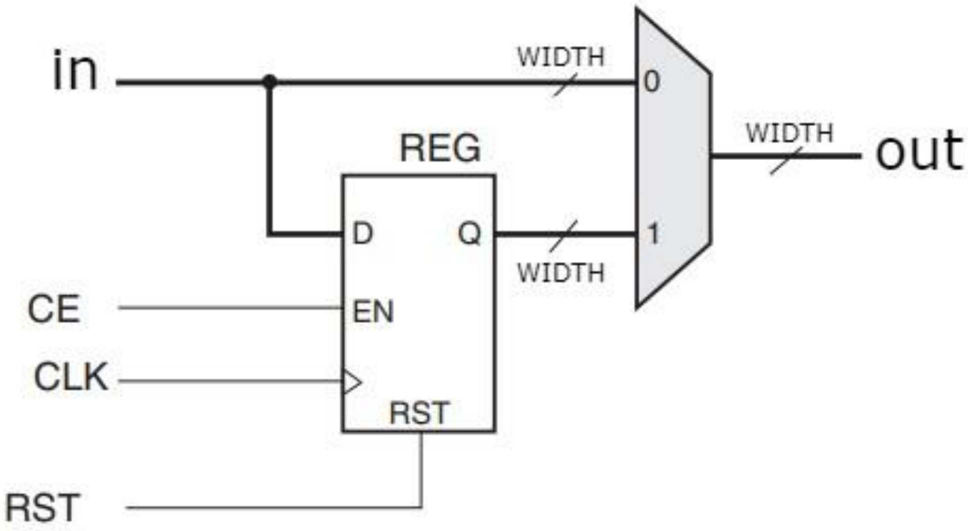
Lower Module



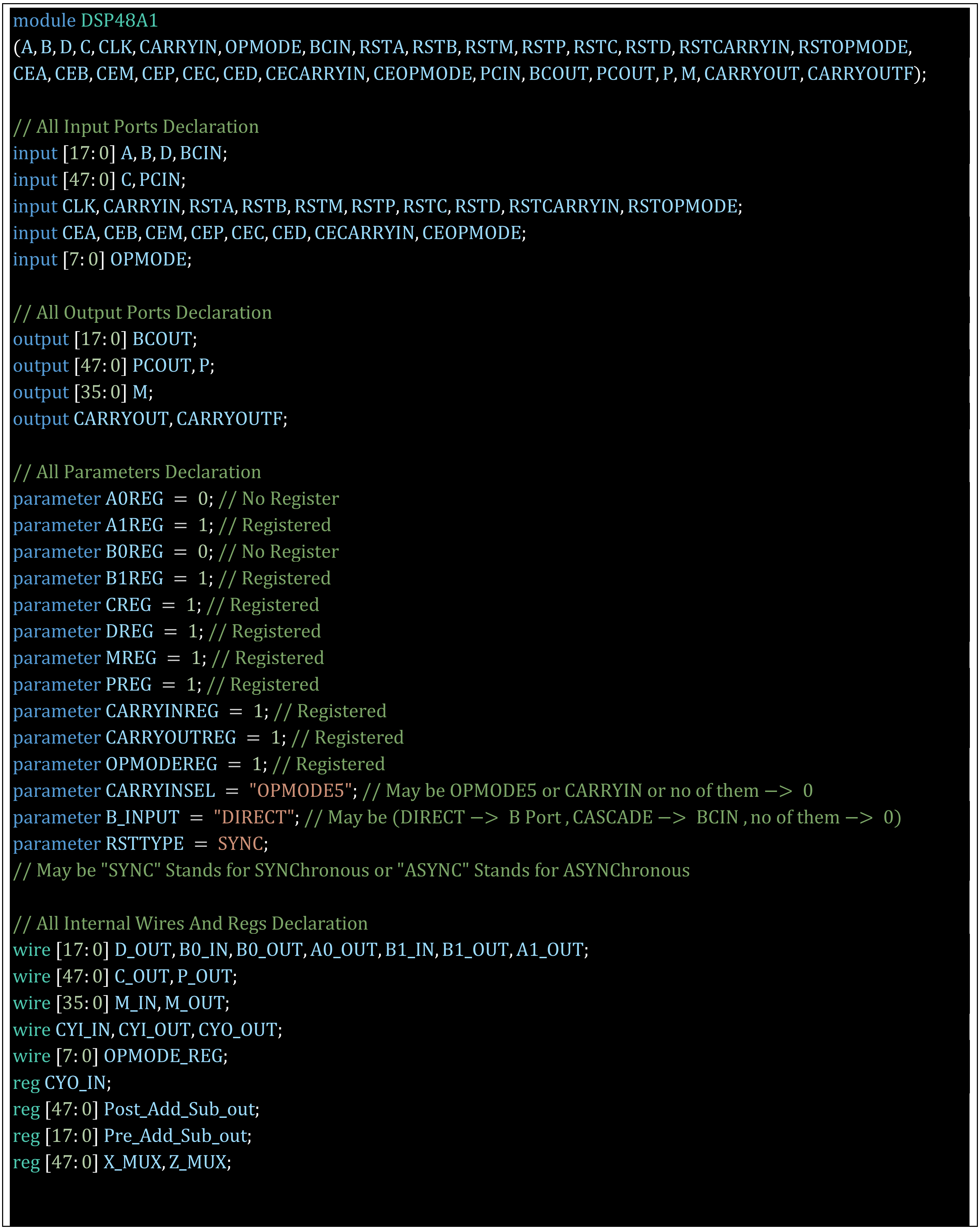
```
module Comb_Seq_MUX (rst, clk, CE, in, out);

// Instanstiation
// Comb_Seq_MUX #(.WIDTH(),.RSTTYPE(),.Sel_REG()) Name (.rst(),.clk(),.CE(),.in(),.out());

parameter WIDTH  =  18;
parameter RSTTYPE  =  "SYNC";
parameter Sel_REG  =  0; // Selection of the MUX

input rst, clk, CE; // CE stands for Clock Enable
input [WIDTH  -  1 :  0] in;

output [WIDTH  -  1 :  0] out;

reg [WIDTH  -  1 :  0] OUT_Seq;
```



```
generate // Sequential Flip − Flop
   if (RSTTYPE  ==  "SYNC") begin
      always @(posedge clk) begin
         if (rst)
            OUT_Seq  <=  0;
         else
         if (CE)
            OUT_Seq  <=  in;
      end
   end
   else
   if (RSTTYPE  ==  "ASYNC") begin
     always @(posedge clk or posedge rst) begin
         if (rst)
            OUT_Seq  <=  0;
         else
         if (CE)
            OUT_Seq  <=  in;
     end
   end
endgenerate

// If Sel_REG  =  1 −> Sequential Flip  −  Flop , Sel_REG  =  0 −> Combinational
assign out  =  (Sel_REG)? OUT_Seq :  in;

endmodule
```



Top Main Module



```
module DSP48A1
(A, B, D, C, CLK, CARRYIN, OPMODE, BCIN, RSTA, RSTB, RSTM, RSTP, RSTC, RSTD, RSTCARRYIN, RSTOPMODE,
CEA, CEB, CEM, CEP, CEC, CED, CECARRYIN, CEOPMODE, PCIN, BCOUT, PCOUT, P, M, CARRYOUT, CARRYOUTF);

// All Input Ports Declaration
input [17: 0] A, B, D, BCIN;
input [47: 0] C, PCIN;
input CLK, CARRYIN, RSTA, RSTB, RSTM, RSTP, RSTC, RSTD, RSTCARRYIN, RSTOPMODE;
input CEA, CEB, CEM, CEP, CEC, CED, CECARRYIN, CEOPMODE;
input [7: 0] OPMODE;

// All Output Ports Declaration
output [17: 0] BCOUT;
output [47: 0] PCOUT, P;
output [35: 0] M;
output CARRYOUT, CARRYOUTF;

// All Parameters Declaration
parameter A0REG = 0; // No Register
parameter A1REG = 1; // Registered
parameter B0REG = 0; // No Register
parameter B1REG = 1; // Registered
parameter CREG = 1; // Registered
parameter DREG = 1; // Registered
parameter MREG = 1; // Registered
parameter PREG = 1; // Registered
parameter CARRYINREG = 1; // Registered
parameter CARRYOUTREG = 1; // Registered
parameter OPMODEREG = 1; // Registered
parameter CARRYINSEL = "OPMODE5"; // May be OPMODE5 or CARRYIN or no of them -> 0
parameter B_INPUT = "DIRECT"; // May be (DIRECT -> B Port , CASCADE -> BCIN , no of them -> 0)
parameter RSTTYPE = SYNC;
// May be "SYNC" Stands for SYNChronous or "ASYNC" Stands for ASYNChronous

// All Internal Wires And Regs Declaration
wire [17: 0] D_OUT, B0_IN, B0_OUT, A0_OUT, B1_IN, B1_OUT, A1_OUT;
wire [47: 0] C_OUT, P_OUT;
wire [35: 0] M_IN, M_OUT;
wire CYI_IN, CYI_OUT, CYO_OUT;
wire [7: 0] OPMODE_REG;
reg CYO_IN;
reg [47: 0] Post_Add_Sub_out;
reg [17: 0] Pre_Add_Sub_out;
reg [47: 0] X_MUX, Z_MUX;
```

```
// Make Instantiations for Registers From Comb_Seq_MUX Module
Comb_Seq_MUX #(.WIDTH(18),.RSTTYPE(RSTTYPE),.Sel_REG(DREG))
D_REG(.rst(RSTD),.clk(CLK),.CE(CED),.in(D),.out(D_OUT));
Comb_Seq_MUX #(.WIDTH(18),.RSTTYPE(RSTTYPE),.Sel_REG(B0REG))
B0_REG(.rst(RSTB),.clk(CLK),.CE(CEB),.in(B0_IN),.out(B0_OUT));
Comb_Seq_MUX #(.WIDTH(18),.RSTTYPE(RSTTYPE),.Sel_REG(A0REG))
A0_REG(.rst(RSTA),.clk(CLK),.CE(CEA),.in(A),.out(A0_OUT));
Comb_Seq_MUX #(.WIDTH(48),.RSTTYPE(RSTTYPE),.Sel_REG(CREG))
C_REG(.rst(RSTC),.clk(CLK),.CE(CEC),.in(C),.out(C_OUT));
Comb_Seq_MUX #(.WIDTH(18),.RSTTYPE(RSTTYPE),.Sel_REG(B1REG))
B1_REG(.rst(RSTB),.clk(CLK),.CE(CEB),.in(B1_IN),.out(B1_OUT));
Comb_Seq_MUX #(.WIDTH(18),.RSTTYPE(RSTTYPE),.Sel_REG(A1REG))
A1_REG(.rst(RSTA),.clk(CLK),.CE(CEA),.in(A0_OUT),.out(A1_OUT));
Comb_Seq_MUX #(.WIDTH(36),.RSTTYPE(RSTTYPE),.Sel_REG(MREG))
M_REG(.rst(RSTM),.clk(CLK),.CE(CEM),.in(M_IN),.out(M_OUT));
Comb_Seq_MUX #(.WIDTH(1),.RSTTYPE(RSTTYPE),.Sel_REG(CARRYINREG))
CARRYIN_REG(.rst(RSTCARRYIN),.clk(CLK),.CE(CECARRYIN),.in(CYI_IN),.out(CYI_OUT));
Comb_Seq_MUX #(.WIDTH(1),.RSTTYPE(RSTTYPE),.Sel_REG(CARRYOUTREG))
CARRYOUT_REG(.rst(RSTCARRYIN),.clk(CLK),.CE(CECARRYIN),.in(CYO_IN),.out(CYO_OUT));
Comb_Seq_MUX #(.WIDTH(48),.RSTTYPE(RSTTYPE),.Sel_REG(PREG))
P_REG(.rst(RSTP),.clk(CLK),.CE(CEP),.in(Post_Add_Sub_out),.out(P_OUT));
Comb_Seq_MUX #(.WIDTH(8),.RSTTYPE(RSTTYPE),.Sel_REG(OPMODEREG))
Opmode_REG(.rst(RSTOPMODE),.clk(CLK),.CE(CEOPMODE),.in(OPMODE),.out(OPMODE_REG));

// Input Wires Assignments
// MUX Check the B_INPUT Parameter
assign B0_IN = (B_INPUT == "DIRECT")? B : (B_INPUT == "CASCADE")? BCIN : 0;
// MUX Check the CARRYINSEL Parameter
assign CYI_IN = (CARRYINSEL == "OPMODE5")? OPMODE_REG[5] : (CARRYINSEL =="CARRYIN")? CARRYIN 0;

// Pre_MUX Check B1_IN of OPMODE_REG[4]
assign B1_IN = (OPMODE_REG[4])? Pre_Add_Sub_out : B0_OUT;
assign M_IN = B1_OUT * A1_OUT; // Multiplier Output

// Check OPMODE_REG[6]
always @(*) begin
  if (OPMODE_REG[6])
    Pre_Add_Sub_out = D_OUT - B0_OUT;
  else
    Pre_Add_Sub_out = D_OUT + B0_OUT;
end

// Check {OPMODE_REG[3], OPMODE_REG[2]}
always @(*) begin
  case ({OPMODE_REG[3], OPMODE_REG[2]})
    2'b00 : Z_MUX = 0;
    2'b01 : Z_MUX = PCIN;
    2'b10 : Z_MUX = P_OUT;
    2'b11 : Z_MUX = C_OUT;
  endcase
end
```

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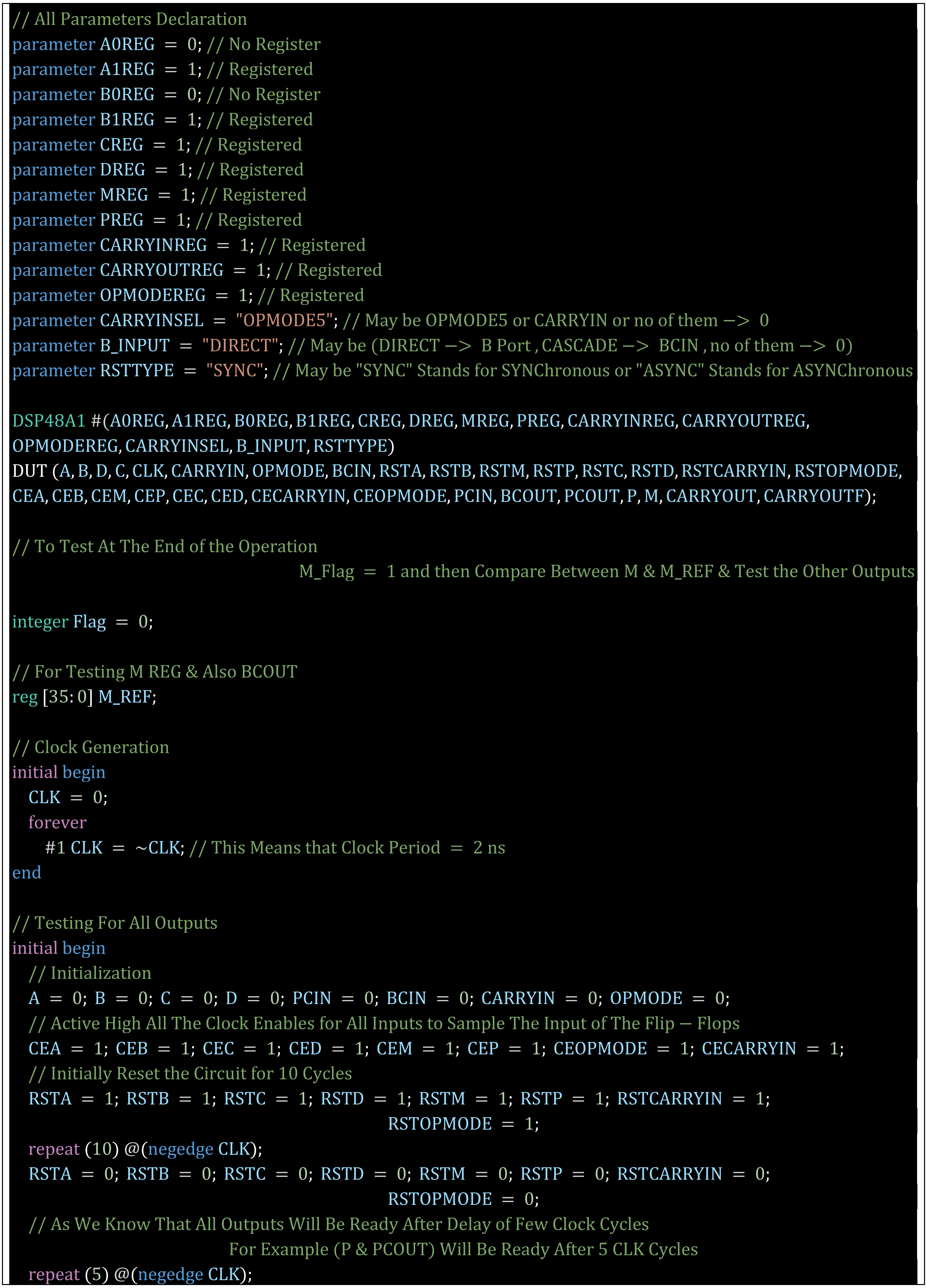
```
// Check {OPMODE_REG[1], OPMODE_REG[0]}
always @(*) begin
  case ({OPMODE_REG[1], OPMODE_REG[0]})
    2'b00 : X_MUX = 0;
    2'b01 : X_MUX = {{12{M_OUT[35]}}, M_OUT}; // Sign Extention
    2'b10 : X_MUX = P_OUT;
    2'b11 : X_MUX = {D_OUT[11:0], A1_OUT, B1_OUT};
  endcase
end

// Check OPMODE_REG[7]
always @(*) begin
  if (OPMODE_REG[7])
    {CYO_IN, Post_Add_Sub_out} = Z_MUX - (X_MUX + CYI_OUT);
  else
    {CYO_IN, Post_Add_Sub_out} = Z_MUX + X_MUX + CYI_OUT;
end

// Outputs Assignments (Duplicated and Cascaded Signals Assignment)
assign P = P_OUT;
assign PCOUT = P_OUT;
assign CARRYOUT = CYO_OUT;
assign CARRYOUTF = CYO_OUT;
assign BCOUT = B1_OUT;
assign M = ~(~M_OUT); // buf(M, M_OUT);

endmodule
```

TESTBENCH

```
module DSP48A1_tb ();

// All Input Ports Declaration
reg [17:0] A, B, D, BCIN;
reg [47:0] C, PCIN;
reg CLK, CARRYIN, RSTA, RSTB, RSTM, RSTP, RSTC, RSTD, RSTCARRYIN, RSTOPMODE;
reg CEA, CEB, CEM, CEP, CEC, CED, CECARRYIN, CEOPMODE;
reg [7:0] OPMODE;

// All Output Ports Declaration
wire [17:0] BCOUT;
wire [47:0] PCOUT, P;
wire [35:0] M;
wire CARRYOUT, CARRYOUTF;
```



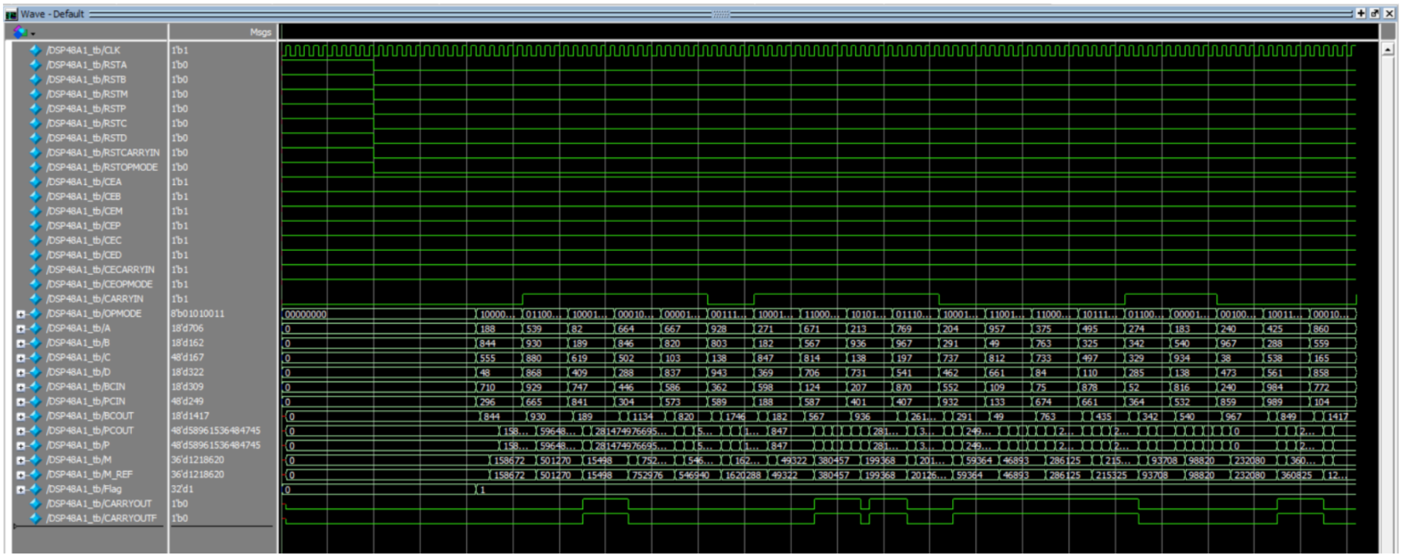
```
// All Parameters Declaration
parameter A0REG = 0; // No Register
parameter A1REG = 1; // Registered
parameter B0REG = 0; // No Register
parameter B1REG = 1; // Registered
parameter CREG = 1; // Registered
parameter DREG = 1; // Registered
parameter MREG = 1; // Registered
parameter PREG = 1; // Registered
parameter CARRYINREG = 1; // Registered
parameter CARRYOUTREG = 1; // Registered
parameter OPMODEREG = 1; // Registered
parameter CARRYINSEL = "OPMODE5"; // May be OPMODE5 or CARRYIN or no of them −> 0
parameter B_INPUT = "DIRECT"; // May be (DIRECT −> B Port , CASCADE −> BCIN , no of them −> 0)
parameter RSTTYPE = "SYNC"; // May be "SYNC" Stands for SYNChronous or "ASYNC" Stands for ASYNChronous

DSP48A1 #(A0REG, A1REG, B0REG, B1REG, CREG, DREG, MREG, PREG, CARRYINREG, CARRYOUTREG,
OPMODEREG, CARRYINSEL, B_INPUT, RSTTYPE)
DUT (A, B, D, C, CLK, CARRYIN, OPMODE, BCIN, RSTA, RSTB, RSTM, RSTP, RSTC, RSTD, RSTCARRYIN, RSTOPMODE,
CEA, CEB, CEM, CEP, CEC, CED, CECARRYIN, CEOPMODE, PCIN, BCOUT, PCOUT, P, M, CARRYOUT, CARRYOUTF);

// To Test At The End of the Operation
                                        M_Flag = 1 and then Compare Between M & M_REF & Test the Other Outputs

integer Flag = 0;

// For Testing M REG & Also BCOUT
reg [35: 0] M_REF;

// Clock Generation
initial begin
  CLK = 0;
  forever
    #1 CLK = ~CLK; // This Means that Clock Period = 2 ns
end

// Testing For All Outputs
initial begin
  // Initialization
  A = 0; B = 0; C = 0; D = 0; PCIN = 0; BCIN = 0; CARRYIN = 0; OPMODE = 0;
  // Active High All The Clock Enables for All Inputs to Sample The Input of The Flip − Flops
  CEA = 1; CEB = 1; CEC = 1; CED = 1; CEM = 1; CEP = 1; CEOPMODE = 1; CECARRYIN = 1;
  // Initially Reset the Circuit for 10 Cycles
  RSTA = 1; RSTB = 1; RSTC = 1; RSTD = 1; RSTM = 1; RSTP = 1; RSTCARRYIN = 1;
                                            RSTOPMODE = 1;
  repeat (10) @(negedge CLK);
  RSTA = 0; RSTB = 0; RSTC = 0; RSTD = 0; RSTM = 0; RSTP = 0; RSTCARRYIN = 0;
                                            RSTOPMODE = 0;
  // As We Know That All Outputs Will Be Ready After Delay of Few Clock Cycles
                              For Example (P & PCOUT) Will Be Ready After 5 CLK Cycles
  repeat (5) @(negedge CLK);
  @(negedge CLK);
  // Testing for 20 iteration
  repeat (20) begin
    #10;
    A = $urandom_range(0,1000);
    B = $urandom_range(0,1000);
    C = $urandom_range(0,1000);
    D = $urandom_range(0,1000);
    PCIN = $urandom_range(0,1000);
    BCIN = $urandom_range(0,1000);
    CARRYIN = $random;
    OPMODE = $random;
    Flag = 1;
  end
  $display("\n\t\t Finish Testbench With 0 Errors & 0 Design Checks\n");

  $stop;
end

always @(M) begin
  M_REF = BCOUT * A;
end

// Test M & BCOUT (Depend On M as M Correct So BCOUT is Correct)
always @(negedge CLK) begin
  if (Flag) begin
    #10;
    if (M ! = M_REF) begin
      $display("The DSP Design is Wrong ! ");
      $stop;
    end
  end
end

// Test P & PCOUT (Depend On P as P is Correct So PCOUT is Correct) & CARRAYOUT & CARRYOUTF
always @(negedge CLK) begin
  if (Flag) begin
    #10;
    // Test P & CARRAYOUT When Out of X_MUX = M & Z_MUX = 0
    if ((OPMODE[1: 0] == 2′b01) && (OPMODE[3: 2] == 2′b00)) begin
      if ((P ! = M) && (CARRYOUT ! = 0)) begin
        $display("The DSP Design is Wrong ! ");
        $stop;
      end
    end
  end
end
initial
$monitor("Time = %0t, A = %d, B = %d, C = %d, D = %d, OPMODE = %b, M = %d, Mref = %d,
                    BCOUT = %d", $time, A, B, C, D, OPMODE, M, M_REF, BCOUT);
endmodule
```

Do File

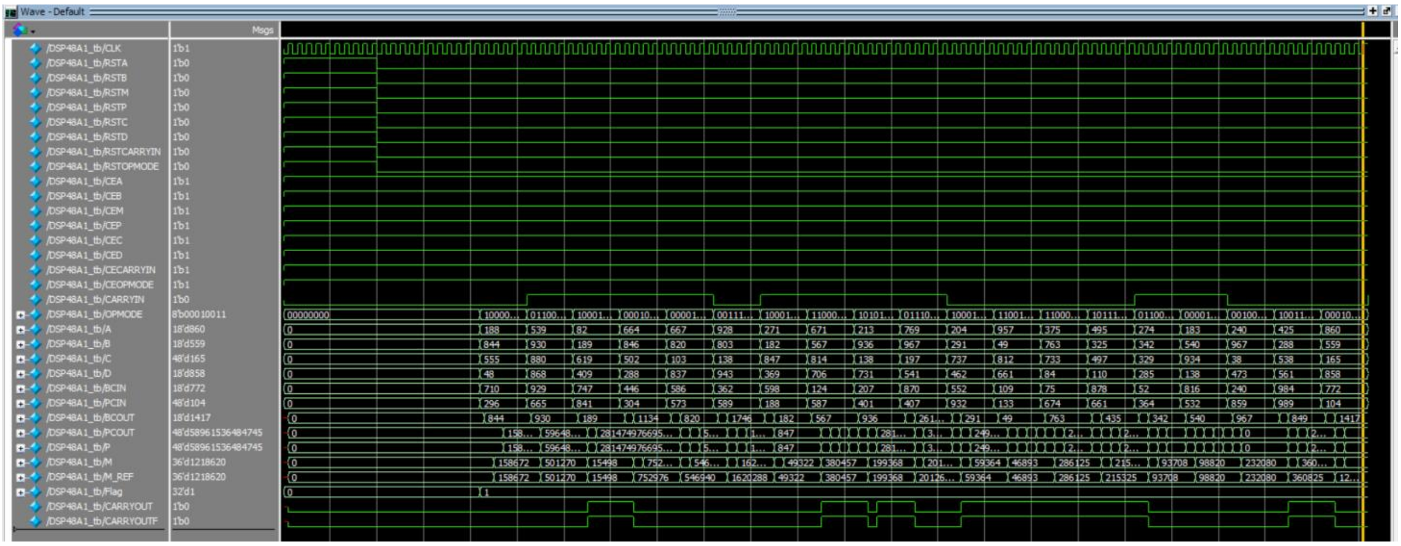
```
vlib work

vlog DSP48A1.v Comb_Seq_MUX.v DSP48A1_tb.v

vsim -voptargs=+acc work.DSP48A1_tb

add wave *

run -all
```

Questa Sim

Waveform

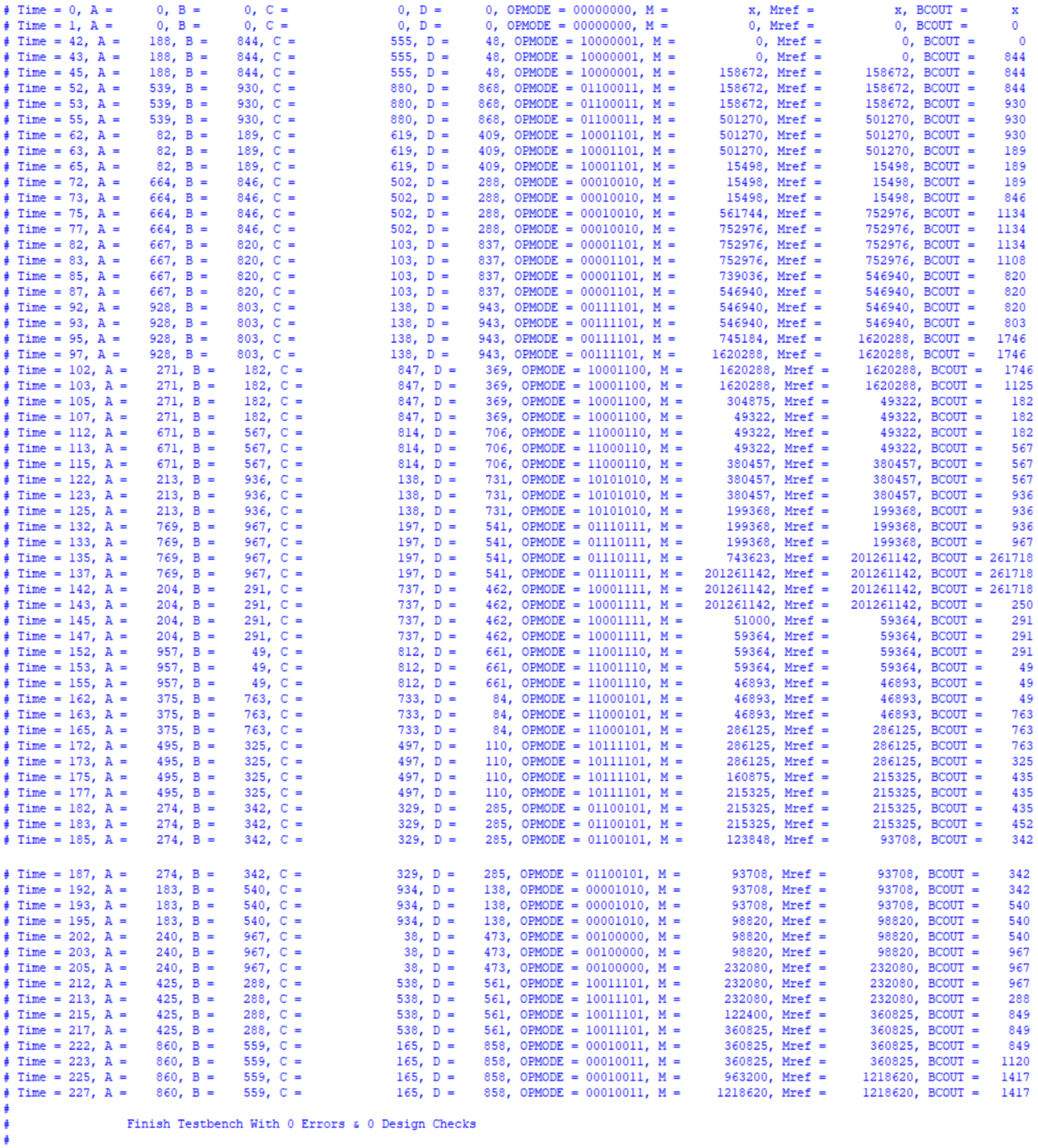


```
Wave - Default
                                   Msgs
/DSP48A1_tb/CLK                    1'b1
/DSP48A1_tb/RSTA                   1'b0
/DSP48A1_tb/RSTB                   1'b0
/DSP48A1_tb/RSTM                   1'b0
/DSP48A1_tb/RSTP                   1'b0
/DSP48A1_tb/RSTC                   1'b0
/DSP48A1_tb/RSTD                   1'b0
/DSP48A1_tb/RSTCARRYIN             1'b0
/DSP48A1_tb/RSTOPMODE              1'b0
/DSP48A1_tb/CEA                    1'b1
/DSP48A1_tb/CEB                    1'b1
/DSP48A1_tb/CEM                    1'b1
/DSP48A1_tb/CEP                    1'b1
/DSP48A1_tb/CEC                    1'b1
/DSP48A1_tb/CED                    1'b1
/DSP48A1_tb/CECARRYIN              1'b1
/DSP48A1_tb/CEOPMODE               1'b1
/DSP48A1_tb/CARRYIN                1'b1
/DSP48A1_tb/OPMODE                 8'b01010011
/DSP48A1_tb/A                      18'd706
/DSP48A1_tb/B                      18'd162
/DSP48A1_tb/C                      48'd167
/DSP48A1_tb/D                      18'd322
/DSP48A1_tb/BCIN                   18'd309
/DSP48A1_tb/PCIN                   48'd249
/DSP48A1_tb/BCOUT                  18'd1417
/DSP48A1_tb/PCOUT                  48'd58961536484745
/DSP48A1_tb/P                      48'd58961536484745
/DSP48A1_tb/M                      36'd1218620
/DSP48A1_tb/M_REF                  36'd1218620
/DSP48A1_tb/Flag                   32'd1
/DSP48A1_tb/CARRYOUT               1'b0
/DSP48A1_tb/CARRYOUTF              1'b0
```



```
Wave - Default
                                   Msgs
/DSP48A1_tb/CLK                    1'b1
/DSP48A1_tb/RSTA                   1'b0
/DSP48A1_tb/RSTB                   1'b0
/DSP48A1_tb/RSTM                   1'b0
/DSP48A1_tb/RSTP                   1'b0
/DSP48A1_tb/RSTC                   1'b0
/DSP48A1_tb/RSTD                   1'b0
/DSP48A1_tb/RSTCARRYIN             1'b0
/DSP48A1_tb/RSTOPMODE              1'b0
/DSP48A1_tb/CEA                    1'b1
/DSP48A1_tb/CEB                    1'b1
/DSP48A1_tb/CEM                    1'b1
/DSP48A1_tb/CEP                    1'b1
/DSP48A1_tb/CEC                    1'b1
/DSP48A1_tb/CED                    1'b1
/DSP48A1_tb/CECARRYIN              1'b1
/DSP48A1_tb/CEOPMODE               1'b1
/DSP48A1_tb/CARRYIN                1'b0
/DSP48A1_tb/OPMODE                 8'b00010011
/DSP48A1_tb/A                      18'd860
/DSP48A1_tb/B                      18'd559
/DSP48A1_tb/C                      48'd165
/DSP48A1_tb/D                      18'd858
/DSP48A1_tb/BCIN                   18'd772
/DSP48A1_tb/PCIN                   48'd104
/DSP48A1_tb/BCOUT                  18'd1417
/DSP48A1_tb/PCOUT                  48'd58961536484745
/DSP48A1_tb/P                      48'd58961536484745
/DSP48A1_tb/M                      36'd1218620
/DSP48A1_tb/M_REF                  36'd1218620
/DSP48A1_tb/Flag                   32'd1
/DSP48A1_tb/CARRYOUT               1'b0
/DSP48A1_tb/CARRYOUTF              1'b0
```

Monitor

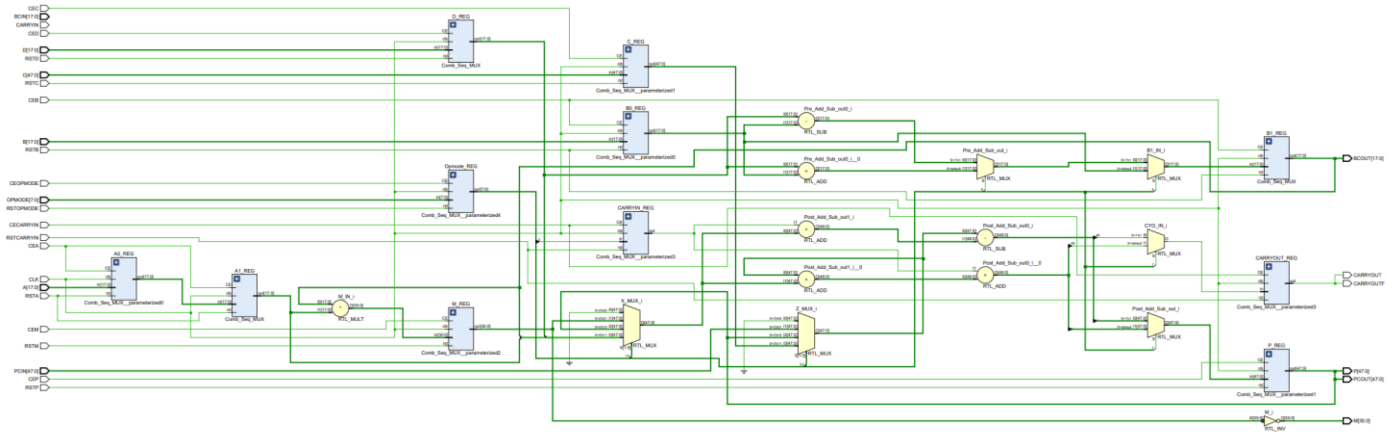


```
# Time = 0, A =      0, B =      0, C =               0, D =      0, OPMODE = 00000000, M =          x, Mref =          x, BCOUT =      x
# Time = 1, A =      0, B =      0, C =               0, D =      0, OPMODE = 00000000, M =          0, Mref =          0, BCOUT =      0
# Time = 42, A =   188, B =    844, C =             555, D =     48, OPMODE = 10000001, M =          0, Mref =          0, BCOUT =      0
# Time = 43, A =   188, B =    844, C =             555, D =     48, OPMODE = 10000001, M =          0, Mref =          0, BCOUT =    844
# Time = 45, A =   188, B =    844, C =             555, D =     48, OPMODE = 10000001, M =     158672, Mref =     158672, BCOUT =    844
# Time = 52, A =   539, B =    930, C =             880, D =    868, OPMODE = 01100011, M =     158672, Mref =     158672, BCOUT =    844
# Time = 53, A =   539, B =    930, C =             880, D =    868, OPMODE = 01100011, M =     158672, Mref =     158672, BCOUT =    930
# Time = 55, A =   539, B =    930, C =             880, D =    868, OPMODE = 01100011, M =     501270, Mref =     501270, BCOUT =    930
# Time = 62, A =    82, B =    189, C =             619, D =    409, OPMODE = 10001101, M =     501270, Mref =     501270, BCOUT =    930
# Time = 63, A =    82, B =    189, C =             619, D =    409, OPMODE = 10001101, M =     501270, Mref =     501270, BCOUT =    189
# Time = 65, A =    82, B =    189, C =             619, D =    409, OPMODE = 10001101, M =      15498, Mref =      15498, BCOUT =    189
# Time = 72, A =   664, B =    846, C =             502, D =    288, OPMODE = 00010010, M =      15498, Mref =      15498, BCOUT =    189
# Time = 73, A =   664, B =    846, C =             502, D =    288, OPMODE = 00010010, M =      15498, Mref =      15498, BCOUT =    846
# Time = 75, A =   664, B =    846, C =             502, D =    288, OPMODE = 00010010, M =     561744, Mref =     752976, BCOUT =   1134
# Time = 77, A =   664, B =    846, C =             502, D =    288, OPMODE = 00010010, M =     752976, Mref =     752976, BCOUT =   1134
# Time = 82, A =   667, B =    820, C =             103, D =    837, OPMODE = 00001101, M =     752976, Mref =     752976, BCOUT =   1134
# Time = 83, A =   667, B =    820, C =             103, D =    837, OPMODE = 00001101, M =     752976, Mref =     752976, BCOUT =   1108
# Time = 85, A =   667, B =    820, C =             103, D =    837, OPMODE = 00001101, M =     739036, Mref =     546940, BCOUT =    820
# Time = 87, A =   667, B =    820, C =             103, D =    837, OPMODE = 00001101, M =     546940, Mref =     546940, BCOUT =    820
# Time = 92, A =   928, B =    803, C =             138, D =    943, OPMODE = 00111101, M =     546940, Mref =     546940, BCOUT =    820
# Time = 93, A =   928, B =    803, C =             138, D =    943, OPMODE = 00111101, M =     546940, Mref =     546940, BCOUT =    803
# Time = 95, A =   928, B =    803, C =             138, D =    943, OPMODE = 00111101, M =     745184, Mref =    1620288, BCOUT =   1746
# Time = 97, A =   928, B =    803, C =             138, D =    943, OPMODE = 00111101, M =    1620288, Mref =    1620288, BCOUT =   1746
# Time = 102, A =    271, B =    182, C =           847, D =    369, OPMODE = 10001100, M =    1620288, Mref =    1620288, BCOUT =   1746
# Time = 103, A =    271, B =    182, C =           847, D =    369, OPMODE = 10001100, M =    1620288, Mref =    1620288, BCOUT =   1125
# Time = 105, A =    271, B =    182, C =           847, D =    369, OPMODE = 10001100, M =     304875, Mref =      49322, BCOUT =    182
# Time = 107, A =    271, B =    182, C =           847, D =    369, OPMODE = 10001100, M =      49322, Mref =      49322, BCOUT =    182
# Time = 112, A =    671, B =    567, C =           814, D =    706, OPMODE = 11000110, M =      49322, Mref =      49322, BCOUT =    182
# Time = 113, A =    671, B =    567, C =           814, D =    706, OPMODE = 11000110, M =      49322, Mref =      49322, BCOUT =    567
# Time = 115, A =    671, B =    567, C =           814, D =    706, OPMODE = 11000110, M =     380457, Mref =     380457, BCOUT =    567
# Time = 122, A =    213, B =    936, C =           138, D =    731, OPMODE = 10101010, M =     380457, Mref =     380457, BCOUT =    567
# Time = 123, A =    213, B =    936, C =           138, D =    731, OPMODE = 10101010, M =     380457, Mref =     380457, BCOUT =    936
# Time = 125, A =    213, B =    936, C =           138, D =    731, OPMODE = 10101010, M =     199368, Mref =     199368, BCOUT =    936
# Time = 132, A =    769, B =    967, C =           197, D =    541, OPMODE = 01110111, M =     199368, Mref =     199368, BCOUT =    936
# Time = 133, A =    769, B =    967, C =           197, D =    541, OPMODE = 01110111, M =     199368, Mref =     199368, BCOUT =    967
# Time = 135, A =    769, B =    967, C =           197, D =    541, OPMODE = 01110111, M =     743623, Mref =  201261142, BCOUT = 261718
# Time = 137, A =    769, B =    967, C =           197, D =    541, OPMODE = 01110111, M =  201261142, Mref =  201261142, BCOUT = 261718
# Time = 142, A =    204, B =    291, C =           737, D =    462, OPMODE = 10001111, M =  201261142, Mref =  201261142, BCOUT = 261718
# Time = 143, A =    204, B =    291, C =           737, D =    462, OPMODE = 10001111, M =  201261142, Mref =  201261142, BCOUT =    250
# Time = 145, A =    204, B =    291, C =           737, D =    462, OPMODE = 10001111, M =      51000, Mref =      59364, BCOUT =    291
# Time = 147, A =    204, B =    291, C =           737, D =    462, OPMODE = 10001111, M =      59364, Mref =      59364, BCOUT =    291
# Time = 152, A =    957, B =     49, C =           812, D =    661, OPMODE = 11001110, M =      59364, Mref =      59364, BCOUT =    291
# Time = 153, A =    957, B =     49, C =           812, D =    661, OPMODE = 11001110, M =      59364, Mref =      59364, BCOUT =     49
# Time = 155, A =    957, B =     49, C =           812, D =    661, OPMODE = 11001110, M =      46893, Mref =      46893, BCOUT =     49
# Time = 162, A =    375, B =    763, C =           733, D =     84, OPMODE = 11000101, M =      46893, Mref =      46893, BCOUT =     49
# Time = 163, A =    375, B =    763, C =           733, D =     84, OPMODE = 11000101, M =      46893, Mref =      46893, BCOUT =    763
# Time = 165, A =    375, B =    763, C =           733, D =     84, OPMODE = 11000101, M =     286125, Mref =     286125, BCOUT =    763
# Time = 172, A =    495, B =    325, C =           497, D =    110, OPMODE = 10111101, M =     286125, Mref =     286125, BCOUT =    763
# Time = 173, A =    495, B =    325, C =           497, D =    110, OPMODE = 10111101, M =     286125, Mref =     286125, BCOUT =    325
# Time = 175, A =    495, B =    325, C =           497, D =    110, OPMODE = 10111101, M =     160875, Mref =     215325, BCOUT =    435
# Time = 177, A =    495, B =    325, C =           497, D =    110, OPMODE = 10111101, M =     215325, Mref =     215325, BCOUT =    435
# Time = 182, A =    274, B =    342, C =           329, D =    285, OPMODE = 01100101, M =     215325, Mref =     215325, BCOUT =    435
# Time = 183, A =    274, B =    342, C =           329, D =    285, OPMODE = 01100101, M =     215325, Mref =     215325, BCOUT =    452
# Time = 185, A =    274, B =    342, C =           329, D =    285, OPMODE = 01100101, M =     123848, Mref =      93708, BCOUT =    342

# Time = 187, A =    274, B =    342, C =           329, D =    285, OPMODE = 01100101, M =      93708, Mref =      93708, BCOUT =    342
# Time = 192, A =    183, B =    540, C =           934, D =    138, OPMODE = 00001010, M =      93708, Mref =      93708, BCOUT =    342
# Time = 193, A =    183, B =    540, C =           934, D =    138, OPMODE = 00001010, M =      93708, Mref =      93708, BCOUT =    540
# Time = 195, A =    183, B =    540, C =           934, D =    138, OPMODE = 00001010, M =      98820, Mref =      98820, BCOUT =    540
# Time = 202, A =    240, B =    967, C =            38, D =    473, OPMODE = 00100000, M =      98820, Mref =      98820, BCOUT =    540
# Time = 203, A =    240, B =    967, C =            38, D =    473, OPMODE = 00100000, M =      98820, Mref =      98820, BCOUT =    967
# Time = 205, A =    240, B =    967, C =            38, D =    473, OPMODE = 00100000, M =     232080, Mref =     232080, BCOUT =    967
# Time = 212, A =    425, B =    288, C =           538, D =    561, OPMODE = 10011101, M =     232080, Mref =     232080, BCOUT =    967
# Time = 213, A =    425, B =    288, C =           538, D =    561, OPMODE = 10011101, M =     232080, Mref =     232080, BCOUT =    288
# Time = 215, A =    425, B =    288, C =           538, D =    561, OPMODE = 10011101, M =     122400, Mref =     360825, BCOUT =    849
# Time = 217, A =    425, B =    288, C =           538, D =    561, OPMODE = 10011101, M =     360825, Mref =     360825, BCOUT =    849
# Time = 222, A =    860, B =    559, C =           165, D =    858, OPMODE = 00010011, M =     360825, Mref =     360825, BCOUT =    849
# Time = 223, A =    860, B =    559, C =           165, D =    858, OPMODE = 00010011, M =     360825, Mref =     360825, BCOUT =   1120
# Time = 225, A =    860, B =    559, C =           165, D =    858, OPMODE = 00010011, M =     963200, Mref =    1218620, BCOUT =   1417
# Time = 227, A =    860, B =    559, C =           165, D =    858, OPMODE = 00010011, M =    1218620, Mref =    1218620, BCOUT =   1417
#
#              Finish Testbench With 0 Errors & 0 Design Checks
#
```

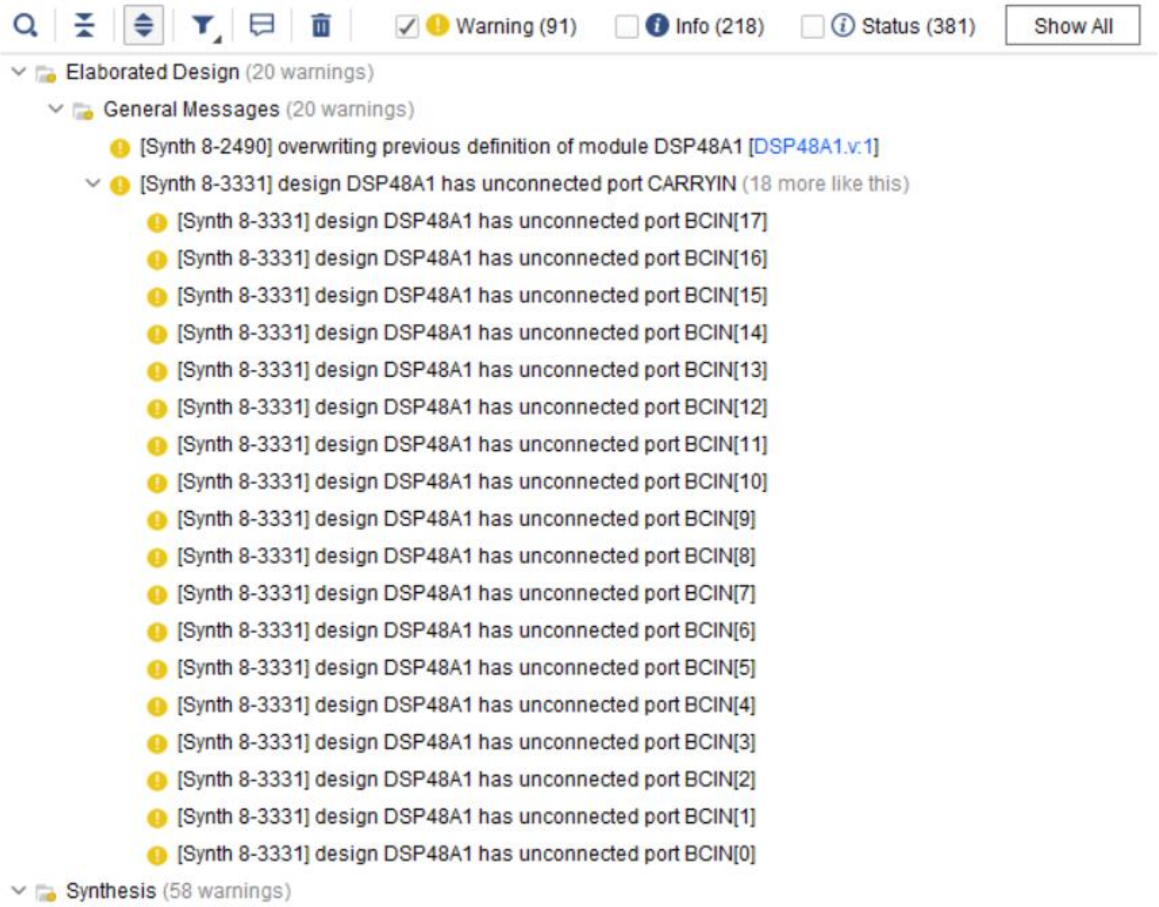
VIVADO

Elaboration

Schematic



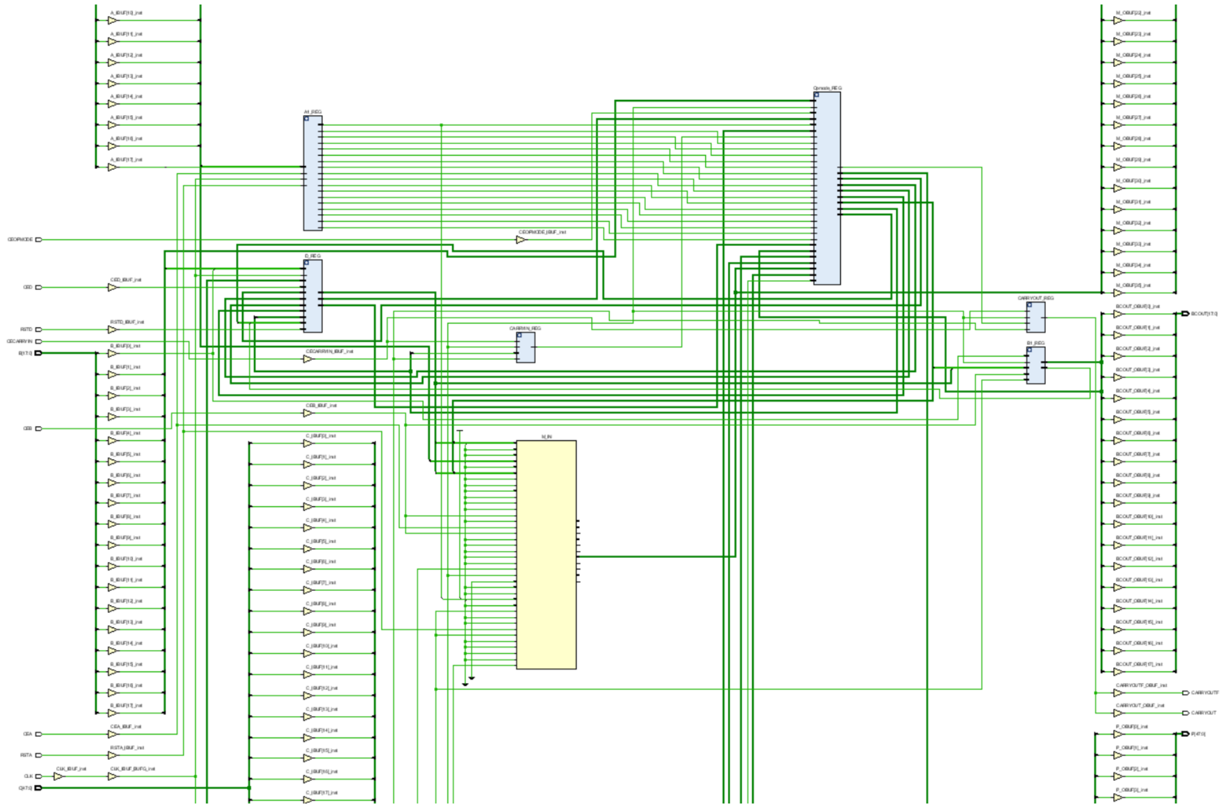
Messages



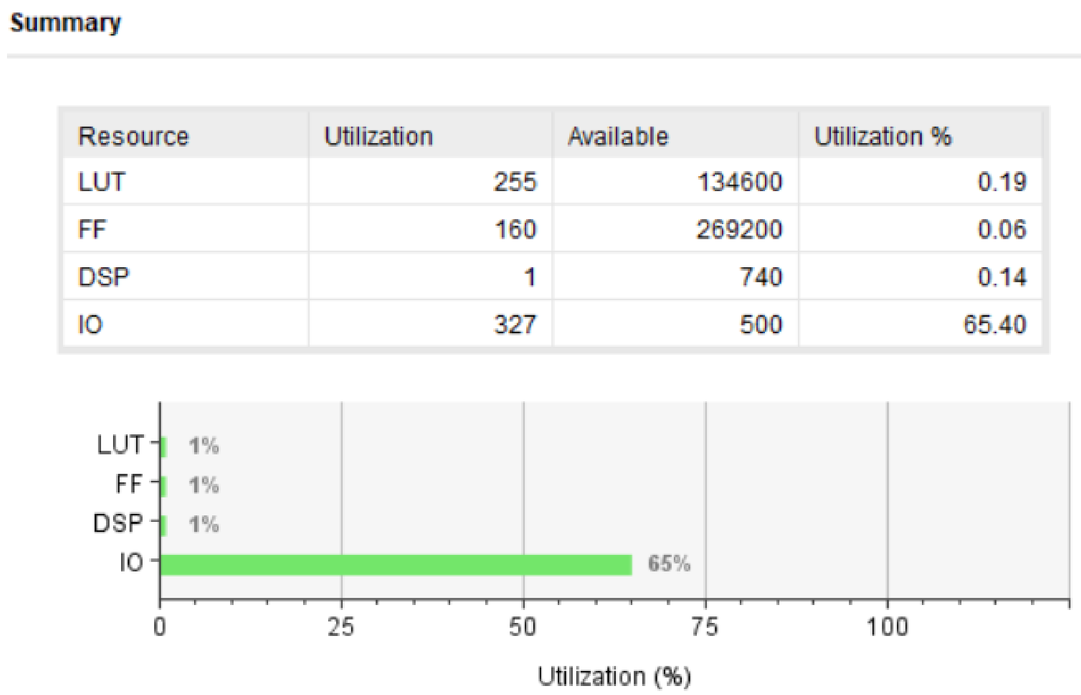
```
☑ Warning (91)   □ Info (218)   □ Status (381)   Show All
Elaborated Design (20 warnings)
    General Messages (20 warnings)
        [Synth 8-2490] overwriting previous definition of module DSP48A1 [DSP48A1.v:1]
        [Synth 8-3331] design DSP48A1 has unconnected port CARRYIN (18 more like this)
            [Synth 8-3331] design DSP48A1 has unconnected port BCIN[17]
            [Synth 8-3331] design DSP48A1 has unconnected port BCIN[16]
            [Synth 8-3331] design DSP48A1 has unconnected port BCIN[15]
            [Synth 8-3331] design DSP48A1 has unconnected port BCIN[14]
            [Synth 8-3331] design DSP48A1 has unconnected port BCIN[13]
            [Synth 8-3331] design DSP48A1 has unconnected port BCIN[12]
            [Synth 8-3331] design DSP48A1 has unconnected port BCIN[11]
            [Synth 8-3331] design DSP48A1 has unconnected port BCIN[10]
            [Synth 8-3331] design DSP48A1 has unconnected port BCIN[9]
            [Synth 8-3331] design DSP48A1 has unconnected port BCIN[8]
            [Synth 8-3331] design DSP48A1 has unconnected port BCIN[7]
            [Synth 8-3331] design DSP48A1 has unconnected port BCIN[6]
            [Synth 8-3331] design DSP48A1 has unconnected port BCIN[5]
            [Synth 8-3331] design DSP48A1 has unconnected port BCIN[4]
            [Synth 8-3331] design DSP48A1 has unconnected port BCIN[3]
            [Synth 8-3331] design DSP48A1 has unconnected port BCIN[2]
            [Synth 8-3331] design DSP48A1 has unconnected port BCIN[1]
            [Synth 8-3331] design DSP48A1 has unconnected port BCIN[0]
Synthesis (58 warnings)
```

Synthesis

Schematic



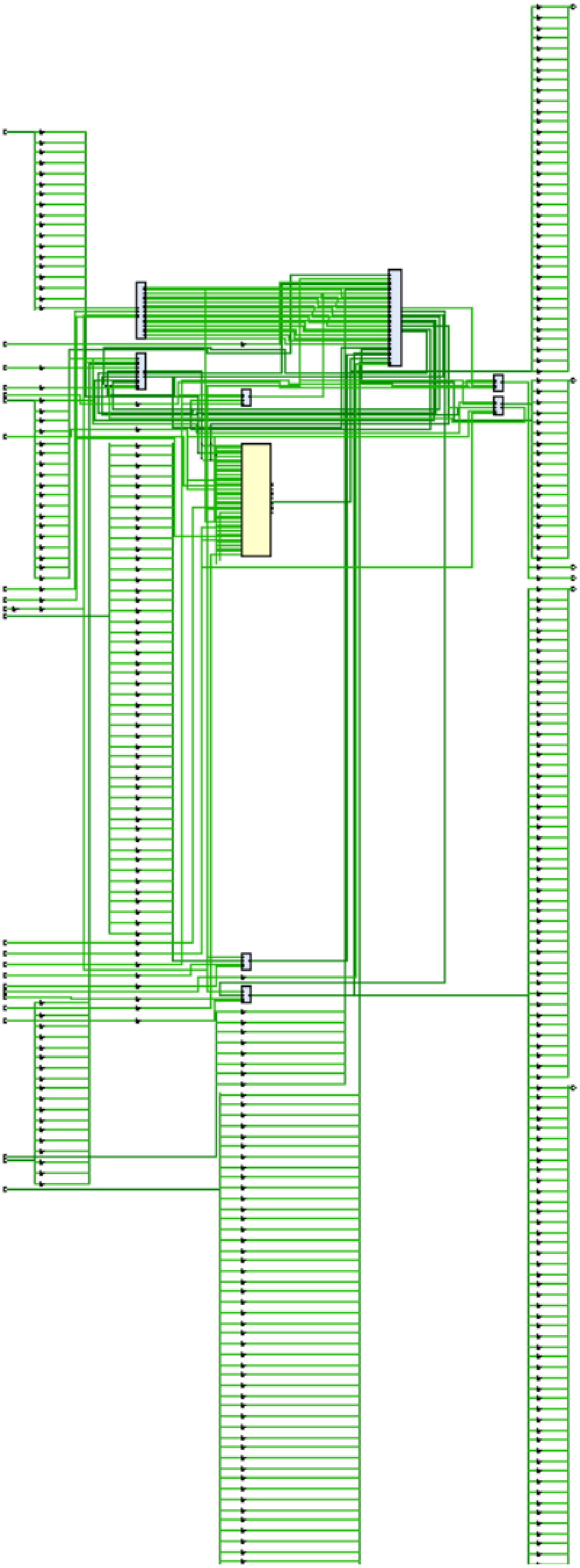
Utilization



Summary

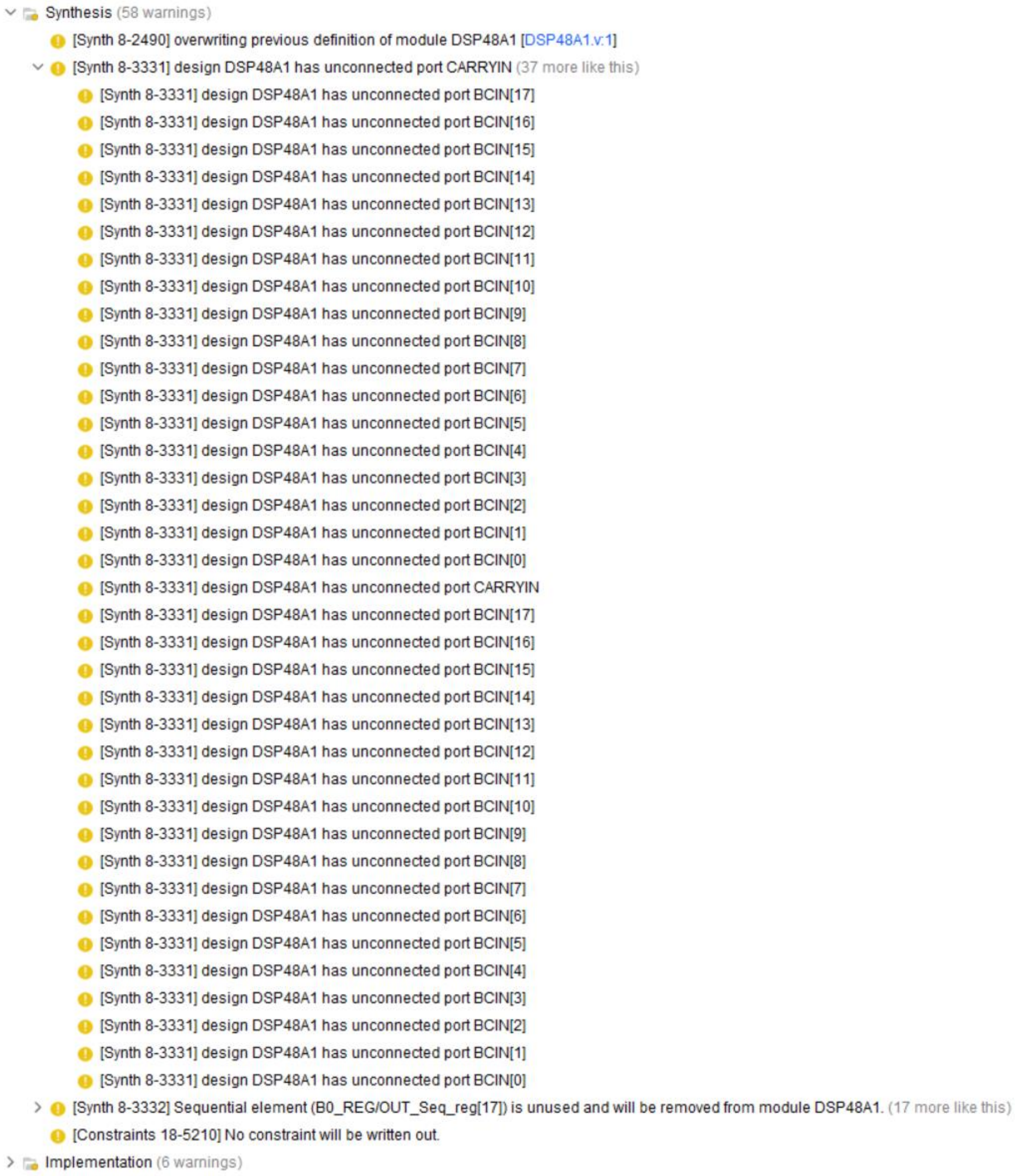
Resource	Utilization	Available	Utilization %
LUT	255	134600	0.19
FF	160	269200	0.06
DSP	1	740	0.14
IO	327	500	65.40

The Linter



The Linter

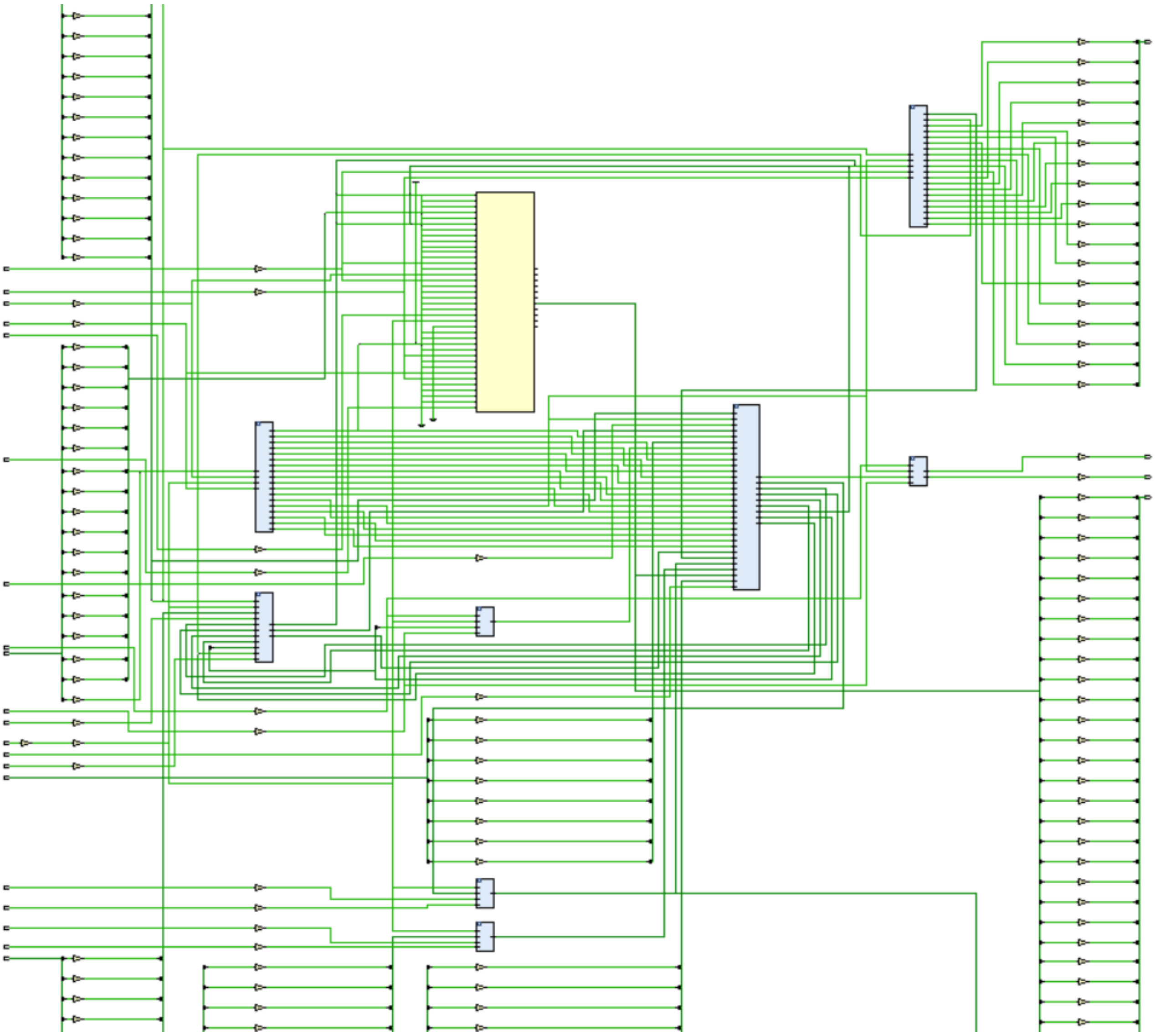
MESSAGES



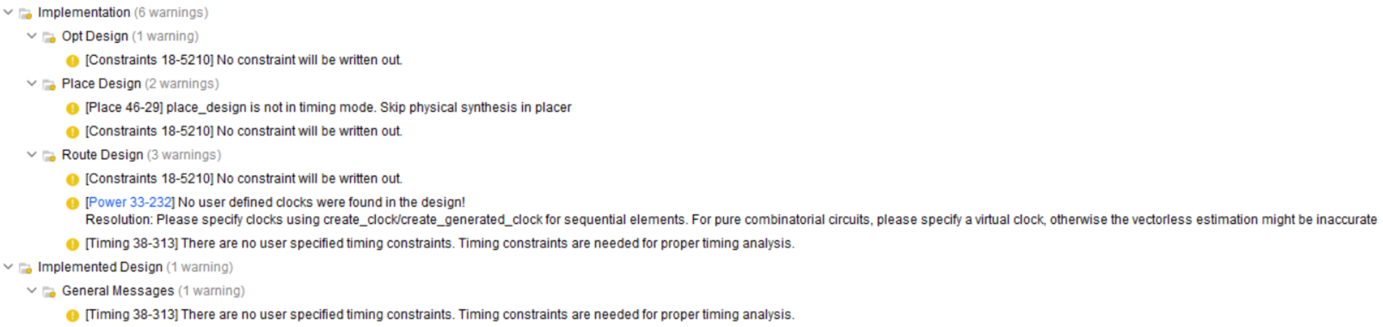
```
Synthesis (58 warnings)
    [Synth 8-2490] overwriting previous definition of module DSP48A1 [DSP48A1.v:1]
    [Synth 8-3331] design DSP48A1 has unconnected port CARRYIN (37 more like this)
        [Synth 8-3331] design DSP48A1 has unconnected port BCIN[17]
        [Synth 8-3331] design DSP48A1 has unconnected port BCIN[16]
        [Synth 8-3331] design DSP48A1 has unconnected port BCIN[15]
        [Synth 8-3331] design DSP48A1 has unconnected port BCIN[14]
        [Synth 8-3331] design DSP48A1 has unconnected port BCIN[13]
        [Synth 8-3331] design DSP48A1 has unconnected port BCIN[12]
        [Synth 8-3331] design DSP48A1 has unconnected port BCIN[11]
        [Synth 8-3331] design DSP48A1 has unconnected port BCIN[10]
        [Synth 8-3331] design DSP48A1 has unconnected port BCIN[9]
        [Synth 8-3331] design DSP48A1 has unconnected port BCIN[8]
        [Synth 8-3331] design DSP48A1 has unconnected port BCIN[7]
        [Synth 8-3331] design DSP48A1 has unconnected port BCIN[6]
        [Synth 8-3331] design DSP48A1 has unconnected port BCIN[5]
        [Synth 8-3331] design DSP48A1 has unconnected port BCIN[4]
        [Synth 8-3331] design DSP48A1 has unconnected port BCIN[3]
        [Synth 8-3331] design DSP48A1 has unconnected port BCIN[2]
        [Synth 8-3331] design DSP48A1 has unconnected port BCIN[1]
        [Synth 8-3331] design DSP48A1 has unconnected port BCIN[0]
        [Synth 8-3331] design DSP48A1 has unconnected port CARRYIN
        [Synth 8-3331] design DSP48A1 has unconnected port BCIN[17]
        [Synth 8-3331] design DSP48A1 has unconnected port BCIN[16]
        [Synth 8-3331] design DSP48A1 has unconnected port BCIN[15]
        [Synth 8-3331] design DSP48A1 has unconnected port BCIN[14]
        [Synth 8-3331] design DSP48A1 has unconnected port BCIN[13]
        [Synth 8-3331] design DSP48A1 has unconnected port BCIN[12]
        [Synth 8-3331] design DSP48A1 has unconnected port BCIN[11]
        [Synth 8-3331] design DSP48A1 has unconnected port BCIN[10]
        [Synth 8-3331] design DSP48A1 has unconnected port BCIN[9]
        [Synth 8-3331] design DSP48A1 has unconnected port BCIN[8]
        [Synth 8-3331] design DSP48A1 has unconnected port BCIN[7]
        [Synth 8-3331] design DSP48A1 has unconnected port BCIN[6]
        [Synth 8-3331] design DSP48A1 has unconnected port BCIN[5]
        [Synth 8-3331] design DSP48A1 has unconnected port BCIN[4]
        [Synth 8-3331] design DSP48A1 has unconnected port BCIN[3]
        [Synth 8-3331] design DSP48A1 has unconnected port BCIN[2]
        [Synth 8-3331] design DSP48A1 has unconnected port BCIN[1]
        [Synth 8-3331] design DSP48A1 has unconnected port BCIN[0]
    [Synth 8-3332] Sequential element (B0_REG/OUT_Seq_reg[17]) is unused and will be removed from module DSP48A1. (17 more like this)
    [Constraints 18-5210] No constraint will be written out.
Implementation (6 warnings)
```

Implementation

Schematic

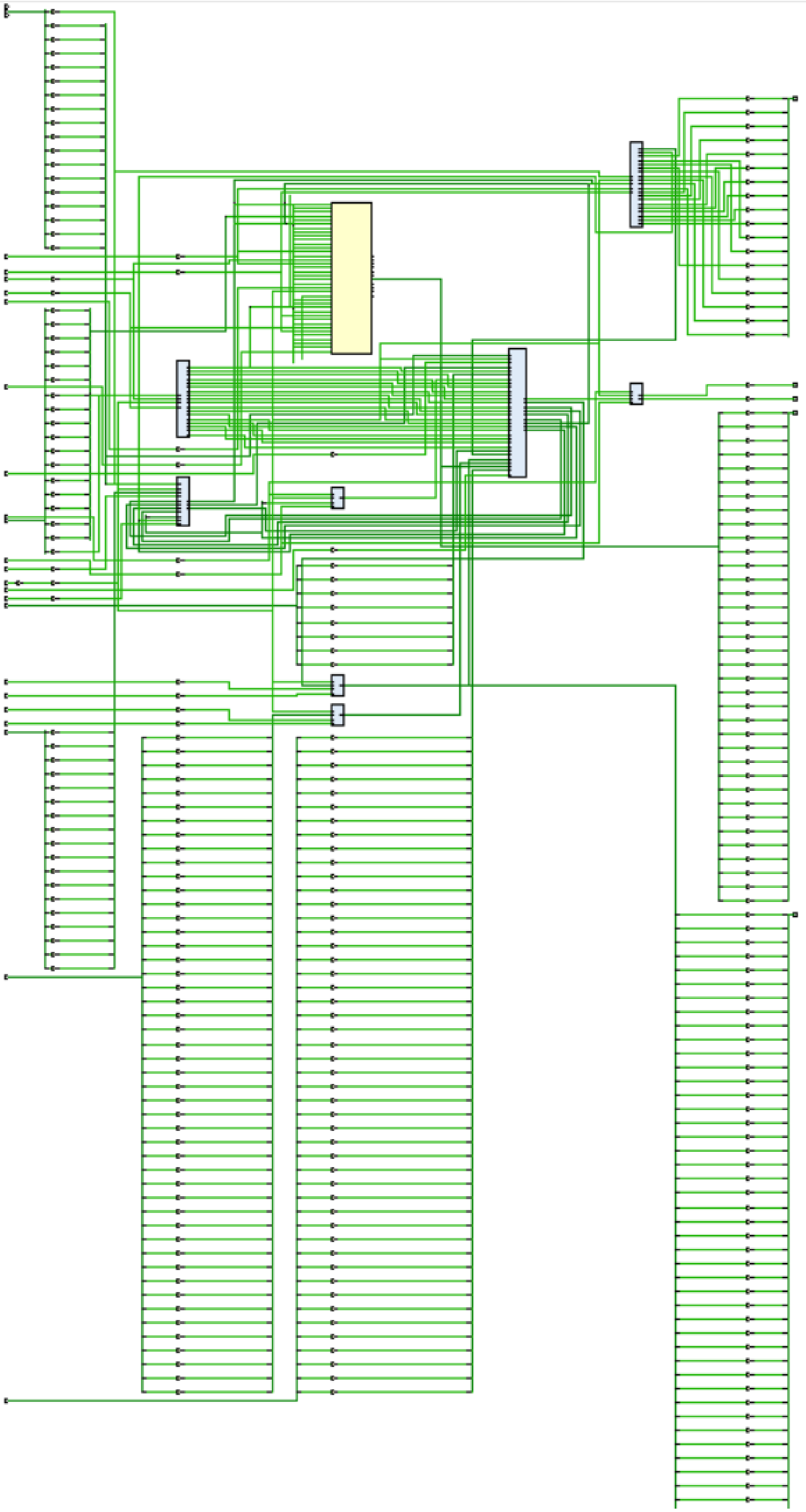


Messages

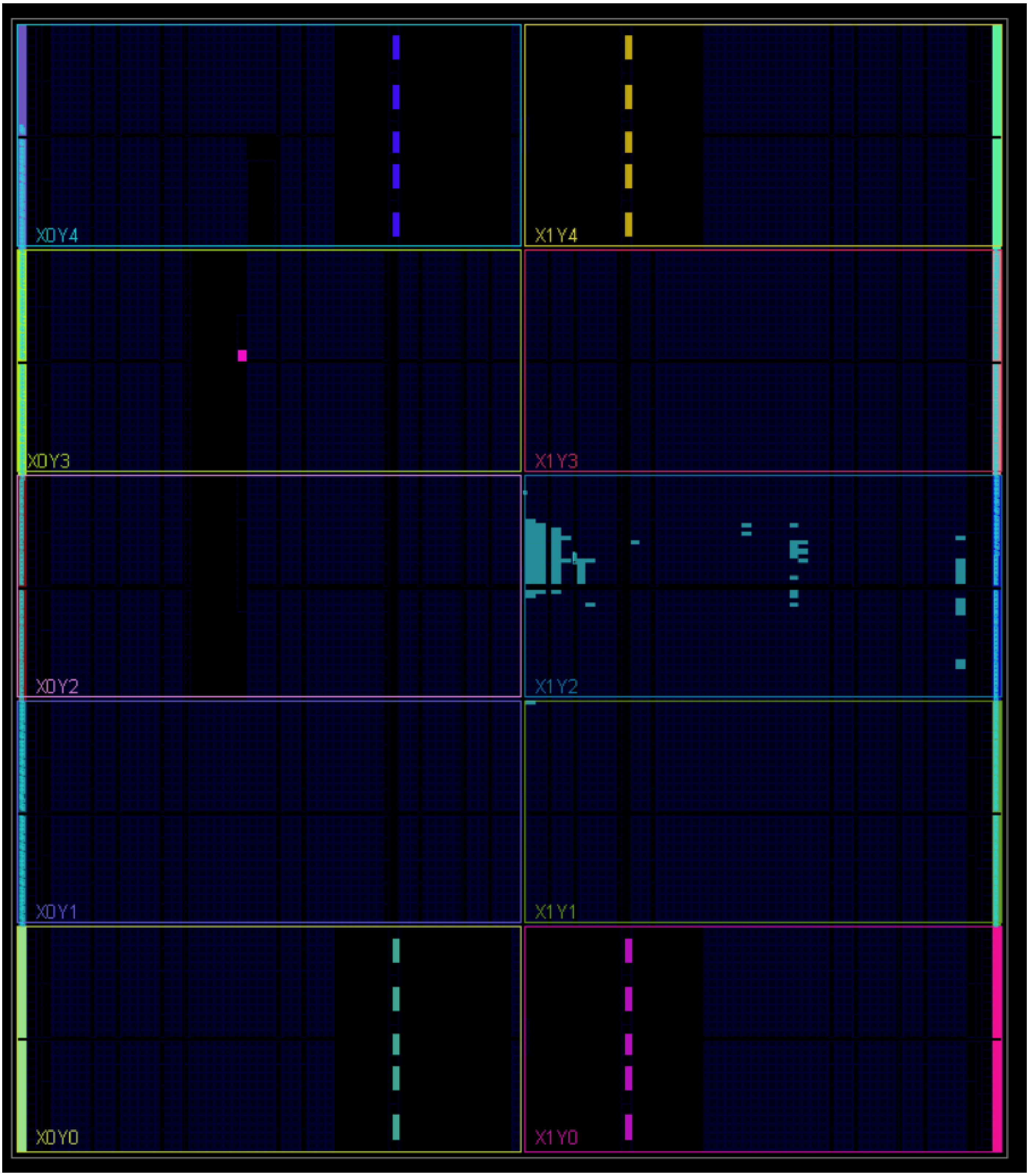


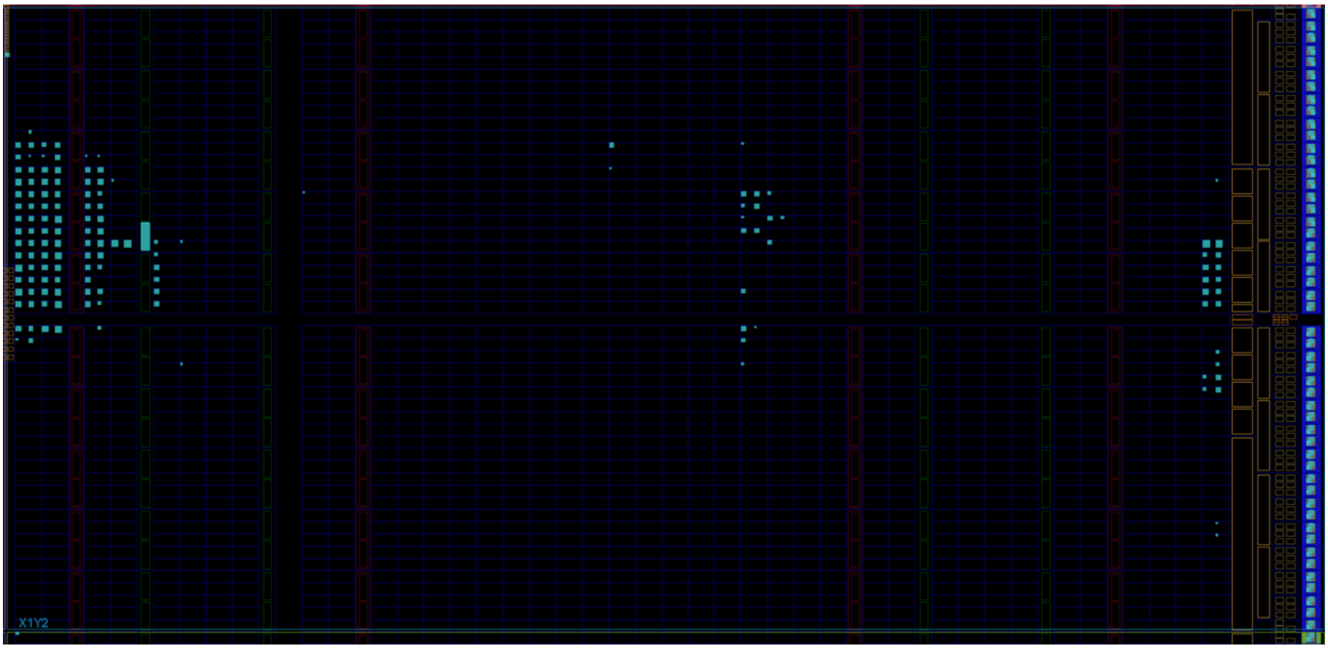
- Implementation (6 warnings)
  - Opt Design (1 warning)
    - [Constraints 18-5210] No constraint will be written out.
  - Place Design (2 warnings)
    - [Place 46-29] place_design is not in timing mode. Skip physical synthesis in placer
    - [Constraints 18-5210] No constraint will be written out.
  - Route Design (3 warnings)
    - [Constraints 18-5210] No constraint will be written out.
    - [Power 33-232] No user defined clocks were found in the design!
      Resolution: Please specify clocks using create_clock/create_generated_clock for sequential elements. For pure combinatorial circuits, please specify a virtual clock, otherwise the vectorless estimation might be inaccurate
    - [Timing 38-313] There are no user specified timing constraints. Timing constraints are needed for proper timing analysis.
- Implemented Design (1 warning)
  - General Messages (1 warning)
    - [Timing 38-313] There are no user specified timing constraints. Timing constraints are needed for proper timing analysis.

The Linter

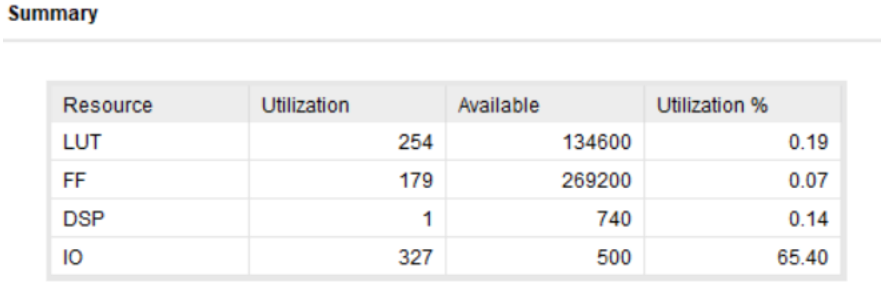


Device



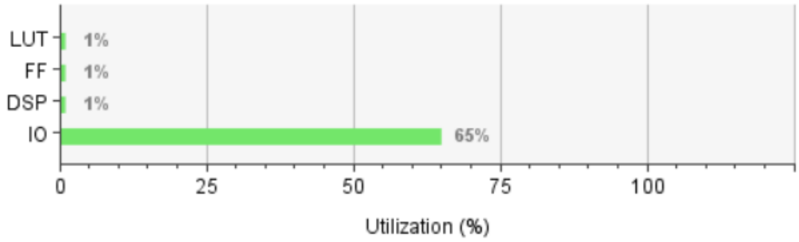


Utilization



Summary

Resource	Utilization	Available	Utilization %
LUT	254	134600	0.19
FF	179	269200	0.07
DSP	1	740	0.14
IO	327	500	65.40


LUT
FF
DSP
IO
Utilization (%)