Verification plan & Subroutines

Requirements for the assignment in both questions:

- Create a test plan (same as slide 26).
- Create a self-checking testbench either by calculating the correct result as done in the class or creating a golden reference in the testbench to check the functionality.
- Task for checking the normal operation of the design.
- Task for checking the reset functionality.
- Counters to keep track of the correct and error count. Display them by the end of your testbench.
- 100% design code coverage. Less than 100% must be justified.

1) ALU design will be provided and has the following characteristics.

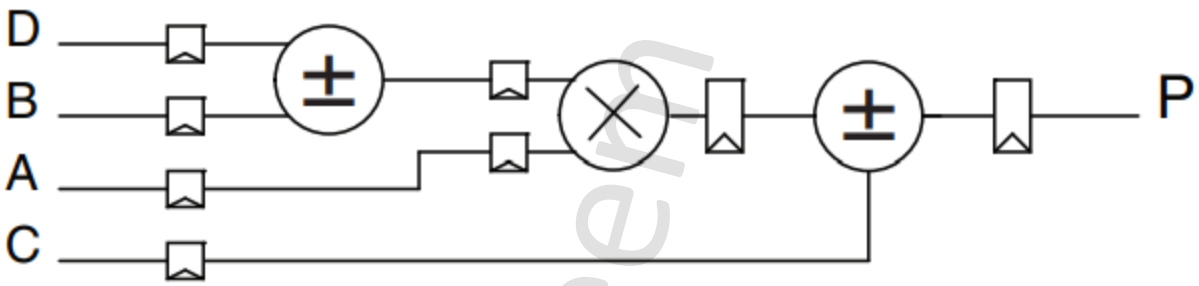
1. Reset which resets C to 0.
2. 4-bit signed inputs, A and B
3. 5-bit registered signed output C
4. 4 op-codes
   - add
   - sub (A-B)
   - bitwise invert input A
   - reduction OR input B

Assume the following encoding of the opcodes.

Opcode	**Encoding**
Add	2'b00
Sub	2'b01
bitwise invert input A	2'b10
reduction OR input B	2'b11

2) Verify the functionality of the following simplified version of the DSP block DSP48A1. All the registers are positive-edge triggered with the clock and have an async active low reset. Assume that we will only use the DSP in the addition mode only. For simplicity, you can drive the DSP inputs every 4 clock cycles to check the P output.

Note: it is an unsigned DSP block.



Port	Type	Width
A	Input	18
B	Input	18
C	Input	48
D	Input	18
Clk	Input	1
rst_n (async active low)	Input	1
P	Output	48

Parameters:

1. OPERATION: take 2 values either “ADD” or “SUBTRACT”, Default value “ADD”
    - When subtracting use “D - B” and “multiplier_out – C”. multiplier_out is an internal signal

Deliverables:

One .rar file having the following:

1. Design file
    a. If the design has bugs, then fix them otherwise upload the given design file.
2. Testbench file
3. Do file
4. Coverage report text file
    a. Add this option (-du <design_module_name>) to the coverage save command to save only the coverage of the design and exclude the testbench
    b. Add this option (-output coverage_rpt.txt) to the vcover command to save the coverage in external file
1. PDF having the following
    a. **Clear and neat** QuestaSim waveform snippets showing the functionality of the design with **each test plan item**
    b. Branch, statement and toggle coverage report snippets with justification if you could not reach 100% coverage for the designs.