Verification plan & Subroutines – Extra

1)

Verify the functionality of the following D-FF:

- **Inputs:** clk, rst (active high sync), d, en
- **Outputs:** q
- **Parameters:** USE_EN (if equals 1 then use the enable to update the q output when the reset is deasserted, else ignore the en input)

Since the design has a parameter, we need to verify the functionality of both modes when the USE_EN equals 1 and zero.

Requirements:

- You should create 2 testbenches (dff_t1_tb.sv & dff_t2_tb.sv) to verify the functionality of both modes.
- Use exhaustive test patterns where all combinations of inputs are tested using directed testing.
- Use a task to check the functionality of the design.
- Create a golden model reference (always block with to generate the correct expected functionality) inside of the testbench to compare the DUT output to your reference output.
- Use a do file
    - Compile the design and 2 testbenches
    - Run simulation for the first testbench
    - Close the simulation (quit -sim) to save the coverage database (dff_t1.ucdb) to test1
    - Run simulation for the second testbench
    - Close the simulation (quit -sim) to save the coverage database (dff_t2.ucdb) to test2
    - Use this command to merge the 2 databases generated
        - vcover merge dff_merged.ucdb dff_t1.ucdb dff_t2.ucdb -du dff
    - Generate a coverage report for the merged ucdb

Deliverables:

One .rar file having the following:

1. Design file
    a. If the design has bugs, then fix them otherwise upload the given design file.
2. Testbench file
3. Do file
4. Coverage report text file

    a. Add this option (-output coverage_rpt.txt) to the vcover command to save the coverage in external file

1. PDF having the following
    a. **Clear and neat** QuestaSim waveform snippets showing the functionality of the design with **each test plan item**
    b. Branch, statement and toggle coverage report snippets with justification if you could not reach 100% coverage for the designs.