SVA Assignment

Q1. Write assertions for the following:

1) Write assert statement for signal a is high in a positive edge of a clock then signal b should be high after 2 clock cycles
2) Write a sequence s11a, where signal a is high and signal b is high and then signal c is high 1 to 3 clock cycle later
3) Write a sequence s11b, after 2 positive clock edges, signal b should be low
4) Write a property that check that if sequence s11a occurs then s11b will occur
5) Write a property that checks on a positive clock edge, if signal a is high then signal b should be eventually high from the next clock cycle, then after that signal c should be eventually high starting the same clock cycle in which signal b was high

Q2. Write an assertion to make sure that 3to8 decoder output is only one bit high with every clock cycle.

Q3. Verify the functionality of counter provided in the assignment 3 – extra pdf by adding assertions to the design. The reset of the design has changed to asynchronous.

Assertion to be added in a new file based on the following specs to be checked:

1. When the load control signal is active, then the dout has the value of the din
2. When the load control signal is not active and the enable is off then the dout does not change
3. When the load control signal is not active and the enable is active, and the up_down is high then the dout is incremented.
4. When the load control signal is not active and the enable is active, and the up_down is low then the dout is decremented.
5. When the asynchronous reset is asserted then the counter output is tied to low at the same instant. Note that you can use assert final to sample the new value of a signal.
6. max_count output is high when the counter output is maximum.
7. zero output is high when the counter output is zero.

<u>Requirements for Q3:</u>

1- Create an interface with DUT and TEST modports
2- Create a top module where clock gen will take place and connections of interface
3- Create SVA module and bind it in the top module
4- Create the testbench as instructed in assignment 3 – extra pdf

5- Adjust your verification requirements document in the the functionality check column, add if the requirement is checked against golden model, assertion or both. In case of assertion then mention its label used in your SVA module

Deliverables:

One PDF file having the following.

1. Testbench code
2. Package code
3. Design code
4. Snippet to your verification requirement document
5. Do file
6. Code Coverage & Functional Coverage report snippets
7. QuestaSim snippets