Digital FPGA Internship 2025 - **Project**

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$$Z = real + imag \times i$$

$$P_z = Z \times Z^* = real^2 + imag^2$$

$$P_{dB} = 10\log_{10}(P_z) = \frac{10}{\log_2(10)} \times \log_2(P_z)$$

Complex Power Calculation

1. Function Description

The Power Block computes the instantaneous signal power of a complex input $(x + jy)$using one multiplier and one adder.

It performs the operation:

$$\text{Power} = x^2 + y^2$$

where x and y are the real and imaginary parts of the input signal, respectively.

The design registers inputs, squares each component using the shared multiplier, accumulates results using the adder, and produces a valid output after a fixed number of clock cycles.

It is optimized for hardware efficiency, minimizing area by reusing arithmetic units rather than parallelizing them.

2. Signals SPECS Table

Signal Name	Direction	Bit Width	Description
clk	Input	1	System clock signal: all operations are synchronized to the rising edge.
rstn	Input	1	Active-low ASYNCH reset signal clears registers and internal signals.
enable_in	Input	1	Enables the processing of new input samples when asserted high.
real_in	Input	IN_WIDTH (default 16)	Signed real component of the complex input signal.
imag_in	Input	IN_WIDTH (default 16)	Signed imaginary component of the complex input signal.
power_out	Output	2*IN_WIDTH (default 32)	Unsigned output representing the computed power $x^2 + y^2$
valid_out	Output	1	Indicates that power_out contains a valid result (asserted high).

3. Mathematical Description

Given a complex input signal:

$$Z = \text{real\_in} + j \times \text{imag\_in}$$

The power of the signal is defined as the product of the signal and its conjugate:

$$P = Z \times Z^* = (\text{real\_in} + j \times \text{imag\_in})(\text{real\_in} - j \times \text{imag\_in})$$

Expanding the expression: $P = \text{real\_in}^2 + \text{imag\_in}^2$
Thus, the **Power Block** performs: $\text{power\_out} = \text{real\_in}^2 + \text{imag\_in}^2$

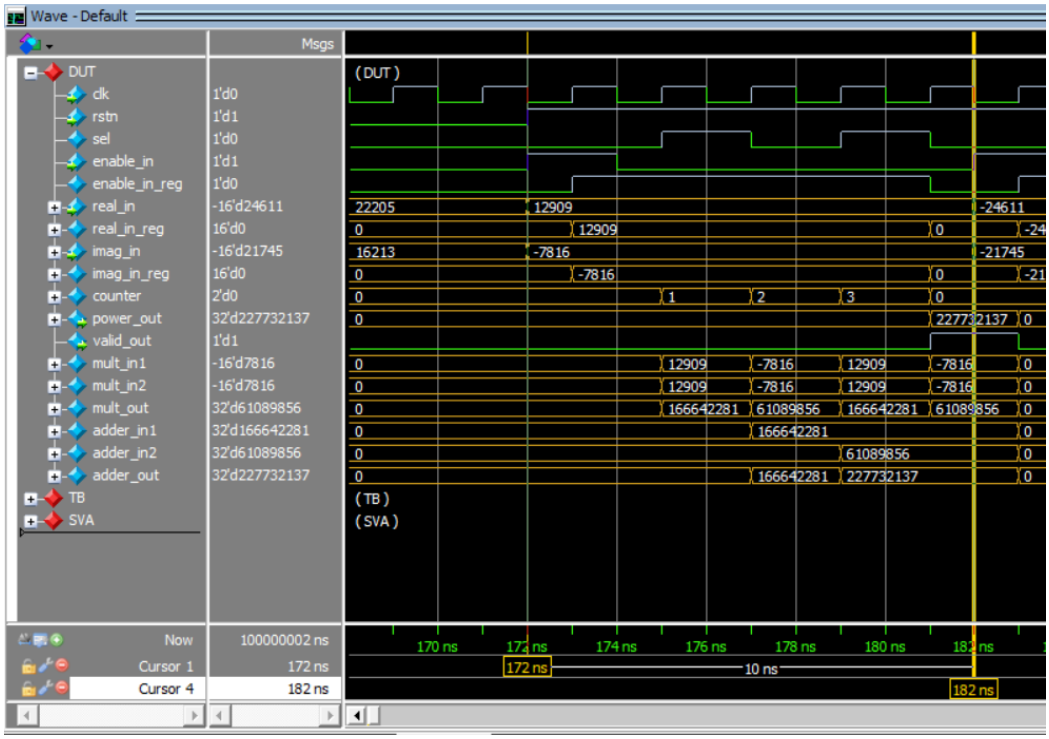
and asserts valid_out = 1 when the computation completes.

4. Key Design Features

- Single Multiplier and Adder Architecture: Reduces hardware area by time-multiplexing arithmetic operations.
- Sequential Pipelined Execution: Computes real and imaginary squares over multiple clock cycles.
- Signed Inputs and Unsigned Output: Accepts signed integer inputs (real_in, imag_in) and generates an unsigned integer output (power_out).
- Initial Latency: Produces the first valid output **after 5 clock cycles** from the assertion of enable_in.
- Asynchronous Reset: Utilizes an active-low asynchronous reset (rstn) to clear all registers immediately.
- Parameterizable Input Width (IN_WIDTH): Scalable design supporting variable input precision.
- Fully Synchronous Data Path: All computations are triggered by the rising edge of clk.

5. RTL Design Simulation

Questa-Simulation Waveform



As shown in the figure, when enable_in is asserted for one clock cycle at 172 ns, the internal signal enable_in_reg remains active for four clock cycles to perform the power computation. In the fifth cycle (at 182 ns), the valid_out signal is asserted, indicating that the power output has been successfully calculated. Thus, the design requires 10 ns (5 clock cycles) to complete power computation.

Code, Functional, and SVA Coverage Percentage

```
================================================================================
=== Design Unit: work.power
================================================================================
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                        28        28         0   100.00%
    Conditions                       3         3         0   100.00%
    Statements                      46        46         0   100.00%
    Toggles                        272       272         0   100.00%


Total Coverage By Design Unit (filtered view): 100.00%

TOTAL COVERGROUP COVERAGE: 100.00%  COVERGROUP TYPES: 1
```

6. FPGA Simulation and Implementation Results Summary

Target Device Information

Parameter	Value
FPGA Family	Cyclone 10 LP
Device Part Number	10CL010YE144I7G
Package	EQFP-144
Speed Grade	7
Tool Used	Intel® Quartus® Prime Lite Edition
Simulation Environment	ModelSim – Intel FPGA Edition

Timing Constraints Summary

The SDC constraints ensure reliable 150 MHz timing with proper I/O margins, excluding the asynchronous reset (rstn) from timing analysis.

```
# Create Clock
create_clock -name clk -period 6.667 -waveform {0 3.334} [get_ports clk];

# Set false paths for Asynchronous signals
set_false_path -from [get_ports rstn];

# Set Input Delay
set_input_delay -max 0.10 -clock [get_clocks clk] [get_ports {real_in imag_in enable_in}];
# Set input delay for setup analysis
set input delay -min 0.05 -clock [get clocks clk] [get ports {real in imag in enable in}];
# Set input delay for hold analysis

# Set Output Delay
set output delay -max 0.10 -clock [get clocks clk] [get ports {power out valid out}];
# Set output delay for setup analysis
set output delay -min 0.05 -clock [get clocks clk] [get ports {power out valid out}];
# Set output delay for hold analysis
```

Quartus Automated TCL Build Commands

To automate the synthesis and analysis process, the following Quartus TCL script was used:

```
# Create the Project
project_new power -overwrite

# Declare FPGA family, Device, Top level file
set_global_assignment -name FAMILY "Cyclone 10 LP"
set_global_assignment -name DEVICE 10CL010YE144I7G
set_global_assignment -name VERILOG_FILE adder.v
set_global_assignment -name VERILOG_FILE multiplier.v
set_global_assignment -name VERILOG_FILE power.v
set_global_assignment -name SDC_FILE Timing_Constraints.sdc
set_global_assignment -name TOP_LEVEL_ENTITY power
```

Project Summary

Timing Analyzer Summary

<<Filter>>

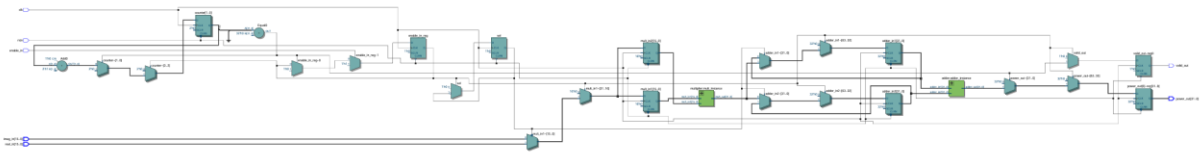
Quartus Prime Version	Version 24.1std.0 Build 1077 03/04/2025 SC Lite Edition
Timing Analyzer	Timing Analyzer
Revision Name	power
Device Family	Cyclone 10 LP
Device Name	10CL010YE144I7G
Timing Models	Final
Delay Model	Combined
Rise/Fall Delays	Enabled

Operating Frequency

Clocks

<<Filter>>

	Clock Name	Type	Period	Frequency	Rise	Fall	Duty Cycle
1	clk	Base	6.667	149.99 MHz	0.000	3.334	



Maximum Frequency

Slow 1200mV 100C Model Fmax Summary

<<Filter>>

	Fmax	Restricted Fmax	Clock Name	Note
1	178.7 MHz	178.7 MHz	clk	

Utilization

Analysis & Synthesis Summary

<<Filter>>

Analysis & Synthesis Status	Successful - Sun Oct 12 22:18:07 2025
Quartus Prime Version	24.1std.0 Build 1077 03/04/2025 SC Lite Edition
Revision Name	power
Top-level Entity Name	power
Family	Cyclone 10 LP
Total logic elements	135
Total registers	133
Total pins	68
Total virtual pins	0
Total memory bits	0
Embedded Multiplier 9-bit elements	2
Total PLLs	0

Setup Slack

Slow 1200mV 100C Model Setup Summary

<<Filter>>

	Clock	Slack	End Point TNS
1	clk	1.071	0.000

Hold Slack

Slow 1200mV 100C Model Hold Summary

<<Filter>>

	Clock	Slack	End Point TNS
1	clk	0.416	0.000

Power in dB - Implement $10.\log_{10}(x)$ from $\log_2(x)$

1. Function Description

The Power in dB Block computes the logarithmic power (in decibels) of a given input value using a base-2 logarithm approximation.

Instead of directly implementing $\log_{10}(x)$, the design efficiently derives it from $\log_2(x)$ using the mathematical relation:

$$10\log_{10}(x) = \frac{10}{\log_2(10)} \times \log_2(x)$$

The module internally instantiates the Log2 Block to compute the base-2 logarithm of the input and then scales the result to produce the power in decibels (power_dB_out).
This implementation is optimized for fixed-point arithmetic and hardware efficiency, making it suitable for FPGA-based digital signal processing applications such as power measurement, spectrum analysis, and communication PHY layers.

2. Signals SPECS Table

Signal Name	Direction	Bit Width	Description
clk	Input	1	System clock signal: all operations are synchronized to the rising edge.
rstn	Input	1	Active-low ASYNCH reset signal clears registers and internal signals.
enable_in	Input	1	Enables the processing of new input samples when asserted high.
Log10 in	Input	WIDTH (default 32)	Input linear power value to be converted to dB scale.
Log10_out	Output	WIDTH (default 32)	Output represents $10\log_{10}(\log_2\_out)$.
valid_out	Output	1	Indicates that 10.log10_out contains a valid result (asserted high).

3. Mathematical Description

The power in decibels is mathematically defined as:

$$P_{dB} = 10\log_{10}(P)$$

Using the logarithmic base conversion formula:

$$\log_{10}(P) = \frac{\log_2(P)}{\log_2(10)}$$

Therefore: $$P_{dB} = \frac{10}{\log_2(10)} \times \log_2(P)$$

Given that $\log_2(10) \approx 3.321928$, the scaling factor becomes:

$$\frac{10}{\log_2(10)} \approx 3.0103$$

Hence, the implemented hardware operation is:

$$\text{power\_dB\_out} = 3.0103 \times \log2(\text{power\_in})$$

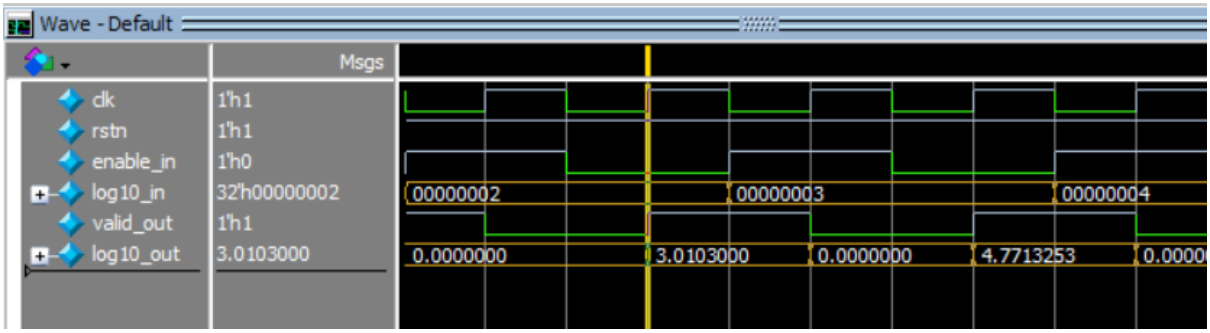
The Log2 Block provides the base-2 logarithmic result, which is then multiplied by a constant coefficient (≈ 3.0103) to produce the final decibel output.

4. Key Design Features

- **Derived Log10 from Log2:** Efficiently computes $10\log_{10}(x)$ using the base2 logarithm to reduce implementation complexity.
- **Fixed-Point Arithmetic:** Supports Q-format (e.g., Q8.24) representation for precision in FPGA-friendly arithmetic.
- **Resource Efficiency:** Reuses the existing Log2 computation block, minimizing DSP and logic element utilization.
- **Scalable Design:** Parameterized input width (WIDTH) for flexible precision control.
- **Latency:** Produces a valid output after a fixed number of clock cycles (same as the internal log2 block latency = 2 clock cycle).

5. RTL Design Simulation

Waveform Shown $10.\log_{10}(3) \approx 3.0103$



Questa-Simulation Transcript

```
# log2_out[0] = 0.0
# log2_out[1] = 0.0
# log2_out[2] = 1.0
# log2_out[3] = 1.5850
# log2_out[4] = 2.0
# log2_out[5] = 2.3219
# log2_out[6] = 2.5850
# log2_out[7] = 2.8074
# log2_out[8] = 3.0
# log2_out[9] = 3.1699
# log2_out[10] = 3.3219
# log2_out[11] = 3.4594
# log2_out[12] = 3.5850
# log2_out[13] = 3.7004
# log2_out[14] = 3.8074
# log2_out[15] = 3.9069
# log2_out[16] = 4.0
# log2_out[17] = 4.875
# log2_out[18] = 4.1699
# log2_out[19] = 4.2479
# log2_out[20] = 4.3219
# log2_out[21] = 4.3923
# log2_out[22] = 4.4594
# log2_out[23] = 4.5236
# log2_out[24] = 4.5850
# log2_out[25] = 4.6439
# log2_out[26] = 4.7004
# log2_out[27] = 4.7549
# log2_out[28] = 4.8074
# log2_out[29] = 4.8580
# log2_out[30] = 4.9069
# log2_out[31] = 4.9542
# log2_out[32] = 5.0
# log2_out[33] = 5.444
# log2_out[34] = 5.875
# log2_out[35] = 5.1293
# log2_out[36] = 5.1699
# log2_out[37] = 5.2095
# log2_out[38] = 5.2479
# log2_out[39] = 5.2854
# log2_out[40] = 5.3219
# log2_out[41] = 5.3576
# log2_out[42] = 5.3923
# log2_out[43] = 5.4263
# log2_out[44] = 5.4594
# log2_out[45] = 5.4919
# log2_out[46] = 5.5236
# log2_out[47] = 5.5546
# log2_out[48] = 5.5850
# log2_out[49] = 5.6147
# log2_out[50] = 5.6439
```

```
# 10.log10_out[0] = 0.000000
# 10.log10_out[1] = 0.000000
# 10.log10_out[2] = 3.010300
# 10.log10_out[3] = 4.771325
# 10.log10_out[4] = 6.020600
# 10.log10_out[5] = 6.989615
# 10.log10_out[6] = 7.781625
# 10.log10_out[7] = 8.451116
# 10.log10_out[8] = 9.030900
# 10.log10_out[9] = 9.542350
# 10.log10_out[10] = 9.999915
# 10.log10_out[11] = 10.413832
# 10.log10_out[12] = 10.791925
# 10.log10_out[13] = 11.139314
# 10.log10_out[14] = 11.461416
# 10.log10_out[15] = 11.760941
# 10.log10_out[16] = 12.041200
# 10.log10_out[17] = 12.304601
# 10.log10_out[18] = 12.552650
# 10.log10_out[19] = 12.787453
# 10.log10_out[20] = 13.010215
# 10.log10_out[21] = 13.222140
# 10.log10_out[22] = 13.424132
# 10.log10_out[23] = 13.617393
# 10.log10_out[24] = 13.802225
# 10.log10_out[25] = 13.979532
# 10.log10_out[26] = 14.149614
# 10.log10_out[27] = 14.313675
# 10.log10_out[28] = 14.471716
# 10.log10_out[29] = 14.624037
# 10.log10_out[30] = 14.771241
# 10.log10_out[31] = 14.913628
# 10.log10_out[32] = 15.051500
# 10.log10_out[33] = 15.185157
# 10.log10_out[34] = 15.314901
# 10.log10_out[35] = 15.440732
# 10.log10_out[36] = 15.562950
# 10.log10_out[37] = 15.682158
# 10.log10_out[38] = 15.797753
# 10.log10_out[39] = 15.910639
# 10.log10_out[40] = 16.020515
# 10.log10_out[41] = 16.127983
# 10.log10_out[42] = 16.232440
# 10.log10_out[43] = 16.334791
# 10.log10_out[44] = 16.434432
# 10.log10_out[45] = 16.532266
# 10.log10_out[46] = 16.627693
# 10.log10_out[47] = 16.721012
# 10.log10_out[48] = 16.812525
# 10.log10_out[49] = 16.901931
# 10.log10_out[50] = 16.989832
```

6. FPGA Simulation and Implementation Results Summary

Target Device Information

Parameter	Value
FPGA Family	MAX 10
Device Part Number	10M50DAF484C7G
Tool Used	Intel® Quartus® Prime Lite Edition
Simulation Environment	ModelSim – Intel FPGA Edition

Timing Constraints Summary

The SDC constraints ensure reliable 50 MHz timing with proper I/O margins, excluding the asynchronous reset (rstn) from timing analysis.

```
# Create Clock
create_clock -name clk -period 20 -waveform {0 10} [get_ports clk] ;

# Set false paths for Asynchronous signals
set  false  path -from [get  ports rstn] ;
```

Project Summary

Timing Analyzer Summary

<<Filter>>

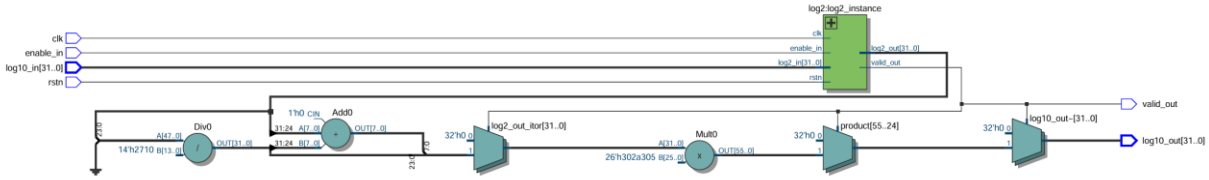
Quartus Prime Version	Version 24.1std.0 Build 1077 03/04/2025 SC Lite Edition
Timing Analyzer	Legacy Timing Analyzer
Revision Name	dB_10log10
Device Family	MAX 10
Device Name	10M50DAF484C7G
Timing Models	Final
Delay Model	Combined
Rise/Fall Delays	Enabled

Operating Frequency

Clocks

<<Filter>>

	Clock Name	Type	Period	Frequency	Rise	Fall
1	clk	Base	20.000	50.0 MHz	0.000	10.000



Maximum Frequency

Slow 1200mV 85C Model Fmax Summary

<<Filter>>

	Fmax	Restricted Fmax	Clock Name
1	52.34 MHz	52.34 MHz	clk

Utilization

Analysis & Synthesis Summary

<<Filter>>

Analysis & Synthesis Status	Successful - Tue Oct 28 17:29:42 2025
Quartus Prime Version	24.1std.0 Build 1077 03/04/2025 SC Lite Edition
Revision Name	dB_10log10
Top-level Entity Name	dB_10log10
Family	MAX 10
Total logic elements	13,173
Total registers	6711
Total pins	68
Total virtual pins	0
Total memory bits	0
Embedded Multiplier 9-bit elements	8
Total PLLs	0
UFM blocks	0
ADC blocks	0

Setup Slack

Slow 1200mV 85C Model Setup Summary

<<Filter>>

	Clock	Slack	End Point TNS
1	clk	0.893	0.000

Hold Slack

Slow 1200mV 85C Model Hold Summary

<<Filter>>

	Clock	Slack	End Point TNS
1	clk	1.006	0.000