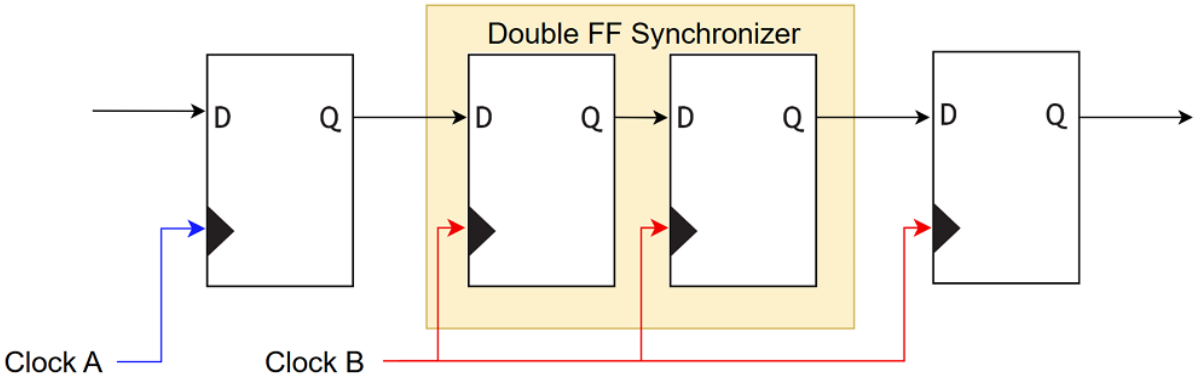
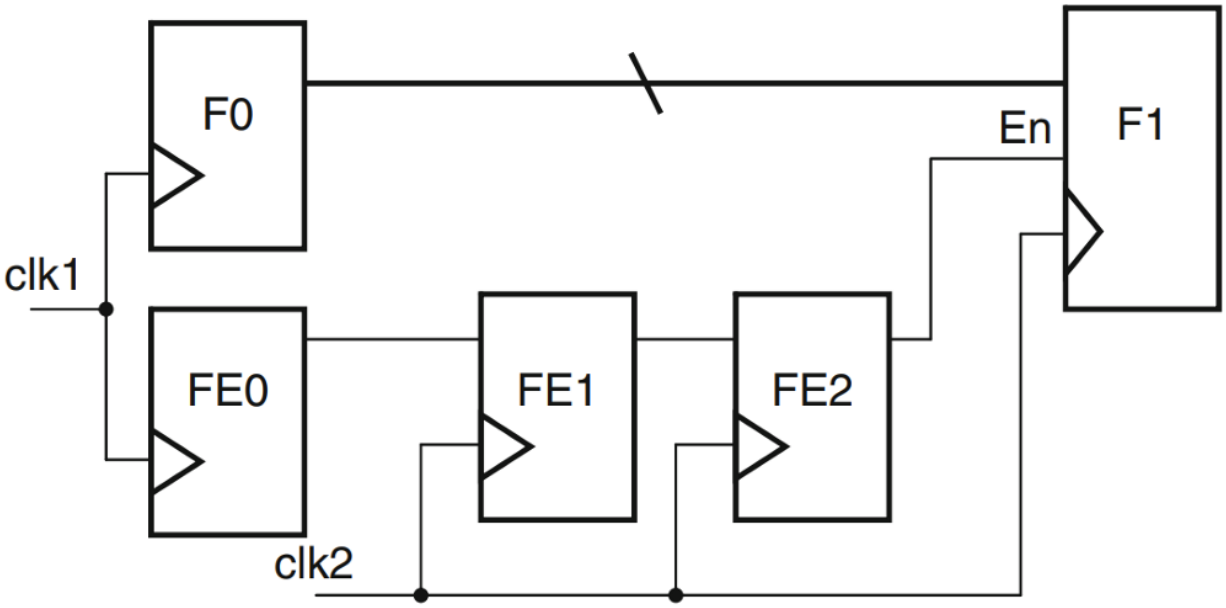
Submit a ZIP file that contains for each one of these CDC circuits

- Verilog codes
- Testbench codes
- Screanshots for simulation waveforms

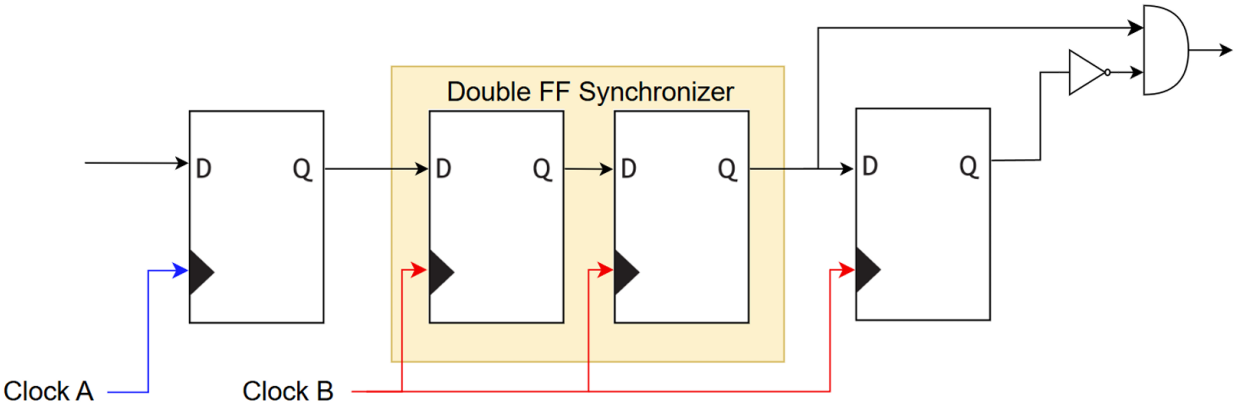
1. Double FF synchronizer.



2. Enable-based synchronizer.



3. Slow to fast pulse to pulse synchronizer.



4. Fast to slow pulse to pulse synchronizer.