

File Edit View Project Assignments Processing Tools Window Help

qsys_control

Project Navigator

Files

- BeMicro_Max10_top.bdf
- qsys_control.sdc
- nios2_control/synthesis/nios2_control.qip
- BeMicro_MAX10_top.sdc

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Flow Summary

<<Filter>>

Flow Status	Successful - Fri Aug 11 16:33:22 2023
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	qsys_control
Top-level Entity Name	BeMicro_Max10_top
Family	MAX 10
Device	10M08DAF484C8GES
Timing Models	Preliminary
Total logic elements	4,796 / 8,064 (59 %)
Total registers	2835
Total pins	13 / 250 (5 %)
Total virtual pins	0
Total memory bits	80,664 / 387,072 (21 %)
Embedded Multiplier 9-bit elements	6 / 48 (13 %)
Total PLLs	1 / 2 (50 %)
UFM blocks	1 / 1 (100 %)
ADC blocks	0 / 1 (0 %)

Tasks

Compilation

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate programming files)
- Timing Analysis
- EDA Netlist Writer
- Edit Settings

Messages

Type ID Message

293000 Quartus Prime Full Compilation was successful. 0 errors, 283 warnings

System (3) Processing (482)

100% 00:01:35

4:34 PM

8/11/2023

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