

Quartus Prime Lite Edition - C:/AlteraPrj/pipemultQP16_1M4V4/Schematic/pipemult - pipemult2

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project Navigator

Entity: Instance

MAX 10: 10M08DAF484C8GES

pipemult

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Slow 1200mV 85C Model Fmax Summary

	Fmax	Restricted Fmax	Clock Name	Note
1	35.11 MHz	35.11 MHz	clk1	

This panel reports FMAX for every clock in the design, regardless of the user-specified clock periods. FMAX is only computed for paths where the source and destination registers or ports are driven by the same clock. Paths of different clocks, including generated clocks, are ignored. For paths between a clock and its inversion, FMAX is computed as if the rising and falling edges

IP Catalog

- Installed IP
 - Project Directory
 - No Selection Available
 - Library
 - Basic Functions
 - Arithmetic
 - Bridges and Adaptors
 - Clocks; PLLs and Resets
 - Configuration and Programming
 - I/O
 - Miscellaneous
 - On Chip Memory
 - Simulation; Debug and Verification
 - DSP
 - Interface Protocols
 - Memory Interfaces and Controllers
 - Processors and Peripherals
 - University Program
- Search for Partner IP

tasks

Compilation

- Task
 - Compile Design
 - Analysis & Synthesis
 - Fitter (Place & Route)
 - Assembler (Generate programming files)
 - Timing Analysis
 - Edit Settings
 - View Report

Messages

System Processing (18)

Quartus Prime Shell was successful. 0 errors, 1 warning

Magdy Ahmed

100% 00:00:06 8:51 PM 8/11/2023