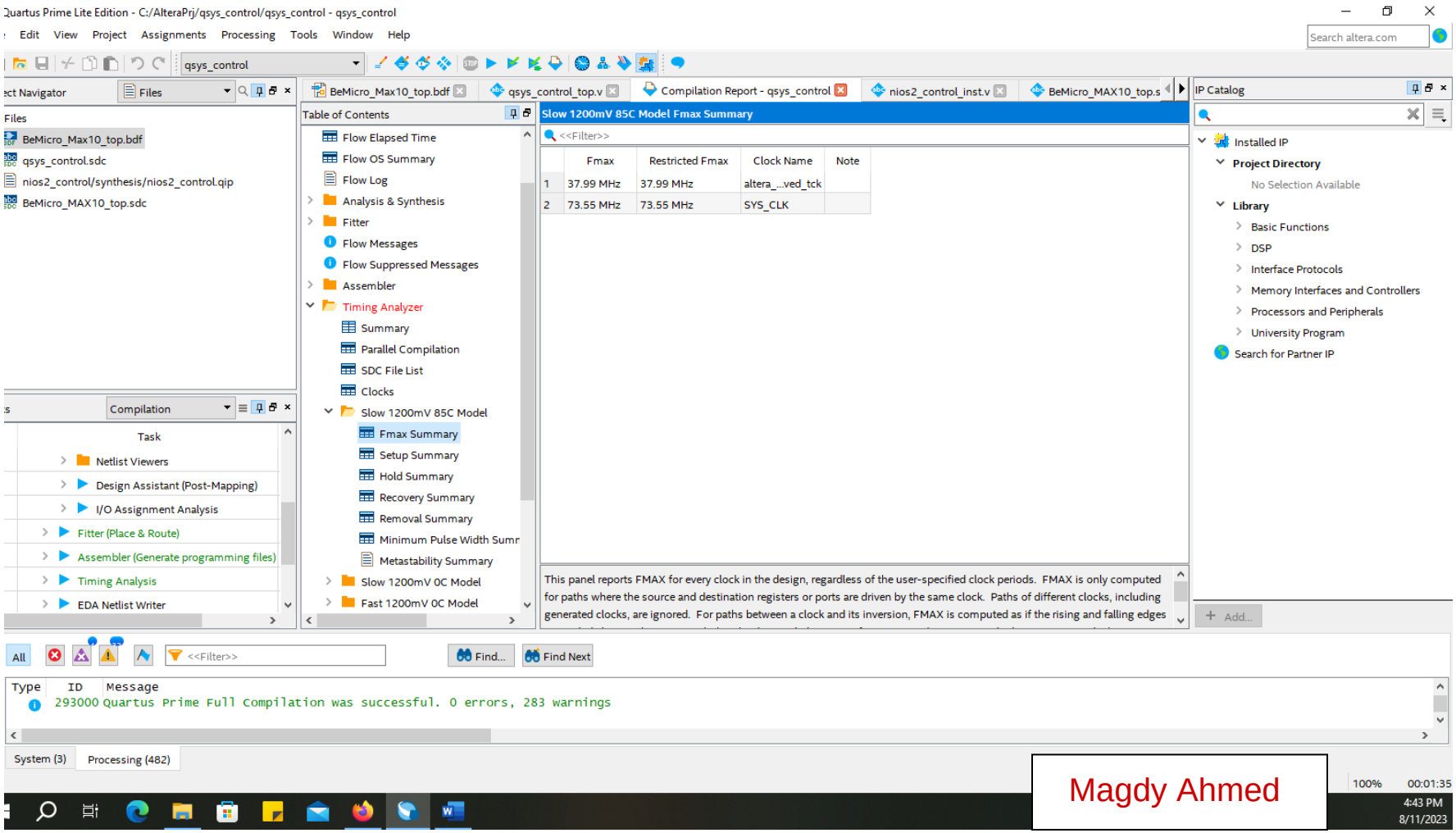
Quartus Prime Lite Edition - C:/AlteraPrj/qsys_control/qsys_control - qsys_control
Edit View Project Assignments Processing Tools Window Help
Search altera.com
qsys_control
Files
BeMicro_Max10_top.bdf
qsys_control.sdc
nios2_control/synthesis/nios2_control.qip
BeMicro_MAX10_top.sdc
Compilation
Task
Netlist Viewers
Design Assistant (Post-Mapping)
I/O Assignment Analysis
Fitter (Place & Route)
Assembler (Generate programming files)
Timing Analysis
EDA Netlist Writer
BeMicro_Max10_top.bdf
qsys_control_top.v
Compilation Report - qsys_control
nios2_control_inst.v
BeMicro_MAX10_top.s
Table of Contents
Flow Elapsed Time
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Metastability Summary
Slow 1200mV 0C Model
Fast 1200mV 0C Model
Slow 1200mV 85C Model Fmax Summary
<<Filter>>
Fmax
Restricted Fmax
Clock Name
Note
1 37.99 MHz 37.99 MHz altera_...ved_tck
2 73.55 MHz 73.55 MHz SYS_CLK
This panel reports FMAX for every clock in the design, regardless of the user-specified clock periods. FMAX is only computed for paths where the source and destination registers or ports are driven by the same clock. Paths of different clocks, including generated clocks, are ignored. For paths between a clock and its inversion, FMAX is computed as if the rising and falling edges
IP Catalog
Installed IP
Project Directory
No Selection Available
Library
Basic Functions
DSP
Interface Protocols
Memory Interfaces and Controllers
Processors and Peripherals
University Program
Search for Partner IP
Add...
All
<<Filter>>
Find...
Find Next
Type ID Message
293000 Quartus Prime Full Compilation was successful. 0 errors, 283 warnings
System (3)
Processing (482)
100%
00:01:35
4:43 PM
8/11/2023

Magdy Ahmed