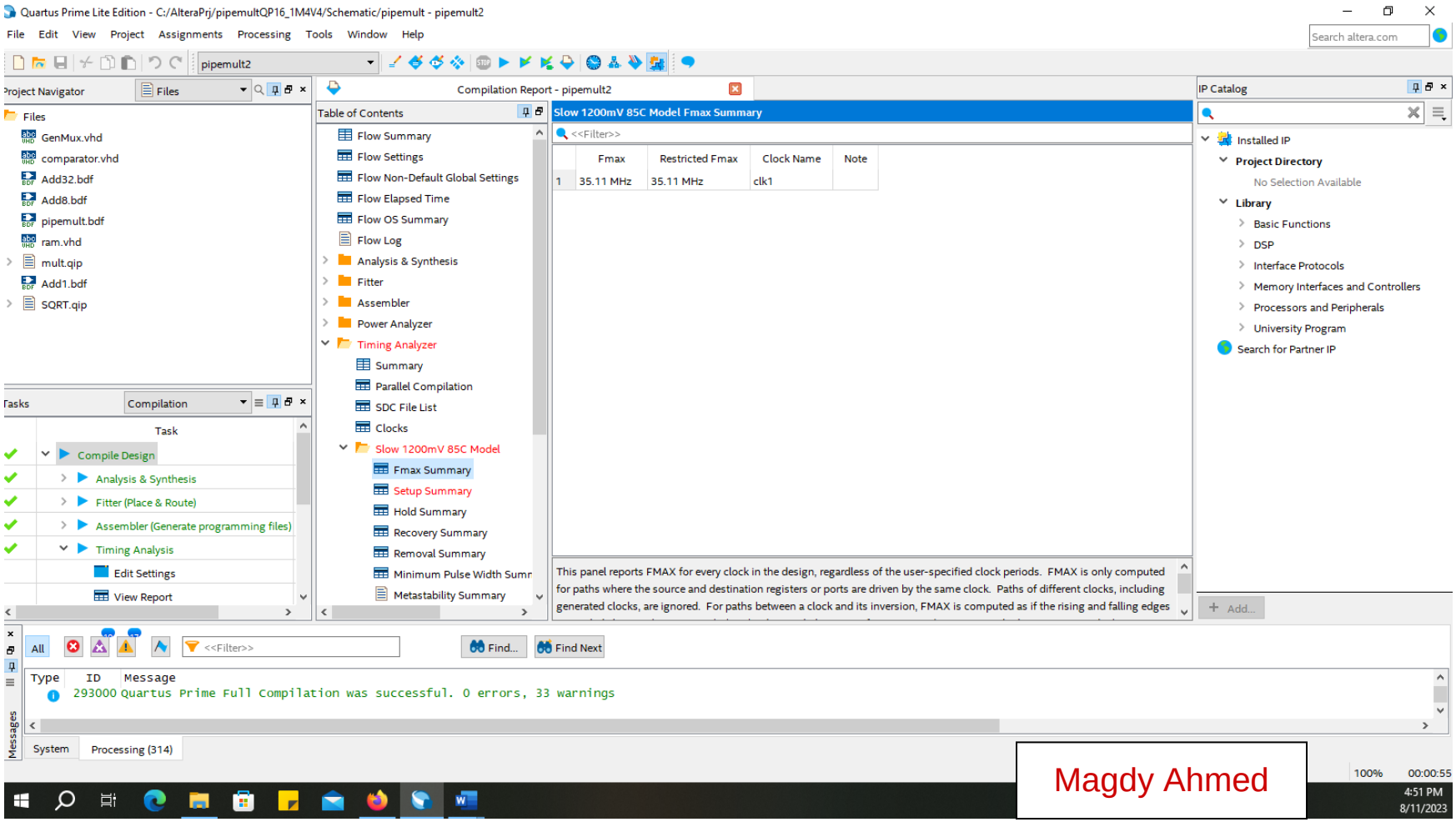
Quartus Prime Lite Edition - C:/AlteraPrj/pipemultQP16_1M4V4/Schematic/pipemult - pipemult2
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Search altera.com
pipemult2
Project Navigator
Files
GenMux.vhd
comparator.vhd
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Add8.bdf
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ram.vhd
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Add1.bdf
SQRT.qip
Compilation Report - pipemult2
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Slow 1200mV 85C Model Fmax Summary
<<Filter>>
Fmax
Restricted Fmax
Clock Name
Note
1
35.11 MHz
35.11 MHz
clk1
This panel reports FMAX for every clock in the design, regardless of the user-specified clock periods. FMAX is only computed for paths where the source and destination registers or ports are driven by the same clock. Paths of different clocks, including generated clocks, are ignored. For paths between a clock and its inversion, FMAX is computed as if the rising and falling edges
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Timing Analysis
Edit Settings
View Report
All
<<Filter>>
Find...
Find Next
Type ID Message
293000 Quartus Prime Full Compilation was successful. 0 errors, 33 warnings
Messages
System
Processing (314)
100%
00:00:55
4:51 PM
8/11/2023
Magdy Ahmed