Magdy's Assignment (1) FPGA Design

Question (1): -

Using only logic gates, design a 2-bit full adder with carry. Here is a partial truth table for the circuit.

INPUTS					OUTPUTS		
A0	A1	B0	B1	Ci	S0	S1	Co
0	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0
0	1	0	0	0	0	1	0
1	0	1	0	0	0	1	0
0	1	0	1	0	0	0	1
0	1	0	0	1	1	1	0
1	0	1	0	1	1	1	0
1	1	1	1	1	1	1	1

Where A and B are inputs, Ci is Carry in, Si is output, and Co is Carry out.

Draw a schematic showing the gate interconnections. Include either a Boolean equation or an explanation of your design that matches the schematic you submit.

Solution

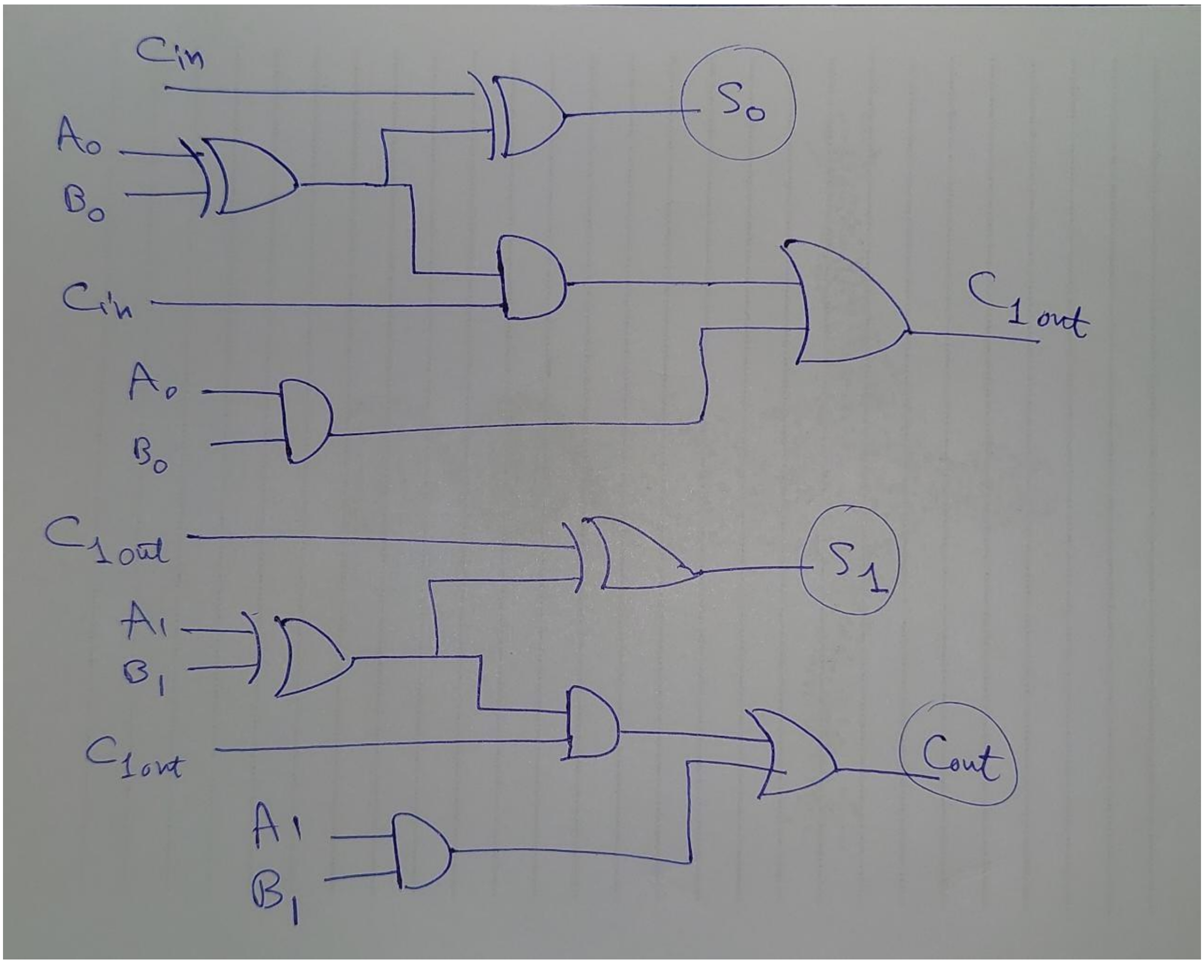
1st Solution:

Explanation: Using 4 XORs, 4 AND gates, 2 OR gates.

$S_o = A_o \text{ XOR } B_o \text{ XOR } C_{in}$

$S_1 = A_1 \text{ XOR } B_1 \text{ XOR } C_{0_{out}}$, where $C_{0_{out}} = (A_o \text{ AND } B_o) \text{ OR } \left(C_{in} \text{ AND } (A_o \text{ XOR } B_o)\right)$

$C_o = (A_1 \text{ AND } B_1) \text{ OR } \left(C_{0_{out}} \text{ AND } (A_1 \text{ XOR } B_1)\right)$



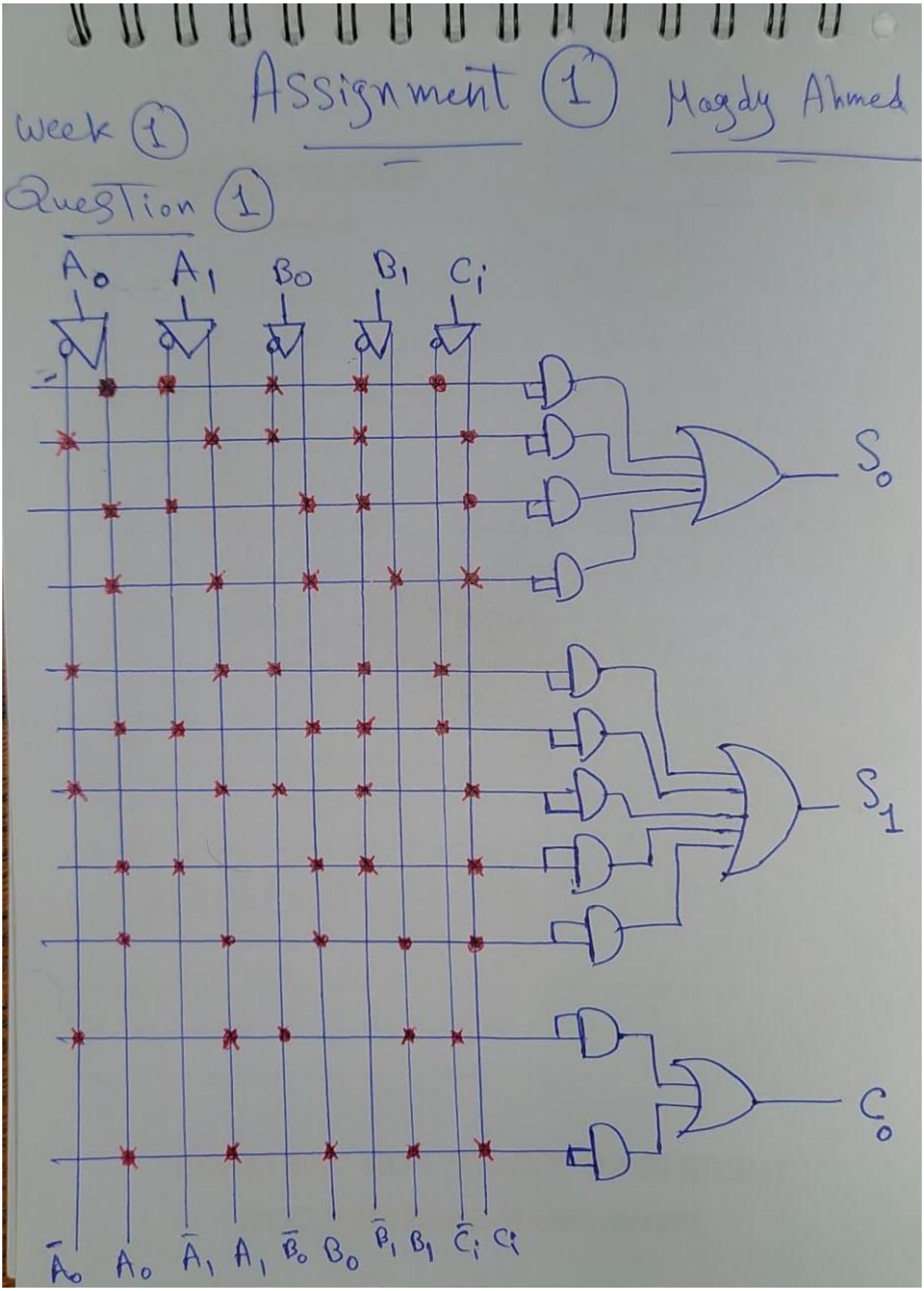
2nd Solution:

Explanation: Using 5 Inputs and their inverters, 11 AND gates, 3 OR gates.

$S_o = A_o\overline{A_1}\,\overline{B_o}\,\overline{B_1}\,\overline{C_i} + \overline{A_o}A_1\overline{B_o}\,\overline{B_1}\,C_i + A_o\overline{A_1}\,B_o\,\overline{B_1}\,C_i + A_oA_1B_oB_1C_i$

$S_1 = \overline{A_o}A_1\overline{B_o}\,\overline{B_1}\,\overline{C_i} + A_o\overline{A_1}\,B_o\overline{B_1}\,\overline{C_i} + \overline{A_o}A_1\overline{B_o}\,\overline{B_1}\,C_i + A_o\overline{A_1}\,B_o\,\overline{B_1}\,C_i + A_oA_1B_oB_1C_i$

$C_o = \overline{A_o}A_1\overline{B_o}\,B_1\,\overline{C_i} + A_oA_1B_oB_1C_i$

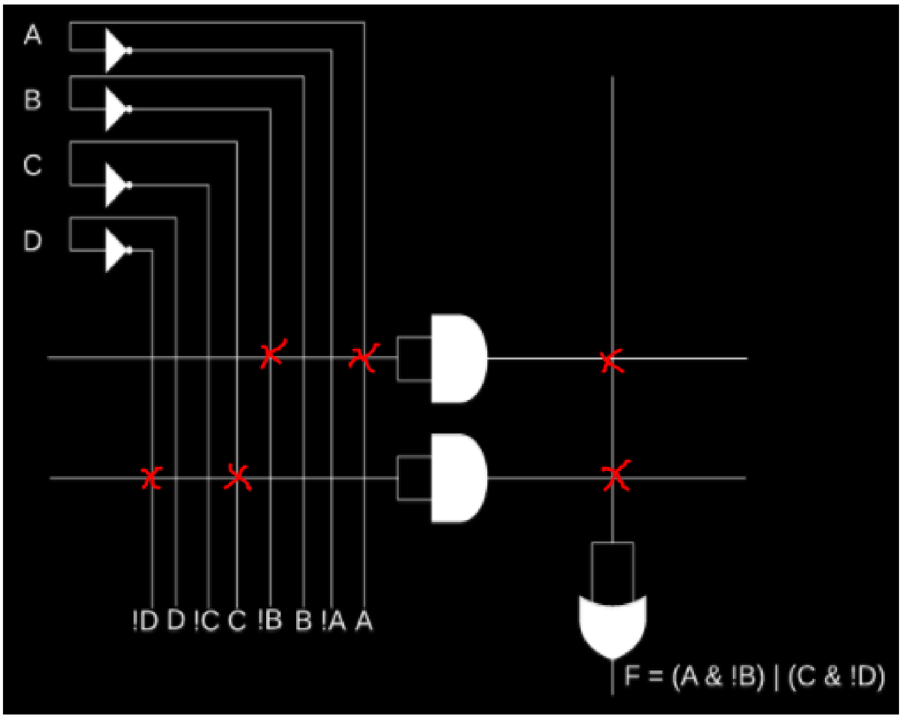


Question (2): -

Show how the logic equation (A AND NOT(B)) OR (C AND NOT(D)) can be implemented using the following:

Solution

A. The PLA shown here:



Explanation: Fuse the wires of (A, ! B) for the first AND gate (C, ! D) for the Second AND then make ORing

B. The LUT shown here:

RAM CONTENTS				
Address				Output Data
A	**B**	**C**	**D**	**F**
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0

Explanation: Apply F = (A & ! B) | (C & ! D) to each combination of inputs the put it in the Truth Table.