

Quartus Prime Lite Edition - C:/AlteraPrij/pipemultQP16_1Timing2/Schematic/pipemult - pipemult2

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Project Navigator

Entity: Instance

MAX 10: 10M08DAF484C8GES

pipemult

Compilation

Task

- Compile Design
 - Analysis & Synthesis
 - Fitter (Place & Route)
 - Assembler (Generate programming files)
 - Timing Analysis
 - EDA Netlist Writer
 - Edit Settings

pipemult.bdf add1.bdf Add8.bdf Add32.bdf Compilation Report - pipemult2 comparator.vhd GenMu

Diagram showing a complex digital logic circuit with multiple adders (Add1, Add8, Add32) and a multiplier (Mult) connected to a 32-bit adder (Add32). The circuit is implemented in a MAX 10 FPGa.

IP Catalog

- Installed IP
 - Project Directory
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 - Library
 - Basic Functions
 - Arithmetic
 - ALTERA_CORDIC
 - ALTERA_FP_ACC_CUSTOM
 - ALTERA_FP_FUNCTIONS
 - ALTMEMMULT
 - ALTMULT_ACCUM (MAC)
 - ALTMULT_ADD
 - ALTMULT_COMPLEX
 - ALTSQRT
 - LPM_COMPARE
 - LPM_COUNTER
 - LPM_DIVIDE
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 - PARALLEL_ADD
 - Bridges and Adaptors
 - Clocks; PLLs and Resets

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293000 Quartus Prime Full Compilation was successful. 0 errors, 195 warnings

System Processing (494)

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3:24 PM
8/9/2023

Magdy Ahmed