Faculty of Enigeering

Cairo University

Microwaves Engineering Project

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Design and Analysis of Wilkinsion power divider

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1. Framework

1.1. Introduction:

The Power divider is a device that divides input power into N ports with a designated power ratio. However, certain factors like **Insertion loss, return loss, Isolation and Balancing** between output ports must be considered for optimal performance in various applications. In RF and microwave applications, the Wilkinson power divider is commonly used to divide the input signal into two or more output signals with equal power.

ZigBee, a wireless communication protocol, operates in the **2.4 GHz** frequency band and is frequently used in low-power, low-data-rate applications such as home automation, industrial automation, and sensor networks. The Wilkinson power divider can be utilized in the context of ZigBee protocol to distribute RF power from a transmitter to multiple antennas, thereby improving the coverage and reliability of the ZigBee network. This is particularly useful when multiple ZigBee devices need to communicate over a wide area. Moreover, in ZigBee mesh networks where multiple devices act as routers and relay data between other devices, using a Wilkinson power divider to distribute RF power from a transmitter to multiple antennas can increase the range and coverage of each router and, therefore, improve the overall performance of the network.

In summary, the Wilkinson power divider is a valuable component in ZigBee protocol applications that require the distribution of RF power to multiple antennas or devices. By evenly distributing RF power, the coverage and reliability of the ZigBee network can be improved, making it useful in applications such as home automation, industrial automation, and sensor networks.

1.2: Agenda:

We aim to perform a comparative analysis between Wilkinson power divider designs in order to find optimal performance according to our application (Zigbee Low Power Applications) the Design workflow is as follows:

- Lumped components - based design.
  - ✓ Wilkinsion power divider in classical circuits.
  - ✓ Proposed Design setup $(\pi - \mathrm{Model})$.
  - ✓ S – Parameters Analysis.
  - ✓ Schematics and Charts on ADS and Performance Assessment.
- Microstrip line - based design.
  - ✓ Concept of the Microstrip Design (outages and potential mismatches).
  - ✓ Single - Stage Wilkinsion Design.
  - ✓ Multi - Stage Wilkinsion Design.

2. Lumped Components - based Design

2.1 Wilkinsion power divider in classical circuits

The modular design of the power divider is mainly inspired by microwave engineering, but we can achieve an equivalent model in a classical circuit regardless of any potential parasitic coupling that could deviate performance from the ideal transmission line design.

2.2 (π - Model) Proof.

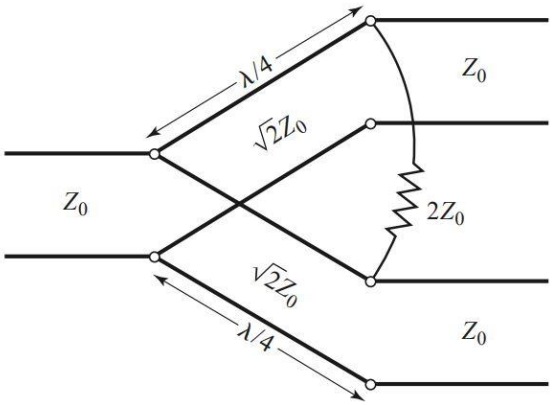


Figure 1: Wilkinsion TL Ideal design

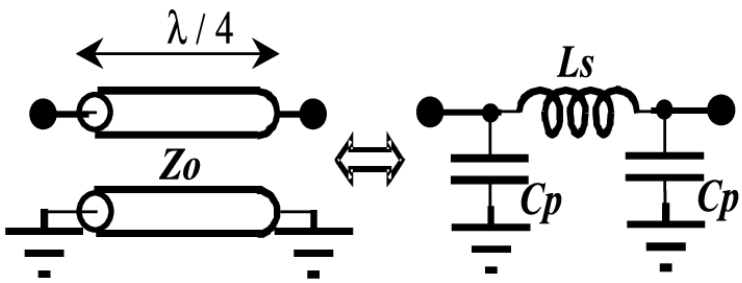


Figure 2: λ/4 Section equivalence to π – Model

The Inductor used to model series inductance of transmission line, while Caps. To ground provides a Low - Impedance path for high frequency signals, which reduces signal reflections and maintains good matching [1].

$$V_1 = AV_2 - BI_2 \rightarrow V(Z) = A\left(e^{-j\beta Z} + \Gamma_L e^{j\beta Z}\right),$$
$$I_1 = CV_2 - DI_2 \rightarrow I(z) = \frac{A}{Z_o}\left(e^{-j\beta Z} - \Gamma_L e^{j\beta Z}\right)$$

$$A = \frac{V_1}{V_2}\Big|_{I_2=0} \text{ (open circuit) } = \frac{V(-d)}{v(0)} = \frac{2A\left(\frac{e^{j\beta d}+e^{-j\beta d}}{2}\right)}{A\left(1+(1)(1)\right)} = \frac{2A\cos\beta d}{2A} \rightarrow A = \cos\ \beta d$$

$$C = \frac{I_1}{V_2}\Big|_{I_2=0} = \frac{(2j)\frac{A}{z_0}\left(\frac{e^{+\beta d}-e^{-j\beta d}}{(2j)}\right)}{2A}, C = jY_0\sin(\beta d),$$

$$B = \frac{-V_1}{I_2}\Big|_{V_2=0} \Gamma_{L=-1} = \frac{-A\left(\frac{e^{j\beta d}-e^{-j\beta}}{2j}\right)\times 2j}{\frac{A}{Z_0}(1-(-1)(1))} = \frac{-2jA\sin(\beta d)}{\frac{A}{Z_0}(2)}$$

$$\therefore B = -jz_0\sin\beta d\ , \because D = \frac{-I_1}{I_2}\Big|_{V_2=0} = \frac{-\frac{A}{z_0}\left(\frac{e^{j\beta\gamma}+e^{-j\beta d}}{2}\right)\times 2}{\frac{A}{Z_0}(1-(-1)(1))} = -\cos\ \beta d$$

- Main Definitions of ABCD parameters is:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cos\ \beta d & jz_0 \sin\ \beta d \\ jY_0 \sin(\beta d) & \cos(\beta d) \end{bmatrix}, \begin{bmatrix} V_1 = A(V_2) + B(-I_2) \\ I_1 = C(V_2) + D(-I_2) \end{bmatrix}$$

for $\frac{\lambda}{4}, \sqrt{2}Z_0$, lossless transmission line:

$$\begin{bmatrix} 0 & \frac{j}{50\sqrt{2}} \\ \frac{j}{50\sqrt{2}} & 0 \end{bmatrix}, \because V_1 = I_1 \times \frac{\left(SL+\frac{1}{SC}\right)}{\frac{1}{SC}+\frac{1}{SC}+SL} \times \left(\frac{1}{SC}\right), \because V_2 = \frac{I_1 \times \frac{1}{SC}}{SL\frac{1}{SC}+\frac{1}{SC}} \times \left(\frac{1}{SC}\right), \because C = \frac{I_1}{V_2}\Big|_{I=0}$$

$$\therefore C = S^3LC^2 + 2SC \rightarrow (1), \text{ let } S = j\omega, \therefore \frac{j}{50\sqrt{2}} = (j\omega)^3C^2L + 2j\omega C$$

To be equivalent with ABCD of $\frac{\lambda}{4}$ section.

$$\frac{1}{Z_0} = \frac{1}{50\sqrt{2}} = -\omega^3C^2L + 2c\omega \rightarrow (2), \because A = \frac{V_1}{V_L}\Big|_{I_2=0}$$

from (1) $\therefore \frac{V_1}{V_2} = \frac{\left(sL+\frac{1}{sc}\right)}{\frac{2}{sc}+sl} \times \frac{1}{sc} \times (s^3c^2L + 2sc)$

$$\therefore A = \frac{\left(SL+\frac{1}{5C}\right)(S^2CL+2)}{\left(\frac{2}{sC}+SL\right)} = 0 \rightarrow (3)$$

from (2): $SL + \frac{1}{SC} = 0$, $S^2LC = -1$, $-\omega^2LC = -1 \rightarrow \omega = \frac{1}{\sqrt{LC}} \rightarrow (4)$

$$\frac{1}{z_0} = -\frac{c^2l}{lc} \times \frac{1}{\sqrt{Lc}} + \frac{2c}{\sqrt{Lc}} \rightarrow \therefore \frac{1}{Z_0} = \frac{-C}{\sqrt{LC}} + \frac{2C}{\sqrt{LC}} \rightarrow \frac{C}{\sqrt{LC}} = \frac{1}{Z_0} \rightarrow (5)$$

from (4) and (5):

We got the Equivalent L, C to $\frac{\lambda}{4}$ Transmission line and we will check it from the simulation if the equations are Right or not.

$\omega = \frac{1}{\sqrt{LC}}, \frac{C}{\sqrt{LC}} = \frac{1}{Z_0}$, By using $Z_o = 50\ \Omega, f = 2.4\ GHZ$ Solve the two Equations.

$L = 4.68915\ nH, C = 0.93783\ pF \rightarrow$ Used in ADS Schematic in the $\pi -$ Model.

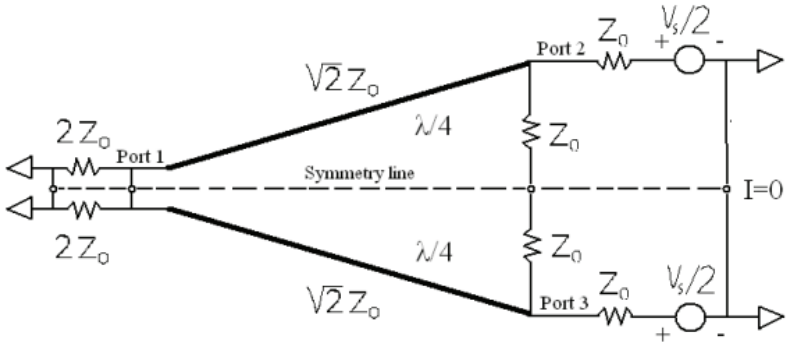
2.3 S-Parameters Analysis.

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \end{bmatrix} = \begin{bmatrix} s_{11} & s_{12} & s_{13} \\ s_{21} & s_{22} & s_{23} \\ s_{31} & s_{32} & s_{33} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \end{bmatrix}$$

As we want it to be internally and output matched, so $s_{11} = s_{22} = s_{33} = 0$ and to be reciprocal and isolated, we need $s_{32} = s_{23} = 0$ [2]

$b_1 = S_{11}a_1 + s_{12}a_2 + S_{13}a_3 \rightarrow V_0(S_{12} + S_{13})$ even mode
$b_1 = S_{11}a_1 + s_{12}a_2 + S_{13}a_3 \rightarrow V_0(-s_{12} + s_{13})$ odd mode

Even mode:



$V_3^+ = V_2^+ = V_0$
$V_1^+ = 0$
$V_1^- = V_0(S_{12+}S_{33})$
$V_3^- = V_0(S_{23} + S_{33}) = V_2^-$

$\therefore Z_{in} = \frac{Z_0^2}{Z_l} = \frac{Z^2}{2Z_o} = Z_o$

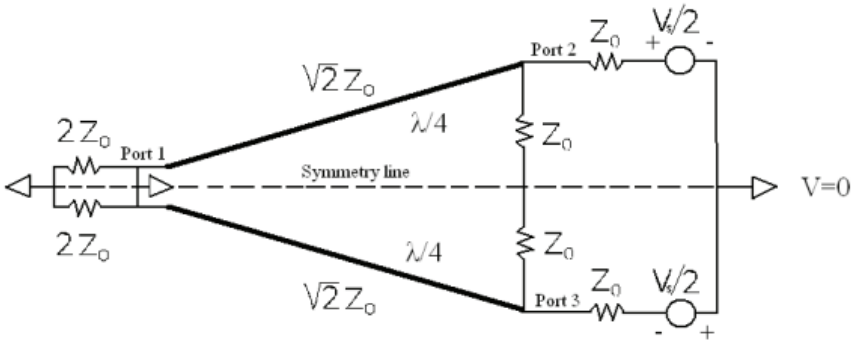
$\therefore Z_2\sqrt{2}Z_0 \ \because V_0(S_{23} + S_{33}) = 0 \ \therefore S_{23} = -S_{33}$
$\because V(z) = V^+\left(e^{-j\beta z} + \Gamma e^{+j\beta z}\right) \ \because V(0) = V_1^- = V_1^+(1 + \Gamma) \rightarrow$ (1)
$\therefore V\left(-\frac{\lambda}{4}\right) = V_0 = V^+(j - j\Gamma) \ \therefore V^+ = \frac{V_0}{j - j\Gamma} \rightarrow$ (2)

From (1), (2) $\therefore \Gamma = \frac{2z_0 - \sqrt{2}z_0}{2z_0 + \sqrt{2}z_0} = \frac{2-\sqrt{2}}{2+\sqrt{2}}$,

$V_+ = -jV_o\sqrt{2}$
$s_{12} + s_{13} = -j\sqrt{2} \rightarrow$ (3)

Odd mode:

$V_3^+ = V_0, V_2^+ = -V_0 \ \therefore S_{1,} = -S_{33} \rightarrow$ (4)
$\because V_1^- = V_2^+ s_{12} + V_3^+ s_{13} = -V_0 s_{12} + V_0 s_{13} = V_0(s_{13} - s_{12}) = 0$
$\therefore S_{13} = S_{12}$, from (3) $S_{13} = S_{12} = -\frac{i\sqrt{2}}{2}$
Zequ. $= R//Z_{in} = R//\infty = R$ (Avoiding reflection $(V_3^- = 0)$)
$\therefore R = Z_0$
$\because V_3^- = V_2^+ s_{23} + V_3^+ s_{33} = -v_0 s_{23} + V_0 s_{33} = V_0(s_{33} - s_{33}) = 0$
$\therefore s_{33} = s_{23} \rightarrow$ (5)
from (4), (5) $\therefore s_{23} = s_{33} = 0$



$\because Z_{in} = Z_x//Z_x = \frac{Z_x}{2}$
$\because Z_x = \frac{(\sqrt{2}Z_0)^2}{Z_0} = Z_0$
$\therefore Z_{in} = Z_0, \ \therefore$ (Matched) $\therefore s_{11} = 0$
$\therefore S_{matrix} = (-\frac{j}{\sqrt{2}})\begin{bmatrix} 0 & 1 & 1 \\ 1 & 0 & 0 \\ 1 & 0 & 0 \end{bmatrix}$

2.4 Schematics and Charts on ADS and Performance Assessment.

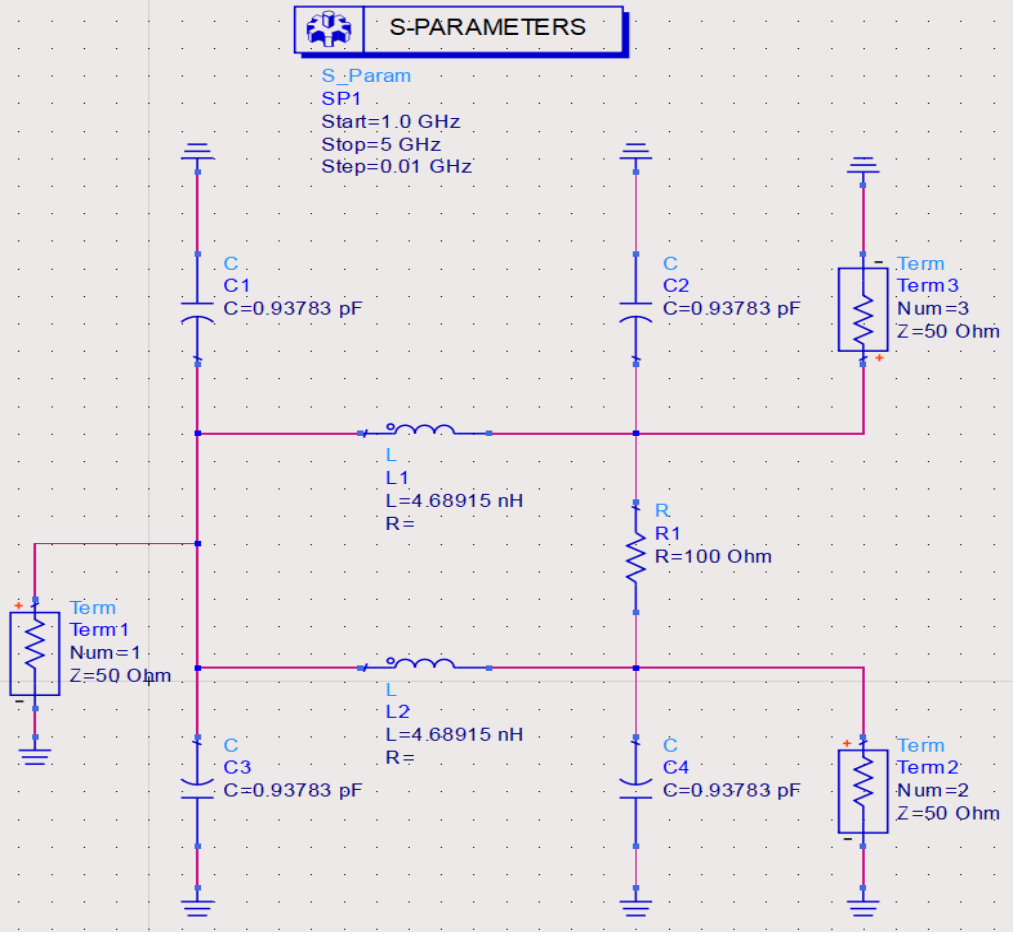


Figure 3: Equivalent π - Model Schematic

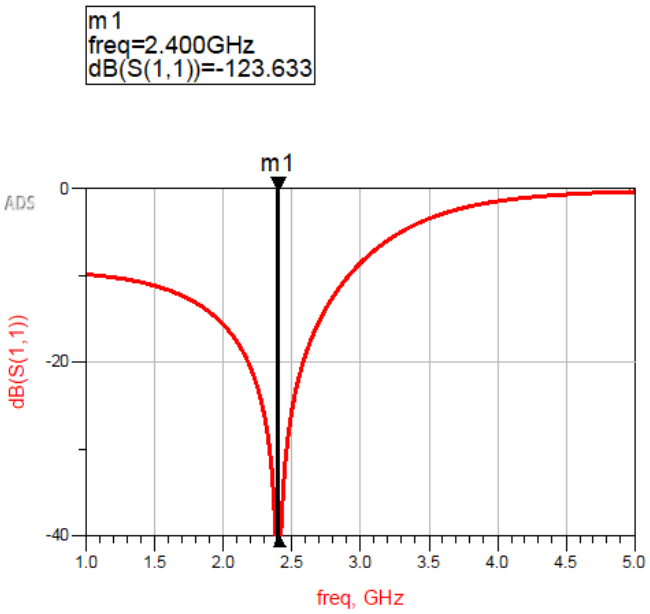


Figure 4: dB (mag (S_11)) Return Loss

Comments: The Circuit behaves Ideally @ the design frequency 2.4 GHZ with $\mathrm{RL} = 123.633\ \mathrm{dB}$ **(return loss)** Which Corresponds High **Matching** at Port 1 with nearly no Reflection @ the input port 1.

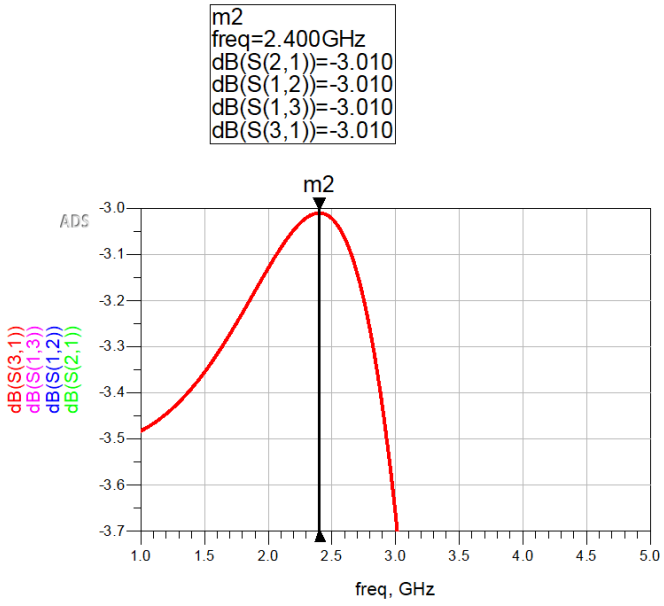


Figure 5:Mag (insertion loss)

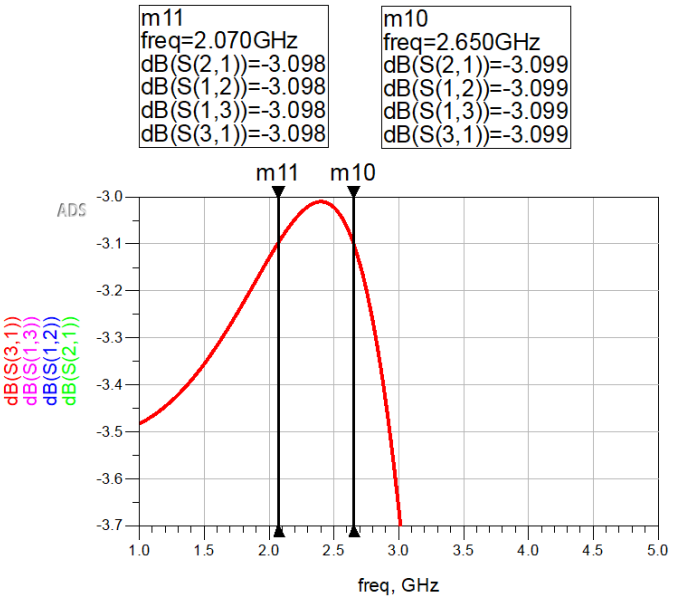


Figure 6:Mag(insertion loss band)

Comments: From Fig. (5)

→ **insertion loss** represented reflects nearly equal power division ≈ 3 dB

→ **reciprocity** can be deduced from the completely overlaid (S_{13}, S_{31}) / (S_{12}, S_{21}).

From Fig. (6)

→ The Insertion loss BW has been designed for the Zigbee Low Power Application (3.1 dB BW = 580 MHZ).

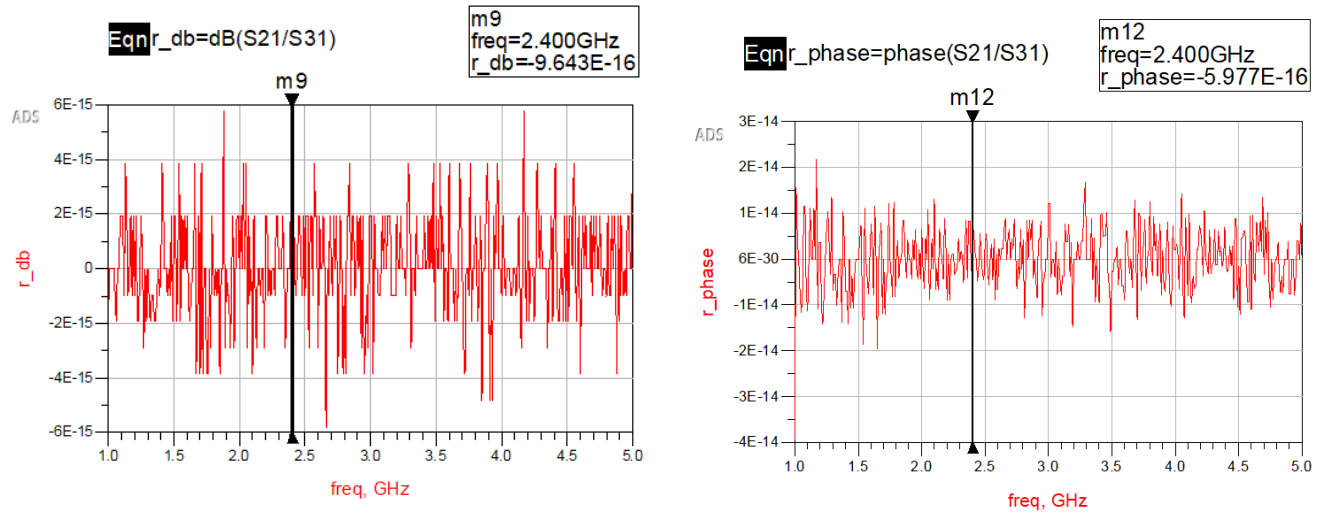


Figure 7: Magnitude & Phase Imbalance for forward Transmission coefficient

Comments: From Fig. (7)

→ **Equal Balanced** is Satisfied which implies equal magnitude splitting and phase matching.

→ $r_{dB} = dB\left(\frac{S_{21}}{S_{31}}\right)$, $r_{phase} = Phase\left(\frac{S_{21}}{S_{31}}\right)$ Which Ideally equal **Zero** as Shown in Fig. (7).

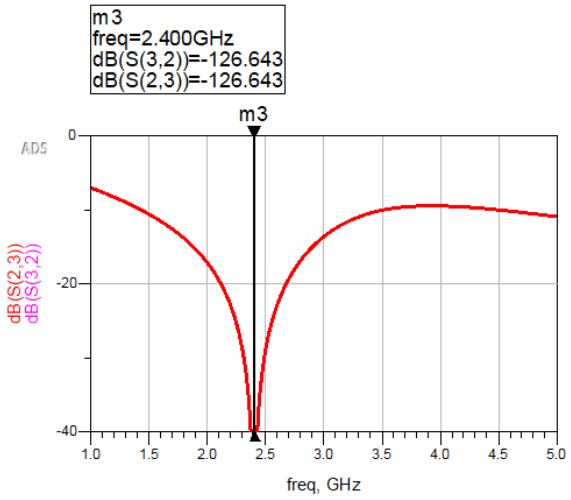


Figure 9 : Output Isolation

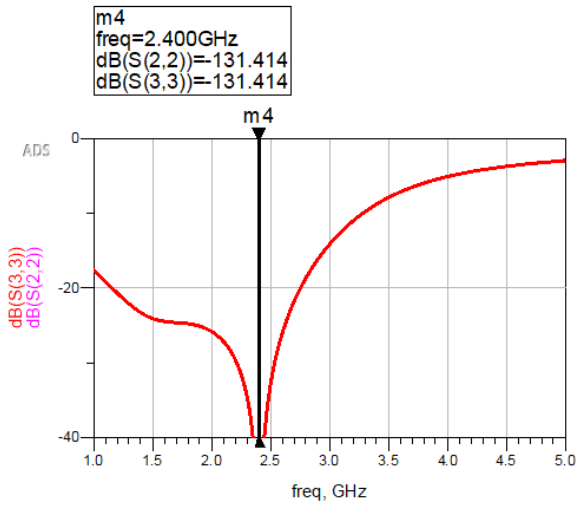


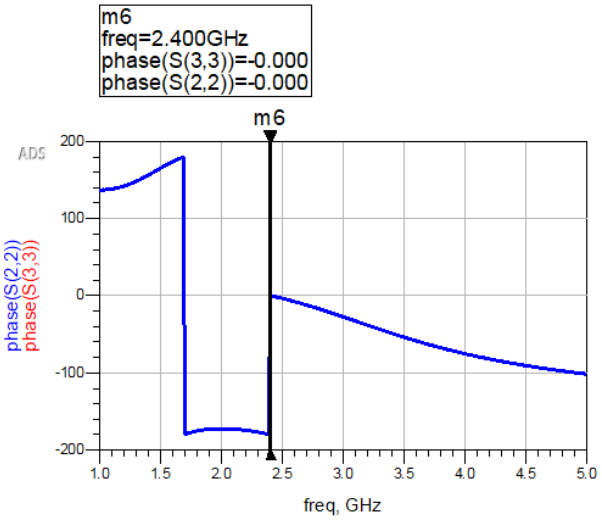
Figure 8 : Outports matching.

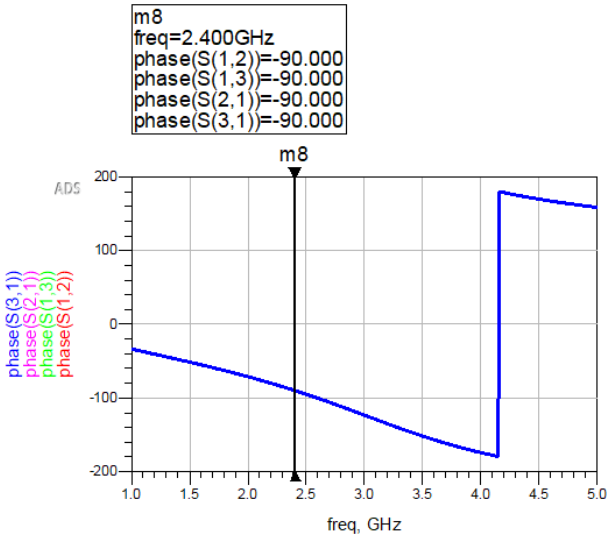
Comments: From Fig. (8):

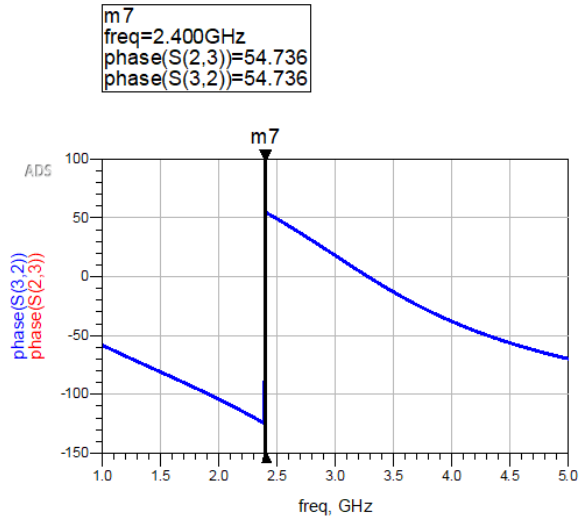
→ Outports **are isolated** given the isolation coefficients -126.643 dB nearly ideally (Expected $-\infty$ dB).

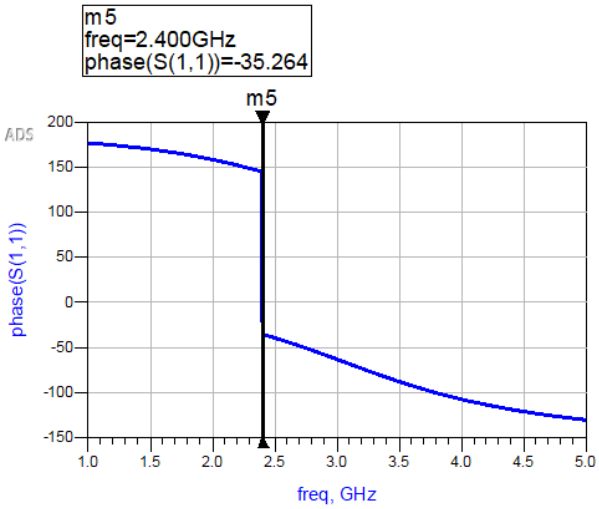
From Fig. (9):

→ Port 2 & 3 are Matched as well ∴ **internally matched** Ports are Satisfied.









Comments: Ideally **Phase** S_{12} , S_{13} , S_{21} , $S_{31} = -90°$

3. Microstrip line - based design.

3.1 concept of microstrip manipulation

As per discussed in the last section, the lumped-based design results into limited bandwidth so we need to head over the microstrip design to gain some advantages as:

Miniaturization (scalability)	Low-cost
Low loss	Wide band design

3.1.1 Microstrip laminate parameters

The substrate used for the base design is the rogers **RO4003C** laminate with the depicted parameters as in Fig. (11) & Fig. (12):

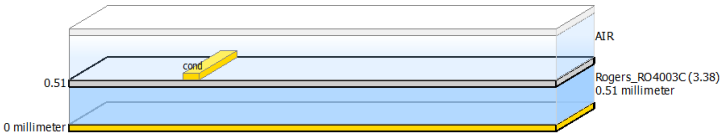


Figure 10: Substrate Summary

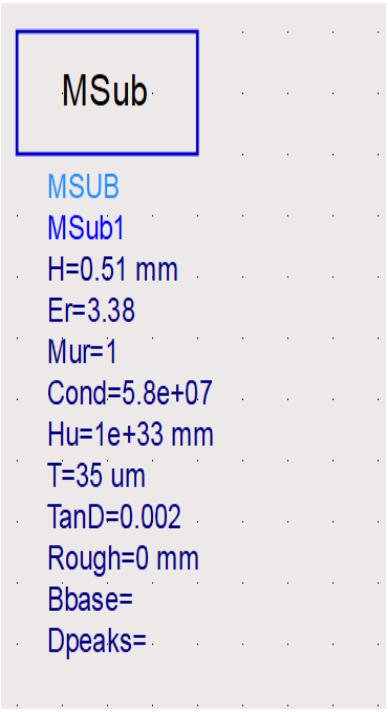


Figure 11: Schematic Substrate

Property	Typical Value RO4003C	Typical Value RO4350B	Direction	Units	Condition	Test Method
Dielectric Constant, e_r Process	3.38 ± 0.05	[1] 3.48 ± 0.05	Z	-	10 GHz/23°C	IPC-TM-650 2.5.5.5 Clamped Stripline
[2] Dielectric Constant, e_r Design	3.55	3.66	Z	-	8 to 40 GHz	Differential Phase Length Method
Dissipation Factor tan, d	0.0027 0.0021	0.0037 0.0031	Z	-	10 GHz/23°C 2.5 GHz/23°C	IPC-TM-650 2.5.5.5
Thermal Coefficient of e_r	+40	+50	Z	ppm/°C	-50°C to 150°C	IPC-TM-650 2.5.5.5
Volume Resistivity	1.7 X 10^{10}	1.2 X 10^{10}	-	MΩ-cm	COND A	IPC-TM-650 2.5.17.1
Surface Resistivity	4.2 X 10^{9}	5.7 X 10^{9}	-	MΩ	COND A	IPC-TM-650 2.5.17.1
Electrical Strength	31.2 (780)	31.2 (780)	Z	KV/mm (V/mil)	0.51mm (0.020")	IPC-TM-650 2.5.6.2
Tensile Modulus	19,650 (2,850) 19,450 (2,821)	16,767 (2,432) 14,153, (2,053)	X Y	MPa (ksi)	RT	ASTM D638
Tensile Strength	139 (20.2) 100 (14.5)	203 (29.5) 130 (18.9)	X Y	MPa (ksi)	RT	ASTM D638
Flexural Strength	276 (40)	255 (37)	-	MPa (kpsi)	-	IPC-TM-650 2.4.4
Dimensional Stability	<0.3	<0.5	X,Y	mm/m (mils/inch)	after etch +E2/150°C	IPC-TM-650 2.4.39A
Coefficient of Thermal Expansion	11 14 46	10 12 32	X Y Z	ppm/°C	-55 to 288°C	IPC-TM-650 2.4.41
Tg	>280	>280	-	°C TMA	A	IPC-TM-650 2.4.24.3
Td	425	390	-	°C TGA		ASTM D3850
Thermal Conductivity	0.71	0.69	-	W/m/°K	80°C	ASTM C518
Moisture Absorption	0.06	0.06	-	%	48 hrs immersion 0.060" sample Temperature 50°C	ASTM D570
Density	1.79	1.86	-	g/cm³	23°C	ASTM D792
Copper Peel Strength	1.05 (6.0)	0.88 (5.0)	-	N/mm (pli)	after solder float 1 oz. EDC Foil	IPC-TM-650 2.4.8
Flammability	N/A	[3] V-0	-	-	-	UL 94
Lead-Free Process Compatible	Yes	Yes	-	-	-	-

Figure 12: Process Parameters

Physical Data

Dimensions (mm) & Weight (g)

	L	W	T max	A	B min	C	Wt.
0603	1.5±0.1	0.8±0.1	0.55	0.3±0.15	0.6	0.3±0.15	0.002
0805	2.0±0.3	1.25±0.2	0.7	0.3±0.15	0.9	0.3±0.15	0.012
1206	3.2±0.4	1.6±0.2	0.7	0.4±0.2	1.7	0.4±0.15	0.020
2010	5.1±0.3	2.5±0.2	0.8	0.6±0.3	3.0	0.6±0.25	0.036
2512	6.5±0.3	3.2±0.2	0.8	0.6±0.3	4.4	0.6±0.25	0.055

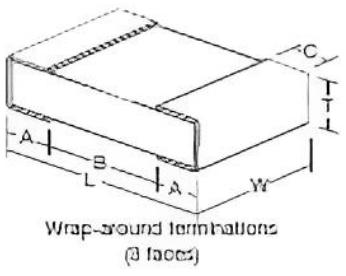


Figure 13 : SMD 0805 Resistor

Comments: We Used this Parameters According to the Egyptian industry Standards [3].

3.2 Single - Stage Wilkinsion Design.

The Layout of the Single - Stage Microstrip Design is Shown @ Fig. (14)

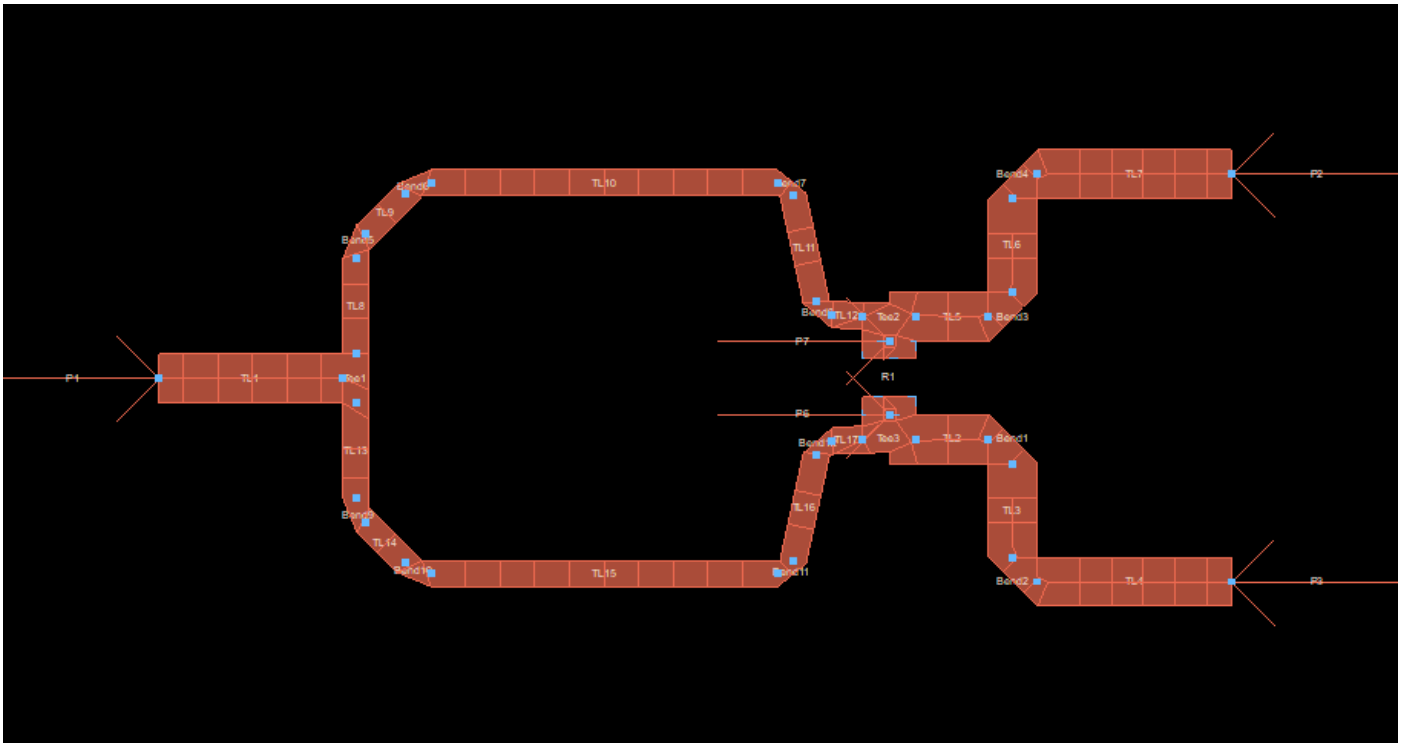


Figure 14 : Single - Stage Layout

3.2.1 Design Considerations:

- We considered **the Bends** of the layout to be **mitered by 50 %** to reduce potential Parasitic [4].
- In order to account for the size of the circuit we have the following Length and Width as Shown in the Figures (15) & (16).

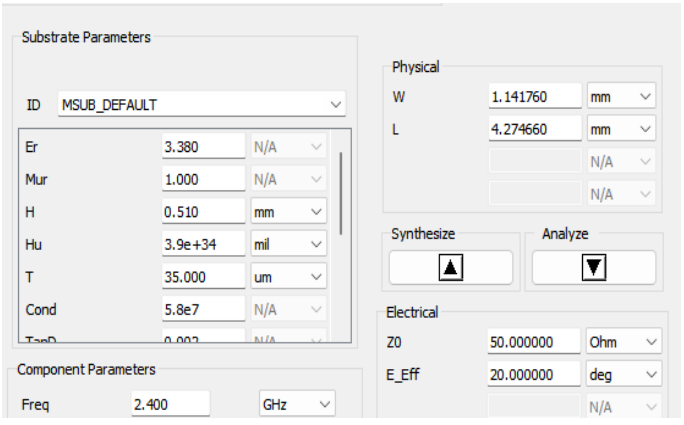


Figure 16: 50 - ohm Section

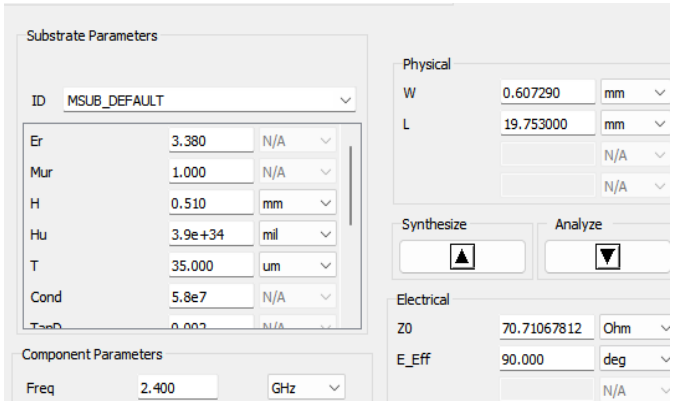


Figure 15: λ/4 Section

Note: The 50 - Ohm Section is Designed on A very Low Electrical Length Since we assume only Matching Termination (Also to Decrease the Size).

3.2.2 Discontinuity Considerations:

- The **Discontinuities** due to Interfacing the Mismatched Sections, Design metering, ... etc. Has been considered as in the Schematic **(Fig. (17)).**
- The Discontinuities have been Represented Using **T - Junctions** and **Curved Bends**.

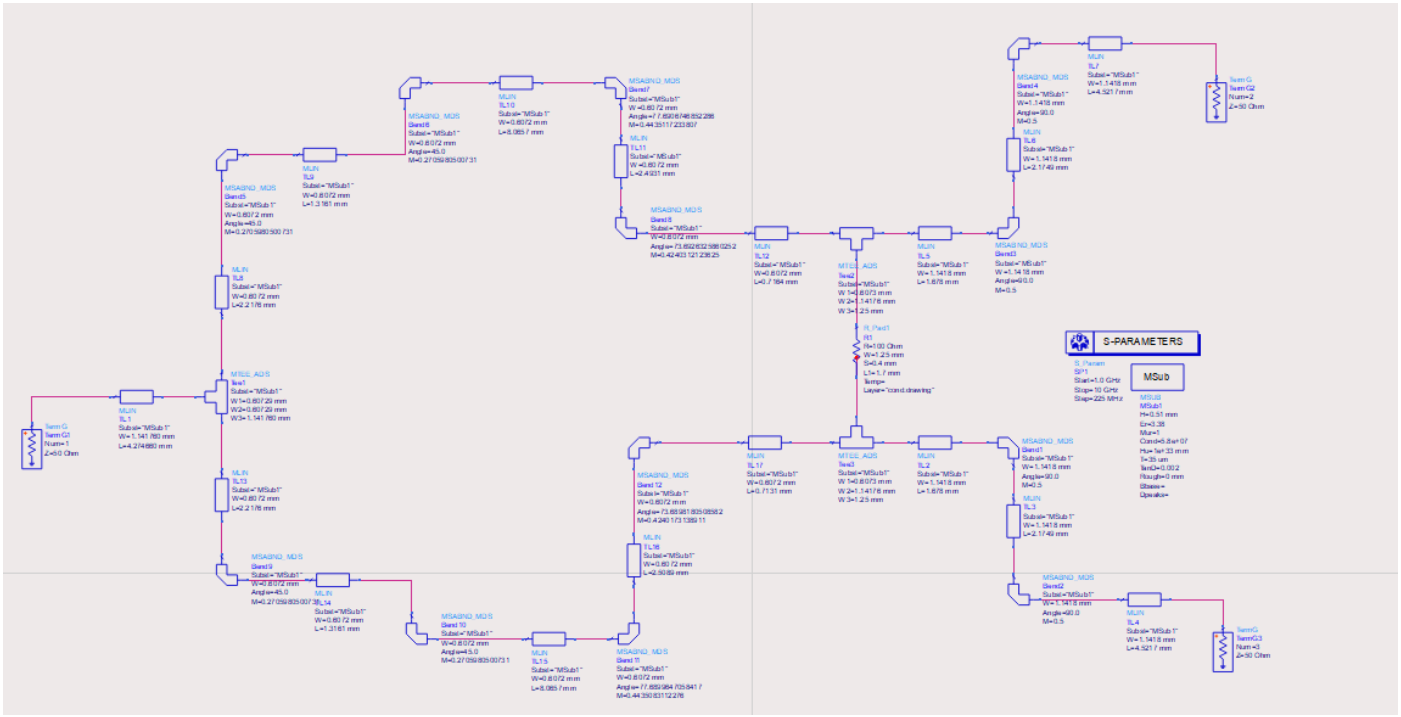


Figure 17: Schematic with Discontinuity Model

3.2.3 Analysis and Simulations:

- In Order to Obtain a Comparative analysis Among the Different Designs, The Following Analysis will be Carried out in Compare with the ideal model for $\mathbf{F} \in [\mathbf{0}, \mathbf{10}]$ **GHZ**
  As shown in (Fig. (18)).

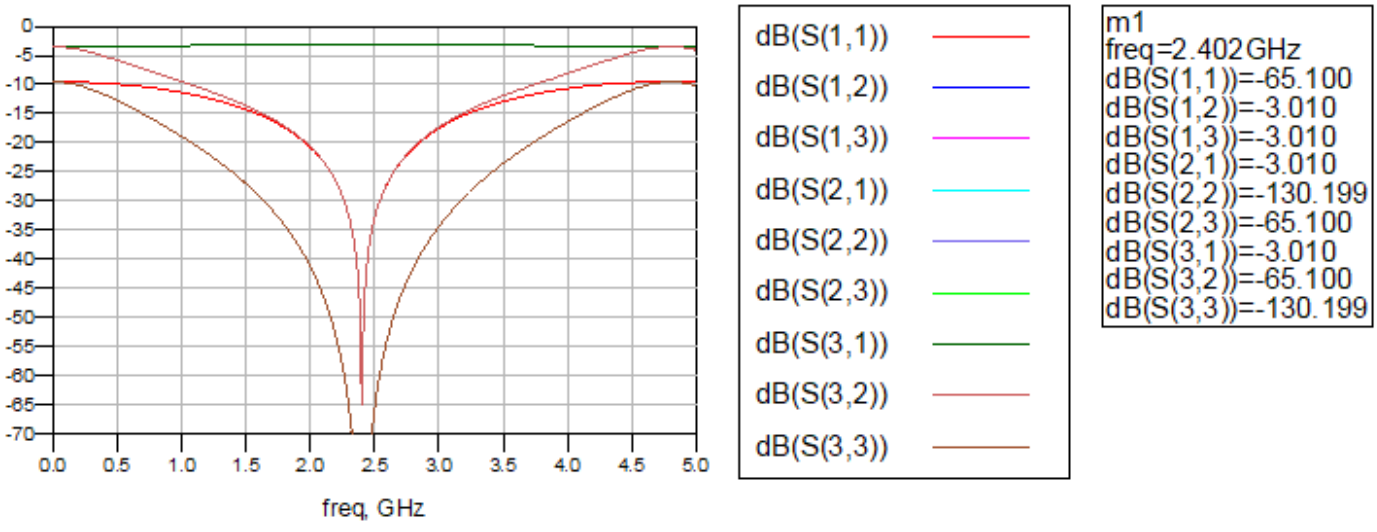


Figure 18 Ideally Performance Summary

❖ EM Simulation:

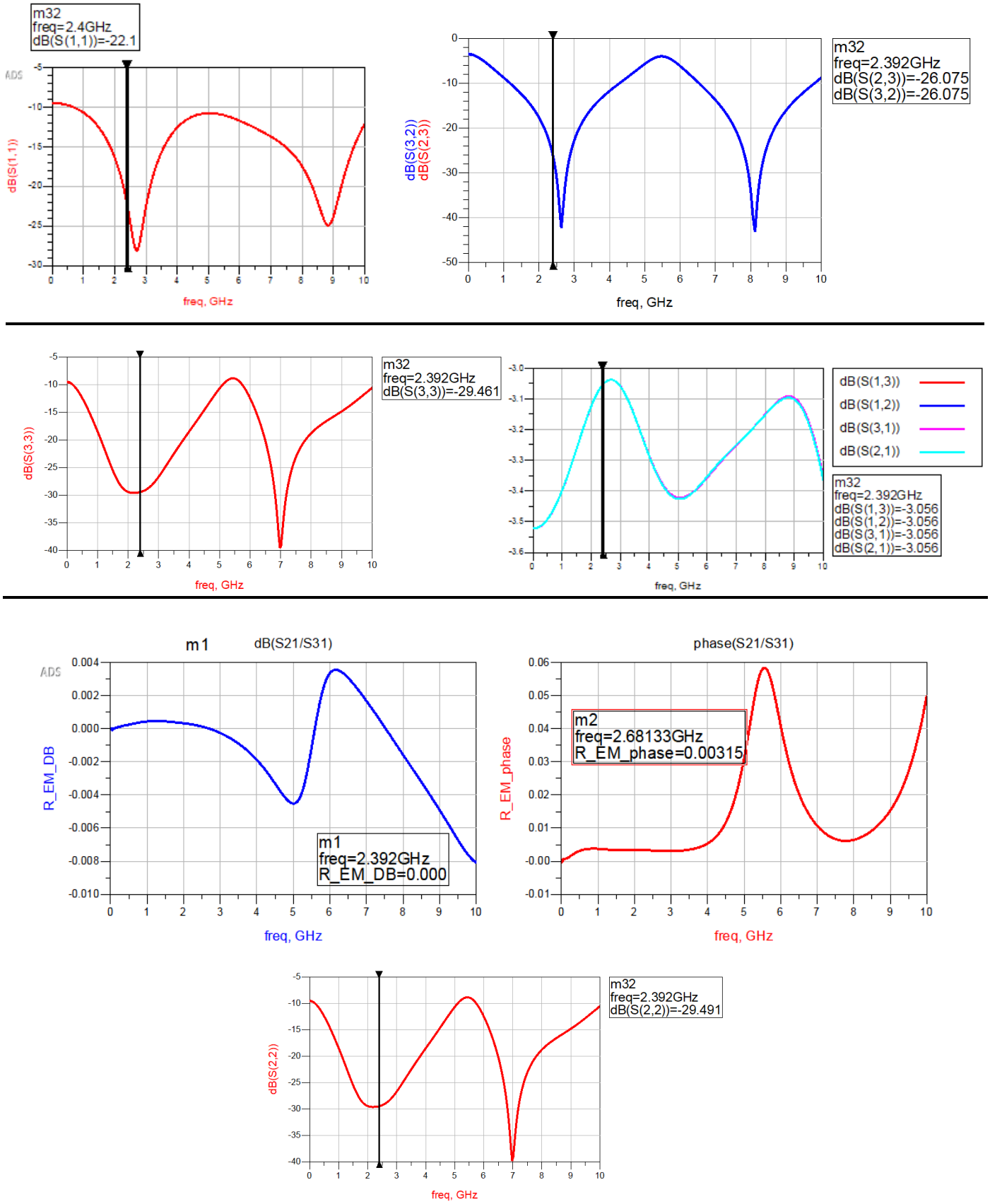


Figure 19: EM Simulation Charts

Comments: The EM Simulation is carried out with "Momentum RF" Simulation

1) Circuit shows acceptable **Insertion Loss** = 3.056 dB.
2) Circuit shows **Adequate Isolation**
   "According to Zigbee Low power Applications" = 26.075 dB
3) Circuit shows acceptable **Return Loss** = 22.1 dB.
4) The Circuit Copes with the **Ideal Balancing** (Phase (Imbalance) = $0.00315°$)
   and (magnitude (Imbalance) = 0 dB).
5) The Circuit Has Input and output **Matching** ($S_{11} = -22.1$, $S_{22} = -29.49$, $S_{33} = -29.46$) dB.
6) The Design is Still Satisfying the Reciprocity as the Basic Wilkinsion Circuit.

3.2.4 Characterization of BW (Band - Width):

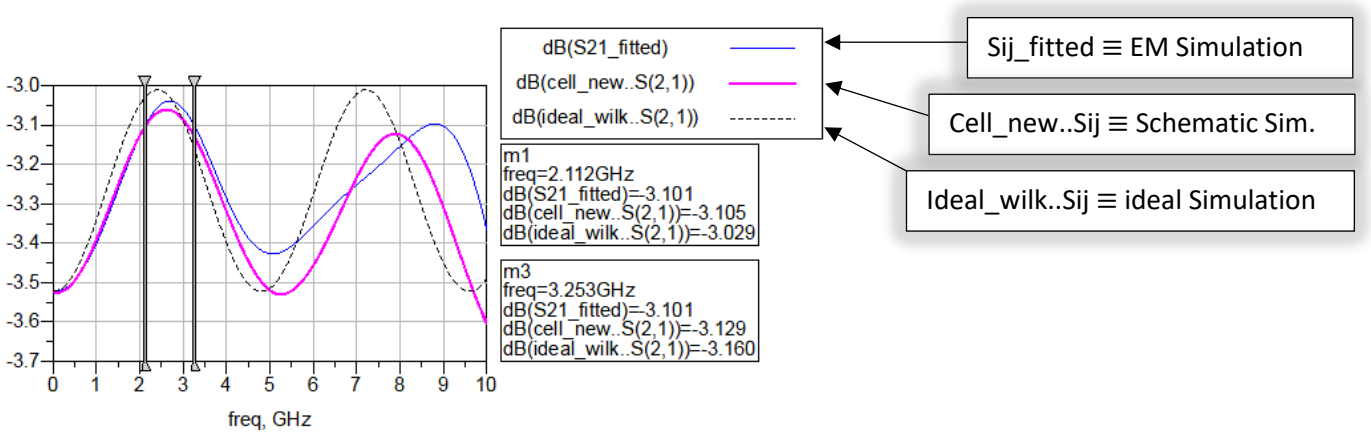


Figure 20: Insertion loss Band "3.1 dB"

Comments: We will find a metric to help us and since we are working on Wilkson power divider evenly, we have decided that BW is the insertion loss band and since we are working on a low power application, we have decided that the maximum input loss we accept is 3.1 dB hence our definition of BW. $(F_{High} = 3.253\ GHZ)$ & $(F_{Low} = 2.112\ GHZ)$

- **Center Frequency Definition:**
  Since we need to charactarize the Performance @ the BW we tried to define the center frequency of the BW to be the Artimetic mean of the Borders of the Band (F_{High}, F_{Low}).
  i. e: $F_{Center} = \frac{F_{High}+F_{Low}}{2}$

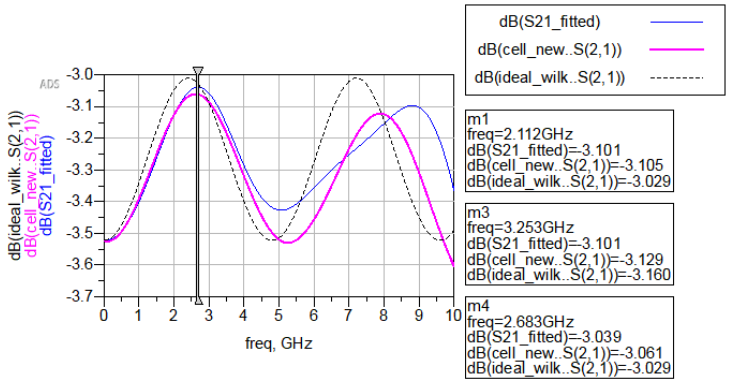


Figure 21: Insertion Loss Band Center Frequency

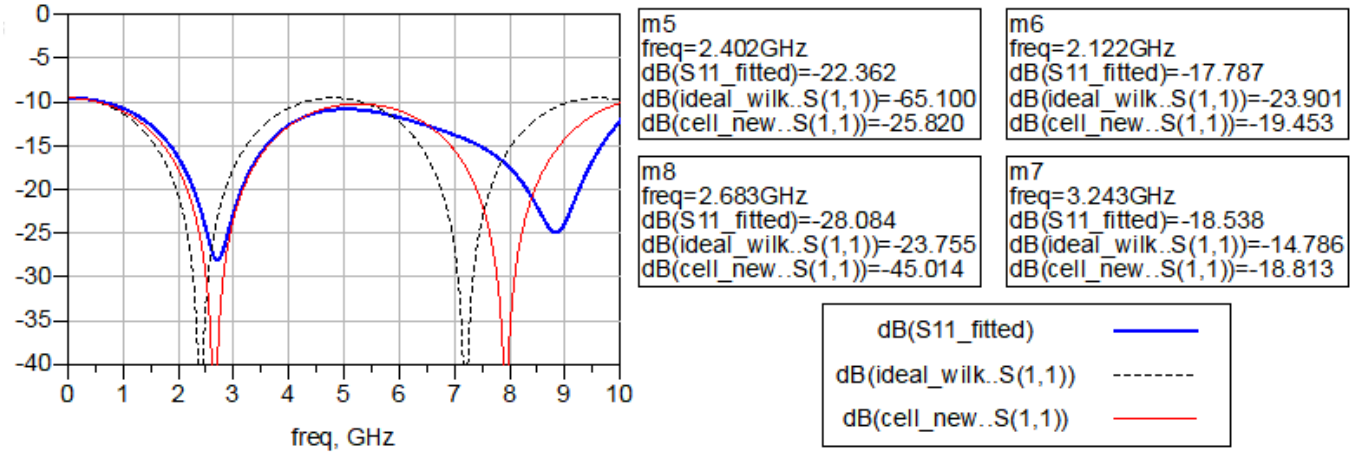


Figure 22: Reflection Coeff. port 1 (Schematic / EM / ideal)

Comments: Degradation of the performance of the Wilkinsion power divider from the ideal reference to the designed layout as follows:

→ Both the EM Simulation and the Simulation of the Discontinuity model show deviation of performance from the Center Frequency.

→ The Discontinuity model (Schematic) is almost showing all the parasitic present in the practical model, except for Higher Frequencies. On the other hand, the Practical model and the Schematic agree with Each other in the Design BW. (Observation).

→ **Both the practical and the model assures best Return loss @ the Center Frequencies.**

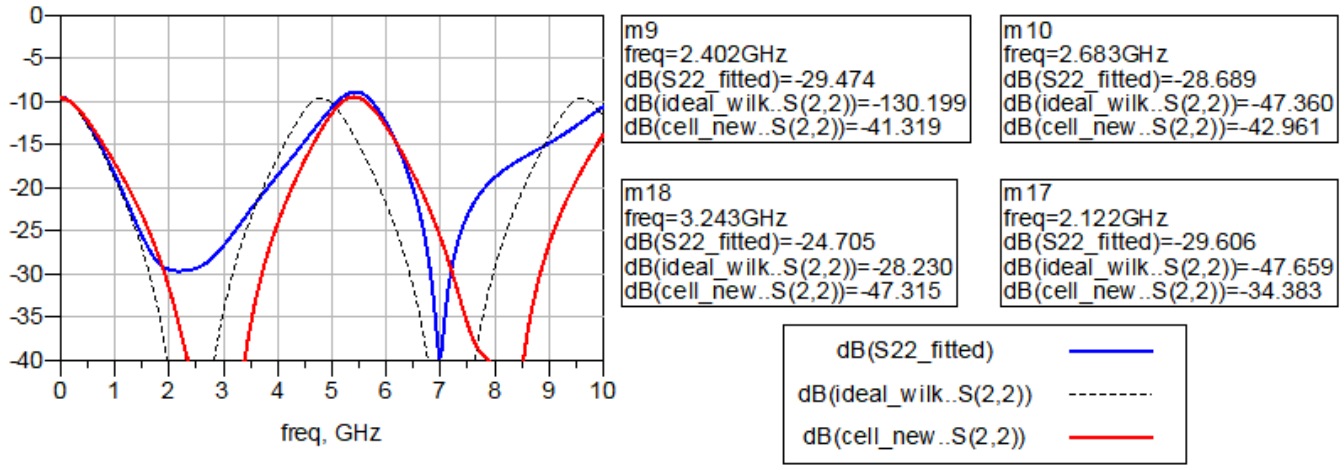


Figure 23: Reflection Coeff. port 2 (Schematic / EM / ideal)

Comments: There is a Mismatch Between Schematic and Practical Model in the Design BW although Coping with Each other in the other Frequencies.

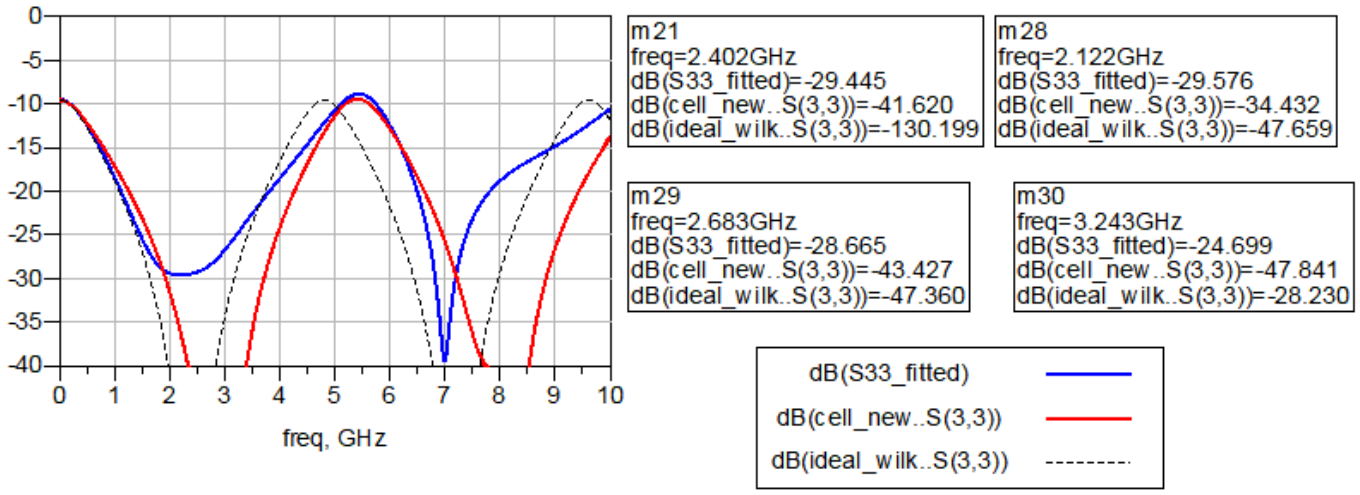


Figure 24: Reflection Coeff. port 3 (Schematic / EM / ideal)

Comments: There is a Mismatch Between Schematic and Practical Model in the Design BW although Coping with Each other in the other Frequencies, therefore, the Ratio Between Matching of Both Port 2 & 3 is nearly equal.

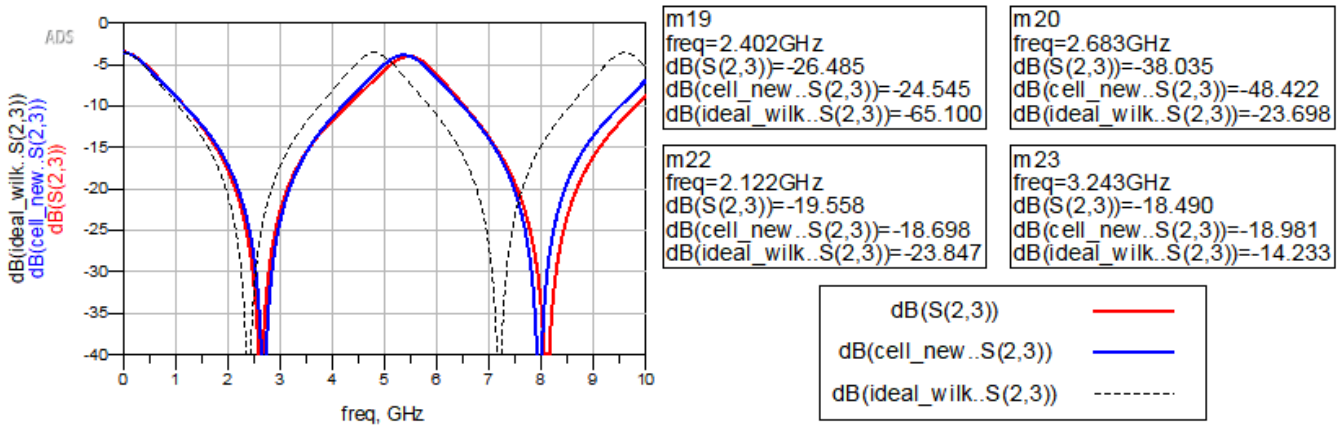


Figure 25: Isolation between the two Output Ports

Comments: Isolation is nearly equal in ALL Models.

→ isolation is the Best @ the center Frequency.

❖ Balancing Analysis

Practical Mismatch

```
EqnR_EM_DB=dB(S(2,1)/S(3,1))
EqnR_EM_phase=phase(S(2,1)/S(3,1))
EqnR_schema_DB=dB(cell_new..S(2,1)/cell_new..S(3,1))
EqnR_schema_phase=phase(cell_new..S(2,1)/cell_new..S(3,1))
EqnR_ideal_DB=dB(ideal_wilk..S(2,1)/ideal_wilk..S(3,1))
EqnR_ideal_phase=phase(ideal_wilk..S(2,1)/ideal_wilk..S(3,1))
```

Figure 26: Equations of Magnitude and Phase imbalance (Schematic / EM / Ideal)

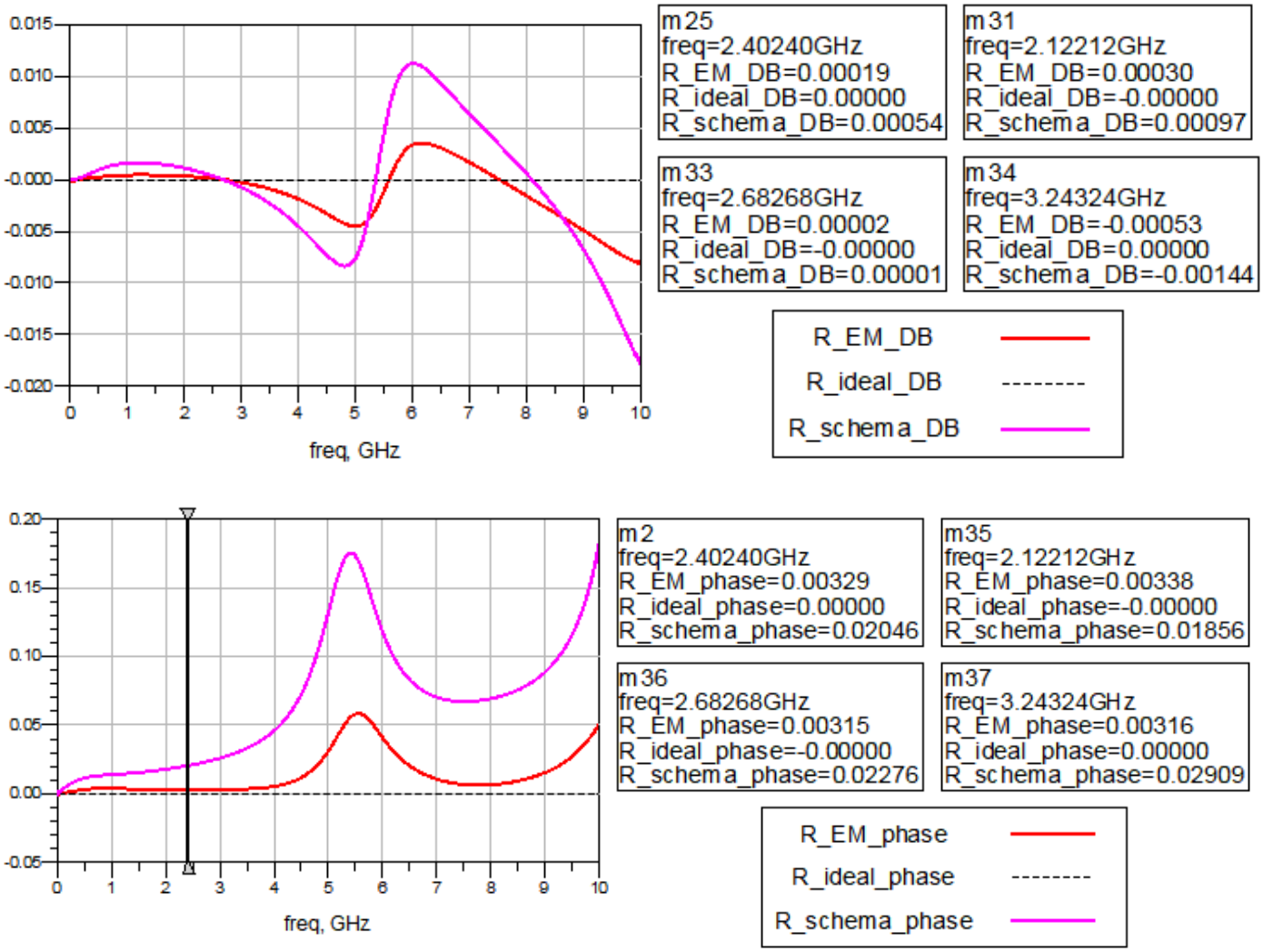


Figure 27: Magnitude & Phase imbalance (Schematic / EM / ideal)

Comments: Positive Results for Both the Schematic and EM Simulations

→ **Both the practical and the model assures best balance @ the Center Frequencies.**

- ❖ <u>From the Previous we can Conclude that the Circuit Can Obtain Best Overall Performance @ the Center Frequency, while in the Ideal Design the Best Performance Occurs @ the Design Frequency**.**</u>

- **Therefore, the Performance also Has Been Shifted Due to the Practical Mismatch.**

<u>Summary for ILB (Insertion Loss Band):</u>

$\text{Bandwidth}_{3.1\ \text{IL}} = 1.128\ \text{GHZ}$ (IL = Insertion Loss)

from (F_L): 2.12 GHZ , To (F_H): 3.248 GHZ ,
$F_H \equiv$ High Frequency , $F_L \equiv$ Low Frequency

$F_{\text{Center}} = 2.684\ \text{GHZ}, \rightarrow \Delta F_{\text{Shift}} = 284\ \text{MHZ}.$

- ✓ The Downfall of the Single - stage Design:
  - Although the Isolation and Matching of the Output Ports are Adequate For our application (Low - Power) But this will limit the Scalability of the Design.

    ∴ therefore, for a more practical Design we can look forward to enhancing the BW and the isolation accepting any possible Tradeoffs Such as insertion Loss.

3.3 Multi - Stage Wilkinsion Design.

3.3.1 Concept of Multi - Stage Design.

To comprehend the expected margin of error, it is crucial to examine the compromises associated with the design before establishing the next design objective.

A narrower bandwidth allows for a more equal distribution of power within a limited range of frequencies, while a wider bandwidth results in a less equal distribution of power across a broader range of frequencies.

Another trade-off in designing the Wilkinson power divider is between the size of the device and its performance. A smaller device offers convenience and potential improvements in performance by reducing unwanted effects. However, a smaller device may have a narrower bandwidth and lower power handling capability.

In summary, designing a Wilkinson power divider requires careful consideration of these trade-offs to optimize the device's performance for a specific application [5].

Hint:

The multistage Wilkinson power divider design is not suitable for the ZigBee application, but it is suitable for antenna applications. (High Power).

One major limitation of the Wilkinson Power Divider is its relatively limited bandwidth. However, this issue can be mitigated by incorporating a quarter-wavelength section before the power combiner. This approach allows for impedance transformation to occur in two stages, resulting in an improved bandwidth.

Alternatively, the bandwidth of the power divider can be expanded by dividing the two quarter-wavelength sections into multiple sections, with a resistor placed between each section. A popular approach is to utilize three sections instead of just one, although additional sections can also be employed for further enhancement of the bandwidth.

3.3.2. Design Setup:

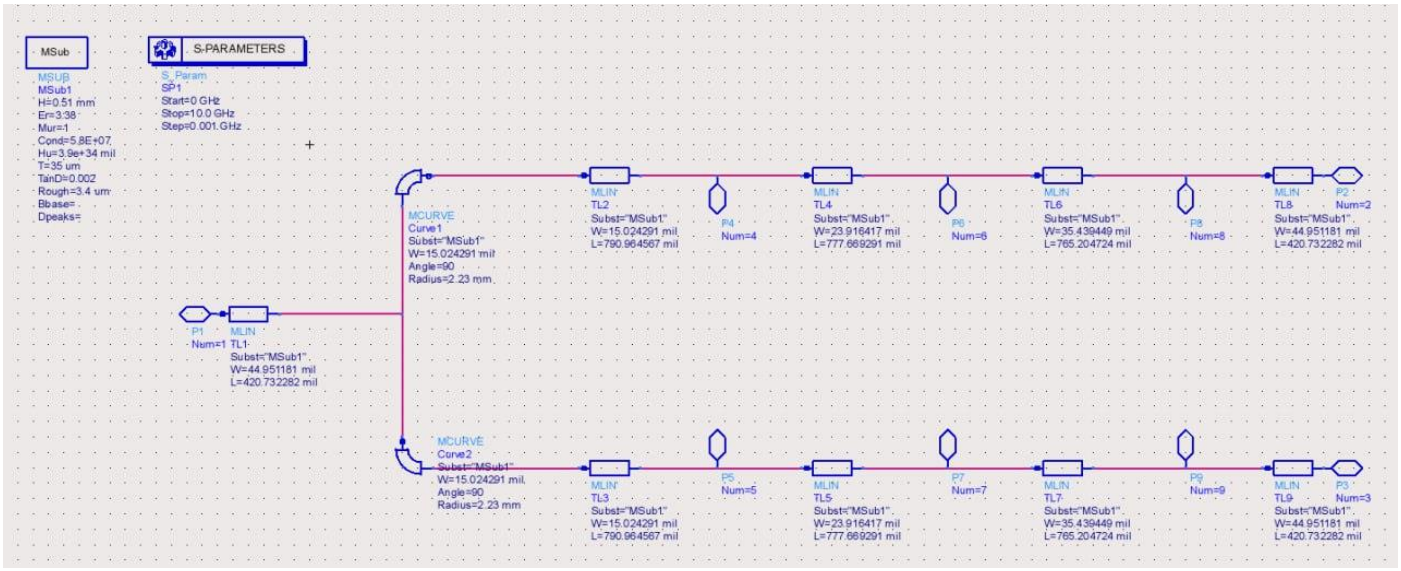


Figure 28: Start Up Schematic for 3 - stage Design.

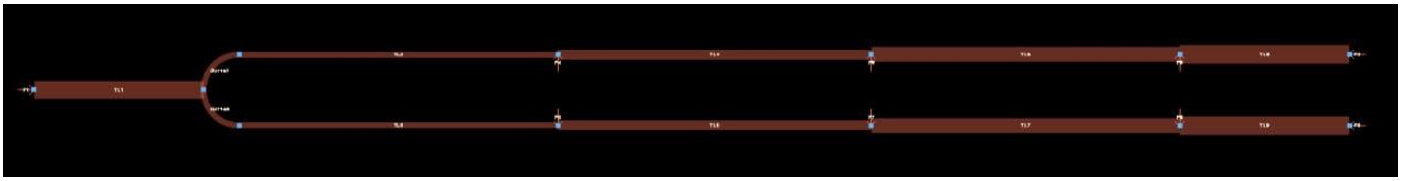


Figure 29: Layout Design 3 - stage Design

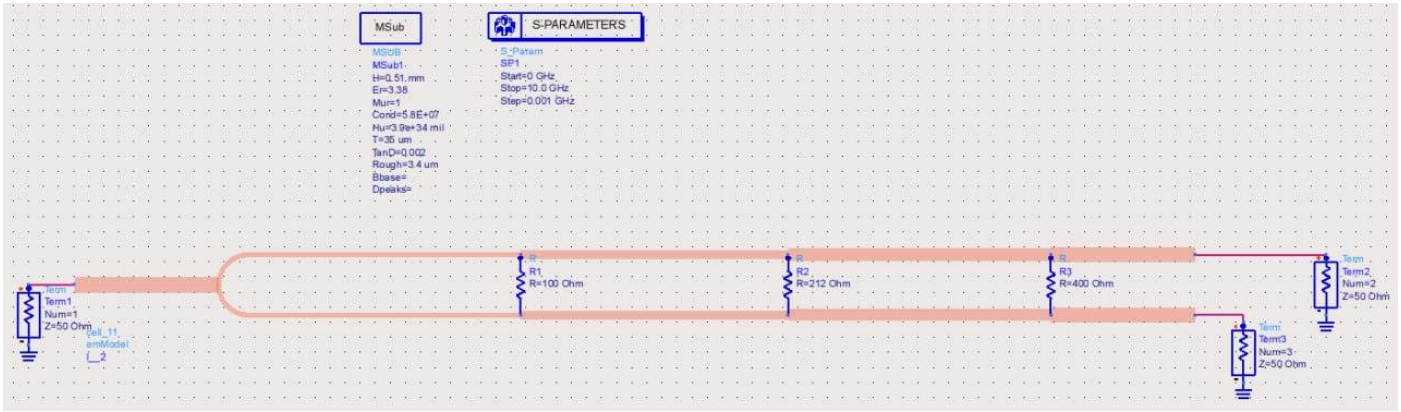


Figure 30: Final Schematic after making Symbol.

3.3.3 Characterization of BW (Band - Width):

To prove the wider bandwidth for multistage, we design a three stage Wilkinson microstrip power divider.

We will use different Characterization of the BW other than the insertion loss mentioned above.

- **Return Loss Band:**

A Band which the set of frequencies that assures least reflection on the input port.

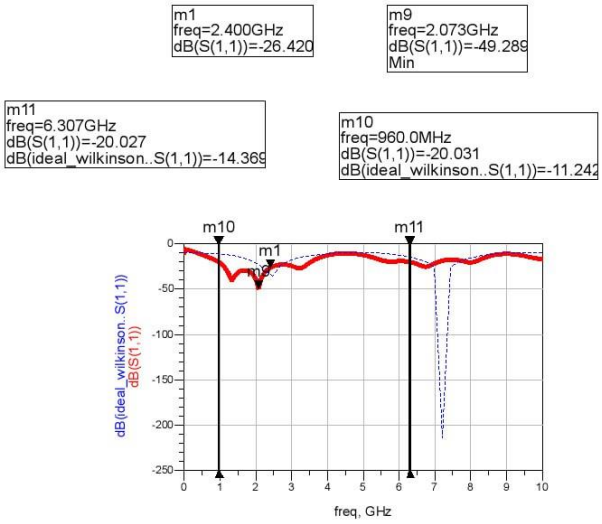


Figure 31: dB(S11) in 3 stages Design

Comments: the return loss band = high freq.-low freq.=6.304 GHz – 960 MHz=5.344 GHz as shown in figure (31).

---

for the reflection coefficient for the output ports S_{22} and S_{33} are represented as shown in figure (32).

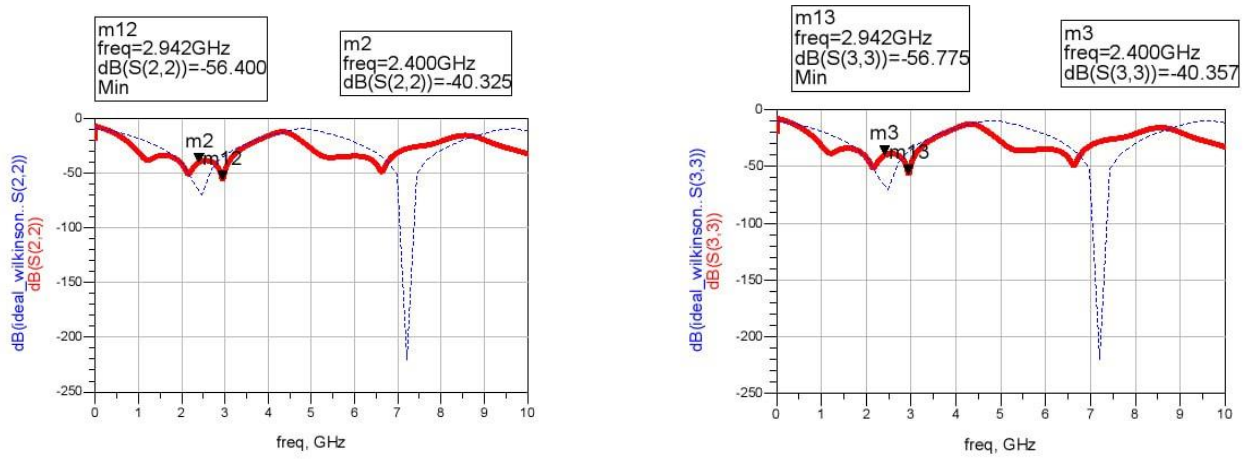


Figure 32: Reflection Coeff. For port 2, 3 at 3 -stage Design.

After that we will show the insertion loss Which is the S_{21} .Moreover we conclude

That the average value of the insertion loss Is occur at $3.4265\ \mathrm{GHz}$.in addition to that we

Will show the phase S_{21} which doesn't equate 90 degrees; therefore, we focus on obtaining the

Phase relative with each other which is defined by phase imbalance $[\mathrm{R\_phase}\ = \mathrm{phase}\ (S_{21}/S_{31})]$

and we also declare the dB value of imbalance which $[\ \mathrm{R\_dB} = \mathrm{dB}\ (S_{21}/S_{31})]$.

for more illustration the graph of S_{21}, phase (S_{21}), $\mathrm{R\_dB}$ and its phase $\mathrm{R\_phase}$ is shown in figure (33), figure (34).

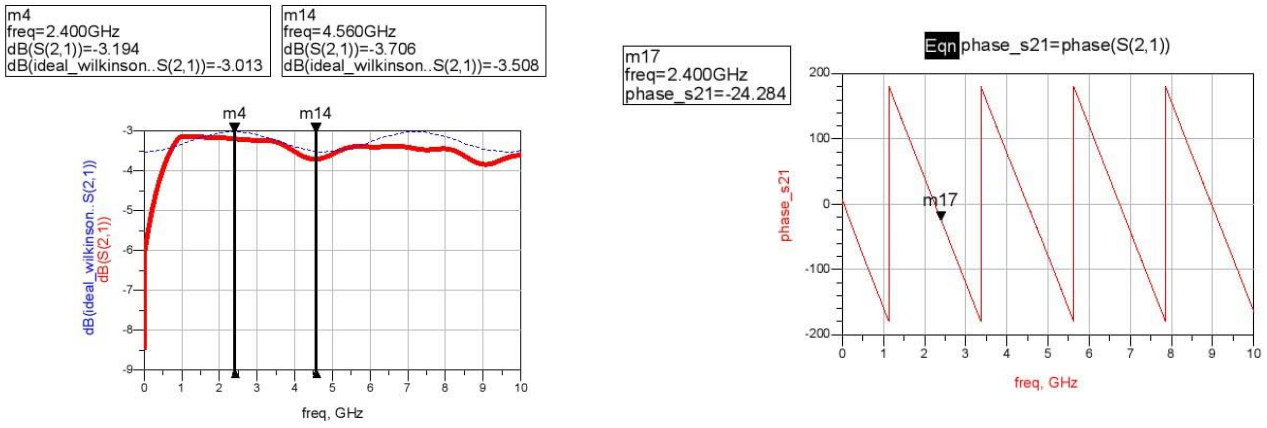


Figure 33: magnitude & Phase (S21) in 3 - stage Design.

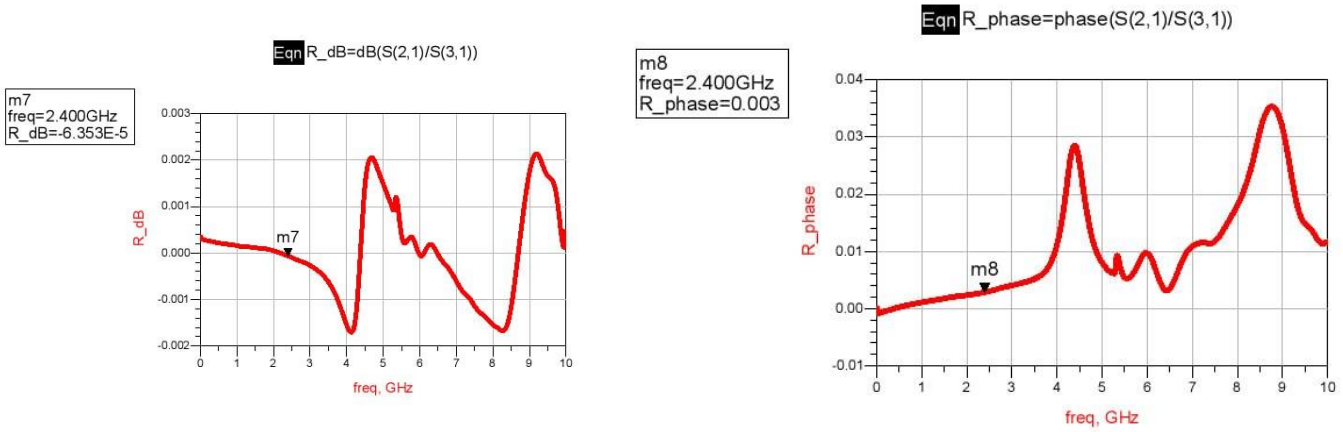


Figure 34: Magnitude & phase imbalance in 3 - stage Design.

Our design satisfies the good multistage Wilkinson power divider as the figures of

$\mathrm{R\_dB}$ and $\mathrm{R\_phase}$ nearly approximate zero. Moreover, we satisfy the condition for the insertion loss $\mathrm{dB}(S_{21})$ which is approximately equal to $-3\ \mathrm{dB}$ at the design freq. $\mathrm{f} = 2.4\ \mathrm{GHz}$

We also satisfy the isolation between the two output ports as $\mathrm{dB}(S_{32}) < -20\ \mathrm{dB}$ as shown in figure (35).

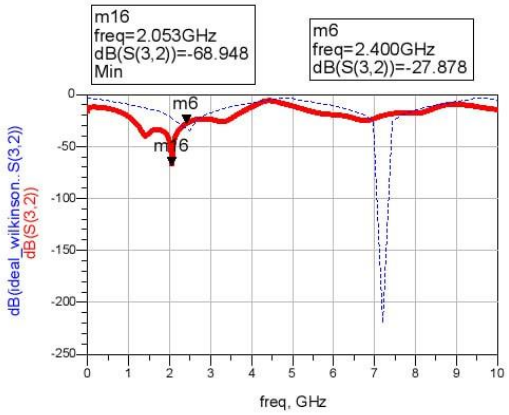


Figure 35: Isolation in 3 - stage Design

Notice that we no longer can have a perfect Wilkinson Power Divider, even at the design frequency. This is because of the parasitic effects of the components, mainly the resistive losses. The main reason that S_{32} deviates noticeably from the ideal components case, is that the phase of S_{21} is no longer $90°$.

---

4. Performance Summary

Design Metrics	Lumped	Microstrip 1 - stage	Microstrip 3 - Stages
Type of BW	IL Band	IL	RL
|Isolation|	126.643 dB	26.075 dB	27.787 dB
$\|Port_o$ Matching|	131.414 dB	29.491 dB	40.3 dB
Balancing	0	0	0
Insertion loss Band	580 MHZ	1.128 GHZ	-
Insertion loss	3.1 dB	3.1 dB	3.194 dB
Return loss Band	-	-	5.344 GHZ
Return loss	123.633 dB	22.1 dB	20 dB

5. References

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