FPGA-Only MVT Digitizer for TOF PET

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***Abstract*—The multi-voltage threshold (MVT) method, proposed by us, is a method for digitizing a PET event pulse by sampling with respect to certain reference voltages. Previously, we have implemented this method by using discrete voltage comparators together with discrete time-to-digital converters (TDCs) or TDCs implemented on a field-programmable-gate-array (FPGA), and shown that the method is useful for developing PET detectors capable of time-of-flight (TOF) measurement. In this paper, we investigate an FPGA-only implementation in which the differential I/Os of the FPGA operating in the low-voltage-differential-signaling (LVDS) receiver mode are configured to provide the function of the voltage comparators. Using an Altera Cyclone II Family FPGA (EP2C70F896C7), we built two MVT digitizing channels, each of which contains four comparators to yield eight samples for each event pulse. We describe the design, implementation and calibration of this FPGA-only MVT digitizer and report its performance properties. By connecting the channels to SensL's silicon photomultipliers (SiPMs) FM30035 coupled to $2 \times 2 \times 10$ mm^3 LYSO crystals, we measured an energy resolution of $\sim 16\%$ (at 511 keV) and a coincidence resolving time (CRT) of $\sim$ 500 ps (FWHM). These resolutions are promising for developing PET and TOF PET detectors. On the other hand, based on digitized waveforms of pulses generated by the same SiPMs and LYSOs acquired by using a 50 giga-sample-per-second (Gsps) digital oscilloscope (Tektronics DPO71604B), we measured an energy resolution of $\sim 9\%$ and a CRT of $\sim$ 390 ps. The comparison suggests that our current implementation of the FPGA-only MVT digitizer contributes an $\sim$ 13% energy resolution and $\sim$ 310 ps CRT.**

***Index Terms*—Digitizer, FPGA, LVDS, MVT, TOF PET.**

I. Introduction

RECENTLY, there is a substantial interest in moving PET detector electronics in the direction of digitizing an event pulse at the earliest possible stage to avoid information-loss during analog filtering/shaping and transmission [1]–[4]. By digitally analyzing the resulting samples, the information carried by the pulse can be extracted [5]–[8]. This digital architecture allows one to tap the power of modern digital electronics and processing algorithms to lower detector cost and shorten the development/upgrade cycle. It can also lead to simplified electronics. Modern PET detectors use fast scintillators (e.g., LSO and LYSO) and photo-detectors to generate short pulses having fast rise time. For such pulses, when using the conventional sampling method that takes samples at a regular time interval, a sampling rate above 1 giga-sample-per-second (Gsps) is needed [9]. This high rate is not practically feasible with the current analog-to-digital converters (ADCs), especially when considering the large number of digitizing channels needed by a PET system. Several research groups, including us, have recently investigated the use of the Domino Ring Sampler (DRS) to provide fast sampling (e.g., 1–5 Gsps) for a limited period of time (e.g., 200 ns) [2], [10], [11]. However, a long conversion time is needed for reading out the stored amplitudes and as a result its count-rate capability is limited. For PET imaging, this issue is a concern but may be resolved as the count rate is limited by the amount of radioactivity that can be administrated to a subject.

As an alternative solution to the sampling-rate challenge discussed above, we have previously proposed a multi-voltage threshold (MVT) sampling method that takes samples of a pulse with respect to a set of reference voltages[1][12]. By choosing the reference voltages properly, the MVT method can always obtain samples at the fast leading edge of a pulse. By utilizing in analysis the known characteristic shape of the pulse, from samples obtained at the leading edge and trailing tail of a pulse one can derive its time and energy. We have shown that, for PET detectors it is sufficient to use only a few reference voltages to obtain a small number of samples. As the pulses are instantaneously digitized and the number of samples per pulse is small, this sampling method can have a high count-rate capability without requiring a large on-board buffer for storing the samples.

We have shown that the MVT sampling method can be useful for building PET and time-of-flight (TOF) PET detectors [1], [13] and have developed a preclinical PET scanner based on it [14], [15]. Our implementations of the sampling method were based on using discrete voltage comparators with discrete time-to-digital converters (TDCs) or TDCs implemented on a field-programmable-gate-array (FPGA). The scope of this paper is to demonstrate a new FPGA-only implementation that can be readily applied to build many MVT digitizing channels, and to characterize its performance properties when applied

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[1]Thus, one can consider the conventional ADC as time-based sampling and the MVT method as amplitude-based sampling.

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to pulses generated by LYSOs coupled to silicon photomultipliers (SiPMs). This goal is of considerable practical interest because nowadays FPGAs are widely, if not ubiquitously, used in data acquisition (DAQ) electronics and the capacity (capacity-to-cost ratio) of FPGAs expand (increases) greatly and quickly. An FPGA-only implementation therefore can greatly simplify the DAQ electronics. It also allows us to readily modify, or add functions to, the implementation without requiring costly hardware changes. When desired, the FPGA implementation can be readily turned into ASICs as well. We are interested in LYSO/SiPM because it is widely considered for developing next-generation PET and TOF PET systems. An LYSO/SiPM based PET detector is expected to require high-density readout and this has posed a significant challenge. With modern FPGAs, high-density readout at affordable cost is possible.

The FPGA-only implementation under consideration is new. A key component of the development is to investigate whether the differential I/Os in certain FPGAs can be configured to function as voltage comparators exhibiting adequate response properties for pulses generated by LYSO/SiPM. This is currently unknown and, as we will report below, the task is not straightforward. The resulting FPGA-only implementation can also lead to a useful research tool for investigating important design questions with the MVT sampling method in our subsequent work, such as how the number of reference levels and reference voltage settings affect its performance, to yield information needed for understanding the characteristics of this new sampling method and optimizing the implementation.

The rest of this paper is organized as follows. In Section II, we describe the design, implementation and calibration of the FPGA-only MVT digitizer. In Section III, we describe performance properties of the resulting MVT digitizer. Concluding remarks and discussion are given in Section IV.

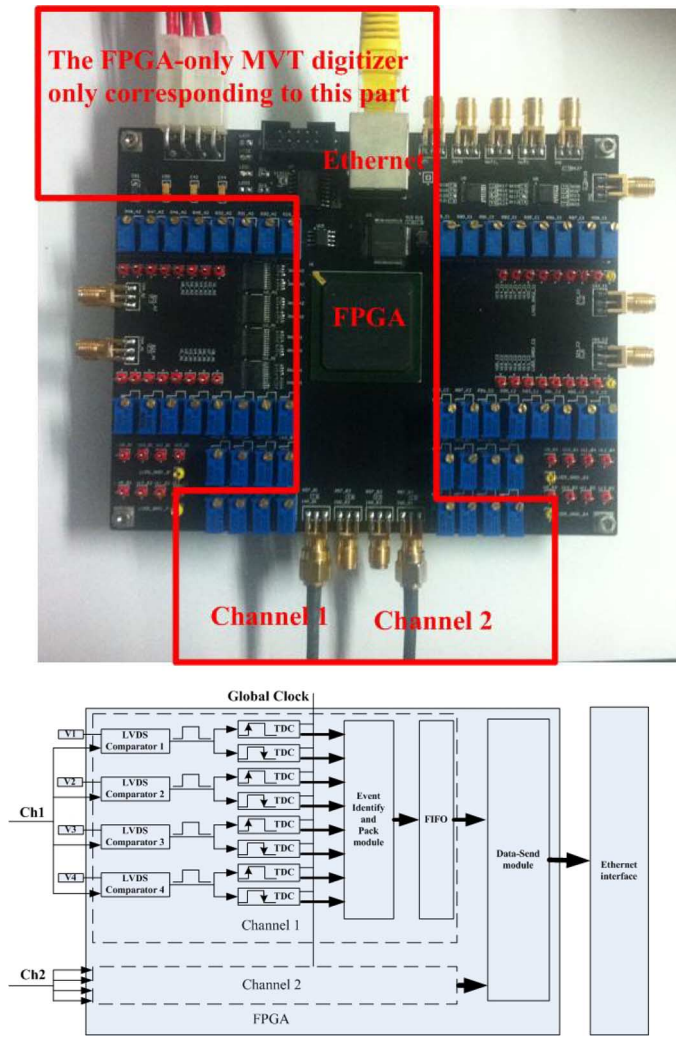

Fig. 1. Top: A photograph of the FPGA-only MVT digitizer board containing two sampling channels. Bottom: Design schematics corresponding to the region identified by the red lines in the photograph. Inside the FPGA, each sampling channel has four comparators, eight TDCs, an Event Identify and Pack module and an FIFO. The FPGA also contains a Data-Send module for providing handshaking/control logics with the Ethernet interface, implemented by using a Winzet W5100 chip.

II. Design, Implementation and Calibration

A. Design of a 2-Channel FPGA-Only MVT Digitizer

As already mentioned above, the central idea of the MVT sampling method, presented in [12], [13], is to sample a pulse with respect to a set of reference voltages. A typical pulse generated by a scintillator-based PET detector has a fast-rising leading edge followed by slower-decaying tail. Disregarding the effect of noise, using N reference voltages will therefore generate N samples at the leading edge (called *leading samples* below) and N samples at the trailing tail (called *trailing samples* below). By analyzing these $2N$ samples in accordance with the *a priori* knowledge about the pulse shape, one can calculate the event time, event energy, and decay constant of the pulse (for building *phoswich* detectors).

Fig. 1 shows the two-channel FPGA-only MVT-digitizer board that we have prototyped by using an Altera EP2C70F896C7 FPGA and its design schematics. As shown, each MVT channel has four comparators to provide four reference voltages. A key feature of the implementation is to use the differential I/Os of the FPGA working in the low-voltage-differential-signaling (LVDS) receiver mode to function as voltage comparators (they are referred to as the *LVDS comparators* below). A PET event pulse generated by a scintillator/photo detector is split into four signals, each of which is fed to an LVDS comparator. The logic output of the LVDS comparator is connected to two TDCs for determining the digital times of its positive and negative transitions, therefore generating a total of eight samples for a pulse having a sufficient amplitude. Since the voltage values are known *a priori*, these samples need only containing the time values generated by the TDCs. The eight time samples generated for a pulse are packaged into an event-word and stored in a FIFO. The FIFO data are sent out via an Ethernet interface for analysis. The LVDS comparators, TDCs, Event Identify and Pack module, and FIFO are all implemented on the FPGA. Also implemented on the FPGA is a Data-Send module for talking to an Ethernet interface that is implemented by using a Winzet W5100 chip.

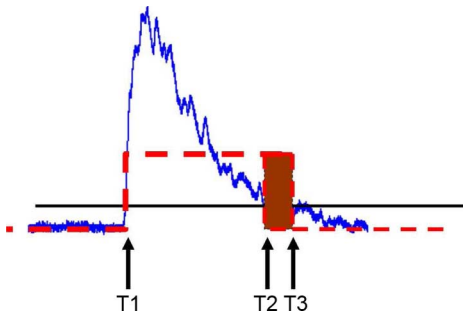

Fig. 2. A sample output of an LVDS comparator (dash line) with respect to the pulse at its positive input (solid curve). The horizontal solid line indicates the reference voltage. Due to noise, multiple transitions are obtained at the trailing tail of the pulse. Currently, we arbitrarily choose to use the last transition for determining the time value of the sample at the trailing tail (i.e., T_3).

B. Implementation

Implementations for key components in Fig. 1 are described below. These implementations take up ~ 6 of the logic elements of the Altera EP2C70F896C7 for one 4-level MVT sampling channel. Therefore, it is possible to implement up to 16 such 4-level sampling channels on this FPGA.

1) LVDS Comparator: An LVDS receiver in an FPGA has a positive input and a negative input and its output is determined by the relative voltages appearing on these inputs. It sends a logic '1' when the voltage at its positive input is higher than that at the negative input; otherwise, it sends out a logic '0'. To employ this I/O to function as a voltage comparator for MVT sampling, we feed the signal pulse to its positive input and apply a constant voltage, serving as the reference voltage, to its negative input. Currently, this reference voltage is provided by a variable resistor (see Fig. 1).

Fig. 2 shows a sample output of an LVDS I/O and the pulse at its positive input. As shown, the output is initially at logic '0' and makes a unique transition to logic '1' at time T_1 when the pulse rises and stays above the reference voltage. At the trailing tail, on the other hand, due to the presence of considerable noise that causes the pulse to randomly cross the reference voltage we obtain multiple transitions between '0' and '1' during time T_2 and T_3. There is no convincing argument to prefer one of these transitions as the true transition and at present we arbitrarily choose to use the last transition from '1' to '0' for purpose of simplifying the implementation. This choice may lead to a bias toward increasing the time value of the sample at the trailing tail.

2) TDC: Our FPGA implementation of the TDC is based on the work of Song *et al.* [16]. Below, for sake of completeness we will briefly review the design and principle.

Fig. 3 depicts the TDC implemented by using a *carry chain* consisting of *N* binary adders by connecting the carry-out Co of *adder* [n-1] to the carry-in Ci of *adder*[n]. By holding *A* and *B* inputs to '1' and '0', each adder in effect transmits the value of its Ci to its Co and outputs the inverse of Ci at S. The only exception is *adder*, which transmits *Signal* to C_o and outputs the inverse of *Signal* at S. The FPGA clock drivers a coarse-time counter and latches the *S-bits* content of the carry chain. Now, consider that the *Signal* makes a positive transition from '0' to '1' between two clocks. Before transition, the S and Co values

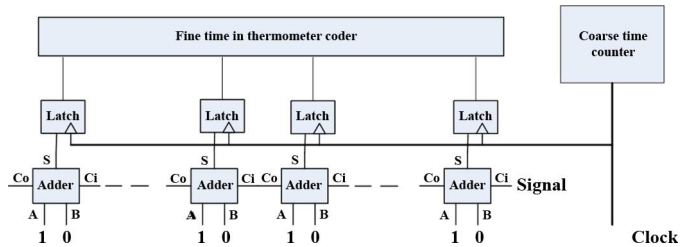

Fig. 3. TDC implementation in the FPGA by using a carry chain.

of all adders will equal '1' and '0'. At transition, the S and Ci values of *adder* will be inverted to '0' and '1'. After a delay, the Co output of *adder* will reach the Ci input of $adder[1]$ and inverts the S and Ci values of *adder* [1] to '0' and '1' as well. Likewise, such inversion will take place in sequence at *adder* [2], *adder* [3] and so on as the Co output of *adder*[n-1] reaches the Ci input of *adder* [n] after some delay. Thus, at the second clock the latched *S*-bits content will have the format '$1110\cdots0$' where the number of least-significant-bit (LSB) zeros is related to the amount of time before the second clock when the positive transition of *Signal* occurs. Similarly, when *Signal* makes a negative transition from '1' to '0', the S-bits content latched in the next clock will have the format '$\cdots0111\cdots1$'. And in this condition, the number of LSB ones will represent the amount time before the next clock when the negative transition of *Signal* occurs. Subsequently, the number of LSB zeros/ones in this *thermometer code* can be counted and converted to the *natural binary code* [17]. This is the *fine time* because it measures time between clocks. Above, we have assumed that the propagation time from *adder* to *adder* [n] is longer than the clock interval.

In our implementation, the carry chain has 128 binary adders, the system clock is 200 MHz, and the fine time has 8 bits (in the natural binary code). In addition, the coarse-time counter has 40 bits and can count up to 90 minutes when using a 200 MHz clock. Thus, the TDC output has a total of 48 bits. The propagation delays between two adders are not identical and need to be measured for calibrating the fine time. Fig. 4 shows the differential non-linearity (DNL) of the fine time generated by a TDC (measured by using the method described in [18], [19], which indicates a bin width of 71.4 ps ± 48.2 ps (mean $\pm$ RMS). Such measurements are performed to obtain the bin widths for all the implemented TDCs during calibration. The measured values are stored and used to calibrate the fine-time measurement of each TDC. According the method provided in [20], the resolution of such TDC is estimated to be 86 ps FWHM.

3) Propagation Delays: In the FPGA-only implementation, the propagation delays from LVDS comparators to their associated TDCs are not constant within the same MVT channel due to the difference in path length. In our first implementation, the variation in the propagation delay was observed to be as large as ± 300 ps and this variation can considerably degrade timing measurements. By manually adjusting the relative positions of the LVDS I/Os and TDCs in the FPGA implementation, we were able to reduce this variation to approximately ± 50 ps.

4) Event Identify and Pack Module, FIFO and Data-Send Module: For each channel, the eight 48-bit time values generated by the TDCs are directly sent to the Event Identify and

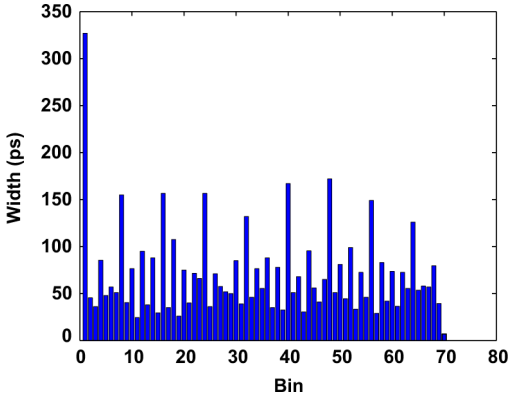

Fig. 4. The differential non-linearity of our FPGA-based TDC. The distribution of the bin width is 71.4 ps ± 48.2 ps.

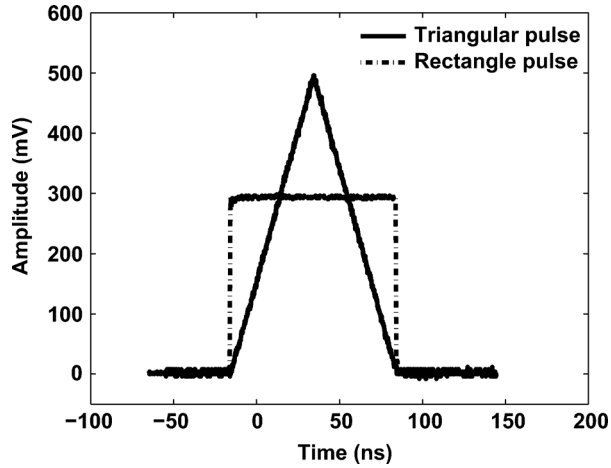

Fig. 5. Test pulses generated by a Tektronix AWG7122C.

Pack module. When the module receives a leading sample corresponding to the lowest reference voltage, an event identification process is triggered as follows. For a valid event, this leading sample must be followed by three leading samples within two clock cycles, which is 10 ns and is sufficiently longer than the rise time of the event pulse. In addition, within 50 clock cycles, which is 250 ns and is sufficiently longer than the duration of the event pulse, the four leading samples must be followed by exactly four trailing samples. If these conditions are satisfied, the four leading samples and the four trailing samples are assigned to a valid event; otherwise, all samples under processing are discarded. For a valid event, we combine the leading and trailing samples produced by the same comparator into a *frame*. The frame is marked by an $'FF'$ identifier at the beginning, which is followed by another byte that encodes the channel and comparator at which the samples are generated. This byte is again followed by the time values of the two samples. A frame is therefore 112-bit wide and contains two times samples. The four frames obtained for each pulse are combined into a 448-bit event-word and sent to the FIFO. It is noted that since we only accept events that have eight samples, the highest reference voltage of the MVT channel will define the lower-energy limit for detection. We will determine the proper reference voltages to use by a calibration process to be discussed in Section II-B.

The FIFO has a capacity of 448 kbits and can store up to 1024 event-words. The FIFO content is read and sent to an external board or computer through a 100 Mbps Ethernet interface, which is implemented by employing a Winzet W5100 chip using the UDP protocol. The Data-Send module combines every two event-words into a 1024-bit frame, with unused bits filled by '0' and sends to the W5100. The W5100 packs the frame to a UDP package and sends it out. Our measurement shows that the implemented Ethernet interface can reliably support a transfer rate of about 56 Mbps. Therefore, the overall count-rate capability of the two-channel MVT digitizer is currently limited to about 0.11 million-count-per-second (Mcps). We are upgrading the Ethernet interface to 1 Gbps to increase the count-rate capability.

C. Voltage Calibration

An important requirement for the MVT sampling is that the pulse samples must be acquired at exactly known reference voltages. In addition, the comparator must make fast and precise state transition when the pulse crosses the reference voltage. In [13], high-quality discrete comparators were employed to meet these requirements. With the FPGA-only implementation, it is not clear whether the LVDS comparators have the needed properties.

To investigate the accuracy in the reference-voltage setting, we employed the triangular test pulse shown in Fig. 5; of which both the positive and negative slope had an absolute value of 10.0 mV/ns and the peak amplitude was 500 mV. The test pulse was generated at precision by using a Tektronix AWG7122C Arbitrary Waveform Generator that had a > 1 GHz analog bandwidth and 12 Gsps sampling rate. We assigned various reference voltages to the LVDS comparators and applied the test pulse. Using the resulting samples, we obtained the time difference between the trailing and leading samples produced by the same comparator to obtain the duration-over-threshold(DOT) at the reference voltage applied to that comparator. From thus measured DOT we could calculate the reference voltage at the comparator: Considering a triangular pulse having a rising slope of k_1 and a falling slope of k_2, the DOT obtained at the reference voltage V_t is given by

$$\tau\left(V_t\right) = \frac{V_p - V_t}{k_1} - \frac{V_p - V_t}{k_2}, \tag{1}$$

where V_p is the peak amplitude. It follows that

$$V_t = V_p - \frac{k_1 \times k_2}{k_2 - k_1} \times \tau\left(V_t\right) = 500.0 - 5 \cdot \tau\left(V_t\right)\ \mathrm{mV}, \tag{2}$$

where the second equality is obtained by using $k_1 = 10\,\mathrm{mV/ns}$, $k_2 = -10\,\mathrm{mV/ns}$, and $V_p = 500.0\,\mathrm{mV}$, and by measuring $\tau(V_t)$ in nanosecond. If the comparator behaviors properly, the applied and calculated reference voltages shall be identical.

Fig. 6 plots, for the four comparators of channel 2, the calculated reference voltages against the applied reference voltages, ranging from 40 mV to 200 mV at a step of 20 mV. As discussed above, in theory the plot shall yield straight lines with a slope of 1 through the origin. As shown, within statistical uncertainty the relationship between the calculated and applied reference voltages does follow a linear relationship with the expected slope. However, there is an offset between the two voltages and this

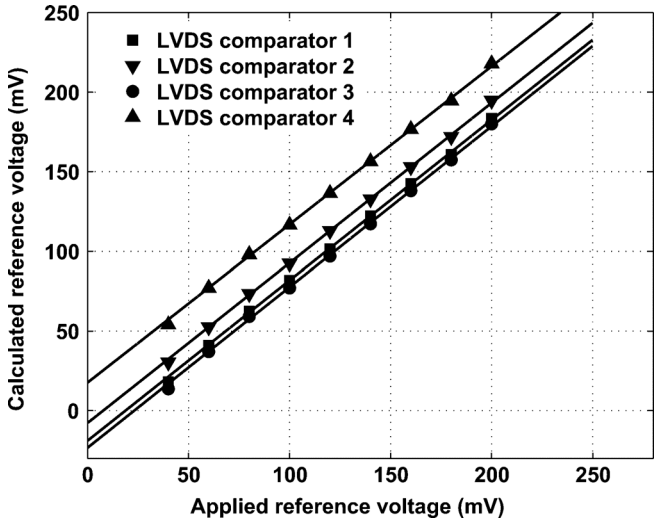

Fig. 6. he calculated reference voltages versus the applied reference voltages for the LVDS comparators of channel 2. Also shown are the straight lines obtained by least-squares fitting.

TABLE I
ESTIMATED VOLTAGE BIAS AT EACH COMPARATOR.

Comparator	1	2	3	4
Channel 1	25 mV	17 mV	23 mV	5 mV
Channel 2	16 mV	6 mV	23 mV	-17 mV

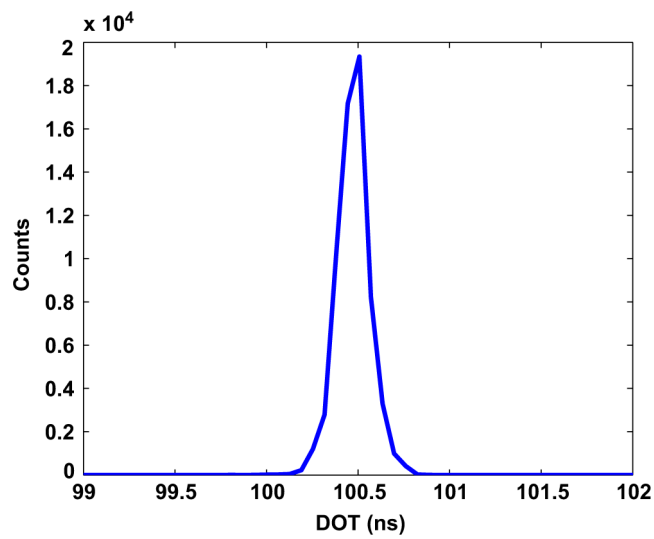

Fig. 7. A distribution of the measured DOT from 10,000 repeated measurements using the rectangular test pulse. By fitting to a Gaussian function, this distribution has a FWHM of $\sim$ 266 ps.

offset varies with the comparator. A simple and plausible explanation to this result is that there is a non-zero bias at the positive or negative input, or both, of the LVDS comparator. This bias, which can be estimated by extrapolating the plot in Fig. 6 to zero applied reference voltage, needs to be calibrated from the applied reference voltage to yield the actual reference voltage at the comparator. Table I shows the estimated biases thus obtained for all the LVDS comparators of our MVT digitizer.

III. PERFORMANCE CHARACTERIZATION

A. Timing Accuracy

To examine timing accuracy of the MVT digitizer, we employed the rectangular test pulse shown in Fig. 5. This test pulse, which had a duration of 100 ns and a rising and falling time of $\sim$ 500 ps, was again generated at precision by using a Tektronix AWG7122C. As the pulse had sharp rising and falling edges with respect to its duration, at all reference voltages the actual DOT should equal the known pulse duration of 100 ns. Table II shows the means and FWHMs of the measured DOTs obtained for two LVDS comparators (and their associated TDCs) at three reference voltages, including 60 mV, 100 mV and 140 mV. These results were calculated from a DOT distribution generated by ten-thousand repeated measurements and Fig. 7 shows an example distribution obtained for 100 mV. From Table II, it is observed that the largest difference in the mean between the measured DOT and the expected value is 2.5 ns. It is also observed that, for both comparators the measured DOT is longer than the expected value at low reference voltages and the value decreases as the reference voltage increases. These observations with the difference-in-the-mean can be explained by the finite analog bandwidth of the digitizer board that slows down the rising and falling edges of the pulse. As a result, the actual DOT at a high reference voltage will be less than the nominal pulse duration, resulting in a shorter DOT.

Table II also shows that the timing resolution on a sampling level of the MVT digitizer is on the order of 300 ps FWHM (ranging from 266 to 373 ps FWHM). This timing resolution is affected by the statistical variation in the transition time of the LVDS comparator between the '0' and '1' states and the precision of the TDCs. The TDC has an resolution of 86 ps (see Section II-A). Since two TDCs are involved in the DOT measurement, the timing resolution due to TDC is 121 ps. This indicates that currently the timing resolution is dominated by the LVDS comparators. We estimate the LVDS comparator contributes about $\sim$ 275 ps timing resolution, suggesting $\sim$ 194 ps variation in the transition time.

The observed timing accuracy can present an obstacle to using the current implementation for developing TOF PET detectors having better than 300–400 ps FWHM coincidence resolving time (CRT). However, it shall be able to support 500–600 ps FWHM CRT. We note that this suboptimal timing accuracy shall not be surprising considering that it is achieved by using a general-purpose FPGA rather than by using discrete comparators and TDCs that are specifically designed for their respective functions.

B. Experimental Setup for Coincidence Detection

We applied the developed MVT digitizer for coincidence detection with the setup shown in Fig. 8 in which two LYSO/SiPM detectors were placed 5 cm apart with a weak ^{18}F source inserted between them. The LYSO crystal, having a dimension of $2\times2\times10\ \mathrm{mm}^3$, was coupled to the central $3\times3\ \mathrm{mm}^2$ active area of the SiPM via one of its $2 \times 2\ \mathrm{mm}^2$ surface by using silicone optical grease (EJ550 from the ELJEN technology). The other five surfaces of the crystal were polished and wrapped in Teflon tape and the wrapping is approximately 0.25 mm thick. We used

TABLE II
DOT (MEAN ± FWHM) MEASURED FOR RECTANGULAR PULSE.

Reference voltage	LVDS comparator 1	LVDS comparator 2
60 mV	102.5 ns±373 ps	102.0 ns±300 ps
100 mV	101.1 ns±303 ps	100.5 ns±266 ps
140 mV	99.5 ns±327 ps	98.9 ns±305 ps

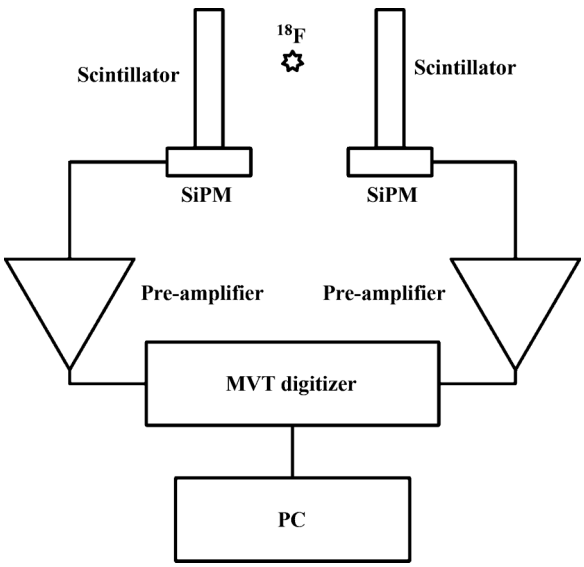

Fig. 8. The experimental setup for coincidence detection. The LYSO/SiPM detector contains a $2 \times 2 \times 10$ mm^3 LYSO coupled to a SensL FM30035 SiPM. The signal is derived from the fast channel of the SiPM. The gain of the preamplifiers is 10. The samples obtained by the MVT digitizer are sent to the PC via the Ethernet.

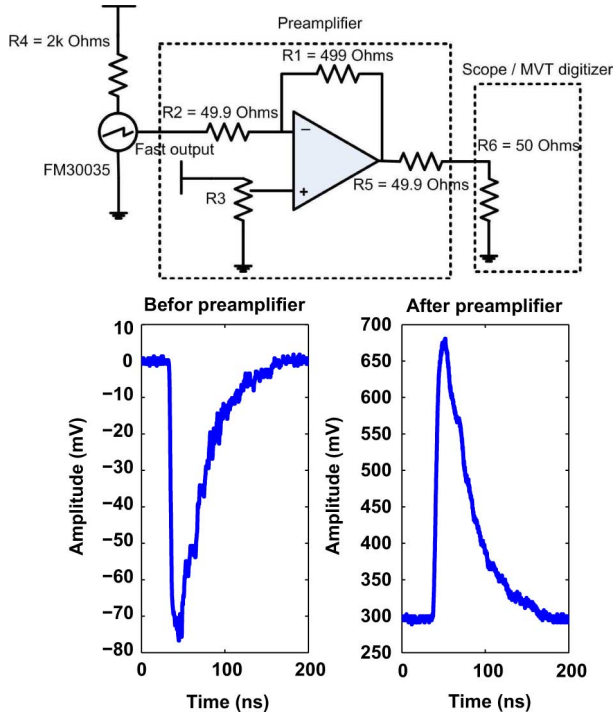

Fig. 9. Schematics of the custom-made preamplifier and the SiPM operating circuit. The amplifier used is TMS3201 from TI. The output signal of the preamplifier is connected to the oscilloscope or MVT digitizer, both having a 50 Ohm input resister. By adjusting the variable resistor R3, a baseline offset can be added to the output signal. The gain of the preamplifier is given by the ratio of the R1 and R2 and is equal to 10 in our design. According to the datasheet for TMS3201, the bandwidth of the preamplifier at this gain is estimated to be > 500 MHz. Bottom: The signal pulse before and after the preamplifier. It can be observed that the preamplifier maintains the pulse shape quite well. The length of both pulses is shorter than 150 ns and the rise time is about 3 ns.

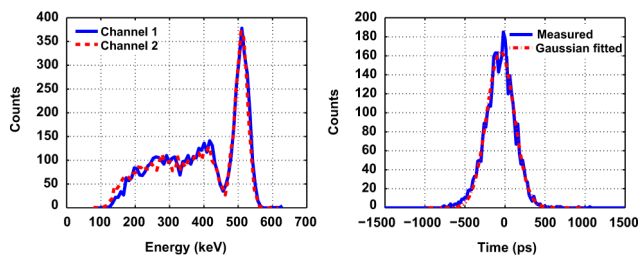

Fig. 10. The energy spectra and coincidence-time histograms obtained from data acquired by a 50 Gsps digital oscilloscope (Tektronix DPO71604B). They show energy resolutions of 9.5% and 8.9% at 511 keV and a CRT of approximately 390 ps FWHM. The charges corresponding to the photo peaks are 261 pC and 263 pC for channels 1 and 2, respectively.

SensL's FM30035 SiPM, which is recently introduced and reported to have a fast timing response attractive for TOF applications [21], [22]. It operated at a bias voltage of 32.0 V and the signal was derived from its fast output channel. The signal was inverted and amplified by a custom-made preamplifier shown in Fig. 9. This preamplifier used a variable resistor R3 for introducing a baseline offset to the signal. Its gain, determined by the ratio of R1 and R2, was equal to 10. The preamplifier output was then connected to a digital oscilloscope or the MVT digitizer.

We first acquired the waveforms of the preamplifier outputs by using a 50 Gsps digital oscilloscope (Tektronix DPO71604B). By adjusting R3, the preamplifiers were set to provide 304 mV and 296 mV baseline offsets so that the two detectors would produce approximately equal absolute maximum value for pulses having the same energy. The energy of an event was obtained by summing the baseline-subtracted waveform samples and applying a linear factor for converting the sum to energy. This scaling factor was determined by setting the location of the photo-peak of the resulting pulse-height histogram to 511 keV. The event time was obtained by digitally applying leading-edge discrimination (LED) by using an optimized threshold of 17 mV above the pulse baseline, which was experimentally determined by varying the threshold. Fig. 10 shows the resulting energy spectra and coincidence-time histograms (using 511 ± 50 keV events), showing energy resolutions of 9.5% and 8.9% at 511 keV and a coincidence resolving time (CRT) of about 390 ps FWHM (obtained by fitting with a Gaussian function).

Using the photo-peaks, we estimated that the peak amplitude for a 511 keV signal pulse for both detectors was about 270 mV above their respective baselines. Accordingly, we chose to set the lowest reference voltage, with respect to the baseline, to 20 mV and increase the reference voltages at a 40 mV step to obtain the highest reference voltage at 140 mV. This highest reference voltage corresponds to a photon energy of ~ 265 keV and, as discussed above in Section II-B.4, it defines the lower-energy limit for detection. It is noted the first reference voltage is

TABLE III
APPLIED REFERENCE VOLTAGES.

LVDS Comparator	1	2	3	4
Channel 1	349 mV	381 mV	427 mV	449 mV
Channel 2	332 mV	362 mV	419 mV	419 mV

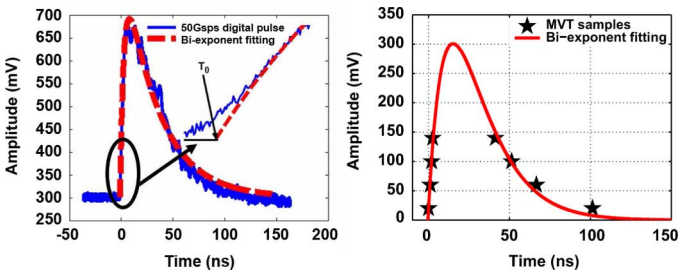

Fig. 11. Left: A sample pulse generated by an LYSO/SiPM detector (solid curve), acquired by using a 50 Gsps digital oscilloscope having a 16 GHz analog bandwidth (Tektronix DPO71604 B), and the least-squares fitting result with the empirical model given by (3) (dash curve). Right: A sample fitting (solid curve) of the empirical model to eight samples generated for an event pulse by the MVT digitizer (stars).

set above the optimized threshold of 17 mV determined for the digital LED and oscilloscope data. This is necessary in order to cope with the higher baseline noise of the MVT digitizer than the oscilloscope. Taking into consideration the baselines provided by the preamplifiers and the voltage offsets observed in Table I, Table III shows the reference voltages to be applied to the LVDS comparators in order to obtain actual reference voltages of 20 mV, 60 mV, 100 mV and 140 mV with respect to the baseline of the pulse.

C. Analysis Method

After the applied reference voltages of the MVT digitizer were determined, the outputs of the LYSO/SiPM detectors after the preamplifiers were connected to the MVT digitizer. The samples obtained were stored on a person computer and processed post-acquisition. The processing, following the work of Xie *et al.* [12], was based on fitting the samples acquired for a pulse to a mathematical model. In [12], fast PMTs were used and it was adequate to describe the acquired pulse as a fast linearly rising edge followed by a single-component exponential decay back to the baseline. In this work, we consider SiPMs and the response characteristics are much more complex. A complete description of the response model of the SiPM is not a trivial task and is beyond the scope of the current work [23]. Therefore, we empirically modeled the event pulse generated by an LYSO/SiPM detector by a bi-exponential function given by

$$y(t) = a \times \exp\left(-\frac{t-t_0}{b}\right) \times \left[1 - \exp\left(-\frac{t-t_0}{d}\right)\right], \quad (3)$$

where a is determined by the pulse amplitude, b and d by the rise and decay time of the pulse, and t_0 by the occurrence time of the pulse. To validate this model, we first applied it to pulses acquired by using the digital oscilloscope. Fig. 11 (left) shows a sample pulse and the least-squares fitting result. Subjectively, the fitting is reasonably well.

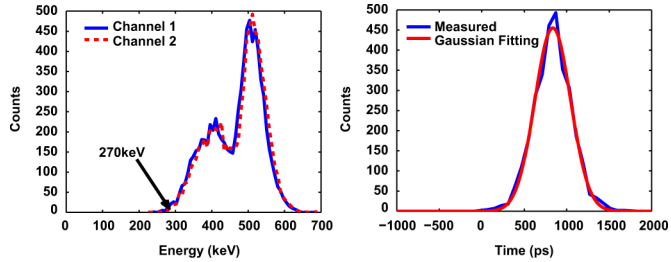

Fig. 12. The energy spectra and coincidence-time histograms generated by the FPGA-only MVT digitizer, showing energy resolutions of 15.8% and 15.3% at 511keV and a CRT of $\sim$ 500 ps FWHM. The charges corresponding to the photopeaks are 264 pC and 265 pC for channels 1 and 2, respectively.

We then fitted the validated empirical model given by (3) to the eight samples acquired for a pulse by the MVT digitizer, again by using the least-squares criterion. Fig. 11 (right) shows such an example fitting. For this example, the time interval between the first and fourth leading samples is about 1.0 ns, and the time between the first leading sample and the last trailing sample is 101.3 ns. These are consistent with $\sim$ 3 ns rise time and shorter than 150 ns pulse duration noted in Fig. 9. After the fitting, the event time was then given by the fitted value of t_0. The event energy was given by the integral of the fitted function, numerically calculated by summing the samples re-generated from the fitted function at a 20 ps interval.

D. Energy Resolution and CRT of the MVT Digitizer

A software coincident algorithm that we previously developed for the Trans-PET system [14] was employed to determine coincidence events with a coincidence time window of 10 ns. Fig. 12 shows the resulting energy spectra and coincidence-time histograms (using 511 ± 50 keV events). As shown, we obtain an energy resolution of $\sim 16\%$ for both detectors and the CRT is ~ 500 ps FWHM. In comparison, the CRT obtained by using only the first leading sample is $\sim$ 530 ps FWHM. Compared to the results obtained by using the digital oscilloscope, we observe that the MVT digitizer contributes an additional $\sim 13\%$ in energy resolution and $\sim$ 310 ps FWHM in CRT (estimated by using quadrature difference). This additional timing-resolution contribution is consistent with the timing uncertainty observed in Table II.

The following observations are noted. First, the energy spectra in Fig. 12 are observed to start at $\sim$ 270 keV and this is consistent with the aforementioned $\sim$ 265 keV lower-energy limit set by the highest reference voltage used. Second, the charge corresponding to 511 keV is slightly higher than that with the oscilloscope data (264 pC in Fig. 12 versus 261 pC in Fig. 10). This is consistent with the stipulation that our trailing samples are biased toward later occurrence, which leads to a longer tail and increases the area under pulse. Third, in our setup shown in Fig. 8 the gamma rays enter the crystals from the side. This arrangement can lead to a better CRT than if the gamma rays enter the crystals from the top. Based on the 10 mm crystal thickness and the measured 500 ps FWHM CRT, however, we do not expect noticeable difference in the CRT between the side-on and head-on arrangements. Fourth, clinical systems use larger crystals, for example $4 \times 4 \times 20$ mm^3, than

considered in this work. When larger crystals are used, the CRT can degrade but the energy resolution may improve. Fifth, as previously reported [21] when directly coupled to an LYSO crystal the response of the SiPM may be saturated for 511 keV photons. Calibration of the response is possible and has been reported. In this work, such calibration is not performed. However, if saturation occurs it affects both the oscilloscope and MVT-digitizer results.

IV. Conclusions and Discussion

In this work, we develop an FPGA-only MVT digitizer. It employs the differential I/Os of the FPGA to function as voltage comparators by operating them in the LVDS receiver mode. We characterize the voltage-setting accuracy at these LVDS comparators and measure the calibrations needed for setting proper reference voltages for MVT sampling. The TDCs are also implemented in the FPGA and our implementation has an average bin width of ~ 71.4 ps. By using rectangular test pulse, we measure that the MVT digitizer has an inherent timing resolution on the order of 300 ps FWHM. We apply the MVT digitizer for coincidence detection with a pair of LYSO/SiPM detectors, and we compare the measured resolutions with those obtained for the same detector pairs using data acquired by a high-speed digital oscilloscope. With the digital oscilloscope, we obtain an energy resolution of $\sim 9\%$ and a CRT of ~ 390 ps FWHM. In comparison, with the MVT-digitizer we obtain an energy resolution of $\sim 16\%$ and a CRT of ~ 500 ps FWHM. The MVT digitizer is therefore observed to contribute an $\sim 13\%$ energy resolution and ~ 310 ps FWHM CRT. This additional ~ 310 ps FWHM timing uncertainty is consistent with that measured with the rectangular test pulse. Although the MVT-digitizer results are inferior to the digital-scope results, they have nonetheless shown the feasibility of FPGA-only MVT digitizers. Also, the resulting energy and timing resolutions of the MVT digitizer are useful for developing PET and TOF PET detectors.

In our current implementation, each MVT channel takes up $\sim 6\%$ of the logic elements of the Altera EP2C70F896C7 FPGA. Therefore, it is possible to implement up to 16 channels on this FPGA and this possibility is under investigation. If 16 channels proves feasible, the cost and power consumption for a single 4-level MVT sampling channel are estimated to be ~ 18 USD and ~ 180 mW, respectively. We can also consider increasing the number of reference levels to 6 or 8 and implement fewer sampling channels. We believe that using more levels will improve the energy resolution, and possibly also the timing resolution. The tradeoff between performance and cost needs to be examined. The count-rate capability is estimated to be ~ 0.11 Mcps. This can be increased by upgrading the Ethernet interface to 1 Gsps and compressing the 448-bit event-word down to 192 bits. This compression is possible because the samples obtained for a pulse generated by LYSO are within a time duration of 250 ns and therefore the 32 most significant bits (MSBs) of their time values are identical and can be shared. After implementing these changes, we estimate that the count-rate capability can reach ~ 5 Mcps, which is useful for clinical imaging.

As the scope of this paper is to demonstrate the feasibility of the FPGA-based MVT sampling technology for PET, our current implementation is far from optimal. In future, we will investigate the use of Wu's Wave Union TDC [24], [25], which is reported to have a resolution of 10 ps (RMS). To improve timing resolution, the propagation delay from the LVDS comparators to TDCs also need to be calibrated. We will more carefully study the characteristics of the LYSO/SiPM output pulses for obtaining a better pulse-shape model and a better analysis method for estimating the event time and energy from samples generated by the MVT digitizer. The benefit of using the analog shaping to reduce baseline line and the fluctuations at the decay part of pulse will be investigated. Our current use of four reference levels at 20 mV, 60 mV, 100 mV, and 140 mV is quite arbitrary. We will extend our FPGA implementation to allow one to programmatically change the threshold settings and emulate sampling channels having more than four reference levels. In subsequent work, we will utilize the extended implementation to investigate the optimal reference voltage settings and the optimal number of reference levels to used for MVT sampling. Recently, Wang *et al.* [26] and Takahashi *et al.* [27] have proposed dynamical time-over-threshold methods; these methods may be useful for addressing the issue of optimal reference-voltage settings and we plan to incorporate them in our FPGA implementation and investigate their benefits.

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