| **Computer Architectures**<br>**[GRB-ZZZ]** | Delivery date:<br>18th November 2022 |
|---|---|
| **Laboratory**<br>**5** | Expected delivery of lab_05.zip must include:<br>- this document compiled possibly in pdf format. |

## 1) Processor configuration and performance checking in gem5

Download from the course site the supporting material: lab5_material.zip
Unzip the file in your working directory (example `my_gem5Dir`) and obtain the following files:

`1) start.sh`

a bash script that correctly sets the gem5 paths to execute the python script: `mygem5script.py`.

`2) mygem5script.py`

a configurable script for gem5 that allows you to set different features to the simulated processor. In a few words, the script configures an Out-of-Order (O3) processor based on the *DerivO3CPU*, a superscalar processor with a reduced number of features.
The processor pipeline stages can be summarized as:

- *Fetch stage*: instructions are fetched from the instruction cache. The `fetchWidth` parameter sets the number of fetched instructions. This stage does branch prediction and branch target prediction.
- *Decode stage*: This stage decodes instructions and handles the execution of unconditional branches. The `decodeWidth` parameter sets the maximum number of instructions processed per clock cycle.
- *Rename stage*: parameters relevant for this stage are the entries in the re-order buffer and the instruction queue (a kind of shared reservation station). Register operands of the instruction are renamed, updating a renaming map (stall may appear if not available entries). The maximum number of instructions processed per clock cycle is set by the `renameWidth` parameter.
- *Dispatch/issue stage*: instructions whose renamed operands are available are dispatched to functional units. For loads and stores, they are dispatched to the Load/Store Queue (LSQ). The simulated processor has a single instruction queue from which all instructions are issued. Ordinarily, instructions are taken in-order from this queue. The maximum number of instructions processed per clock cycle is set by the `dispatchWidth` parameter.
- *Execute stage*: the functional unit processes their instruction. Each functional unit can be configured with a different latency. Conditional branch mispredictions are identified here. The maximum number of instructions processed per clock cycle depends on the different functional units configured and their latencies.
- *Write stage*: it sends the result of the instruction to the reorder buffet. The maximum number of instructions processed per clock cycle is set by the `wbWidth` parameter.
- *Commit stage*: it processes the reorder buffer, freeing up reorder buffer entries. The maximum number of instructions processed per clock cycle is set by the `commitWidth` parameter.

In the event of a branch misprediction, trap, or other speculative execution event, "squashing" can occur at all stages of this pipeline. When a pending instruction is squashed, it is removed from the instruction queues, reorder buffers, requests to the instruction cache, etc.

2) Simulate the program `basicmath_large` (from MiBench) following the next steps. Remember to modify the program to **reduce the simulation time**. Please write here the changes that you have made in your program (`basicmath_large`):

| | |
|---|---|
| • #include <stdio.h> | for (l = 0x3fed0169L; l < 0x3fed**1**169L; l++) |
| • for(a1=1;a1<**6**;a1+=1) | for (X = 0.0; X <= **30.0**; X += .001) |
| • for(b1=**6**;b1>0;b1-=.25) | for (X = 0.0; X <= (**1** * PI + 1e-6); X += (PI / 5760)) |
| • for(c1=5;c1<**9**;c1+=0.61) | |
| • for (i = 0; i < **100**; i+=2) | |

a. Run the `start.sh` script for setting the gem5 paths

```
~/my_gem5Dir$ source start.sh
```

b. Simulate the program

```
~/my_gem5Dir$ /opt/gem5/build/ALPHA/gem5.opt mygem5script.py -c basicmath_large
```

Notice that the program output is automatically redirected to the file `m5out/program.out`.

Check the statistics (in `m5out`) file and collect the following parameters:

a) Number of instructions simulated
b) Number of CPU Clock Cycles
c) Clock Cycles per Instruction (CPI)
d) Number of instructions committed
e) Host time in seconds
f) Prediction ratio for Conditional Branches
   - Prediction ratio = Number of Incorrect Predicted Conditional Branches / Number of Predicted Conditional Branches
g) BTB hits.

Collect these parameters in Table 1 in the column *Basic configuration*.

3) Modify the processor configuration by doubling the parameters in the stages: Fetch, decode, rename, dispatch, execute, write and commit. **Do not change any value related to the branch predictors**. Simulate again the program `basicmath_large` and collect the statistics in Table 1 in the column *X2 configuration*.

Modify one more time the processor configuration by doubling again the parameters in the stages: Fetch, decode, rename, dispatch, execute, write, and commit. **Do not change any value related to the branch predictors**. Simulate again the program `basicmath_large` and collect the statistics in Table 1 in the column *X4 configuration*.

TABLE1: `basicmath_large` program behavior on different CPU configurations

| CPUs / Parameters | Basic configuration | X2 configuration | X4 configuration |
|---|---|---|---|
| Ticks | 334983075500 | 329480182500 | 331282550500 |
| CPU clock domain | 500 | 500 | 500 |
| Clock Cycles | 669966151 | 658960365 | 662565101 |
| Instructions simulated | 284135770 | 284135770 | 284135770 |
| CPI | 2.3579 | 2.3191 | 2.3319 |
| Committed instructions | 288836597 | 288836597 | 288836597 |
| Host seconds | 1798.77 | 1763.53 | 1785.96 |
| Prediction ratio | 0.2055 | 0.2008 | 0.1967 |
| BTB hits | 25525176 | 26120500 | 26655600 |

4) Select one of the previous hardware configurations (Basic, X2, X4):

| Selected hardware Configuration: | X2 |
|---|---|

Despite hardware enhancements for increasing the CPU performance, remember that optimizing compilers for programs in high-level code also exist. The aim of optimizing compilers is to minimize or maximize some attributes of an executable computer program (code size, performance, etc.). They are also aware of hardware enhancements to perform very accurate optimizations.

Compilers can be your best friend (or worst enemy!). The more information you provide in your program, the better the optimized program will be.

a) Compile the program `basicmath_large` using the provided *Makefile* using the ALPHA compiler with different optimization levels (DO NOT CONFUSE WITH O3 PROCESSOR).

*hint:*

add a variable to the Makefile in order to change the optimization level:

```
OPT="-O3"
```

and substitute all the `-O3` occurrences with the new variable as follows:

-O3 → $(OPT)

b) For visualize the enabled optimizations from the compiler perspective, you can run:

```
~/my_gem5Dir$  /opt/alphaev67-unknown-linux-gnu/bin/alphaev67-unknown-linux-gnu-gcc -c -Q -O2 --help=optimizers
```

By changing the "-O2" parameter with the desired one, you will find the enabled/disabled optimizations.

Here are some possible types of optimizations

- https://en.wikipedia.org/wiki/Optimizing_compiler
- https://gcc.gnu.org/onlinedocs/gcc/Optimize-Options.html

c) Simulate the program for different optimization levels and collect statistics (change OPT variable in the Makefile, O3 is the default, you need to change OPT accordingly to the values in parenthesis).

TABLE2: `basicmath_large` program behavior on the different compiler optimization level

| Optimization Parameters | Selected hw configuration (-O3) | Opt lvl 0 (-O0) | Opt lvl 1 (-O1) | Opt lvl 2 (-O2) | Opt size (-Os) | Opt fast (-O3 -ffast-math) |
|---|---|---|---|---|---|---|
| Ticks | 329480182500 | 343493479500 | 328216126000 | 329480182500 | 328721969000 | 2820584395 00 |
| CPU clock domain | 500 | 500 | 500 | 500 | 500 | 500 |
| Clock Cycles | 658960365 | 686986959 | 656432252 | 658960365 | 657443938 | 564116879 |
| Instructions simulated | 284135770 | 289432763 | 284108303 | 284135770 | 284212339 | 256050439 |
| CPI | 2.3191 | 2.3736 | 2.3105 | 2.3192 | 2.3132 | 2.2031 |
| Committed instructions | 288836597 | 294246574 | 288798798 | 288836597 | 288902850 | 260663920 |

| | | | | | | |
|---|---|---|---|---|---|---|
| Host seconds | 1842.42 | 1929.67 | 1807.41 | 1869.06 | 1787.93 | 1640.26 |
| Prediction ratio | 0.2008 | 0.1997 | 0.1998 | 0,2008 | 0.2007 | 0.2024 |
| BTB hits | 26120500 | 26212624 | 26262944 | 26120500 | 26171069 | 25017136 |
| Executable Size (byte) | 905268 | 4096 | 905268 | 905268 | 905268 | 838789 |

**1) Branch predictors comparison**

The gem5 includes different branch predictors:

- LocalBP:
  Implements a local predictor that uses the PC to index into a table of counters. It is like a basic BHT.

- BiModeBP:
  The bi-mode predictor is a two-level branch predictor that has three separate history arrays: a taken array, a not-taken array, and a choice array. The taken/not-taken arrays are indexed by a hash of the PC and the global history. The choice array is indexed by the PC only. Because the taken/not-taken arrays use the same index, they must be the same size.
  The bi-mode branch predictor aims to eliminate the destructive aliasing that occurs when two branches of opposite biases share the same global history pattern. By separating the predictors into taken/not-taken arrays, and using the branch's PC to choose between the two, destructive aliasing is reduced.

- TournamentBP:
  Implements a tournament branch predictor, hopefully identical to the one used in the 21264. It has a local predictor, which uses a local history table to index into a table of counters, and a global predictor, which uses a global history to index into a table of counters. A choice predictor chooses between the two. Both the global history register, and the selected local history are speculatively updated.

Starting from your Custom Configuration and default optimization level (O3), enable one at a time, every one of the different branch predictors in the `mygem5script.py` section called: `BPU SELECTION`, and collect the resulting statistics for any configuration in the following table. Select one of the branch predictors and customize its values. Report the results in the last column of the next table.

TABLE3: `basicmath_large` program behavior on different CPU configurations

| CPUs<br>Parameters | Local predictor | Bimodal predictor | Tournament predictor | Custom configuration |
|---|---|---|---|---|
| Ticks | 329480182500 | 330573405500 | 330569869500 | 313207542500 |
| CPU clock domain | 500 | 500 | 500 | 500 |
| Clock Cycles | 658960365 | 661146811 | 661139739 | 626415085 |
| Instructions simulated | 284135770 | 284135770 | 284135770 | 284135770 |
| CPI | 2.3191 | 2.3268 | 2.3268 | 2.2046 |
| Committed instructions | 288836597 | 288836597 | 288836597 | 288836597 |
| Host seconds | 1842.42 | 1908.37 | 1838.95 | 1721.27 |
| Prediction ratio | 0.2008 | 0.1945 | 0.1932 | 0.0685 |

| | | | | |
|---|---|---|---|---|
| BTB hits | 26120500 | 24892808 | 25179731 | 28169722 |

Report the branch prediction configuration of your custom configuration.

TABLE4: BPU custom configuration Vs. the basic one

| Parameter name | *Basic configuration* value | New value |
|---|---|---|
| TOURNAMENT BP | | |
| localPredictorSize | 32 | 64 |
| localHistoryTableSize | 256 | 1024 |
| globalPredictorSize | 64 | 256 |
| choicePredictorSize | 64 | 256 |
| BTBEntries | 256 | 2048 |