

Exercise 1

1.

$$t = 0.9 \text{ ns}$$

$$F = 1/(0.9\text{ns}) = 1,11 \text{ MHz}$$

2.

$$\text{AMAT} = t_{\text{hit}} + p_{\text{miss}} * t_{\text{miss}}$$

$$\text{AMAT} = 0,9 \text{ ns} + (1-0,94) * 70 \text{ ns} = 5,1 \text{ ns}$$

3.

We need to take into account how many times the processor executes a load/store instruction. Therefore, we multiply by the percentage.

$$\text{CPI} = \text{CPI}_{\text{ideal}} + \text{percentage_of_load/store} * (\text{miss_rate} * \text{miss penalty})$$

$$\text{miss_penalty (in clock cycles)} = \text{miss_time} * \text{clk freq}$$

$$\text{miss_penalty} = 70 \text{ ns} * 1,11 \text{ MHz} = 77,7$$

$$\text{CPI} = 1 + 0,36 * ((1-0,94) * 77,7) = 2.68$$

4.

$$\text{AMAT} = t_{\text{hit_L1}} + p_{\text{miss_L1}} * t_{\text{miss_L1}}$$

$$p_{\text{miss_L2}} = \text{miss rate to main memory} = 0,1$$

Calculate the miss time for L1 cache, so when looking into L2, finding the data or looking into L2 and not finding the data.

$$t_{\text{miss_L1}} = t_{\text{hit_L2}} + p_{\text{miss_L2}} * t_{\text{miss_L2}}$$

$$t_{\text{miss_L1}} = 6 \text{ ns} + 0,1 * 70 \text{ ns} = 13 \text{ ns}$$

$$\text{AMAT} = 0,9 \text{ ns} + 0,06 * 13 \text{ ns} = 1,68 \text{ ns}$$

5.

$$\text{CPI} = \text{CPI}_{\text{ideal}} + p_{\text{miss_L1}} * (\text{hit_time_L2} + p_{\text{miss_L2}} * \text{hit_time_main_memory}) * F_{\text{clk}}$$

$$\text{CPI} = 1 + 0,06 * (6 \text{ ns} + 0,1 * 70 \text{ ns}) * 1,11 \text{ MHz}$$

$$\text{CPI} = 1.87$$

6.

Yes, CPI is $2,68 / 1,87 = 1,43$ times lower. AMAT is $5,1 / 1,68 = 3,04$ times lower. So everything has decreased in time, making it faster.

Exercise 2

1.

$$\text{VA} = 48 \text{ bits}$$

$$\text{Page size} = 8\text{Kb}$$

$$\text{VA size} = \text{Virtual page number size} + \text{page offset size}$$

$$\text{Page offset size} = \log_2(\text{page size}) = \log_2(8\text{KB}) = 13 \text{ bits}$$

$$\text{Virtual page number size} = \text{VA} - \text{page offset} = 48 - 13 = 35 \text{ bits}$$

$$\text{Number of virtual pages} = 2^{(35)} = 34,36\text{e9 pages}$$

2.

Physical address size = physical page number size + page offset size

PTE size = Physical page number size + reserved bits size

PTE size = 4 Bytes = 32 bits

Physical page number size = 32 bits - 12 bits = 20 bits

Physical address size = 20 + 13 = 33 bits

Physical addressable space = 2^{33} = 8,59e9 pages

3.

Total storage needed in bits = number of PTEs in bits + PTE size in bits

PTE size = 4 bytes = 32 bits = 2^5 bits

(Slide 24 of lecture 10 uses PTE size in bytes, but that is incorrect due to different units right?)

Total storage needed in bits = 35 bits + 32 bits = 67 bits

4.

20 bits are reserved for the physical addresses.

Each page is 8KB

This means that there are $2^{20} * 8KB$ = 8,4 GB of physical space