# Exercise 1

1.

Table, calendar

Description automatically generated

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Instr | Components/Hardware element used by the instruction | | | | | | | | |
| R-type | Read PC (2ns) | Instruction memory | Control | Register read |  | Mux (PC) | Write PC | Register write |  |
|  | Add (PC) |  |  |  | ALU Control | ALU |  |  |
|  |  |  |  |  |  |  |  |  |
| Load | Read PC (2ns) |  |  |  |  |  |  |  |  |
|  | Instruction memory |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |

# Exercise 2

1.

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Q1 |  | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 |
|  | lw R1, 0(R3) | F | D | E | M | W |  |  |  |  |  |  |  |  |
|  | lw R2, 0(R4) |  | F | D | E | M | W |  |  |  |  |  |  |  |
|  | beq R1, R2, target |  |  | F | D | E | M | W |  |  |  |  |  |  |
|  | add R3, R3, R4 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | addi R4, R3, 4 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | exit |  |  |  |  |  |  |  |  |  |  |  |  |  |
| target: | lw R5, 0(R4) |  |  |  |  |  | F | D | E | M | W |  |  |  |
|  | add R5, R5, R6 |  |  |  |  |  |  | F | D | E | M | W |  |  |

2.

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Q2 |  | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 |
|  | lw R1, 0(R3) | F | D | E | M | W |  |  |  |  |  |  |  |  |
|  | lw R2, 0(R4) |  | F | D | E | M | W |  |  |  |  |  |  |  |
|  | beq R1, R2, target |  |  | F | D (A2') | \*\* | E | M | W |  |  |  |  |  |
|  | add R3, R3, R4 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | addi R4, R3, 4 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | exit |  |  |  |  |  |  |  |  |  |  |  |  |  |
| target: | lw R5, 0(R4) |  |  |  |  |  |  | F | D | E | M | W |  |  |
|  | add R5, R5, R6 |  |  |  |  |  |  |  | F | D (A2") | \*\* | E | M |  |

3.

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Q3 |  | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 |
|  | lw R1, 0(R3) | F | D | E | M | W |  |  |  |  |  |  |  |  |
|  | lw R2, 0(R4) |  | F | D | E | M | W |  |  |  |  |  |  |  |
|  | beq R1, R2, target |  |  | F | D (A2''') | \*\* | E | M | W |  |  |  |  |  |
|  | add R3, R3, R4 |  |  |  | F (A3''') | -- | -- | -- | -- |  |  |  |  |  |
|  | addi R4, R3, 4 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  | exit |  |  |  |  |  |  |  |  |  |  |  |  |  |
| target: | lw R5, 0(R4) |  |  |  |  | F | D | E | M | W |  |  |  |  |
|  | add R5, R5, R6 |  |  |  |  |  | F | D (A2''') | \*\* | E | M |  |  |  |

4.

Possible branch delay slot usage:

From before: Not possible because of data dependencies from load words

From target: Move “lw R5, 0(R4)” up. So it becomes “beq” followed by “lw” followed by “add”

From not-taken fall-through: You can keep it as it is, the “add” is possible for the branch-delay slot