**UNIVERSITY OF TEHRAN**

**Electrical and Computer Engineering Department**

**Digital Logic Design, ECE 367, Spring 1399-1400**

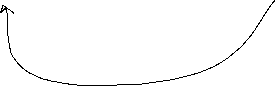
**Computer Assignment 5**

**Mohamad Abaeiani**

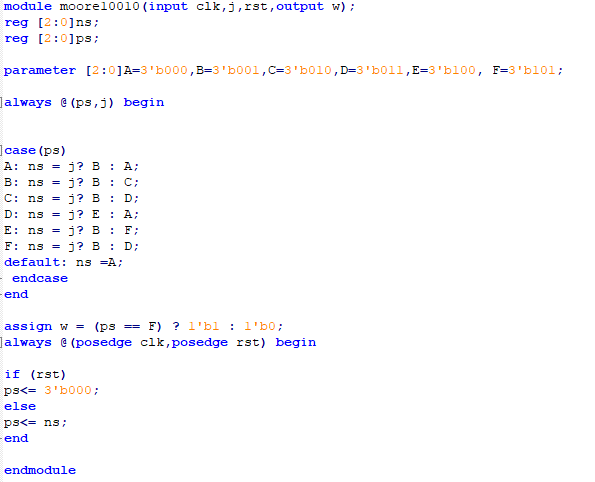
**810198432**

a.

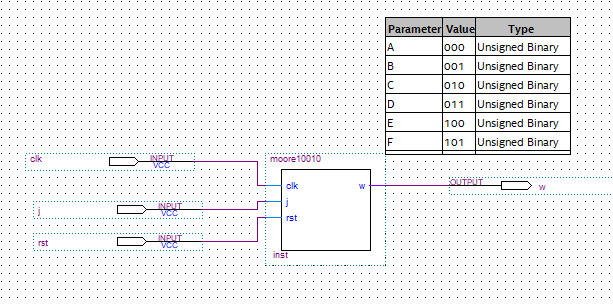
**Moore 10010 state diagram:**



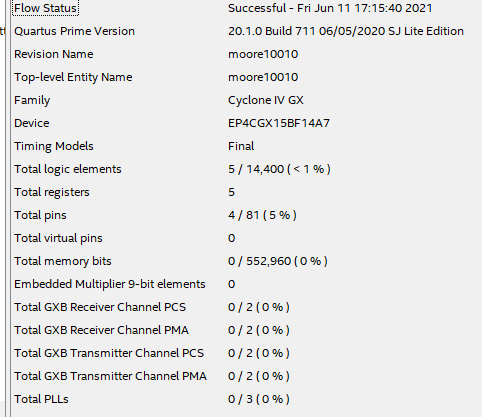
**Code:**



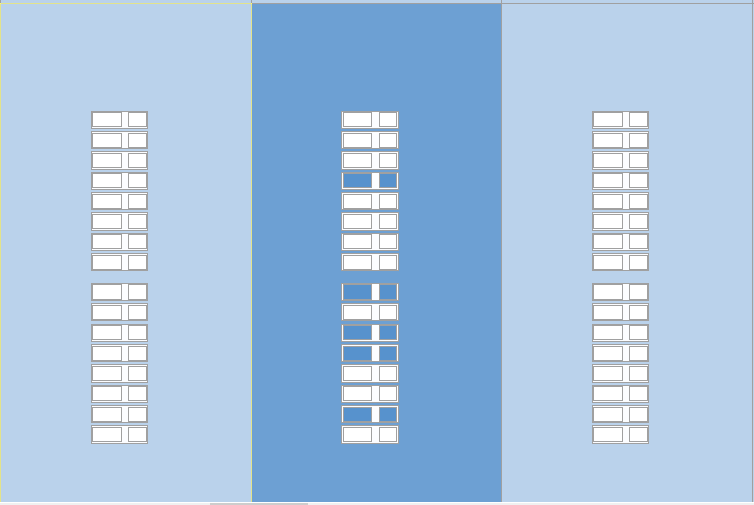
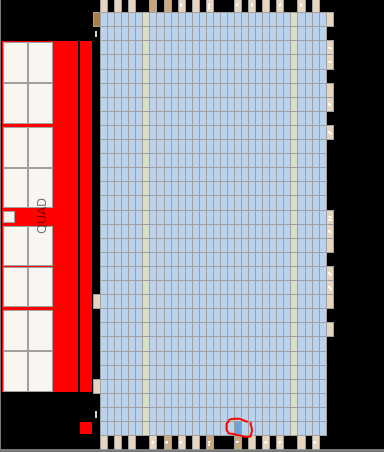
**Symbol:**



**Synthesis report:**



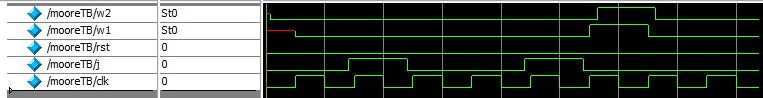
Floor plan:



As we could see the design used 5 cells (which include logic elements and registers) to implement the functionality which is the same as compilation report. It has also used some ports to get and send signals.

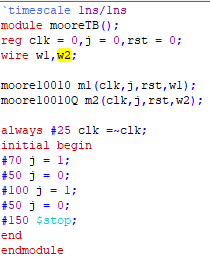
**Pre and post synthesis waveform:**

(w2 is post synthesis and w1 is pre synthesis)



As we could see the post synthesis output triggers a bit after the clock posedge.

**Test Bench Code:**

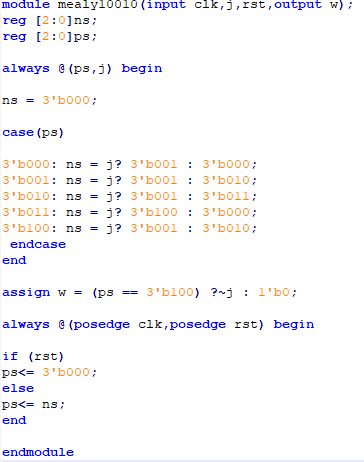


b.

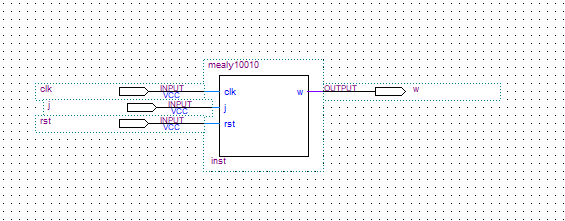
**state diagram:**



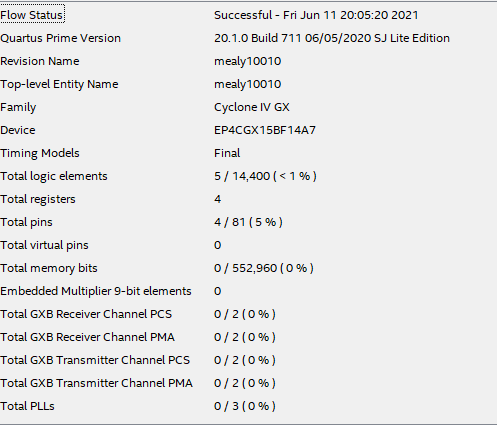
**Code:**



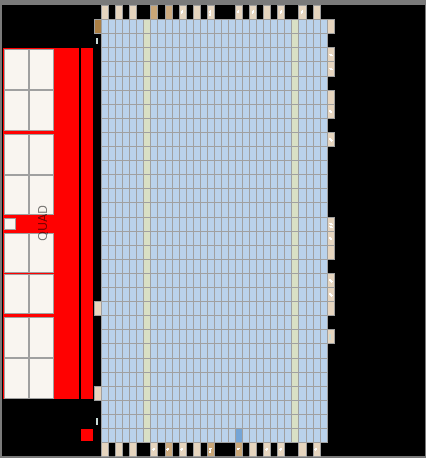
**Symbol:**

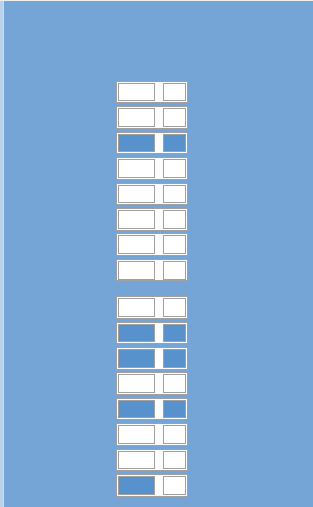


**Synthesis compile report:**



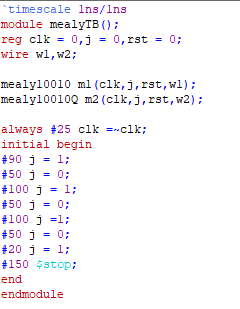
**Floor plan:**





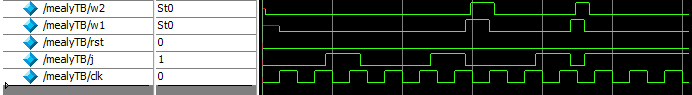
As we could conclude there are 4 registers and 5 logic elements used in this synthesis, so it’s the same as the cmpile report(also there are some ports used to deliver data as the previous part)

**Test Bench:**



**Wave Form:**

(w2 is post synthesis and w1 is pre synthesis)



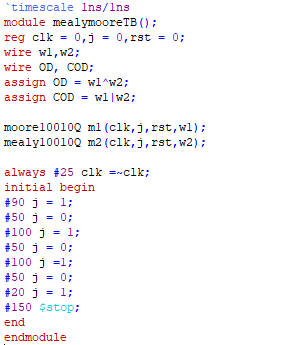
As we could see the post synthesis output triggers a bit after the clock posedge.

Also, as it is expected from mealy behavior the output followed j signal and became 0 a bit sooner than the next clock posedge, leading to smaller on-time than j input.

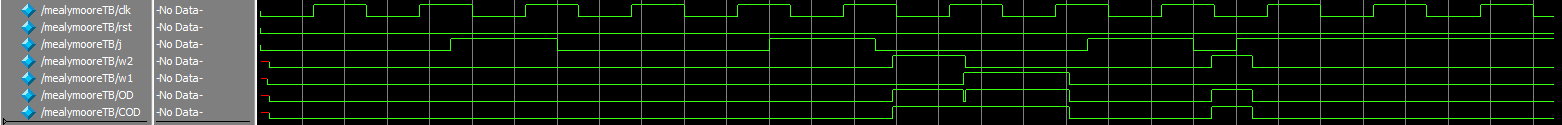
And it may cause glitches by invalid input changes.

C.

**Code(testbench):**



**Waveform:**



OD is for output difference signal and COD is for clean output difference signal.

In the first transition of OD the output difference is due to difference in moore and mealy timing so it can be ignored, but the next transition is where mealy missed the clock and gave faulty output, and this should be considered.

By looking precisely at the OD we see that the is a small gap between mealy and moore transitions, and it is where both outputs are 1 because of gate delay differences, so buy changing xor with or this problem would be solved and we get to COD output.

By looking at COD we can conclude that if the ON-time is less than one clock cycle hen there is a fault in mealy and it should be considered