**University of Tehran**

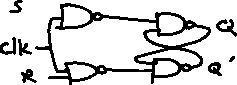
**DLD computer assignment 4**

**Mohammad Abaeiani**

**Std: 810198432**

Part 1&2

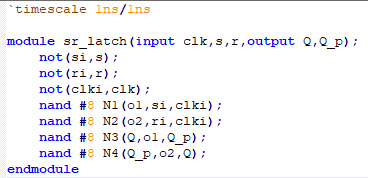
**Shematics:**



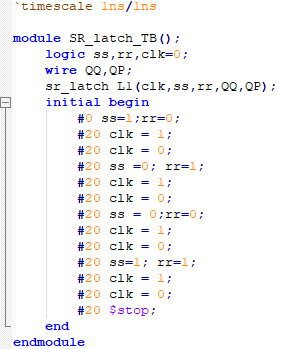
Nand delays :

Max(2\*nmos,pmos) = 2\*4 = 8ns

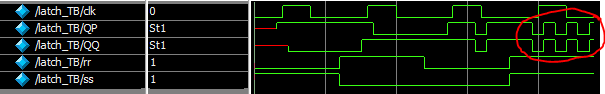
**Verilog:**



**TestBench:**



**WaveForm:**



The highlighted part is the memory loss; in which both s and r become zero and the nand gates alternate between 10 and 11 inputs constantly, while both Q and Q’ are the same.

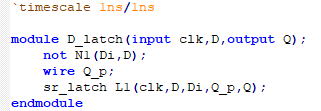
Part 2:

Part 3

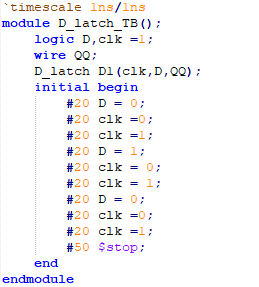
**Schematics:**



**Verilog:**



**TestBench:**



**Waveform:**



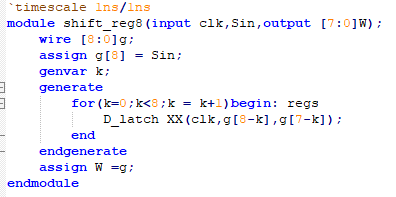
note that the output is Q’ since the inputs of the latch are active low.

Part 4&5

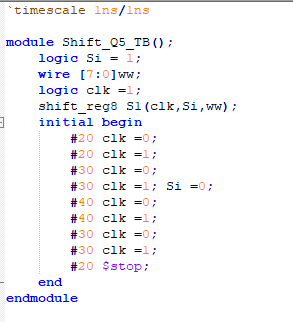
**Schematics:**



**Verilog:**



**TestBench:**



**Wave Form:**



It is concluded from the wave form that by extending the clock active time(from 20 to 30 to 40) the transparency emerges in the wave form and during each cycle there will be more than 1 shift(the more active time the more bit shifts); so this design is not so functional overall.

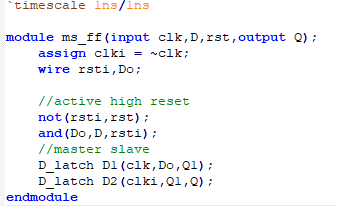
The reason of this is because the shifter turns on not on the edge of the clock but during the whole clock active time.

Part 6&7

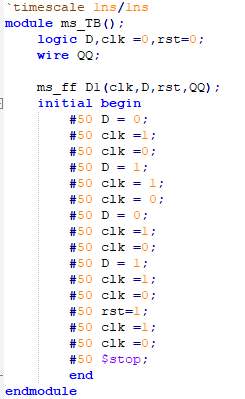
**Schematics:**



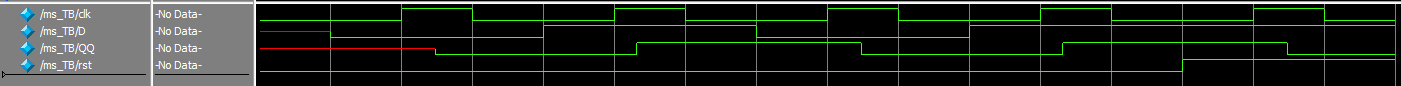
**Verilog:**



**Test Bench:**



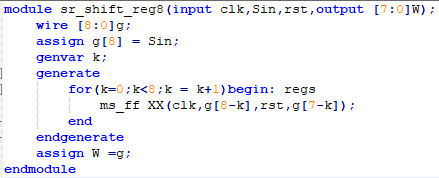
**Wave Form:**



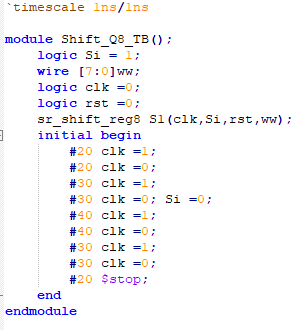
It could be dedicated that at the positive edge of clock the output saves the D input unless reset is active, if it is, the output becomes 0 at the posedge of clock even if the D input is one.

Part 8

**Verilog:**

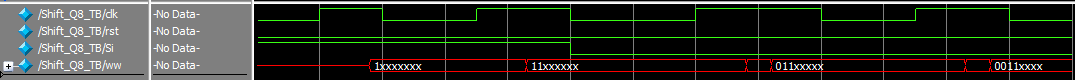


**Test Bench:**



(Here the test bench is the same as the former shift register in order to compare them)

**Wave Form:**

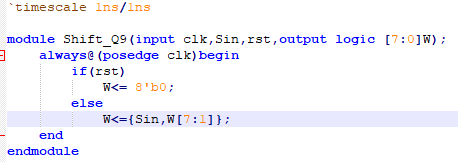


Here it is dedicated that with each clock the output is shifted only once no matter how long the clock active time is, unlike the former shift register.

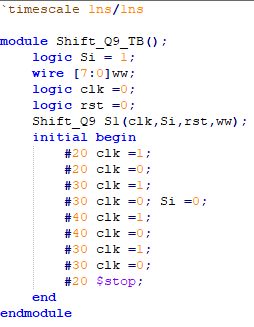
There are some tiny glitches on the shift to 0 from left which are because of time difference between the latch output To0 and To1 time.

Part 9

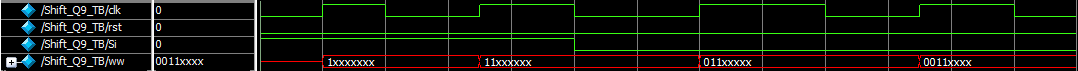
**Verilog:**



**Test Bench:**

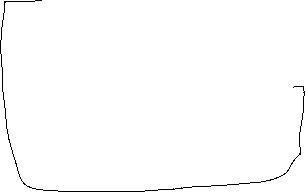
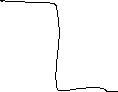


**Wave Form:**

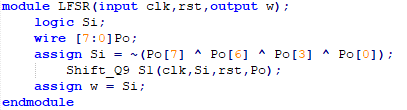


Part 10

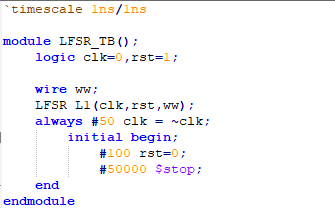
**Schematics:**



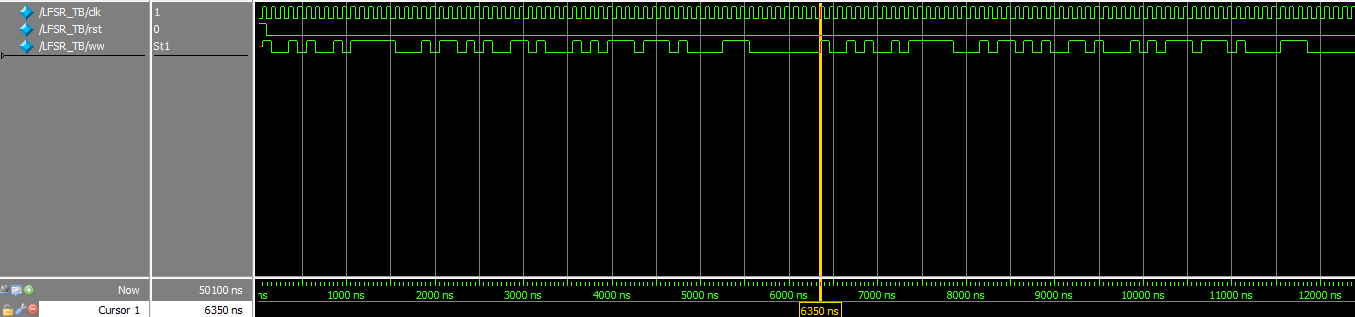
**Verilog:**



**Test bench:**



**Wave form:**



As we can conclude from wave form­ , considering the clocking started at 50ns(0 of rst) knowing each clock cycle is 100ns the period of the pattern is 63 clock cycles.

As I found out every polynomial has its own period no matter what the initial condition is, and by finding the best polynomial we could get 2^n -1 period-length in an n bit shifter.