R.M.K. COLLEGE OF ENGINEERING AND TECHNOLOGY

(An Autonomous Institution)

RSM Nagar, Puduvoyal– 601206, Gummidipoondi (T.K), Thiruvallur (D.T), Tamil Nadu

Approved by AICTE, New Delhi/ Affiliated to Anna University, Chennai

Accredited by NBA (All Eligible Courses) / NAAC with "A" GRADE

An ISO 21001:2018 Certified Institution

24EC102 - DIGITAL PRINCIPLES AND SYSTEMS DESIGN

I – Semester

Common to CSE, CSE(CS) & AI&DS

NAME : …….

REGISTER NUMBER : …….

BRANCH/SECTION : ……

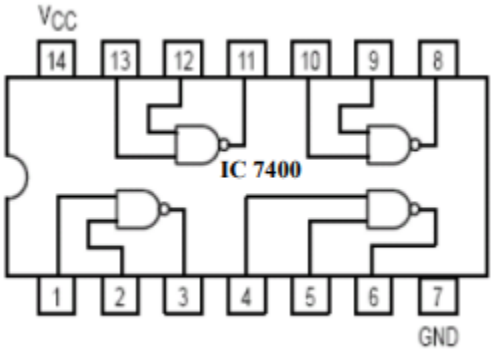
LIST OF EXPERIMENTS

A. Verification of Logic Gates

1. Implementation of Boolean expression using logic gates.
2. Design of adders
3. Design of subtractors.
4. Design of binary adder using IC7483
5. Design of Multiplexers & Demultiplexers.
6. Design of Encoders and Decoders.
7. Implementation of a boolean function using a multiplexer.
8. Design and implementation of 3 bit ripple counters.
9. Design and implementation of 3 bit synchronous counter
10. Design and implementation of shift registers.

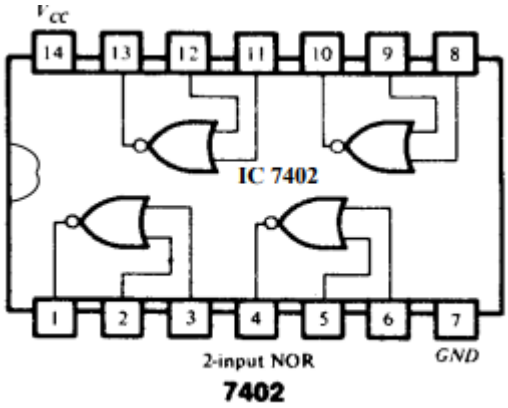
PIN DIAGRAM OF BASIC LOGIC GATES:

NAND GATE



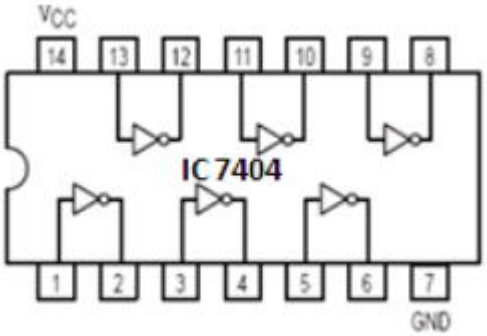
Input		Output
A	B	$Y = \overline{AB}$
0	0	1
0	1	1
1	0	1
1	1	0

NOR



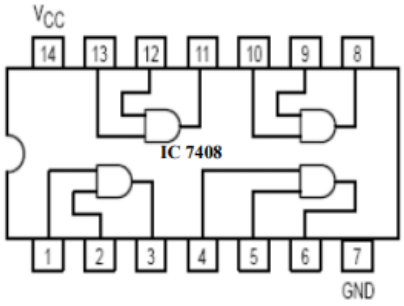
Input		Output
A	B	$Y = \overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

NOT GATE



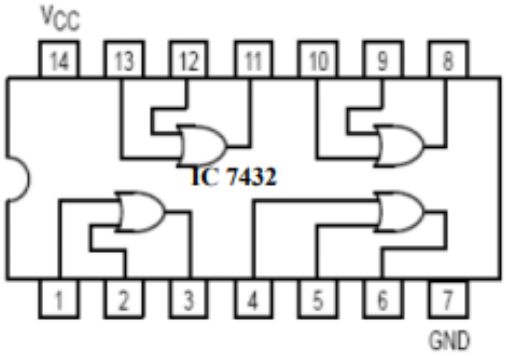
Input	Output
A	$Y = \overline{A}$
0	1
1	0

AND GATE



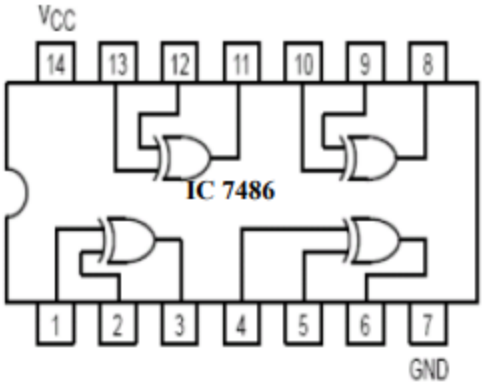
Input		Output
A	B	Y = AB
0	0	0
0	1	0
1	0	0
1	1	1

OR GATE



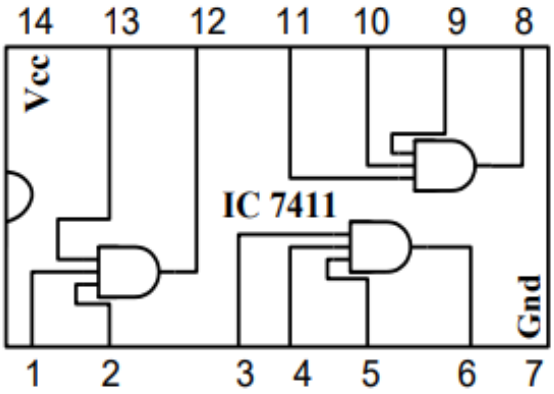
Input		Output
A	B	Y = A+B
0	0	0
0	1	1
1	0	1
1	1	1

EX-OR GATE



Input		Output
A	B	Y = $A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

THREE INPUT AND GATE



Input			Output
A	B	C	Y = ABC
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

EX: NO: A **DATE:**

Verification of Logic Gates

AIM:

To verify the digital logic gates.

Apparatus Required:

SI. No.	COMPONENT	SPECIFICATION	QTY
1.	NOT GATE	IC 7404	1
2.	AND GATE	IC 7408	1
3.	OR GATE	IC 7432	1
4.	NAND GATE	IC 7400	1
5.	NOR GATE	IC 7402	1
6.	EX-OR GATE	IC 7486	1
7.	THREE INPUT NAND GATE	IC 7411	1
6.	DIGITAL IC TRAINER KIT	-	1
7.	PATCH CORD	-	-

Procedure:

1. Verify the gates.
2. Make the connections as per the circuit diagram.
3. Switch on VCC and apply various combinations of input according to truth table.
4. For all input combinations the outputs are verified with the truth table.

Result:

Thus the gates are verified with its truth table using logic gates.