APB with UART Design Specification

Version No: 0.1

Date: 28-FEB-20

Project Name: APB\_UART\_DESIGN

Project Code:

<SDC Address>

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Revision History

| Version No | Date | Prepared by / Modified by | Significant Changes |
| --- | --- | --- | --- |
| 0.1 | 28-Feb-20 |  | Initial Version |
|  |  |  |  |

Glossary

|  |  |
| --- | --- |
| Abbreviation | Description |
| APB | Advanced Peripheral Bus |
| UART | Universal Asynchronous Receiver Transmitter |
| ASB | Advanced System Bus |
| AHB | Advanced High-Performance Bus |
| SoC | System on Chip |

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# Introduction

## Identification

|  |  |
| --- | --- |
| Project Name | APB\_UART\_SPEC |
| Project Code |  |
| Product Name |  |
| Product Version No |  |

## Assumptions

* Signals will run at the frequency of 25 MHz
* The baud rate for the UART 9600 bits/second.

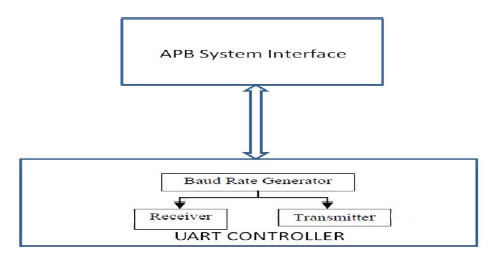
# Functional overview

* The APB (Advanced Peripheral Bus) is part of the AMBA protocol family.
* Every transfer takes at least two cycles.
* The APB can interface with the AMBA AHB or AMBA ASB.
* The APB interface allows access to the UART through APB
* UART is being used in SoC which consists of transmitter, receiver and baud rate generator and therefore connecting it to the APB which is a peripheral bus in AMBA to connect different peripherals.
* The UART takes bytes of data and transmits the individual bits in a sequential fashion. At the destination, a second UART re-assembles the bits into complete bytes.
* The data contains start bit, stop bit and parity bit.

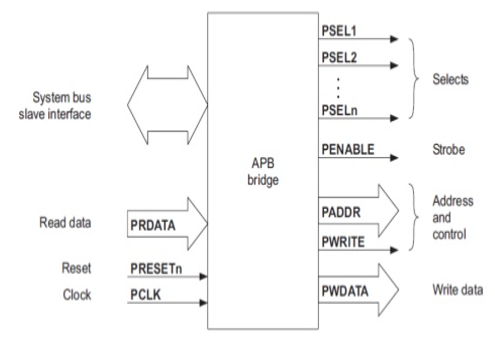
# Interface Details

| Signal Name | Type | Description | Specification |
| --- | --- | --- | --- |
| PADDR | Input | Address | 4 bits |
| PWDATA | Input | Write data (Master to Slave), if PWRITE=1 | 8 bits |
| PWRITE | Input | Write/ Read signal | 1 bit |
| PSELx | Input | Slave Select signal | 1 bit |
| PENABLE | Input | Data transfer enable | 1 bit |
| PCLK | Input | Clock signal | 15Mhz |
| PRESETn | Input | Active low Reset signal | 1 bit |
| PRDATA | Output | Read data (Slave to Master), if PWRITE=0 | 8 bits |
| PREADY | Output | Ready signal from slave to master/ to extent the data transfer | 1 bit |
| PSLVERR | Output | To indicate the transfer failure | 1 bit |
|  |  |  |  |
|  |  | **UART TRANSMITTER** |  |
| wr | Input | Enable for Transmitter | 1 bit |
| PRDATA | Input | Parallel data input | 8 bits |
| Tx | Output | Serial data output | 1 bit |
|  |  | **UART RECEIVER** |  |
| Rx | Input | Serial input data | 1 bit |
| ~wr | Input | Enable for Receiver | 1 bit |
| Data\_out | Output | Received data byte | 8 bits |

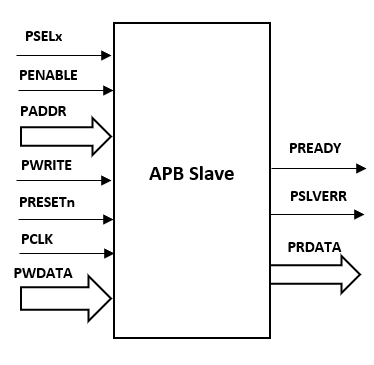
# Functional block diagram



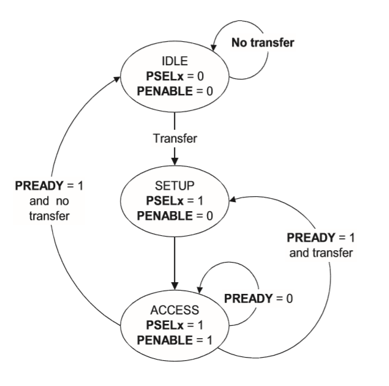
**APB – UART interface**



**APB Bridge**



**APB Slave Interface**

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**State Transition Diagram of APB**

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**Data bits transmitted to/by UART**

# Design Description

The APB - UART is a master/slave that enables serial communication between other UART that is externally connected. Device states are read by the APB using status registers that reflect the completion of UART data transfers. Controller also supports the interrupt pin for indicating the transaction completion or any error in the controller. Standard UART protocol consists of start/stop indicators, data, and parity information. APB with UART uses the following blocks to transmit and receive data.

| SN | Block Name | Functionality |
| --- | --- | --- |
| 1 | APB interface | To send bus signals in UART readable form |
| 2 | UART interface | For asynchronous serial data transmission and reception |

## APB Interface block

The APB bus is used to interface to UART which is low bandwidth and does not require the high performance of a pipelined bus interface. The APB slave interface acts as a bridge between the APB and UART to which the bus is connected. It receives the APB bus signals and converts them to a form in which is understood by UART connected to it.

## UART Interface block

Universal asynchronous receiver-transmitter is device used for [asynchronous serial communication](https://en.wikipedia.org/wiki/Asynchronous_serial_communication) in which the data format and transmission speeds are configurable.

Data is transferred from the data bus to Transmitting UART in parallel form. Then, data is serially transmitted to the receiver which is again converted into parallel form by receiver. UARTs transmit data asynchronously, which means there is no clock signal to synchronize the output of bits from the transmitting UART to the sampling of bits by the receiving UART. Instead of clock signals it uses Start, Stop and parity bits for Synchronization.

## Register Description

### APB\_STATE

* Description: specifies the current state of APB.

| Bits | Field | Access | Description |
| --- | --- | --- | --- |
| apb\_state[1:0] |  | R/W | Determines the state of APB.  2'b00 - IDLE  2'b01 - SETUP  2'b10 - ENABLE |

### 5.3.2 UART INTERFACE

* Description: Command to update the value of transmitter output.

| Bits | Field | Access | Description |
| --- | --- | --- | --- |
| Baud\_clk(1 bit) |  | R/W | Controls the transmission of bits.  3’b111- Tx output gets updated.  !(3’b111)- Tx output remains the same |

# References

## References

* Cortex™-M System Design Kit manual.
* Design And Implementation Of The Advanced Microcontroller Bus Architecture AXI-APB Bridge On FPGA