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B022314(022)

B. Tech. (Third Semester) Examination,
April-May ~~2021~~ 2022

(AICTE Scheme)

(CSE Engg. Branch)

DIGITAL ELECTRONICS & LOGIC DESIGN

Time Allowed : Three hours

Maximum Marks : 100

Minimum Passing Marks - 35

Note : Part (a) is compulsory and attempt any two parts from (b), (c) and (d).

Unit-I

1. (a) Explain laws of Boolean Algebra. 4

(b) Minimize the following expression using k-map and realize using logic gates. 8

(i) $F1(w, x, y, z) = \sum m(0, 3, 4, 8, 10, 12, 15) + d(1, 13)$

(ii) $F2(A, B, C, D) = \pi m(2, 4, 5, 6, 8, 9, 12, 13, 15)$

(c) The Hamming code 101101101 is received. Correct it if any errors. Odd parity is used. 8

(d) Minimize the following digital function using Mc_Cluskey method. 8

$F(P, Q, R, S) = \sum(0, 1, 5, 8, 9, 10, 11, 13) + \sum d(4, 12, 14)$

Unit-II

2. (a) Write short notes on : 4

(i) Noise margin

(ii) Propagation Delay

(b) Compare the performance TTL, CMOS and ECL logic. 8

(c) Implement following function using PLA. 8

$F1(A, B, C) = \sum m(4, 5, 7)$

$F2(A, B, C) = \sum m(4, 5, 7)$

(d) Implement following function using suitable PAL. 8

$W(A, B, C, D) = \sum m(1, 3, 4, 6, 9, 11, 12, 14)$

$X(A, B, C, D) = \sum m(1, 3, 4, 6, 9, 11, 12, 14, 15)$

$y(A, B, C, D) = \sum m(0, 2, 4, 6, 8, 12)$

$z(A, B, C, D) = \sum m(2, 3, 8, 9, 12, 13)$

Unit-III

3. (a) What is Multiplexer? Explain with example. 4

(b) Design BCD adder to add to BCD number. 8

(c) Give a block diagram of 4 × 16 Decoder using 3 × 8 decoders and explain its working. 8

(d) Design full adder using multiplexer. 8

Unit-IV

4. (a) What is flip flop? 4

(b) What is Shift Register? Explain application of Shift Register. 8

(c) Design mod 5 synchronous counter. 8

(d) Design UP/DOWN ripple counter. 8

Unit-V

5. (a) Write difference between Moore and Mealy Machine. 4

(b) Explain lexical element and data object types in VHDL. 8

(c) Write syntax for : 8

(i) entity and

(ii) architecture in VHDL

(d) Explain Mealy machine with example. 8