# Lecture 9: cache coherency

cache memory hierarchy, cache coherency protocol, store-buffer, load-buffer, invalidate-queue, memory barrier, hardware memory model, weak memory model, litmus tests

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https://github.com/Svazars/parallel-programming/blob/main/slides/pdf/l9.pdf

# In previous episodes

Concurrency domain

- Communicating agents (threads)
- Different speed of execution and non-deterministic interleavings (OS scheduler)
- Problems with proper synchronization – race conditions, deadlocks
- Key properties: Safety (correctness), Liveness (progress), Performance

Formalization of concurrent execution

- Timeline, Events, Intervals, Precedence
- Consistency, Linearizability, Linearization points
- Progress conditions: wait-free, lock-free, obstruction-free, starvation-free, deadlock-free
- Atomic register, Snapshot, Consensus number

Practical aspects

- Read-Modify-Write operations
- Memory bus, Cache hierarchy, Cache coherence
- Lock-free algorithms and ABA problem

# Warning: lecture today is going to be like

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# Supplementary materials

Unconditional benefit

- "Memory Barriers: a Hardware View for Software Hackers"[1]
- "What Every Programmer Should Know About Memory"[2]
- "Слабые модели памяти: буферизации записи на x86"[3]

Advanced material

- "A Tutorial Introduction to the ARM and POWER Relaxed Memory Models"[4]
- "Shared Memory Consistency Models: A Tutorial"[5]

Mechanical sympathy (better understand h/w design):

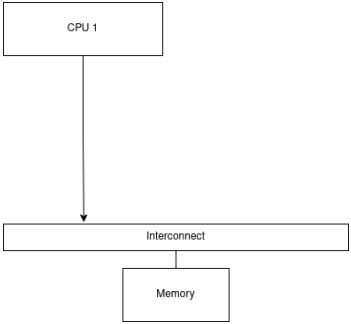
- "Digital Design and Computer Architecture" by David Money Harris, Sarah L. Harris[6]

[1] https://www.researchgate.net/publication/228824849_Memory_Barriers_a_Hardware_View_for_Software_Hackers
[2] https://people.freebsd.org/~lstewart/articles/cpumemory.pdf
[3] https://habr.com/ru/companies/JetBrains-education/articles/523298
[4] https://www.cl.cam.ac.uk/~pes20/ppc-supplemental/test7.pdf
[5] https://dl.acm.org/doi/10.1109/2.546611
[6] https://www.amazon.com/Digital-Design-Computer-Architecture-Harris/dp/0123944244

# Lecture plan

1. Preliminary discussion
2. Cache coherency
3. Hardware optimizations
   - Store buffering
   - Load buffering
   - Optional: Invalidate Queues
   - Interconnect topology
4. Hardware memory model
5. Memory barriers
6. Litmus tests
7. Summary

# Global memory: 1 CPU



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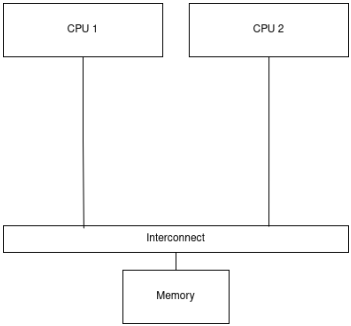

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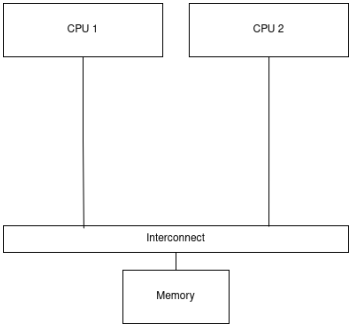


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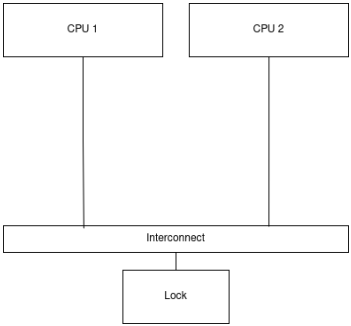

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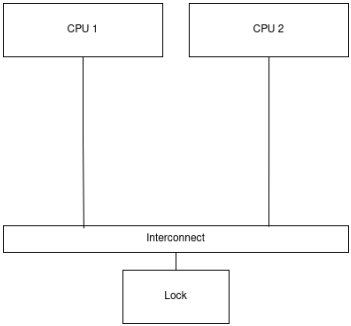


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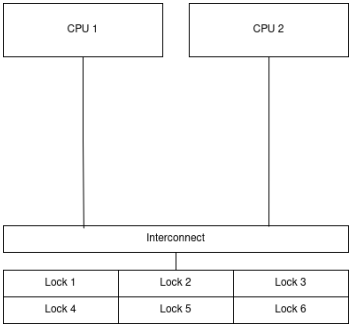

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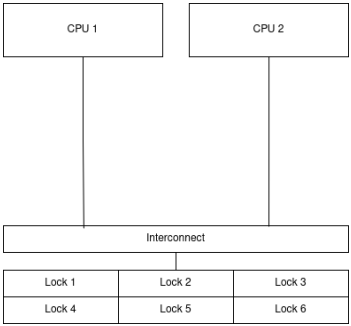


Cache line

- contiguous chunk of memory (e.g 64, 128, 256 bytes)
- auxiliary data associated with the chunk

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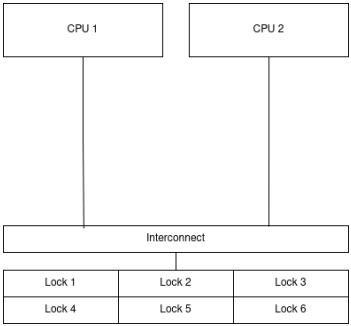


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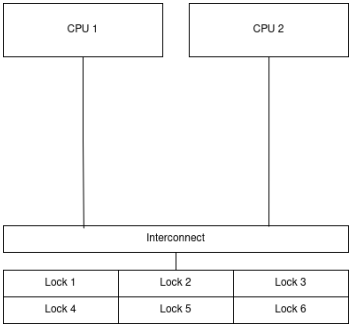


What is optimal cache line size?

- too large – **false sharing** (access to independent data cause performance loss)
- too small – overhead for storing meta information

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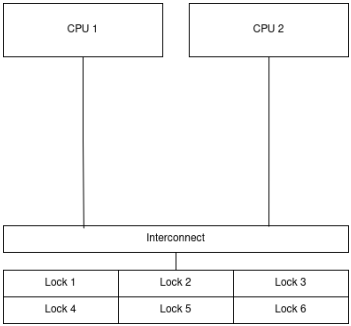


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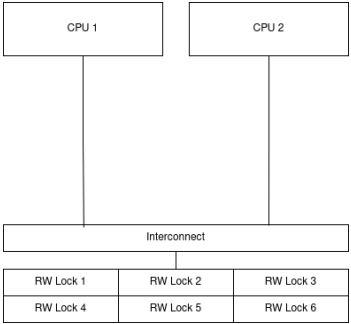

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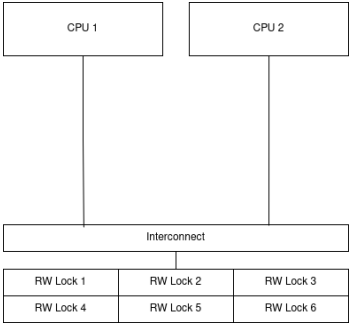


Is it consistent?

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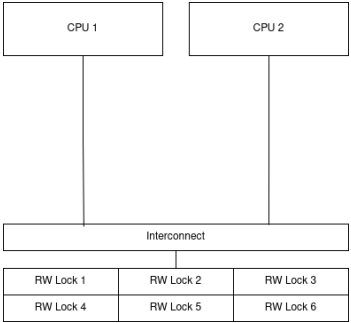


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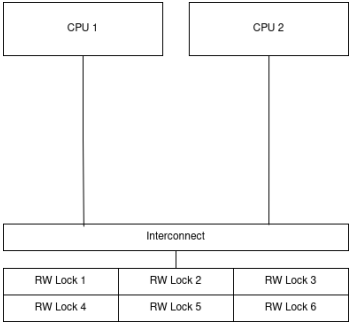


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Initial state: `x = 1`

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void threadA() {
      x = 2;
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Several other executions of the same code are allowed:

- both Thread B reads could read 1
- both Thread B reads could read 2
- first could read 1 and the second 2

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Initial state: `x = 0`

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|---|---|---|---|
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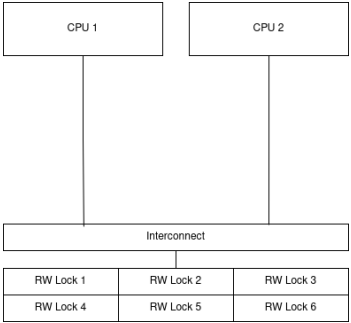


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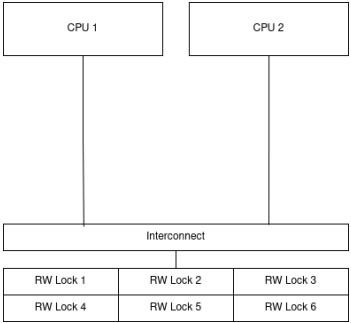


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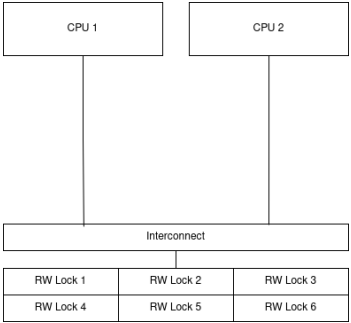


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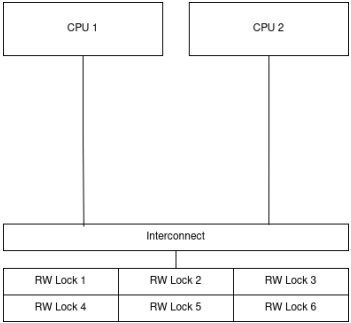


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Let's reorder independent memory operations to improve performance of the CPU!
Every single-threaded program will become faster!
Who cares that concurrent software will misbehave, right?

# Relaxing memory ordering guarantees

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static int x, y;
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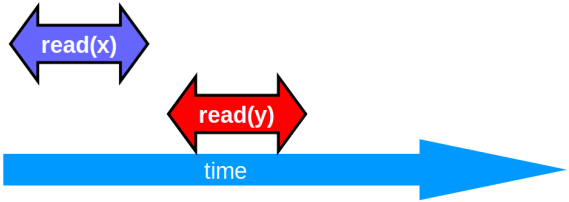

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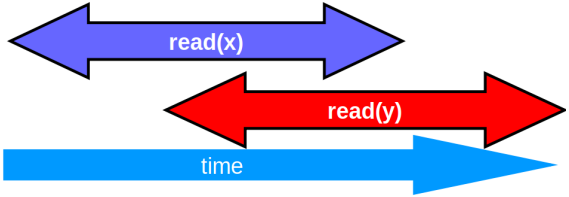

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- Improve efficiency and CPU utilization – faster
- Sacrifice consistency – harder to reason about correctness

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- Empirically study concurrent behaviour of existing hardware via litmus tests

# Lecture plan

# Why do we need caches?

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**Nanoseconds and toilet paper show**

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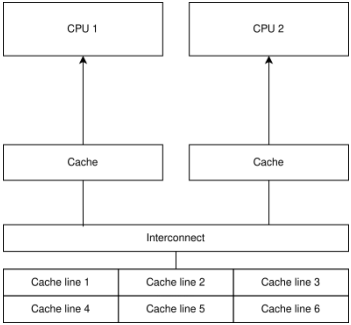
**Nanoseconds and toilet paper show**

https://travisdowns.github.io/blog/2020/07/06/concurrency-costs.html
Level 2 (True Sharing)

# Using caches




Replication pattern:

- Cache line copied to processor-local cache
- Metadata associated with every replicated cache line – state of cache line

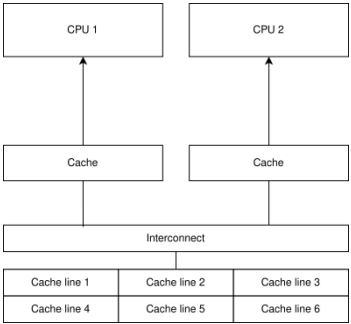
# Homework: caches and associativity

Hardware caches are quite efficient and use hardware-supported N-way associativity
"Is Parallel Programming Hard, And, If So, What Can You Do About It" (perfbook)

- Appendix B "Why Memory Barriers?" , section B.1 "Cache Structure"
- perfbook.B.1

Be ready to draw and explain what is associative hardware cache.

# Distributed caching

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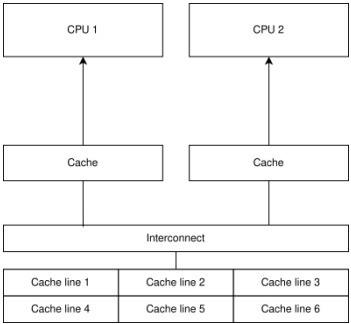


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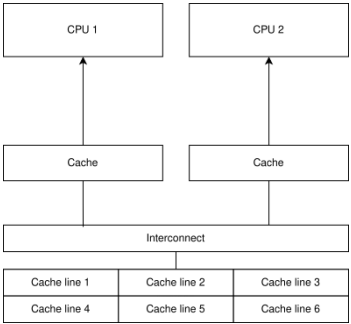


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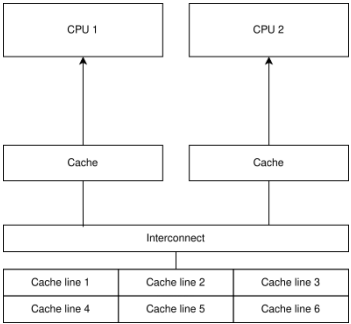


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How to implement that without locks? And without Atomic MRMW registers? Efficient?

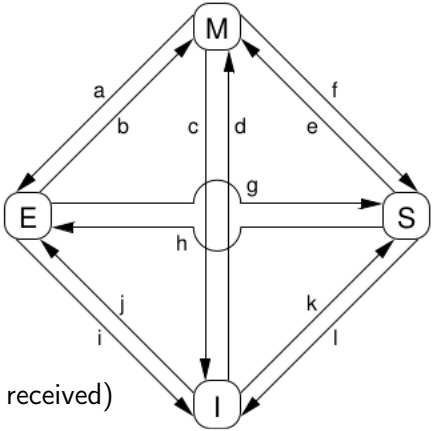
# Cache coherency: MESI

State machine:

- **Modified**
- **Exclusive**
- **Shared**
- **Invalid**

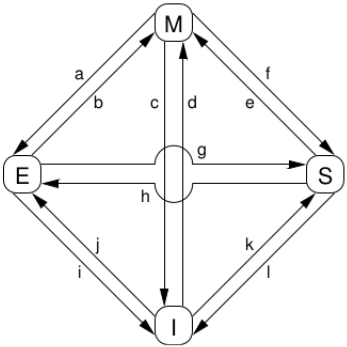
Message passing on some transitions:

- asynchronous (fire and forget)
- synchronous (cannot change state until confirmation received)



# Cache coherency: message passing[7]

- Transition **(k)**: CPU loads data in a cache line that was not in its cache. Send "read", await "read response".
- Transition **(h)**: CPU realizes that it will soon need to write data in this cache line. Send "invalidate" message, await "invalidate acknowledge".
- Transition **(b)**: CPU writes to the cache line that it already had exclusive access to. Nothing to send/receive.
- Transition **(c)**: CPU receives "read invalidate" message for a cache line that it has modified. The CPU must invalidate local copy, respond with "read response" and "invalidate acknowledge".




[7] perfbook B.2.3.

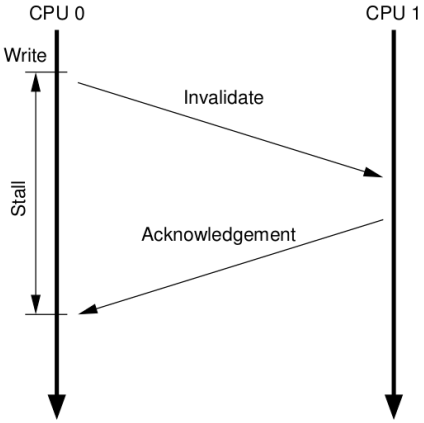
# Homework: more complicated MESI protocol example

Homework: read perfbook.B.2.4. "MESI Protocol Example"

| Sequence # | CPU # | Operation | CPU Cache | | | | Memory | |
|---|---|---|---|---|---|---|---|---|
| | | | 0 | 1 | 2 | 3 | 0 | 8 |
| 0 | | Initial State | -/I | -/I | -/I | -/I | V | V |
| 1 | 0 | Load | 0/S | -/I | -/I | -/I | V | V |
| 2 | 3 | Load | 0/S | -/I | -/I | 0/S | V | V |
| 3 | 0 | Invalidation | 8/S | -/I | -/I | 0/S | V | V |
| 4 | 2 | RMW | 8/S | -/I | 0/E | -/I | V | V |
| 5 | 2 | Store | 8/S | -/I | 0/M | -/I | I | V |
| 6 | 1 | Atomic Inc | 8/S | 0/M | -/I | -/I | I | V |
| 7 | 1 | Writeback | 8/S | 8/S | -/I | -/I | V | V |

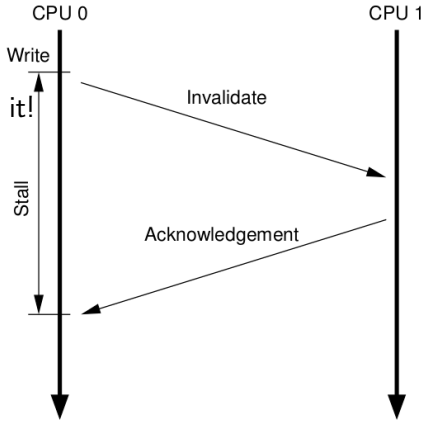
# Unnecessary stalls

- CPU 0 starts write to cache line held by CPU 1
- CPU 0 must wait for the data to arrive



# Unnecessary stalls

- CPU 0 starts write to cache line held by CPU 1
- CPU 0 must wait for the data to arrive
- Why wait? CPU 0 is going to unconditionally overwrite it!



# Cache coherency: takeaways

High-level ideas:

- Memory split into chunks (cache lines) with auxiliary data (cache line state)

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- Cache line size (64, 128, 256 ...)

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- Invalidation storms
- Unnecessary stalls

# Lecture plan

# Concurrent invariants and where to violate them

- **Coherence**: in any execution, for each location, there is a single linear order of all writes to that location which must be respected by all threads
- Step 1: "break" intuitive behaviour to get performance improvement
- Step 2: repair consistency

# Which parts of cache coherence should be optimized?

State machine:

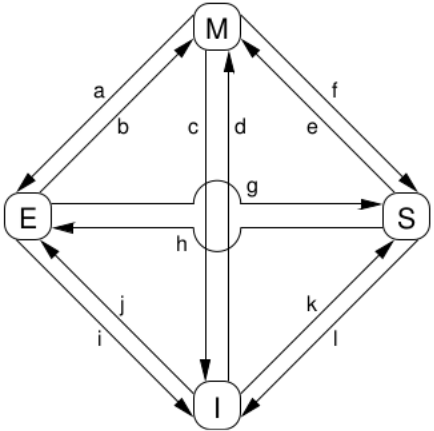
- **Modified**, **Exclusive**, **Shared**, **Invalid**

Message passing on some transitions:

- asynchronous (fire and forget)
- synchronous (await confirmation)

Optimization opportunities:

- Option 1: more states (MESIF, MOESI ...)
- Option 2: more asynchronous operations



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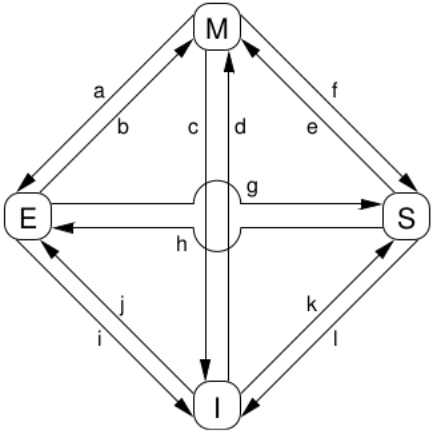

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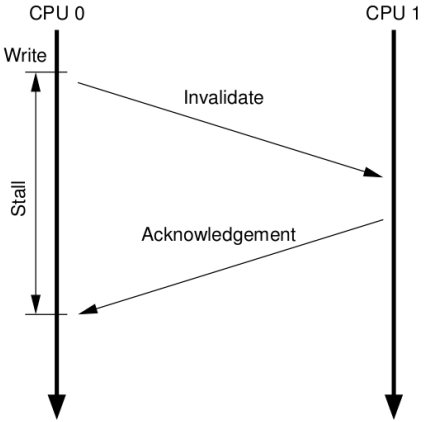

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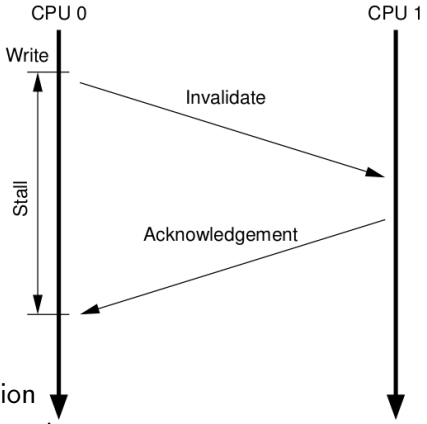


Idea: batch processing

- Buffer of "pending operations" that await confirmation
- Execute other instructions **before** invalidation confirmed
- Modification of the same location "consults" with buffer, not with cache (**store to load forwarding**)

# Lecture plan

# Store buffering

```
int x, y;
```

```
void threadA() {
        x = 1;
    int a = y;
}
```

```
void threadB() {
        y = 1;
    int b = x;
}
```

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```
# thread A
mov [x] , 1  # (A.1)
mov EAX , [y] # (A.2)
```

```
# thread B
mov [y] , 1  # (B.1)
mov EBX, [x] # (B.2)
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# Store buffering

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What could we see in (EAX EBX)?

(1 1) , (0 1) , (1 0) , (0 0)

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Possible executions:

- A.1 -> A.2 -> B.1 -> B.2
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Linearizable answer: (1 1) , (0 1) , (1 0)

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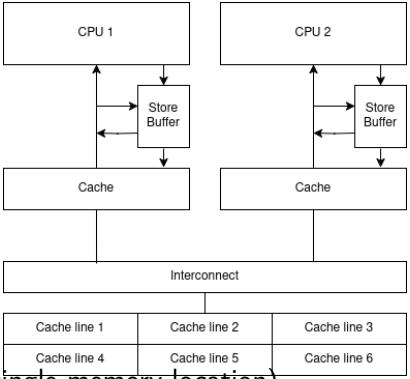


Hardware allows: (EAX=0 EBX=0)

- Looks like CPU reorders memory load and stores
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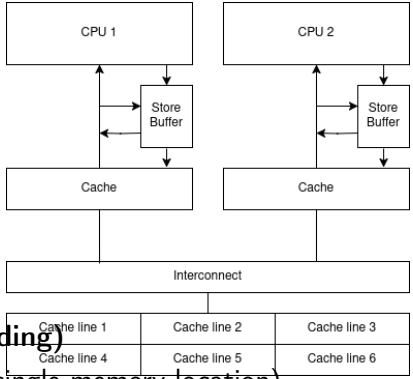


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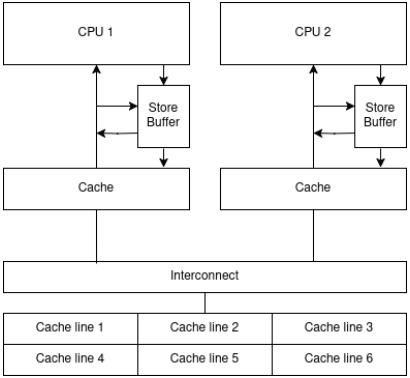


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- CPU 0: commit "`write(a = 1)`" from store buffer (now cache thinks "a is one")
- CPU 0: finish writing to b ("'b is one")
- CPU 0: assert failed

# Store buffering: useful?

- Processor extended with internal buffer to speed-up execution
- In-processor order conforms to program order (**store forwarding**)
  - Perfect single-CPU abstraction
- Other processor may see memory updates to happen in non-program order
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We will discuss few more hardware optimizations before diving into memory barriers.

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# Lecture plan

# Load buffering

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# thread A                    # thread B
mov EAX , [y] # (A.1)         mov EBX, [x] # (B.1)
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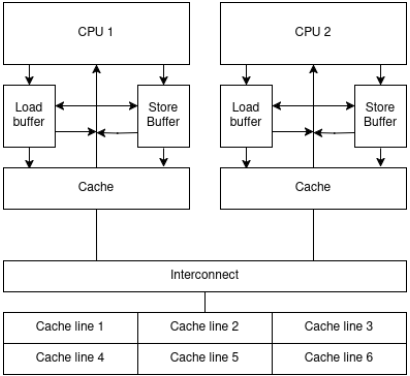

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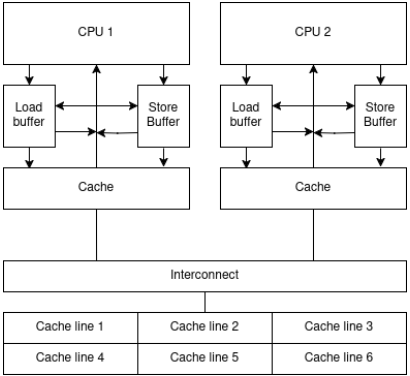

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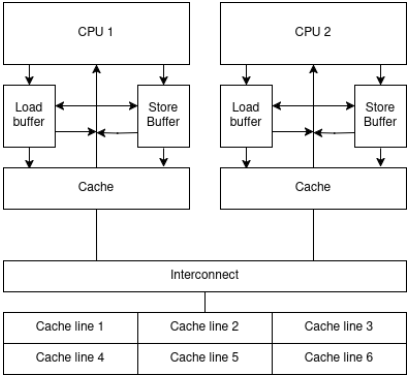

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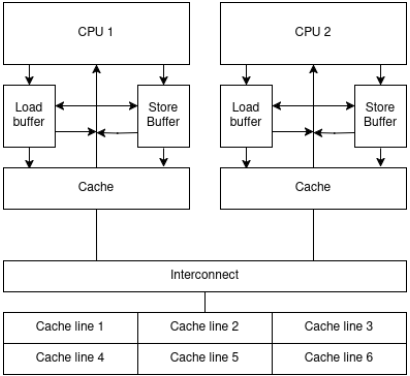


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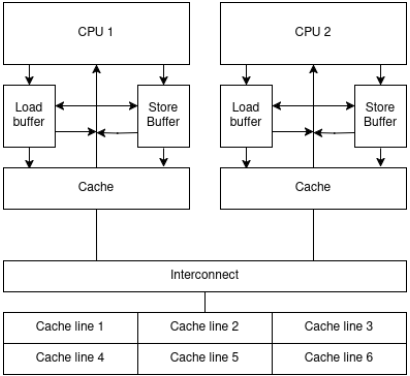


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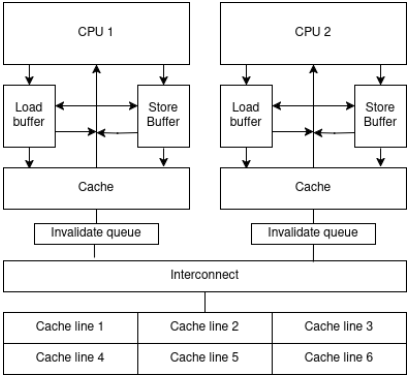
Looks like we need different **kinds** of memory barriers.

# Lecture plan

# Invalidate Queue

```
void foo(void) {
  a = 1;
  smp_mb(); // memory barrier
  b = 1;
}
void bar(void) {
  while (b == 0) continue;
  assert(a == 1); // fails with `a == 0`. WHAT?
}
```



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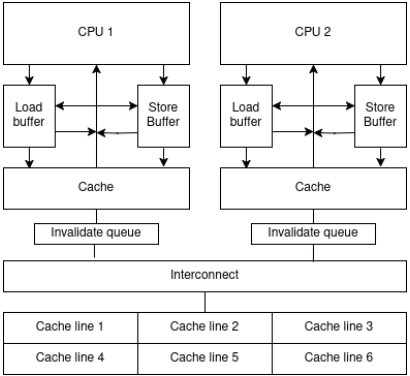


Key insight:

- Synchronization is **always** a **communication**
  - The one to initiate data exchange (writer, request sender)
  - The one to ensure data view is consistent (reader, response sender)
- "My thread executed strongest memory barrier, others will see updated data" is **NOT OK**

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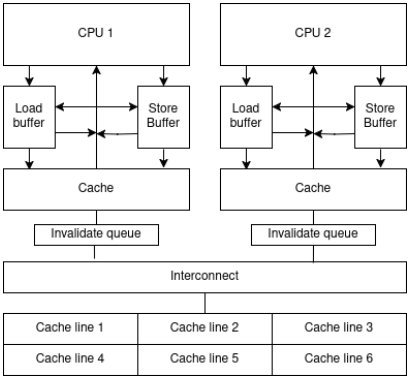
Optional homework: perfbook.B.4.3



# Lecture plan

# Independent Reads of Independent Writes

```
thread1      thread2      thread3      thread4
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Assume there is no in-CPU reordering of memory operations (no load buffering)

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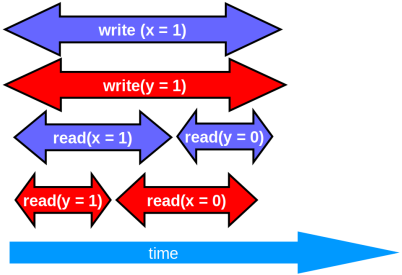

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# Interconnect topology

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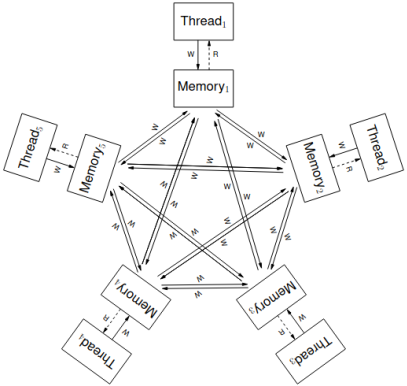


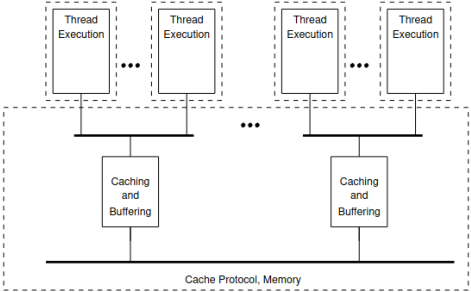

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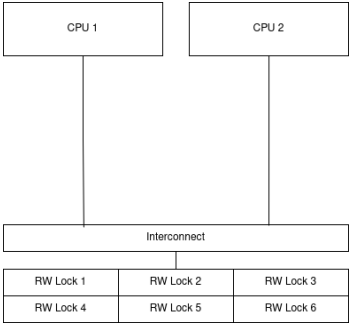

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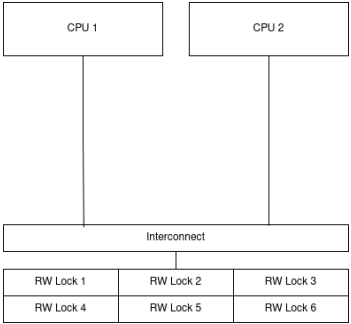


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- **Relaxed** memory model
- **Weak** memory model
- Interesting fact №1: stronger CPU memory model – less bugs you encounter during maintenance of large concurrent software system
- Interesting fact №2: smartphones, laptops, energy-efficient servers tend to use weak hardware

# Lecture plan

# Memory barriers: definition

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```
int x = static.data1;
Store_Store();
Store_Load();
int y = static.data2;
static.data3 = 17;
```

```
int x = static.data1;
Load_Load();

int y = static.data2;
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```

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Memory barriers are needed to:

- implement basics (writing your own OS, compiler, VM)
- get CRITICAL performance and spend a lot of resources to maintain the code
- design useful concurrent programming language (see you at next Lecture)

# Lecture plan

# Litmus test: definition

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**Coherence (CoRR1)**

Initial state: `x = 1`, Forbidden: `r1 = 2, r2 = 1`

```
void threadA() {
      x = 2;
}
```

```
void threadB() {
    int r1 = x;
    int r2 = x;
}
```

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- **Litmus test**: very small concurrent program that access few shared variables and illustrates some relaxed-memory phenomena

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void threadA() {
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**Store buffering**

```
mov [x] , 1  # (A.1)
mov EAX , [y] # (A.2)
```

```
mov [y] , 1  # (B.1)
mov EBX, [x] # (B.2)
```

Hardware allows: (EAX=0 EBX=0)

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- Well-studied problem domain

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# Summary

Cache coherency

- Cache line: granularity, false sharing, tagging with extra info
- Cache coherency protocol: states, transitions, message passing, coherency

Hardware optimizations

- Store buffering, Load buffering, Invalidate Queues, Interconnect topology

Hardware memory model

- Reorderings of memory operations on independent memory locations
- Weak (relaxed) consistency

Memory barriers

- Architecture-specific, Affect local CPU only, Different kinds
- `{Store,Load}_{Store,Load}` taxonomy

Litmus tests

- Basic blocks for many key concurrent algorithms
- Empirical approach to building reliable concurrent software

# Summary: homework

"Is Parallel Programming Hard, And, If So, What Can You Do About It" (perfbook) Appendix B "Why Memory Barriers?"

- section B.1 "Cache Structure". Be ready to draw and explain what is associative hardware cache.
- section B.2.4 "MESI Protocol Example"