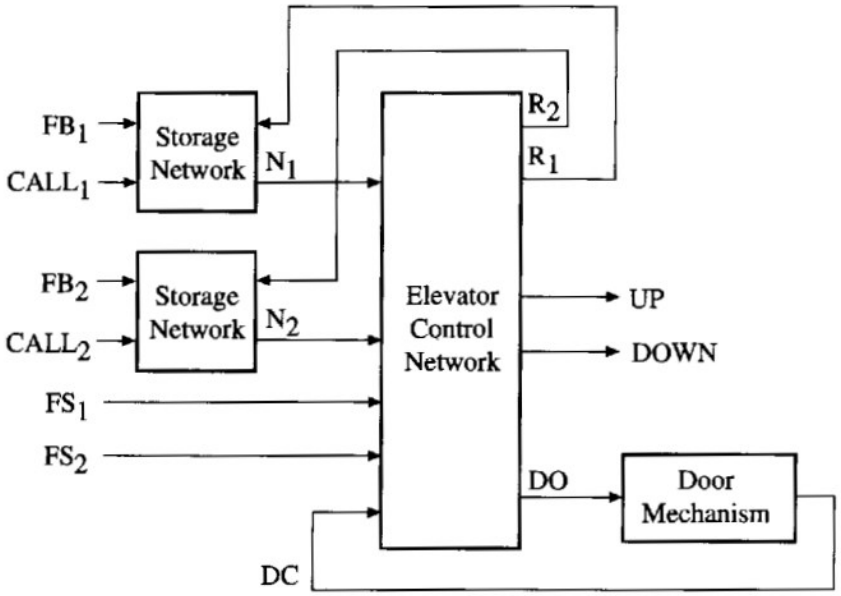
Project specification:

The Block diagram for an elevator for a building with two floors is shown below. The inputs FB1 and FB2 are floor buttons in the elevator. The inputs call1 and call2 are call buttons in the hall. The inputs FS1 and FS2 are floor switches that output a 1 when the elevator is at the first or second floor landing. Outputs UP and DOWN control the motor and the elevator is stopped when UP=DOWN=0. N1 and N2 are the flipflops that indicate when the elevator is needed in the first or second floor. R1, and R2 are the signals that reset the flipflops. DO=1 causes the door to open, and DC=1, indicates that the door is closed.



Project deliverables:

1) Draw an ASM chart for the elevator controller (four states).
2) Follow the synthesis steps according to the class lectures and convert each part to the VHDL code.
3) Try to optimize the design in terms of the required logic (area) and delay (latency).
4) Document the steps of synthesis. The full report of your design the **mandatory** part of deliverables.

The table below shows the marks associated to each abovementioned part.

Deliverable part	ASM	Synthesis and coding	Optimization	Report
Associated mark	15	45	20	20

Project due:

The project due is 6th March 2023. You will deliver your design on Vivado and you will explain your report, part-by part in my office (room 308, department of computer, BASU).

Good Luck!