

Control Unit

Control Signals

opcode	000	001	010	011	100	101	110	111
Instruction	Add(R)	Sub(R)	Beq(I)	And(R)	Lw(I)	Sw(I)	Addi(I)	Ori(I)
RegDst	1	1	x(0)	1	0	x(0)	0	0
RegWrite	1	1	0	1	1	0	1	1
MemToReg	0	0	x(0)	0	1	x(0)	0	0
MemWrite	0	0	0	0	0	1	0	0
MemRead	0	0	0	0	1	0	0	0
ALUsrc	0	0	0	0	1	1	1	1
ExtOp	x(0)	x(0)	x(0)	x(0)	1	1	0	0
Branch	0	0	1	0	0	0	0	0
ALUop[1:0]	00	01	01	10	00	00	00	11
ALUctr	add	sub	sub	and	add	add	add	or