AMBA – Advanced Microcontroller Bus Architecture – A Quick View

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Introduction

- AMBA - **Advanced Micro controller Bus Architecture**
- **Bus Architecture – For Microcontrollers.**
- Open Standard, On-chip interconnect specification for the connection and management of functional blocks in the System on Chip (Means SoC).
- AMBA helps in getting the design right in first attempt with right design. Enables the usage of Large number of Peripherals as well.

Why AMBA?

- To enable the right first time development. Particularly, for the boards where there are more than one microcontrollers or DSPs. (When there are multiple processors, it is real complex)
- To enable technology independent boards to be built (This ensures minimum dependency). The primary motivation of AMBA protocols is to have a standard and efficient way to interconnecting these functional blocks and peripherals with re-use across multiple designs.
- To ensure that the design is all modular and scope for peripheral library development is encouraged.
- To enable the efficient on chip and off chip communication.

What could be on board?

- One or more Microcontrollers.
- One or more Microprocessors
- Memory elements
- DSPs (Digital Signal Processors)
- DMAs (Direct Memory Access)
- USBs
- PCI
- I2C
- Peripherals and so on!

- AMBA is here to interconnect all the above seamlessly and to enable reusability as well.

AMBA Standards

- **The *Advanced High-performance Bus (AHB)***
- **The *Advanced System Bus (ASB)***
- **The *Advanced Peripheral Bus (APB).***
- **The Advanced Trace Bus (ATB)**
- **The AMBA Extensible Interface (AXI)**

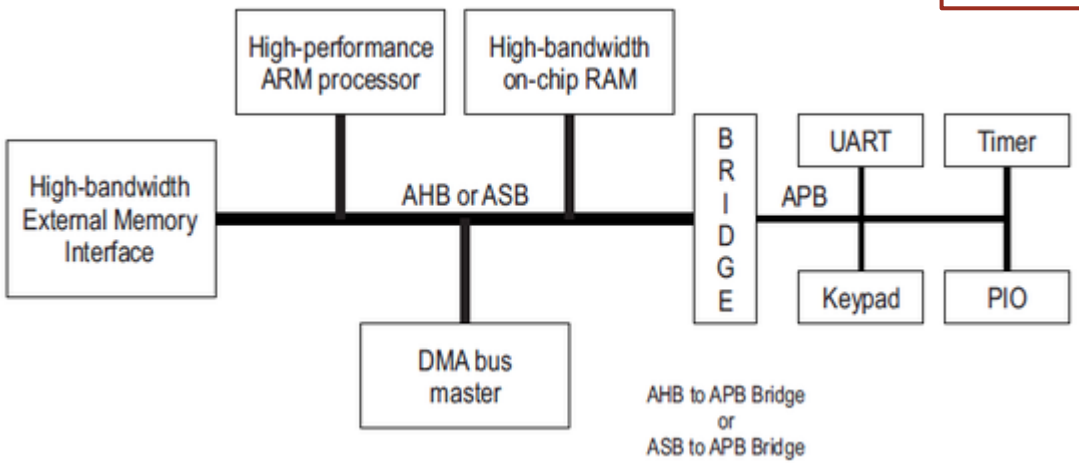
- We may not learn all of these, but, we shall focus on commonly used standards from the above list.

Lets get to the core…

- Refer the diagram (reference from the AMBA 2.0 spec) illustrates a traditional AMBA based SOC design that uses the AHB (Advanced High performance) or ASB (Advanced System Bus) protocols for high bandwidth interconnect and an APB (Advanced Peripheral Bus) protocol for low bandwidth peripheral interconnects.

AHB or ASB -- **This bus provides a high-bandwidth interface between the elements that are involved in the majority of transfers.**

There is a bridge to the lower bandwidth APB, where most of the peripheral devices in the system are located.



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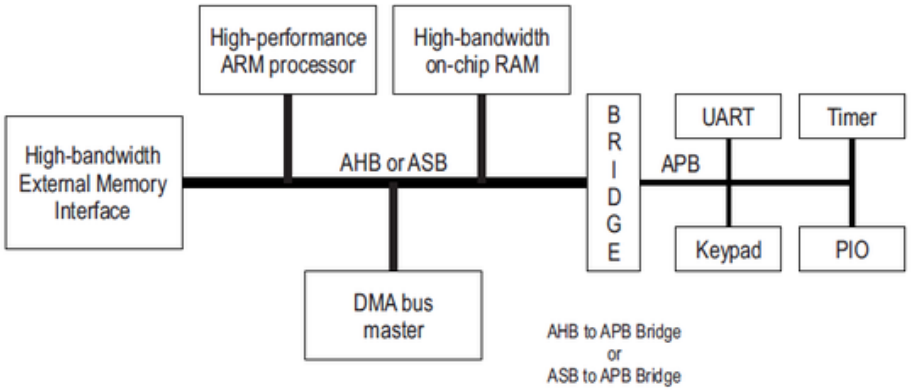
- The number of functional blocks are ever increasing and hence AMBA also had to evolve.
- AMBA 3 has a new standard in picture AXI (Advanced Extensible Interface) which further has been elevated as AXI4.

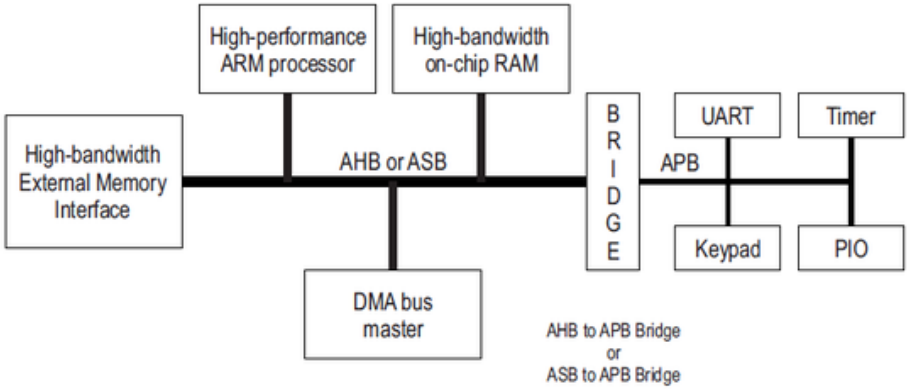
Lets learn these.. One after another.

- **APB :** This is Advanced Peripheral Bus – Used for Connecting Low Bandwidth Peripherals.
- Simple Protocol. No complications. No pipeline support.
- Used for read/write from the bridge to the peripherals. Bridge is the master, Peripherals are the slaves.
- Shares same signals for Read/Write.
- Burst transfer not possible.



AHB – Lets understand this.

- **AHB:** Expanded as Advanced High Performance Bus.
- Used for connecting components where higher bandwidth is required on a shared bus.
- Components can be DMA, DSP etc.
- Like APB, this is also Master – Slave concept.
- Multi masters and multi slaves are supported.
- Burst data transfers supported.



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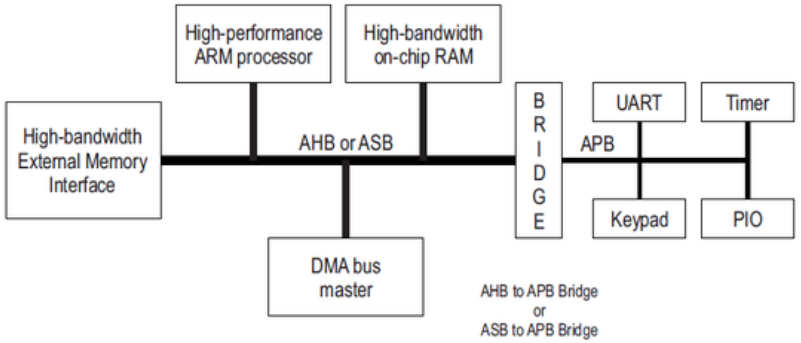
- **AHB-lite** - As you can predict, it is the lighter version of AHB.
- Supports single master! ☺ Hence, there is not need for complexities in terms of ensuring arbitration or retries.

Bus **Arbitration** refers to the process by which the current bus master accesses and then leaves the control of the bus and passes it to the another bus requesting processor unit



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- **AXI:** Advanced Extensible Interface
- Used when High Bandwidth, Low Latency is the requirement.
- Update of the AHB.
- Supports Burst Mode Transfers.
- Supports Pipelined Transfers
- Supports, separate read and write paths and supporting different bus widths.

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- **AXI-lite** protocol is a simplified version of AXI
- No support for burst data transfers.

Learning Shall Evolve

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