AMBA BUS

Advanced Micro controller Bus Architecture

By

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Overview of the AMBA Specification

The Advanced Micro controller Bus architecture (AMBA) specification defines an on-chip communication standard for designing high-performance embedded micro controllers.

Types of AMBA Bus

Three distinct buses are defined within the AMBA specification:

- **The *Advanced High-performance Bus* (AHB)**
- **The *Advanced System Bus* (ASB)**
- **The *Advanced Peripheral Bus* (APB).**
- **The Advanced Trace Bus (ATB)**
- **The AMBA Extensible Interface (AXI)**

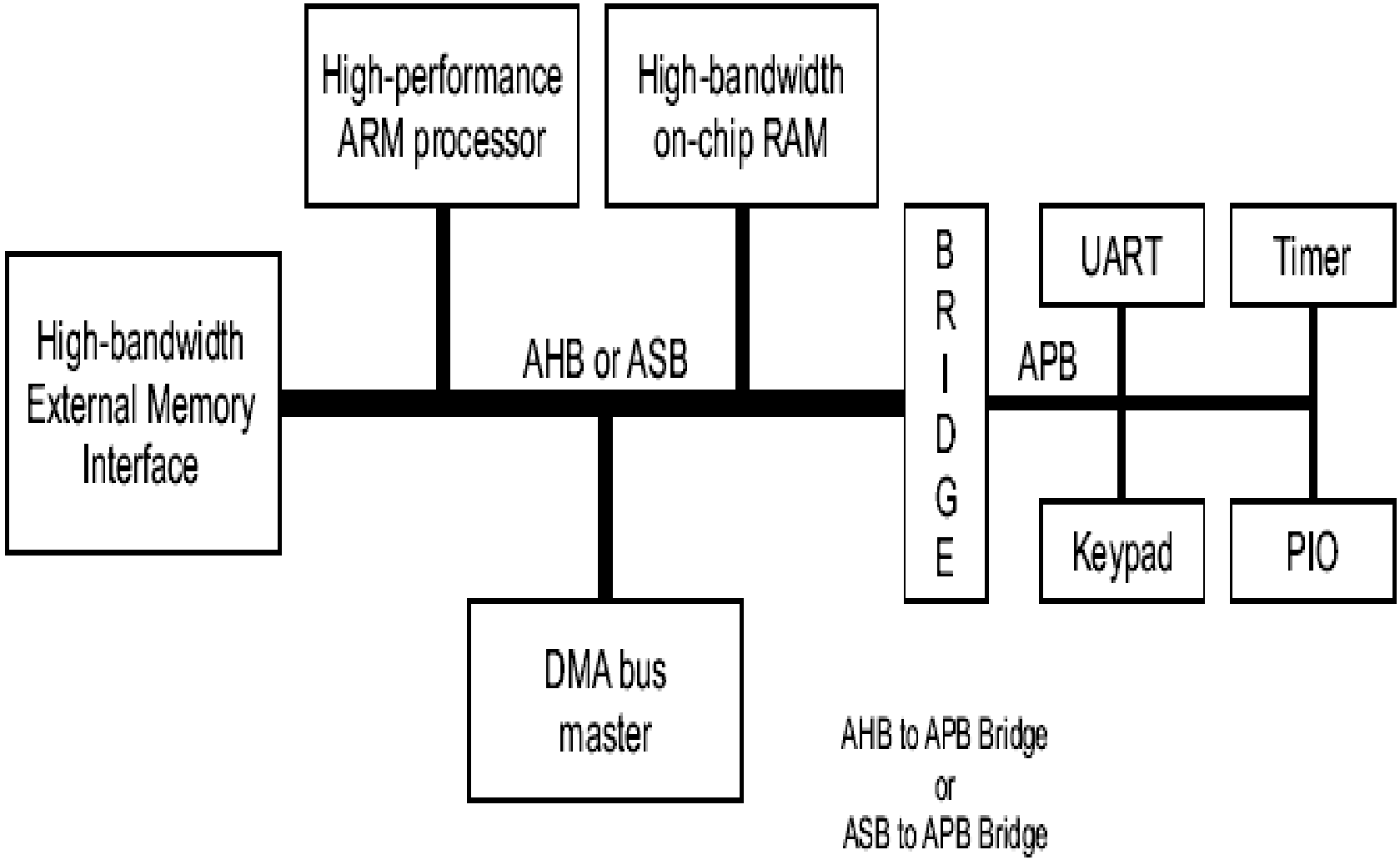
Objectives of AMBA Bus

The AMBA specification has been derived to satisfy four key requirements:

- **To facilitate the *right-first-time* development of embedded micro controller products with one or more CPUs or signal processors.**
- **To be *technology-independent* and ensure that highly reusable peripheral and system macro cells can be migrated across a diverse range of IC processes and be appropriate for full-custom, standard cell and gate array technologies**
- **To encourage *modular system design* to improve processor independence, providing a development road-map for advanced cached CPU cores and the development of peripheral libraries.**
- **To minimize the silicon infrastructure required to support efficient on-chip and off-chip communication for both operation and manufacturing test.**

Typical AMBA Based Micro controller

- An AMBA-based micro controller typically consists of a high-performance system *backbone* bus (AMBA AHB or AMBA ASB).
- Which is able to sustain the external memory bandwidth, on which The CPU, on-chip memory and other *Direct Memory Access* (DMA) devices reside.
- This bus provides a high-bandwidth interface between the elements that are involved in the majority of transfers.
- Also located on the high-performance bus is a bridge to the lower bandwidth APB, where most of the peripheral devices in the system are located.


High-performance ARM processor
High-bandwidth on-chip RAM
High-bandwidth External Memory Interface
AHB or ASB
B R I D G E
APB
UART
Timer
Keypad
PIO
DMA bus master
AHB to APB Bridge
or
ASB to APB Bridge

AMBA AHB

Advanced High Performance Bus

- AHB is a new generation of AMBA bus which is intended to address the requirements of high-performance synthesizable designs.

- It is a high-performance system bus that supports multiple bus masters and provides high-bandwidth operation.

Features of AMBA BUS

AMBA AHB implements the features required for high-performance, high clock frequency systems including:

- **Burst transfers**
- **Split transactions**
- **Single-cycle bus master handover**
- **Single-clock edge operation**
- **Wider data bus configurations (64/128 bits).**

Components of AMBA AHB

A typical AMBA AHB system design contains the
Following components:

AHB master : A bus master is able to initiate read and write operations by providing an address and control information.

AHB slave : A bus slave responds to a read or write operation within a given address-space range.

AHB arbiter : The bus arbiter ensures that only one bus master at a time is allowed to initiate data transfers.

AHB decoder : The AHB decoder is used to decode the address of each transferred provide a select signal for the slave that is involved in the transfer.

Typical Master and slave

- An AMBA AHB design may contain one or more bus masters.
- Typically a system would contain at least the processor and test interface.
- It is also common for a *Direct Memory Access* (DMA) or *Digital Signal Processor* (DSP) to be included as bus masters.
- The external memory interface, APB bridge and any internal memory are the most common AHB slaves.
- Any other peripheral in the system could also be included as an AHB slave.

Overview of AMBA AHB Operation

Before an AMBA AHB transfer can commence the
bus master must be granted access to the bus.

- **Process is started by the master asserting a request signal to the arbiter.**
- **Then the arbiter indicates when the master will be granted use of the bus.**
- **A granted bus master starts an AMBA AHB transfer by driving the address and control signals.**
- **These signals provide information on the address, direction and width of the transfer, as well as an indication if the transfer forms part of a burst.**
- **A write data bus is used to move data from the master to a slave, while a read data bus is used to move data from a slave to the master.**

Basic Transfer

An AHB transfer consists of two distinct sections:

- **The Address Phase, which lasts only a single cycle.**
- **The Data Phase, which may require several cycles.**

AMBA APB

Advanced Peripheral Bus

- The *Advanced Peripheral Bus* (APB) is part of the *Advanced Micro controller Bus Architecture* (AMBA)
- APB is optimized for minimal power consumption and reduced interface complexity.
- The AMBA APB should be used to interface to any peripherals which are low bandwidth and do not require the high performance of a pipelined bus interface.
- The AMBA APB appears as a local secondary bus that is encapsulated as a single AHB or ASB slave device.

Advantages of AMBA APB

- **Performance is improved at high-frequency operation**
- **Performance is independent of the mark-space ratio of the clock static timing analysis is simplified by the use of a single clock edge**
- **No special considerations are required for automatic test insertion**
- **Many *Application-Specific Integrated Circuit* (ASIC) libraries have a better selection of rising edge registers**
- **Easy integration with cycle based simulators.**

AMBA APB Bridge

The APB bridge is the only bus master on the AMBA APB.

In addition, the APB bridge is also a slave on the higher-level system bus.

APB bridge description

The bridge unit converts system bus transfers into

APB transfers and performs the following functions:

- **Latches the address and holds it valid throughout the transfer.**
- **Decodes the address and generates a peripheral select, PSELx. Only one select signal can be active during a transfer.**
- **Drives the data onto the APB for a write transfer.**
- **Drives the APB data onto the system bus for a read transfer.**
- **Generates a timing strobe, PENABLE, for the transfer**

APB slave Description

- **APB slaves have a simple, yet flexible, interface.**

- **The exact implementation of the interface will be dependent on the design style employed and many different options are possible.**

http://en.wikipedia.org/wiki/Advanced_Microcontroller_Bus_Architecture

http://digitalelectronics.blogspot.in/2005/02/advanced-microcontroller-bus.html

THANK YOU